LP5907 250mA 超低噪声、低 I_Q LDO

1 特性

- 输入电压范围：2.2V 至 5.5V
- 输出电压范围：1.2V 至 4.5V
- 与 1µF 陶瓷输入和输出电容搭配使用，性能稳定
- 无需噪声旁路电容
- 支持输出电容远端布置
- 热过载保护和短路保护
- 运行结温范围：-40°C 至 125°C
- 低输出电压噪声：< 6.5μV_{RMS}
- 电源抑制比 (PSRR)：1kHz 频率时为 82dB
- 输出电压容差：±2%
- 极低 I_Q（启用）：12µA
- 低压降：120mV（典型值）
- 使用 LP5907 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 移动电话、平板电脑
- 数码相机和音频设备
- 便携式和电池供电类设备
- 便携式医疗设备
- 智能仪表和现场变送器
- RF、PLL、VCO 和时钟电源
- IP 摄像机
- 无人机

3 说明

LP5907 是一款能提供高达 250mA 输出电流的低噪声 LDO。此器件专门针对射频和模拟电路而设计，可满足其低噪声、高 PSRR、低静态电流以及低线路或负载瞬态响应系数等诸多要求。LP5907 采用创新的设计技术，无需噪声旁路电容便可提供出色的噪声性能，并且支持远距离安置输出电容。

此器件可与 1µF 输入和 1µF 输出陶瓷电容搭配使用（无需独立的噪声旁路电容）。

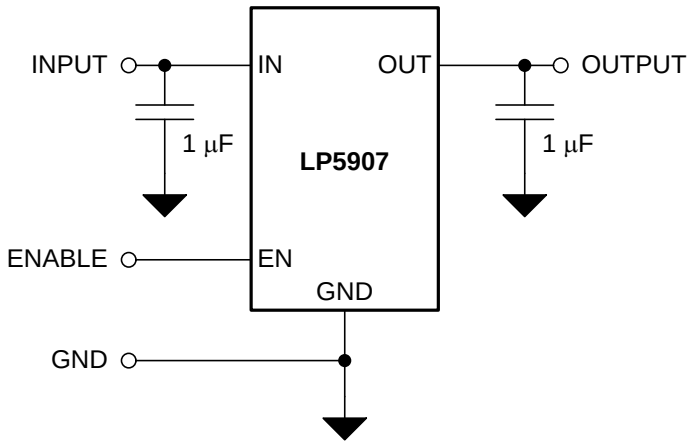
其固定输出电压介于 1.2V 至 4.5V 之间（阶跃为 25mV）。如需特定的电压选项，请联系德州仪器 (TI) 销售代表。

器件信息(1)

器件型号	封装	封装尺寸
LP5907	DSBGA (4)	0.675mm x 0.675mm（最大值）
	SOT-23 (5)	2.90mm x 1.60mm（标称值）
	X2SON (4)	1.00mm x 1.00mm（标称值）

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision M (January 2018) to Revision N — **Page**

- Added *Overshoot on start-up with EN* row to *Electrical Characteristics* table ... 7

Changes from Revision L (August 2016) to Revision M — **Page**

- 已添加 WEBENCH 的链接 ... 1
- 已添加 关于 YKM 封装选项的信息 ... 1
- 已添加 细微的编辑性更改 ... 1

Changes from Revision K (May 2016) to Revision L — **Page**

- 已更改 更改了数据表标题，更新了*应用* 列表以及“说明”部分第一句的*措辞* ... 1
- 已更改 “10μV_{RMS}”改为“6.5μV_{RMS}” ... 1

Changes from Revision J (March 2016) to Revision K — **Page**

- 已更改 标题和“说明”部分第一句中的“线性稳压器”改为 “LDO” ... 1

Changes from Revision I (August 2015) to Revision J — **Page**

- Changed V_{OUT} min and max values and V_{EN} min value in Abs Max table and V_{EN} row of ROC table to correct format errors; replace text of footnote 2 of Abs Max table ... 5

Changes from Revision H (November 2014) to Revision I — **Page**

- 已添加 顶部导航增加了参考设计图标，并将“ΔV_{OUT} 与温度间的关系”图添加到了了*典型特性* ... 1
- Changed Storage Temperature to *Abs Max* table; replace *Handling Ratings* with *ESD Ratings* ... 5
- Deleted "$V_{OUT} \geq 1.8$ V" from first row of ΔVout spec ... 6

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- Added "SOT-23, X2SON packages" to second row of ΔVout spec 6

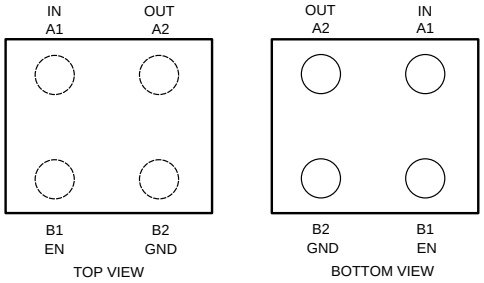
Changes from Revision G (October 2013) to Revision H **Page**

- 已添加 *器件信息* 表和*处理额定值* 表，*特性* *描述*、*器件功能模式*、*应用和实施*、*电源相关建议*、*布局*、*器件和文档支持*以及*机械*、*封装和可订购信息* 部分；已将一些曲线移至*应用曲线* 部分。..... 1

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5 Pin Configuration and Functions

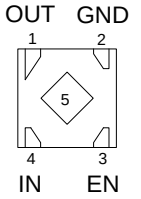
YKE and YKM Packages
4-Pin DSBGA



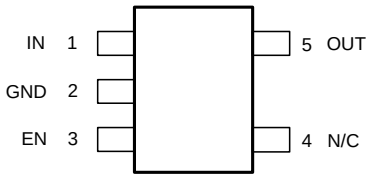
Pin Functions: DSBGA

PIN		I/O	DESCRIPTION
DSBGA NUMBER	NAME		
A1	IN	I	Input voltage supply. Connect a 1-µF capacitor at this input.
A2	OUT	O	Regulated output voltage. Connect a minimum 1-µF low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230-Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).
B1	EN	I	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal 230-Ω pulldown resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. This pin has an internal 1-MΩ pulldown resistor to hold the regulator off by default.
B2	GND	—	Common ground

DQN Package
4-Pin X2SON
Bottom View



DBV Package
5-Pin SOT-23
Top View



Pin Functions: X2SON, SOT-23

PIN			I/O	DESCRIPTION
NAME	X2SON NUMBER	SOT-23 NUMBER		
IN	4	1	I	Input voltage supply. Connect a 1-µF capacitor at this input.
OUT	1	5	O	Regulated output voltage. Connect a minimum 1-µF low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230-Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).
EN	3	3	I	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal 230-Ω pulldown resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. This pin has an internal 1-MΩ pulldown resistor to hold the regulator off by default.
GND	2	2	—	Common ground
N/C	—	4	—	No internal electrical connection.
Thermal Pad	5	—	—	Thermal pad for X2SON package, connect to GND or leave floating. Do not connect to any potential other than GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	See(3)	
V_{EN}	Enable input voltage	–0.3	6	
	Continuous power dissipation(4)	Internally Limited		W
T_{JMAX}	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) Abs Max V_{OUT} is the lessor of V_{IN} + 0.3 V, or 6 V.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage	2.2	5.5	V
V_{EN}	Enable input voltage	0	5.5	
I_{OUT}	Output current	0	250	mA
T_J	Junction temperature	–40	125	°C
T_A	Ambient temperature(3)	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$. See *Application and Implementation*.

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6.4 Thermal Information

THERMAL METRIC[1]		LP5907				UNIT
		DBV (SOT-23)	DQN (X2SON)	YKE (DSBGA)	YKM (DSBGA)	
		5 PINS	4 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.4	216.1	206.1	194.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.1	161.7	1.5	3.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	162.1	37.0	62.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	5.1	15.0	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.3	161.7	36.8	62.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	123.0	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted)[1][2][3]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	T_A = 25°C	2.2		5.5	V
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 250 mA	–2		2	%V_{OUT}
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 250 mA (V_{OUT} < 1.8 V, SOT-23, X2SON packages)	–3		3	
	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA		0.02		%/V
	Load regulation	I_{OUT} = 1 mA to 250 mA		0.001		%/mA
I_{LOAD}	Load current	See[4]	0		250	mA
	Maximum output current		250			
I_Q	Quiescent current[5]	V_{EN} = 1.2 V, I_{OUT} = 0 mA		12	25	µA
		V_{EN} = 1.2 V, I_{OUT} = 250 mA		250	425	
		V_{EN} = 0.3 V (disabled)		0.2	1	
I_G	Ground current[6]	V_{EN} = 1.2 V, I_{OUT} = 0 mA		14		µA
V_{DO}	Dropout voltage[7]	I_{OUT} = 100 mA		50		mV
		I_{OUT} = 250 mA (DSBGA package)		120	200	
		I_{OUT} = 250 mA (SOT-23, X2SON packages)			250	
I_{SC}	Short-circuit current limit	T_A = 25°C[8]	250	500		mA

(1) All voltages are with respect to the device GND terminal, unless otherwise stated.
(2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application $R_{\theta JA}$), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – ($R_{\theta JA}$ × P_{D-MAX}). See *Application and Implementation*.
(4) The device maintains a stable, regulated output voltage without a load current.
(5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(8) Short-circuit current (I_{SC}) for the LP5907 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.

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Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted)(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio(9)	f = 100 Hz, I_{OUT} = 20 mA			90		dB
		f = 1 kHz, I_{OUT} = 20 mA			82		
		f = 10 kHz, I_{OUT} = 20 mA			65		
		f = 100 kHz, I_{OUT} = 20 mA			60		
e_N	Output noise voltage(9)	BW = 10 Hz to 100 kHz	I_{OUT} = 1 mA		10		μV_{RMS}
			I_{OUT} = 250 mA		6.5		
R_{AD}	Output automatic discharge pulldown resistance	V_{EN} < V_{IL} (output disabled)			230		Ω
T_{SD}	Thermal shutdown	T_J rising			160		°C
	Thermal hysteresis	T_J falling from shutdown			15		
LOGIC INPUT THRESHOLDS							
V_{IL}	Low input threshold	V_{IN} = 2.2 V to 5.5 V, V_{EN} falling until the output is disabled				0.4	V
V_{IH}	High input threshold	V_{IN} = 2.2 V to 5.5 V V_{EN} rising until the output is enabled		1.2			V
I_{EN}	Input current at EN pin(10)	V_{EN} = 5.5 V and V_{IN} = 5.5 V			5.5		µA
		V_{EN} = 0 V and V_{IN} = 5.5 V			0.001		
TRANSIENT CHARACTERISTICS							
ΔV_{OUT}	Line transient(9)	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$) + 1.6 V) in 30 µs		–1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$) + 1.6 V) in 30 µs				1	
	Load transient(9)	I_{OUT} = 1 mA to 250 mA in 10 µs		–40			
		I_{OUT} = 250 mA to 1 mA in 10 µs				40	
	Overshoot on start-up(9)	Stated as a percentage of $V_{OUT(NOM)}$				5%	
	Overshoot on start-up with EN(9)	Stated as a percentage of $V_{OUT(NOM)}$, V_{IN} = V_{OUT} + 1 V to 5.5 V, 0.7 µF < C_{OUT} < 10 µF, 0 mA < I_{OUT} < 250 mA, EN rising until the output is enabled				1%	
t_{ON}	Turnon time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$, T_A = 25°C			80	150	µs

(9) This specification is verified by design.
(10) There is a 1-MΩ resistor between EN and ground on the device.

6.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX	UNIT
C_{IN}	Input capacitance(2)	Capacitance for stability	0.7	1		µF
C_{OUT}	Output capacitance(2)		0.7	1	10	µF
ESR	Output/Input capacitance(2)		5		500	mΩ

(1) The minimum capacitance should be greater than 0.5 µF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application must be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.
(2) This specification is verified by design.

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6.7 Typical Characteristics

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

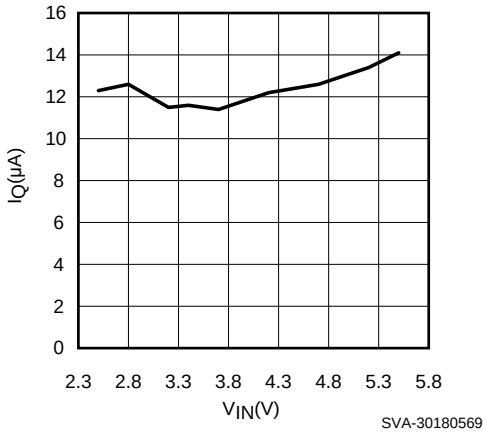


Figure 1. Quiescent Current vs Input Voltage

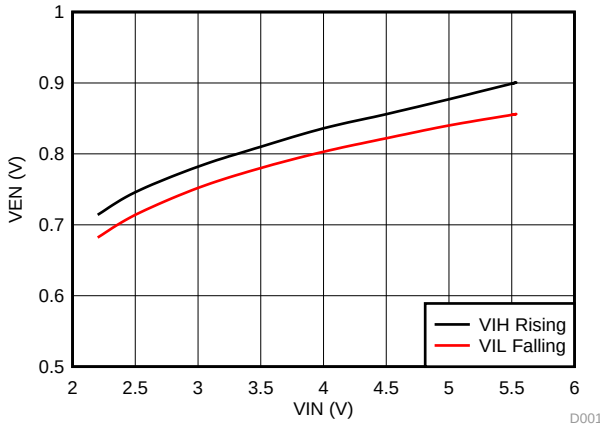
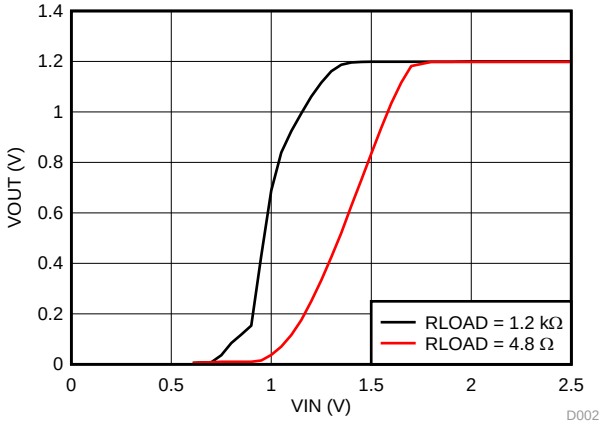
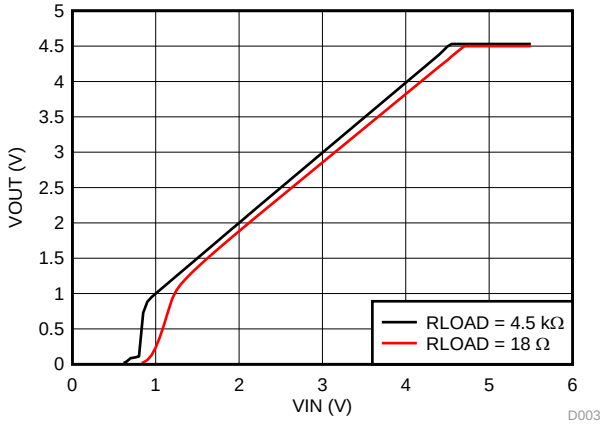


Figure 2. V_{EN} Thresholds vs V_{IN}



V_{OUT} = 1.2 V, V_{EN} = V_{IN}

Figure 3. V_{OUT} vs V_{IN}



V_{OUT} = 4.5 V, V_{EN} = V_{IN}

Figure 4. V_{OUT} vs V_{IN}

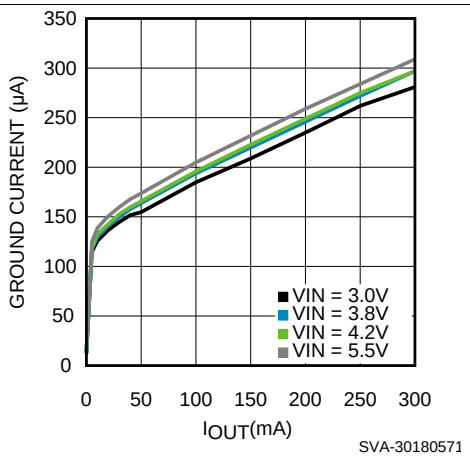


Figure 5. Ground Current vs Output Current

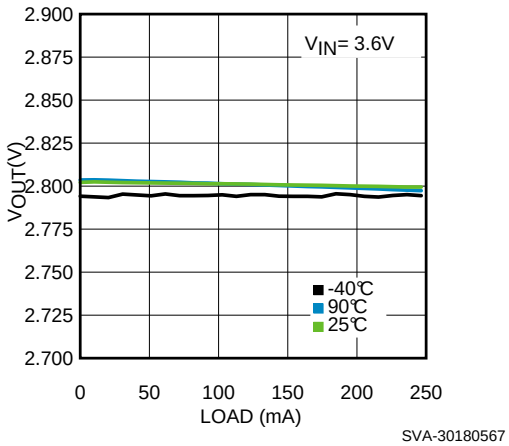


Figure 6. Load Regulation

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Typical Characteristics (continued)

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

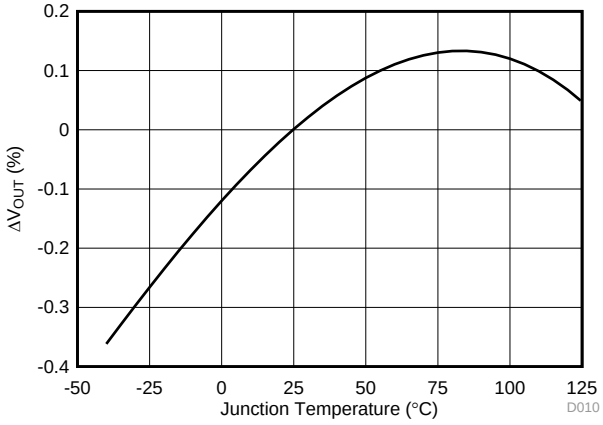


Figure 7. ΔV_{OUT} vs Temperature

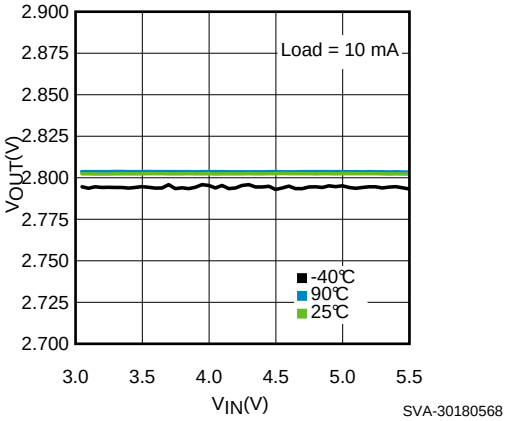


Figure 8. Line Regulation

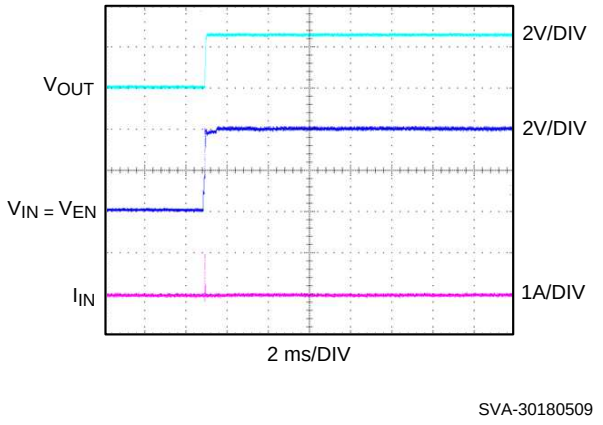
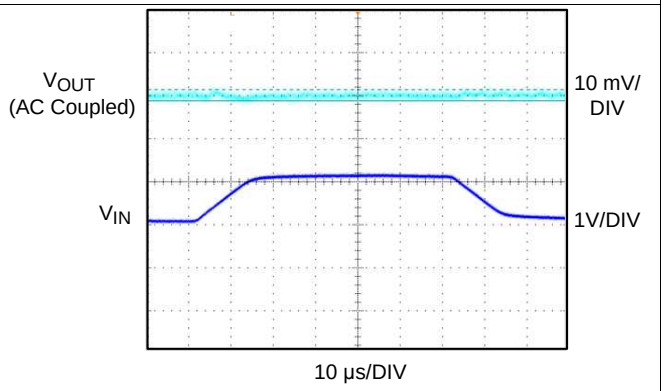
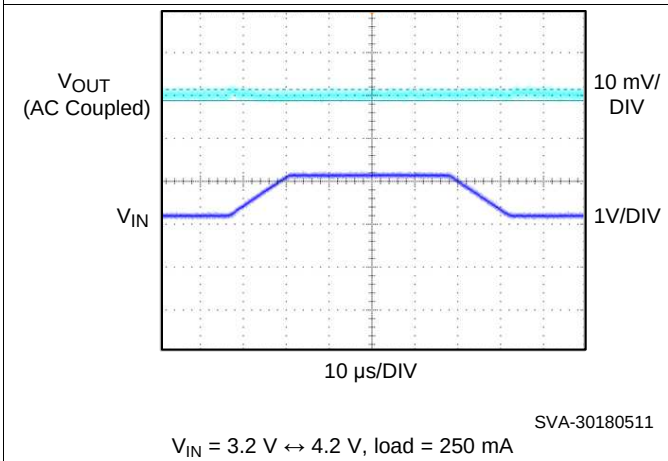


Figure 9. Inrush Current



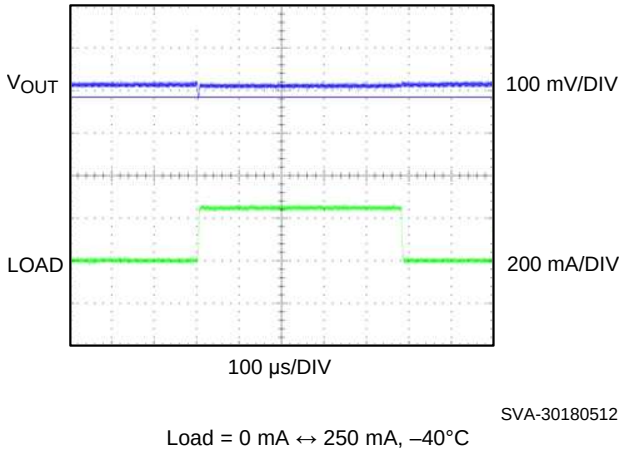
V_{IN} = 3.2 V ↔ 4.2 V, load = 1 mA

Figure 10. Line Transient



V_{IN} = 3.2 V ↔ 4.2 V, load = 250 mA

Figure 11. Line Transient



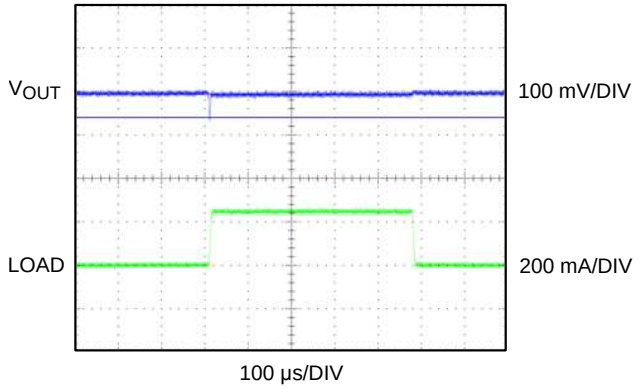
Load = 0 mA ↔ 250 mA, –40°C

Figure 12. Load Transient

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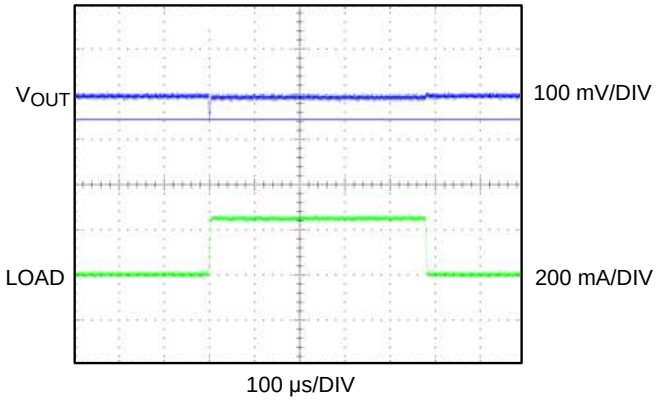
Typical Characteristics (continued)

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)



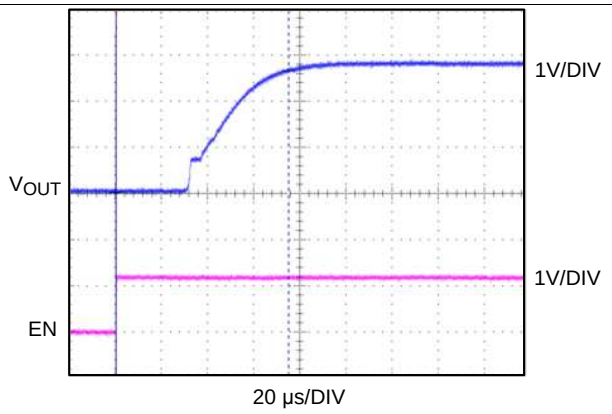
Load = 0 mA ↔ 250 mA, 90°C

Figure 13. Load Transient



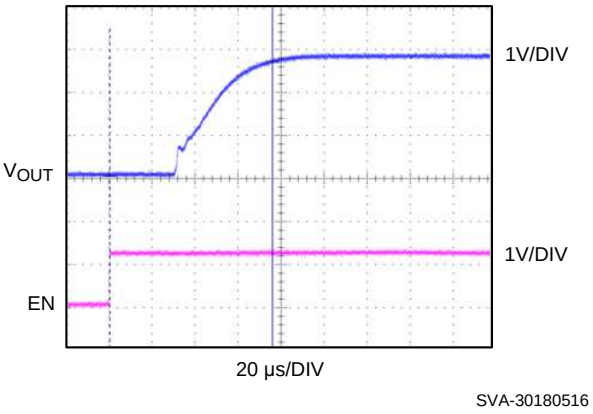
Load = 0 mA ↔ 250 mA, 25°C

Figure 14. Load Transient



Load = 0 mA

Figure 15. Start-Up



Load = 250 mA

Figure 16. Start-Up

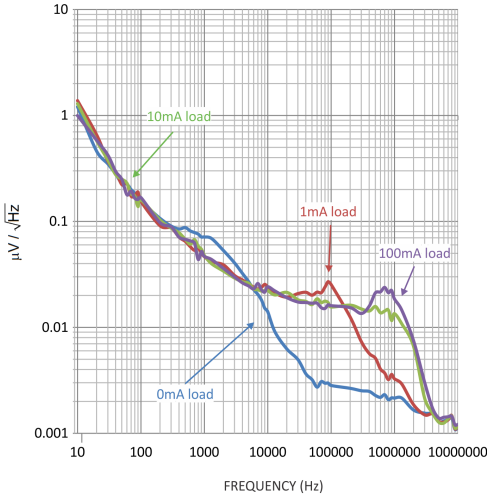


Figure 17. Noise Density Test

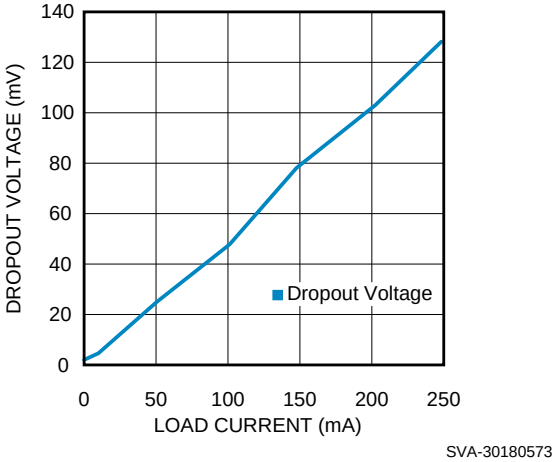


Figure 18. Dropout Voltage vs Load Current

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Typical Characteristics (continued)

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

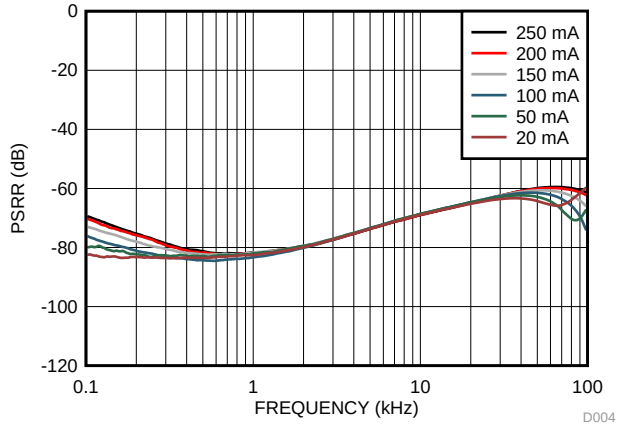


Figure 19. PSRR Loads Averaged 100 Hz to 100 kHz

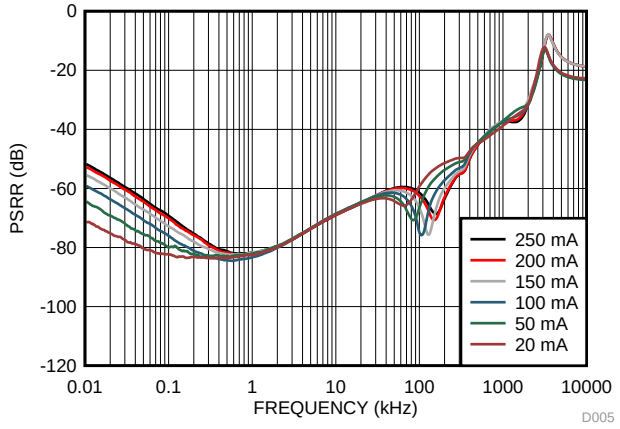


Figure 20. PSRR Loads Averaged 10 Hz to 10 MHz

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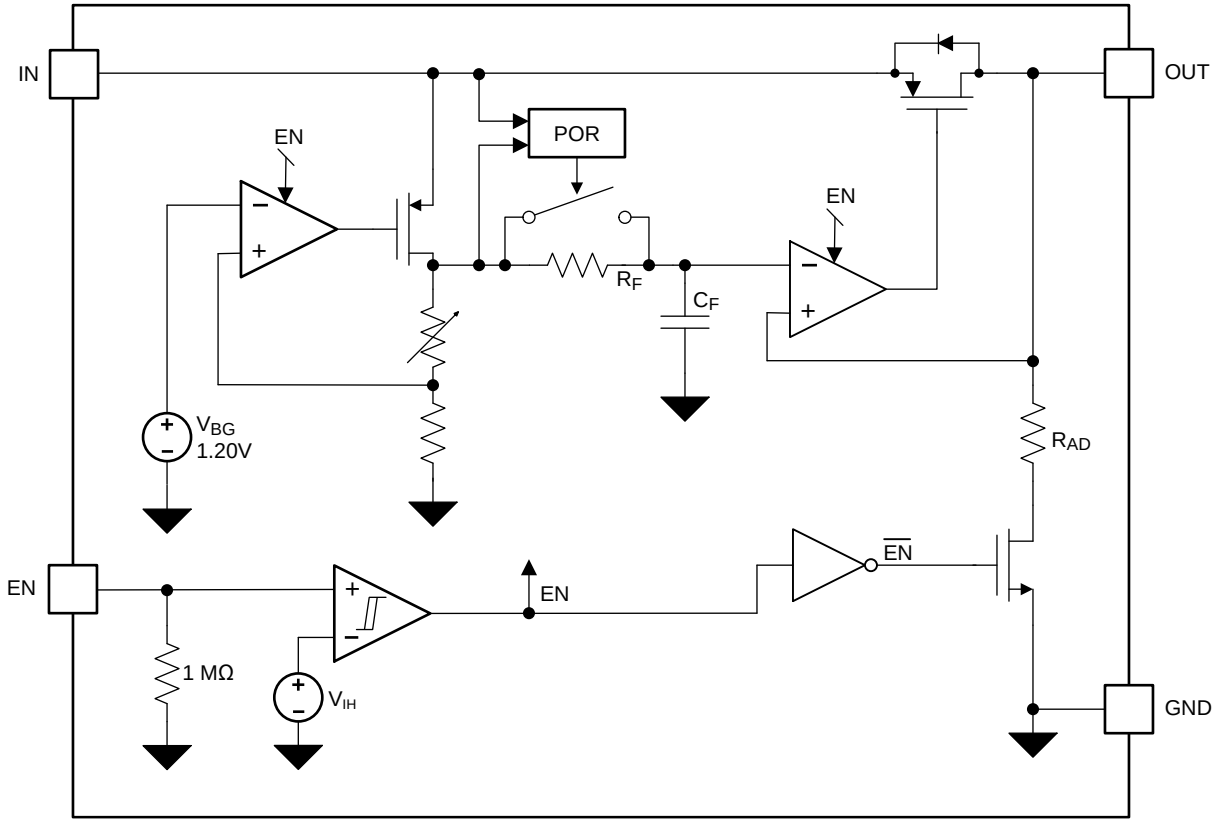
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5907 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using new innovative design techniques, the LP5907 offers class leading noise performance without the need for a separate noise filter capacitor.

The LP5907 is designed to perform with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor. With a reasonable PCB layout, the single 1-µF ceramic output capacitor can be placed up to 10 cm away from the LP5907 device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The LP5907 EN pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

7.3.2 Low Output Noise

Any internal noise at the LP5907 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a –3 dB cut-off frequency of approximately 0.1 Hz.

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Feature Description (continued)

7.3.3 Output Automatic Discharge

The LP5907 output employs an internal 230-Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

7.3.4 Remote Output Capacitor Placement

The LP5907 requires at least a 1-µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

7.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907 has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the LP5907 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5907 Enable (EN) pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230-Ω (typical) pulldown resistance.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907 does not include any dedicated UVLO circuitry. The LP5907 internal circuitry is not fully functional until V_{IN} is at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or (V_{OUT} + V_{DO}).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5907 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The LP5907 delivers this performance in industry standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of –40°C to 125°C.

8.2 Typical Application

Figure 21 shows the typical application circuit for the LP5907. Input and output capacitances may need to be increased above the 1 µF minimum for some applications.

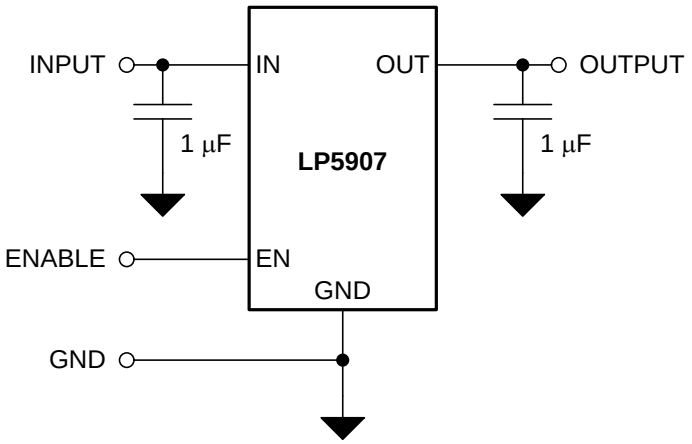


Figure 21. LP5907 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2 V to 5.5 V
Output voltage	1.8 V
Output current	200 mA
Output capacitor range	0.7 µF to 10 µF
Input/Output capacitor ESR range	5 to 500 mΩ

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LP5907 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 3:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (3)$$

Alternately, if $T_{A\text{-}MAX}$ can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the V_{IN}–V_{OUT} term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.3 External Capacitors

Like most low-dropout regulators, the LP5907 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.4 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1 µF capacitor has to be connected between the LP5907 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1 µF.

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The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907, TI recommends increasing the input capacitor to at least 10 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it should be verified by the manufacturer to have a surge current rating sufficient for the application. The initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 µF over the entire operating range.

8.2.2.5 Output Capacitor

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 1 µF to 10 µF range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP5907 application circuit. For this device the output capacitor should be connected between the OUT pin and a good connection back to the GND pin.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability. Like the input capacitor, the initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 µF over the entire operating range.

8.2.2.6 Capacitor Characteristics

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5907.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 10 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.7 Remote Capacitor Operation

The LP5907 requires at least a 1-µF capacitor at the OUT pin, but there is no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

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As a good design practice, keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close to ground layer as possible and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

8.2.2.8 No-Load Stability

The LP5907 remains stable, and in regulation, with no external load.

8.2.2.9 Enable Control

The LP5907 may be switched ON or OFF by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 µA. Additionally, an output pulldown circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-MΩ pulldown resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the *Electrical Characteristics* under V_{IL} and V_{IH}.

8.2.3 Application Curves

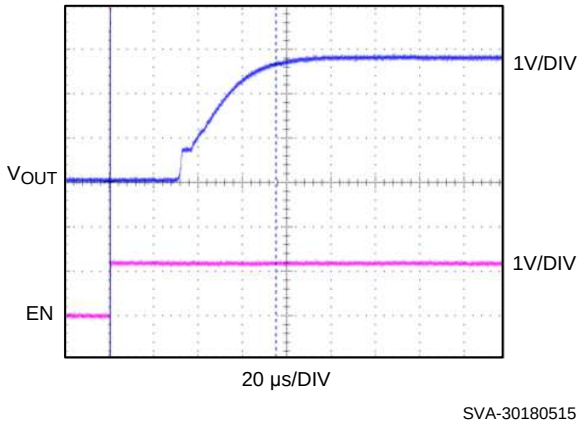


Figure 22. Start-Up

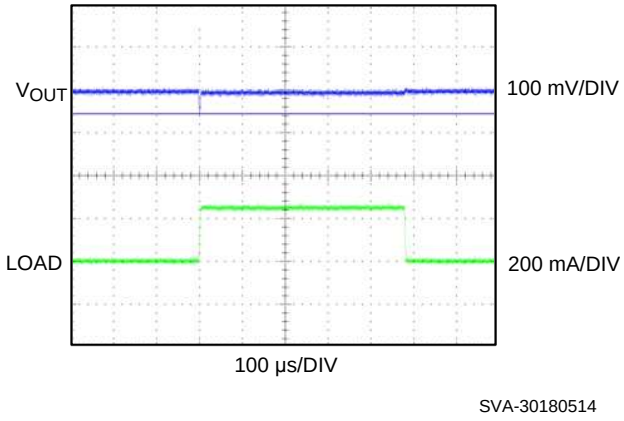


Figure 23. Load Transient Response

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2 V to 5.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5907 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 1 V. A minimum capacitor value of 1 µF is required to be within 1 cm of the IN pin.

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10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5907 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5907.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907, and as close to the package as is practical. The ground connections for C_{IN} and C_{OUT} must be back to the LP5907 ground pin using as wide and short a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.1.1 X2SON Mounting

The X2SON package thermal pad must be soldered to the printed circuit board for proper thermal and mechanical performance. For more information, see the *QFN/SON PCB Attachment* application report.

10.1.2 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package*. For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.1.3 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

10.2 Layout Examples

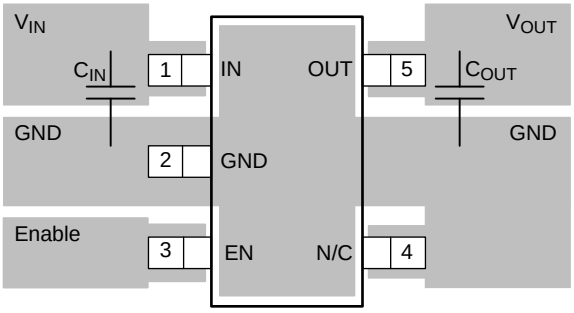


Figure 24. LP5907MF-x.x (SOT-23) Typical Layout

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Layout Examples (continued)

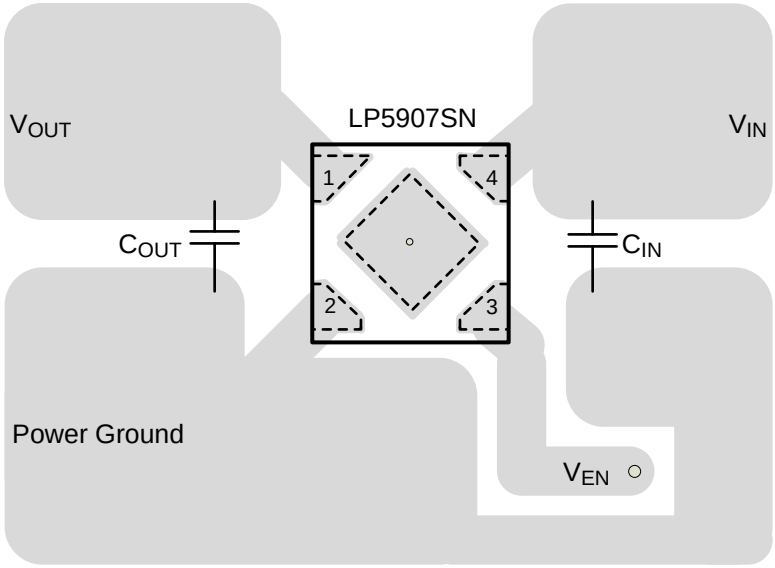


Figure 25. LP5907SN-xx (X2SON) Typical Layout

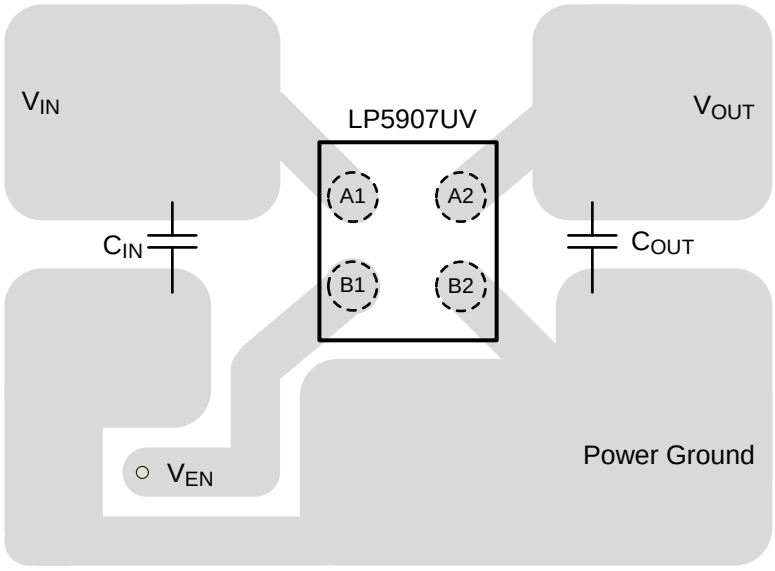


Figure 26. LP5907A/UV-x.x (DSBGA) Typical Layout

11 器件和文档支持

11.1 文档支持

11.1.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 LP5907 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先键入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键参数设计，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.1.2 相关文档

如需相关文档，请参阅：

- *AN-1112 DSBGA 晶圆级芯片级封装*
- *《QFN/SON PCB 连接》应用报告*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907A28YKMR	ACTIVE	DSBGA	YKM	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	Q	Samples
LP5907A29YKMR	ACTIVE	DSBGA	YKM	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	Y	Samples
LP5907A33YKMR	ACTIVE	DSBGA	YKM	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	N	Samples
LP5907MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LLTB	Samples
LP5907MFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LN8B	Samples
LP5907MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LLUB	Samples
LP5907MFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LN7B	Samples
LP5907MFX-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LLYB	Samples
LP5907MFX-2.85/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LN4B	Samples
LP5907MFX-2.9/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1E5X	Samples
LP5907MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LLZB	Samples
LP5907MFX-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LN5B	Samples
LP5907MFX-3.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LN6B	Samples
LP5907MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LLVB	Samples
LP5907MFX-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	LLXB	Samples
LP5907SNX-1.2/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF	Samples
LP5907SNX-1.8/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CG	Samples
LP5907SNX-1.9	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3Z	Samples
LP5907SNX-2.2/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EP	Samples
LP5907SNX-2.5/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F9	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907SNX-2.7/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH	Samples
LP5907SNX-2.75	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HI	Samples
LP5907SNX-2.8/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI	Samples
LP5907SNX-2.85/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
LP5907SNX-2.9/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GV	Samples
LP5907SNX-3.0/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK	Samples
LP5907SNX-3.1/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
LP5907SNX-3.2/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM	Samples
LP5907SNX-3.3/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CN	Samples
LP5907SNX-4.0/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GU	Samples
LP5907SNX-4.5/NOPB	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CO	Samples
LP5907UVE-1.2/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVE-1.8/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVE-2.8/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVE-2.85/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVE-3.0/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVE-3.1/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVE-3.2/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVE-3.3/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVE-4.5/NOPB	ACTIVE	DSBGA	YKE	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX-1.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907UVX-1.6/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	J	Samples
LP5907UVX-1.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVX-2.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP5907UVX-2.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
LP5907UVX-2.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVX-2.85/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVX-3.0/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVX-3.1/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVX-3.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVX-3.3/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVX-4.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX19/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP5907UVX37/NOPB	ACTIVE	DSBGA	YKE	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples
LP5907YKGR-2.0	ACTIVE	DSBGA	YKG	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	W	Samples
LP5907YKGR-2.8	ACTIVE	DSBGA	YKG	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	3	Samples
LP5907YKGR-2.825	ACTIVE	DSBGA	YKG	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	5	Samples
LP5907YKGR-2.85	ACTIVE	DSBGA	YKG	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 125	P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LP5907 :

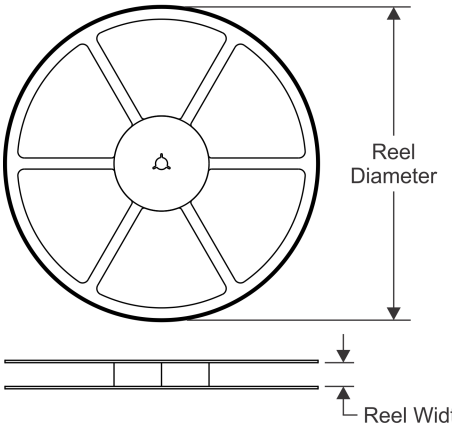
- Automotive : LP5907-Q1

NOTE: Qualified Version Definitions:

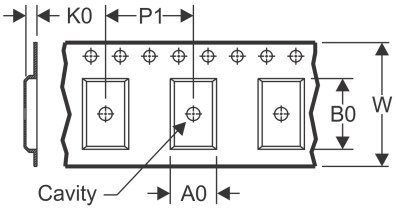
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

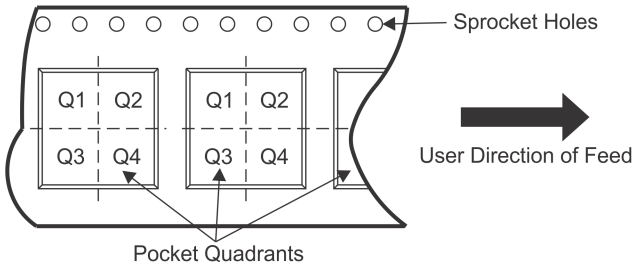


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



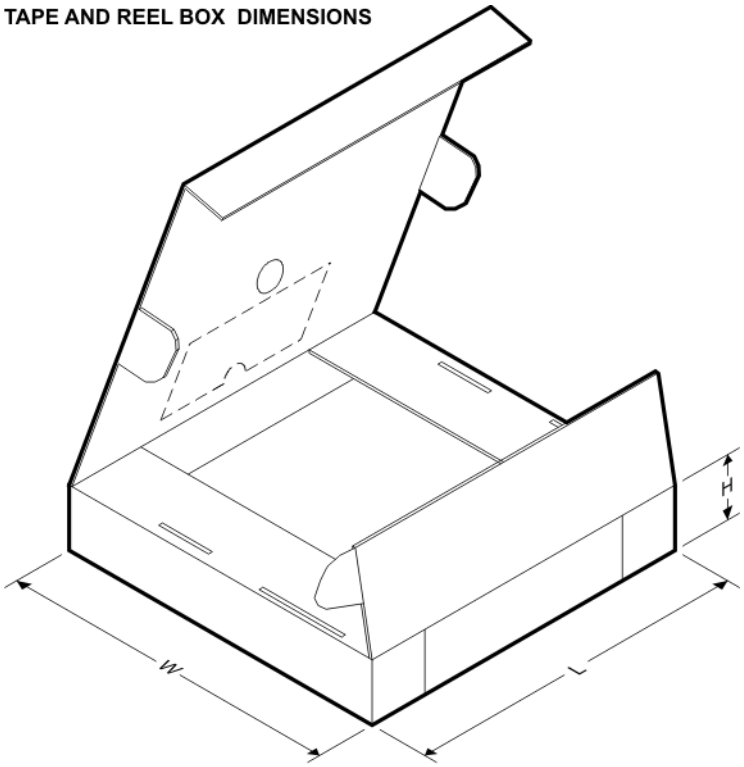
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907A28YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907A29YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907A33YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.9	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.75	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-1.6/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-2.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.74	0.74	0.5	2.0	8.0	Q1
LP5907YKGR-2.0	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1
LP5907YKGR-2.8	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1
LP5907YKGR-2.825	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1
LP5907YKGR-2.85	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907A28YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907A29YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907A33YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.9	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.75	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0

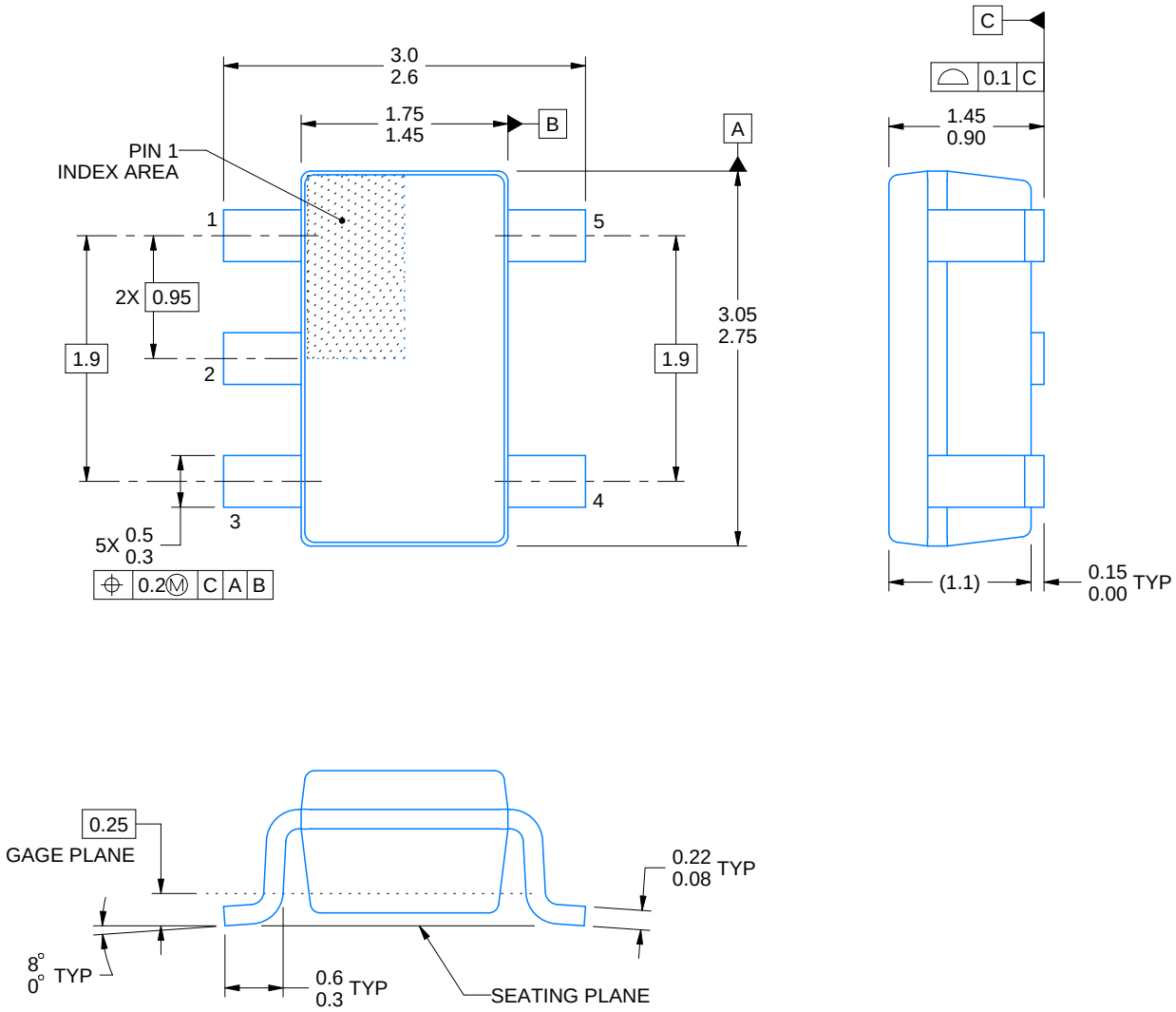
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	220.0	220.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-1.6/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-2.2/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907YKGR-2.0	DSBGA	YKG	4	3000	220.0	220.0	35.0
LP5907YKGR-2.8	DSBGA	YKG	4	3000	220.0	220.0	35.0
LP5907YKGR-2.825	DSBGA	YKG	4	3000	220.0	220.0	35.0
LP5907YKGR-2.85	DSBGA	YKG	4	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

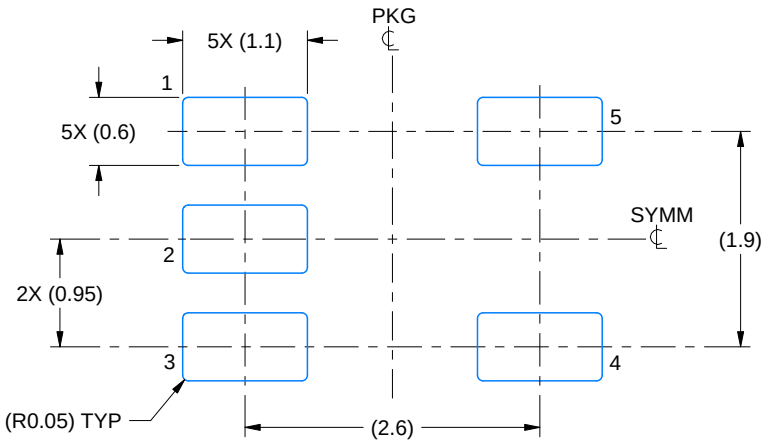
SMALL OUTLINE TRANSISTOR



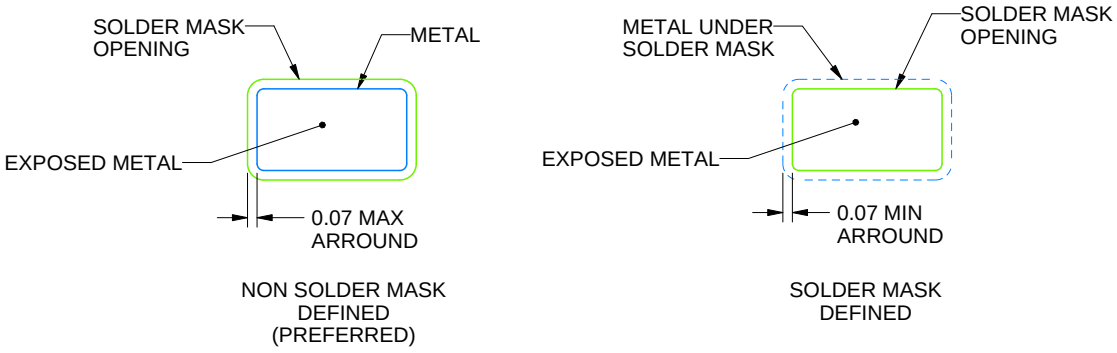
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

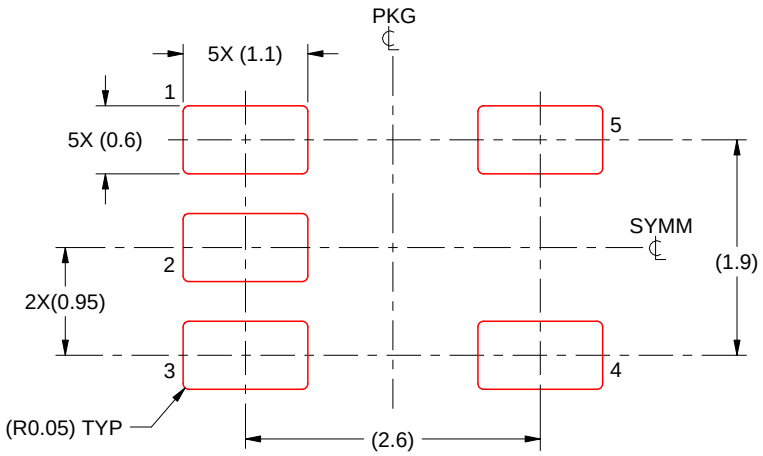


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

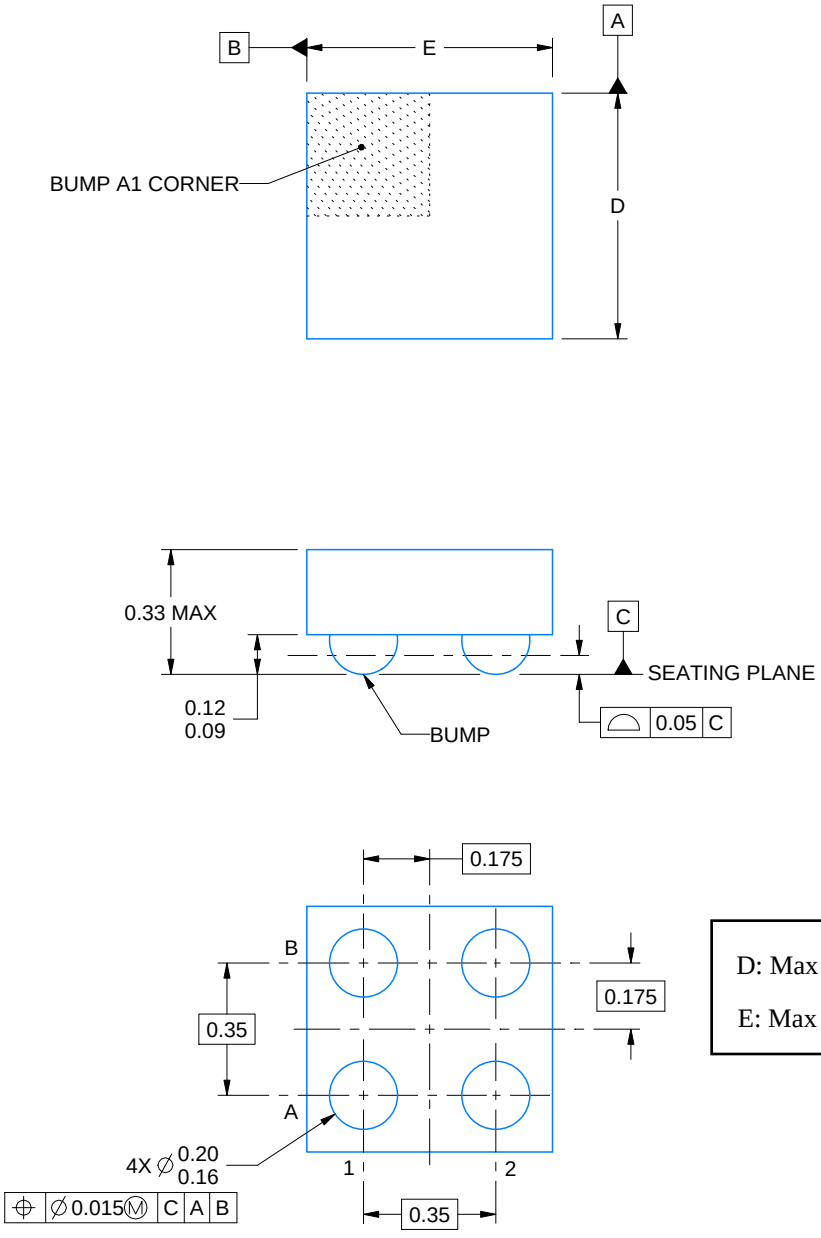
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YKG0004

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



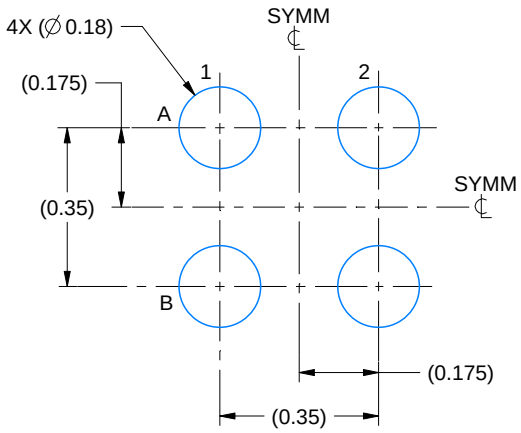
D: Max = 0.675 mm, Min =0.615 mm

E: Max = 0.675 mm, Min =0.615 mm

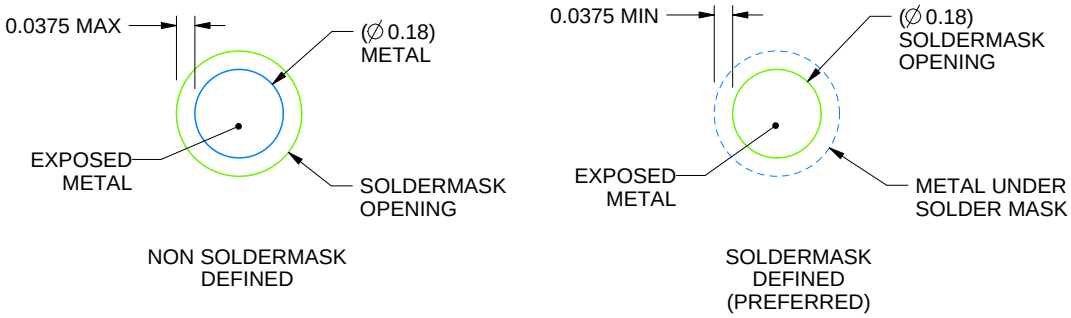
4218366/E 05/2020

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

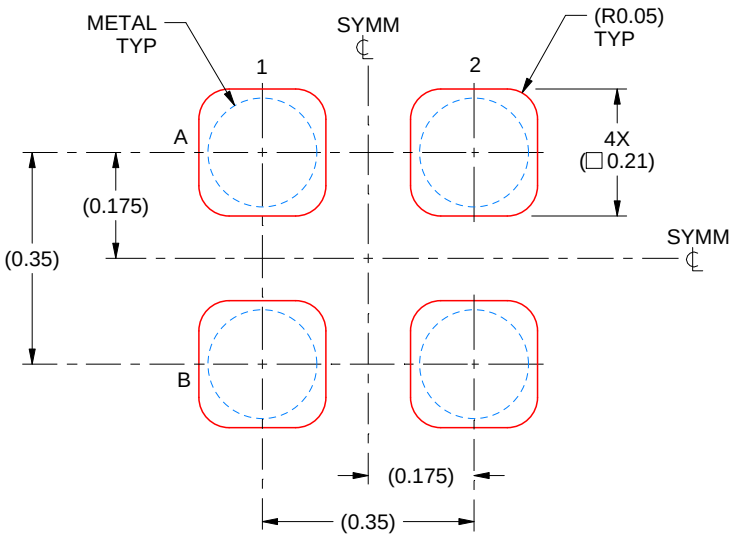


SOLDERMASK DETAILS
NOT TO SCALE

4218366/E 05/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

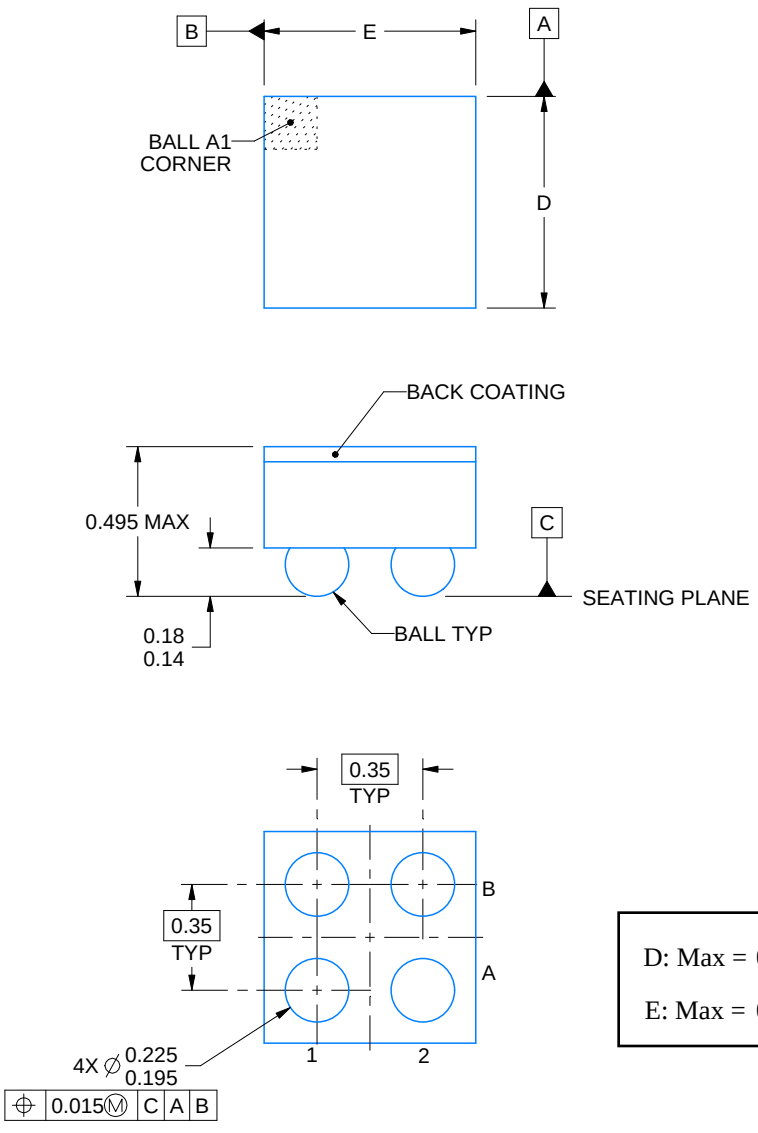


SOLDERPASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE:80X

4218366/E 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



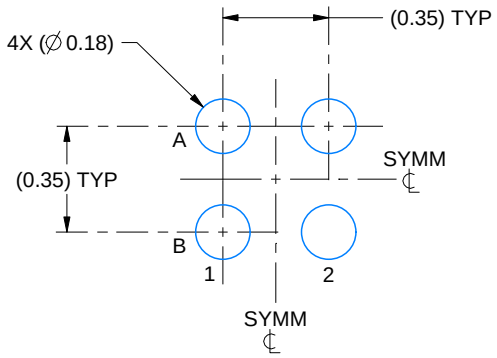
D: Max = 0.675 mm, Min =0.615 mm

E: Max = 0.675 mm, Min =0.615 mm

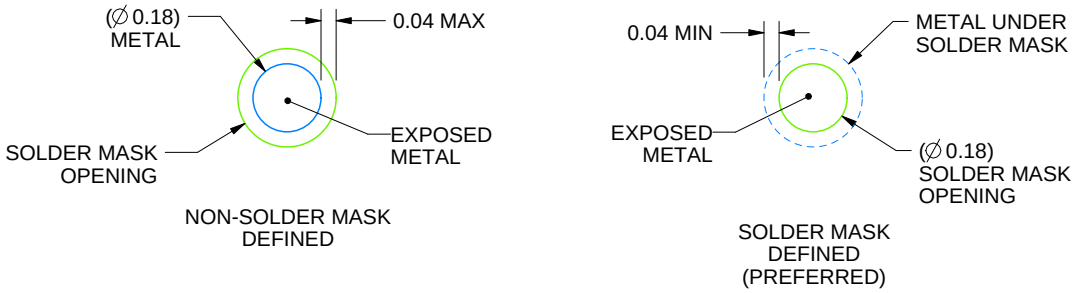
4223494/A 11/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223494/A 11/2014

NOTES: (continued)

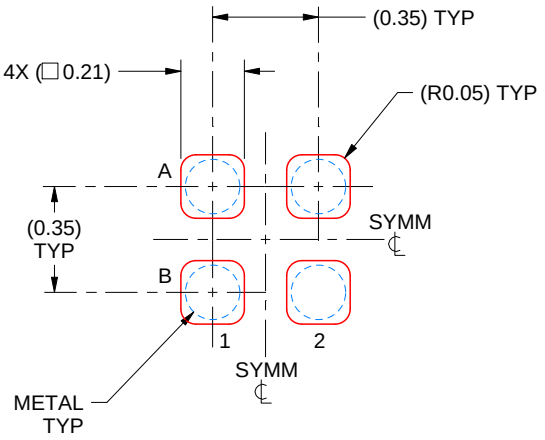
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKM0004

DSBGA - 0.495 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

4223494/A 11/2014

NOTES: (continued)

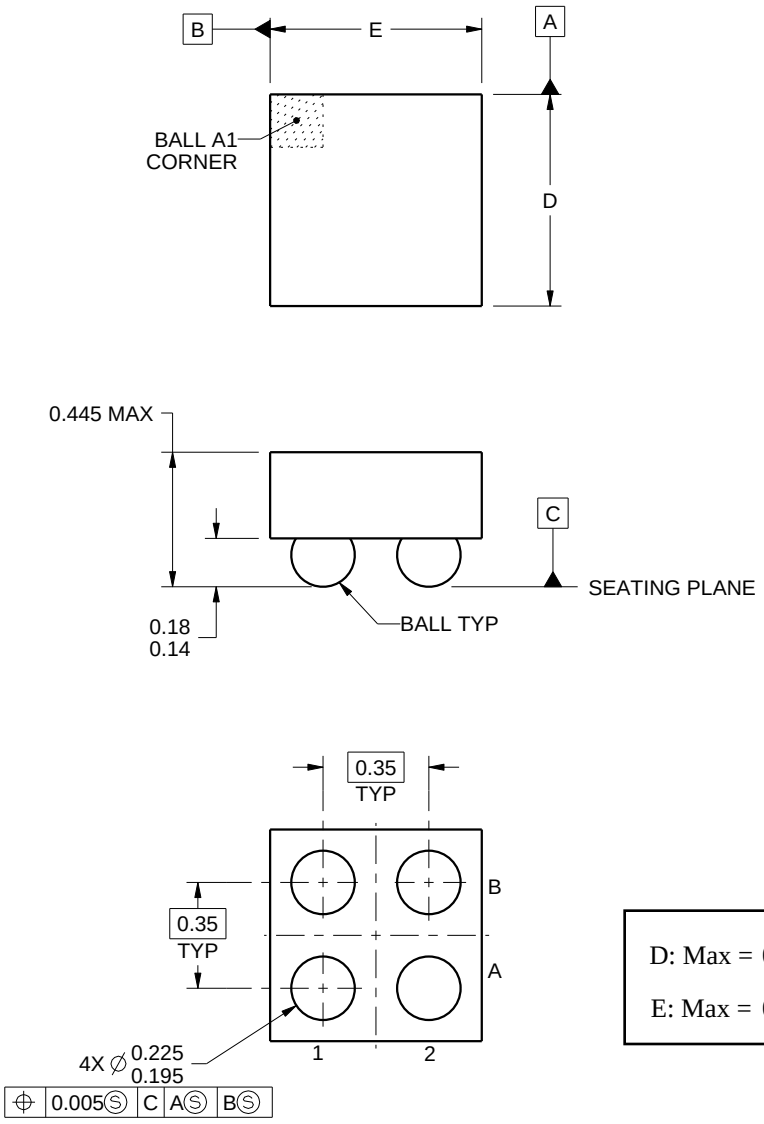
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min =0.615 mm

E: Max = 0.675 mm, Min =0.615 mm

4220102/A 11/2014

NOTES:

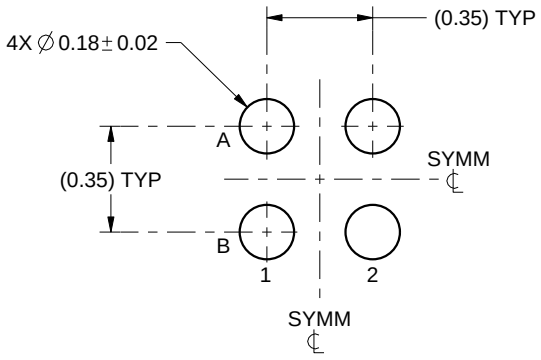
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

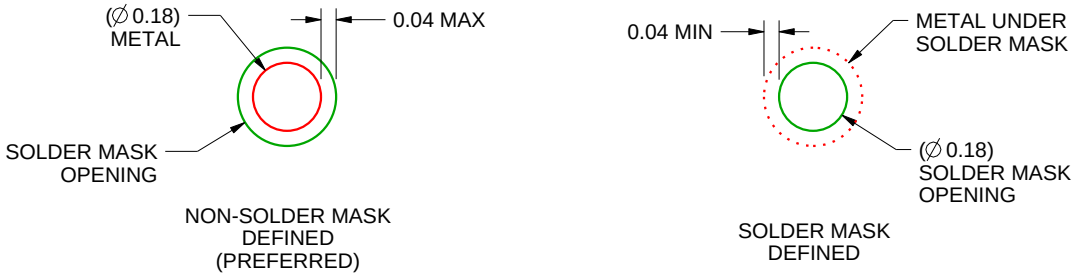
YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4220102/A 11/2014

NOTES: (continued)

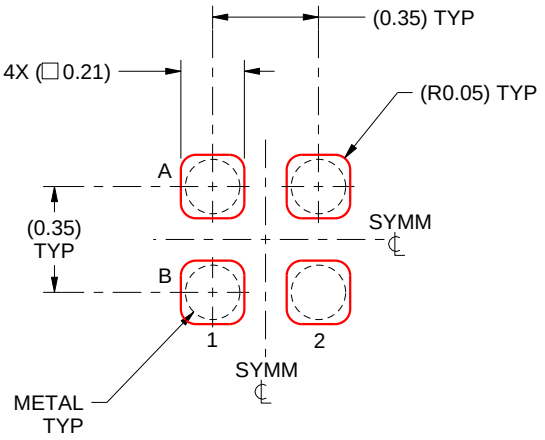
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

4220102/A 11/2014

NOTES: (continued)

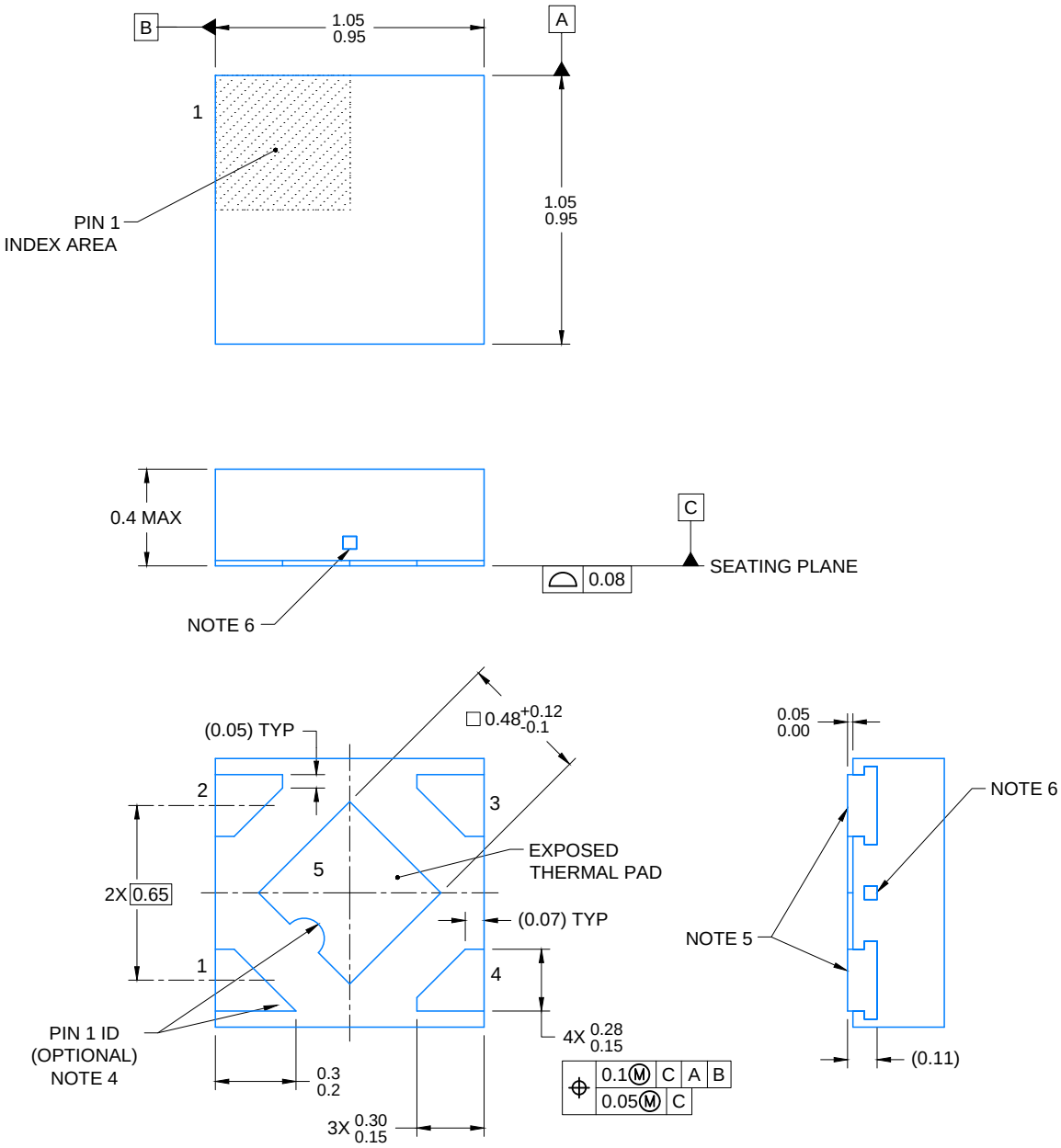
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DQN0004A

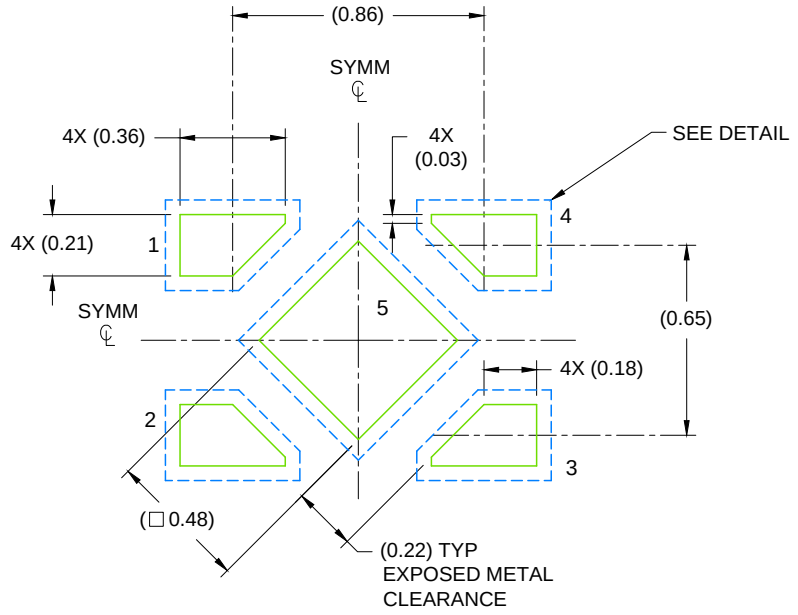
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



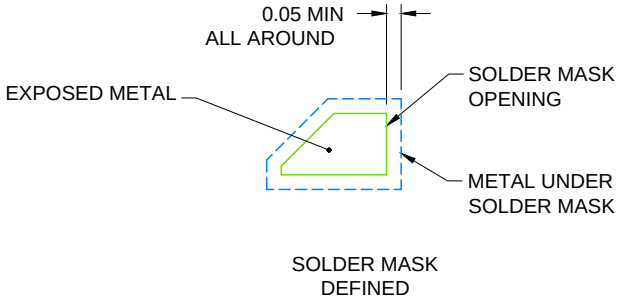
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

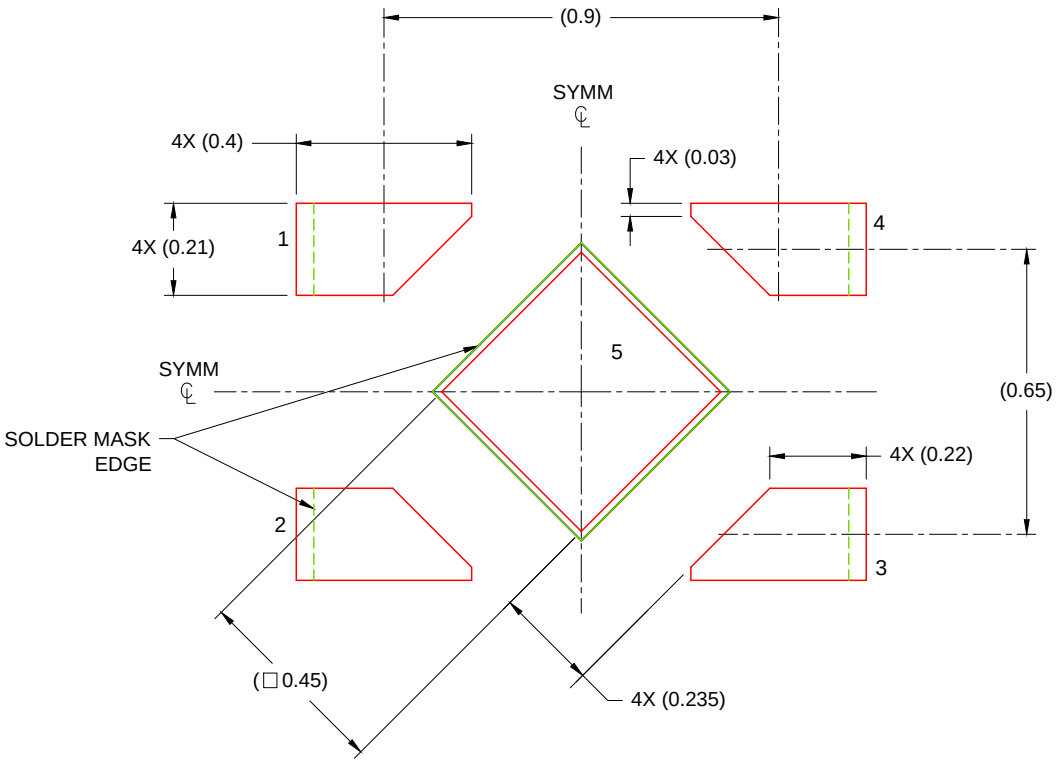


SOLDER MASK DETAIL

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NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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