# LP38513-ADJ 3A Fast-Transient Response Adjustable Low-Dropout Linear Voltage Regulator

**Check for Samples: LP38513-ADJ**

## FEATURES

- **2.25V to 5.5V Input Voltage Range**
- **Adjustable Output Voltage Range of 0.5V to 4.5V**
- **3.0A Output Load Current**
- **±2.0% Accuracy over Line, Load, and Full-Temperature Range from -40°C to +125°C**
- **Stable with tiny 10 µF ceramic capacitors**
- **Enable pin**
- **Typically less than 1 µA of Ground pin current when Enable pin is low**
- **25dB of PSRR at 100 kHz**
- **Over-Temperature and Over-Current Protection**
- **TO-263 THIN 5-Pin Surface Mount Package**

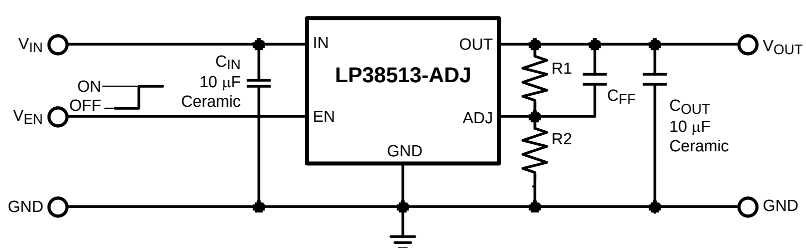
## APPLICATIONS

- **Digital Core ASICs, FPGAs, and DSPs**
- **Servers**
- **Routers and Switches**
- **Base Stations**
- **Storage Area Networks**
- **DDR2 Memory**

## DESCRIPTION

The LP38513-ADJ Fast-Transient Response Low-Dropout Voltage Regulator offers the highest-performance in meeting AC and DC accuracy requirements for powering Digital Cores. The LP38513-ADJ uses a proprietary control loop that enables extremely fast response to change in line conditions and load demands. Output Voltage DC accuracy at 2.5% over line, load and full temperature range from -40°C to +125°C. The LP38513-ADJ is designed for inputs from the 2.5V, 3.3V, and 5.0V rail, is stable with 10 µF ceramic capacitors, and has an adjustable output voltage. The LP38513-ADJ provides excellent transient performance to meet the demand of high performance digital core ASICs, DSPs, and FPGAs found in highly-intensive applications such as servers, routers/switches, and base stations.

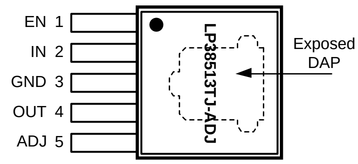
### Typical Application Circuit



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**Connection Diagram**
**Top View**




**See Package Number NDQ0005A**

### Pin Descriptions for TO-263 THIN Package

| Pin # | Pin Name | Function |
|---|---|---|
| 1 | EN | Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven. |
| 2 | IN | Input Supply Pin |
| 3 | GND | Ground |
| 4 | OUT | Regulated Output Voltage Pin |
| 5 | ADJ | The feedback to the internal Error Amplifier to set the output voltage |
| DAP | DAP | The TO-263 THIN DAP connection is used as a thermal connection to remove heat from the device to an external heat-sink in the form of the copper area on the printed circuit board. The DAP is physically connected to backside of the die, but is not internally connected to device ground. The DAP should be soldered to the Ground Plane copper.. |

## ABSOLUTE MAXIMUM RATINGS [(1)]

| | |
|---|---|
| Storage Temperature Range | −65°C to +150°C |
| Soldering Temperature [(2)] | |
| Thin TO-263 | 260°C, 10s |
| ESD Rating [(3)] | ±2 kV |
| Power Dissipation [(4)] | Internally Limited |
| Input Pin Voltage (Survival) | -0.3V to +6.0V |
| Enable Pin Voltage (Survival) | -0.3V to +6.0V |
| Output Pin Voltage (Survival) | -0.3V to +6.0V |
| ADJ Pin Voltage (Survival) | -0.3V to +6.0V |
| $I_{OUT}$ (Survival) | Internally Limited |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not specific performance limits. For specifications and conditions, see the Electrical Characteristics.
(2) Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperatures and times are for Sn-Pb (STD) only.
(3) The human body model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22-A114.
(4) Device operation must be evaluated, and derated as needed, based on ambient temperature ($T_A$), power dissipation ($P_D$), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance ($\theta_{JA}$). The typical $\theta_{JA}$ rating given is worst case based on minimum land area on two-layer PCB (EIA/JESD51-3). See POWER DISSIPATION/HEAT-SINKING for details.

## OPERATING RATINGS [(1)]

| | |
|---|---|
| Input Supply Voltage, $V_{IN}$ | 2.25V to 5.5V |
| Output Voltage, $V_{OUT}$ | $V_{ADJ}$ to 5V |
| Enable Input Voltage, $V_{EN}$ | 0.0V to 5.5V |
| Output Current (DC) | 1 mA to 3A |
| Junction Temperature [(2)] | −40°C to +125°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not specific performance limits. For specifications and conditions, see the Electrical Characteristics.
(2) Device operation must be evaluated, and derated as needed, based on ambient temperature ($T_A$), power dissipation ($P_D$), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance ($\theta_{JA}$). The typical $\theta_{JA}$ rating given is worst case based on minimum land area on two-layer PCB (EIA/JESD51-3). See POWER DISSIPATION/HEAT-SINKING for details.

## ELECTRICAL CHARACTERISTICS

Unless otherwise specified: $V_{IN}$= 2.50V, $V_{OUT}$ = $V_{ADJ}$, $I_{OUT}$= 10 mA, $C_{IN}$= 10 µF, $C_{OUT}$= 10 µF, $V_{EN}$= 2.0V. Limits in standard type are for $T_J$= 25°C only; limits in **boldface type** apply over the junction temperature ($T_J$) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$= 25°C, and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ADJ}$ | $V_{ADJ}$ Accuracy (1) | 2.25V ≤ $V_{IN}$ ≤ 5.5V<br>10 mA ≤ $I_{OUT}$ ≤ 3A | 495.0<br>**490.0** | 500. | 505.0<br>**510.0** | mV |
| $I_{ADJ}$ | ADJ Pin Bias Current | 2.25V ≤ $V_{IN}$ ≤ 5.5V | - | 1 | - | nA |
| $\Delta V_{ADJ}/\Delta V_{IN}$ | $V_{ADJ}$ Line Regulation (2) (1) | 2.25V ≤ $V_{IN}$ ≤ 5.5V | - | 0.03<br>**0.06** | - | %/V |
| $\Delta V_{ADJ}/\Delta I_{OUT}$ | $V_{ADJ}$ Load Regulation (3) (1) | 10 mA ≤ $I_{OUT}$ ≤ 3A | - | 0.15<br>**0.20** | - | %/A |
| $V_{DO}$ | Dropout Voltage (4) | $I_{OUT}$ = 3A | - | - | **470** | mV |
| $I_{GND}$ | Ground Pin Current, Output Enabled | $I_{OUT}$ = 10 mA | - | 8 | 10<br>**12** | mA |
| | | $I_{OUT}$ = 3A | - | 12 | 14<br>**16** | |
| | Ground Pin Current, Output Disabled | $V_{EN}$ = 0.50V | - | 1 | 5<br>**10** | µA |
| $I_{SC}$ | Short Circuit Current | $V_{OUT}$ = 0V | - | 5.2 | - | A |
| **Enable Input** | | | | | | |
| $V_{EN(ON)}$ | Enable ON Voltage Threshold | $V_{EN}$ rising from <0.5V until $V_{OUT}$ = ON | 0.90<br>**0.80** | 1.20 | 1.50<br>**1.60** | V |
| $V_{EN(OFF)}$ | Enable OFF Voltage Threshold | $V_{EN}$ falling from 1.6V until $V_{OUT}$ = OFF | 0.70<br>**0.60** | 1.00 | 1.30<br>**1.40** | |
| $V_{EN(HYS)}$ | Enable Voltage Hysteresis | $V_{EN(ON)}$ - $V_{EN(OFF)}$ | - | 200 | - | mV |
| $I_{EN}$ | Enable Pin Current | $V_{EN}$ = $V_{IN}$ | - | 1 | - | nA |
| | | $V_{EN}$ = 0V | - | -1 | - | |
| $t_{d(OFF)}$ | Turn-off delay | Time from $V_{EN}$ < $V_{EN(TH)}$ to $V_{OUT}$ = OFF, $I_{LOAD}$ = 3A | - | 5 | - | µs |
| $t_{d(ON)}$ | Turn-on delay | Time from $V_{EN}$ >$V_{EN(TH)}$ to $V_{OUT}$ = ON, $I_{LOAD}$ = 3A | - | 5 | - | |
| **AC Parameters** | | | | | | |
| PSRR | Ripple Rejection | $V_{IN}$ = 2.5V<br>f = 120Hz | - | 73 | - | dB |
| | | $V_{IN}$ = 2.5V<br>f = 1 kHz | - | 70 | - | |
| $\rho_{n(l/f)}$ | Output Noise Density | f = 120Hz | - | 0.4 | - | µV/√Hz |
| $e_n$ | Output Noise Voltage | BW = 10Hz - 100kHz | - | 25 | - | $\mu V_{RMS}$ |
| **Thermal Characteristics** | | | | | | |
| $T_{SD}$ | Thermal Shutdown | $T_J$ rising | - | 165 | - | °C |
| $\Delta T_{SD}$ | Thermal Shutdown Hysteresis | $T_J$ falling from $T_{SD}$ | - | 10 | - | |
| $\theta_{J\text{-}A}$ | Thermal Resistance Junction to Ambient (5) | TO-263 THIN | - | 67 | - | °C/W |
| $\theta_{J\text{-}C}$ | Thermal Resistance Junction to Case | TO-263 THIN | - | 2 | - | °C/W |

(1) The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
(2) Line regulation is defined as the change in $V_{ADJ}$ from the nominal value due to change in the voltage at the input.
(3) Load regulation is defined as the change in $V_{ADJ}$ from the nominal value due to change in the load current at the output.
(4) Dropout voltage ($V_{DO}$) is typically defined as the input to output voltage differential ($V_{IN}$ - $V_{OUT}$) where the input voltage is low enough to cause the output voltage to drop 2%. For the LP38513-ADJ, the minimum operating voltage of 2.25V is the limiting factor when the programed output voltage is less than typically 1.80V.
(5) Device operation must be evaluated, and derated as needed, based on ambient temperature ($T_A$), power dissipation ($P_D$), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance ($\theta_{JA}$). The typical $\theta_{JA}$ rating given is worst case based on minimum land area on two-layer PCB (EIA/JESD51-3). See POWER DISSIPATION/HEAT-SINKING for details.

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = 2.50V, $V_{OUT}$ = $V_{ADJ}$, $V_{EN}$ = 2.0V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 10 mA.

**$V_{ADJ}$ vs Temperature**

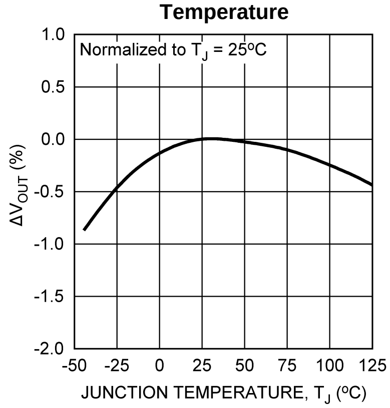



**Figure 1.**

**$V_{OUT}$ vs $V_{IN}$**

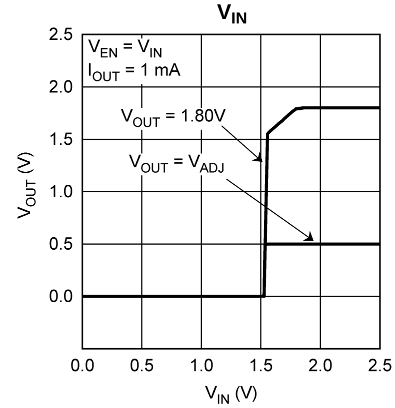



**Figure 2.**

**Ground Pin Current ($I_{GND}$) vs $V_{IN}$**

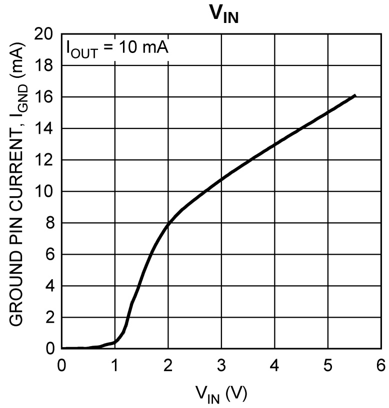



**Figure 3.**

**Ground Pin Current ($I_{GND}$) vs Temperature**

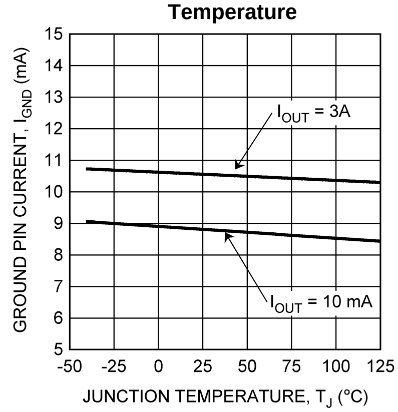



**Figure 4.**

**Ground Pin Current ($I_{GND}$) vs Temperature**

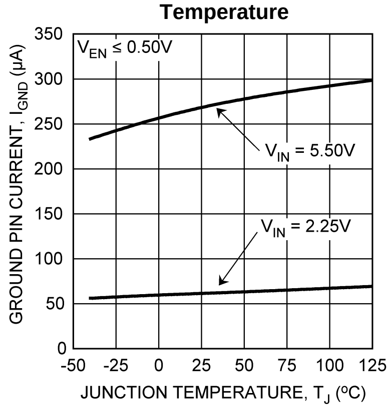



**Figure 5.**

**Enable Threshold vs Temperature**

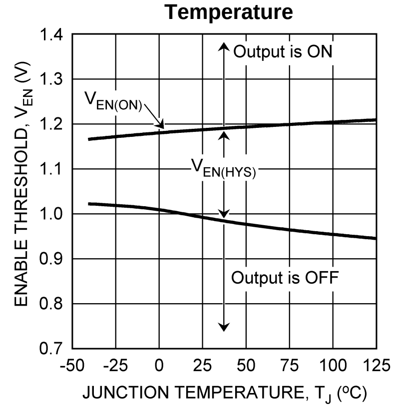



**Figure 6.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = 2.50V, $V_{OUT}$ = $V_{ADJ}$, $V_{EN}$ = 2.0V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 10 mA.

**$V_{OUT}$ vs $V_{EN}$**

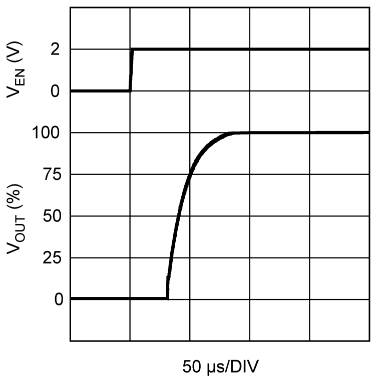



**Figure 7.**

**Load regulation vs Temperature**

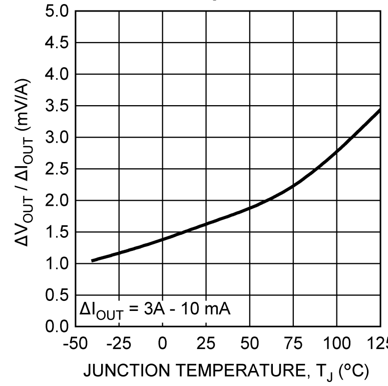



**Figure 8.**

**Line Regulation vs Temperature**

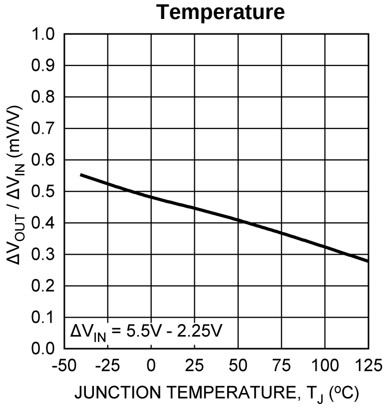



**Figure 9.**

**Current Limit vs Temperature**

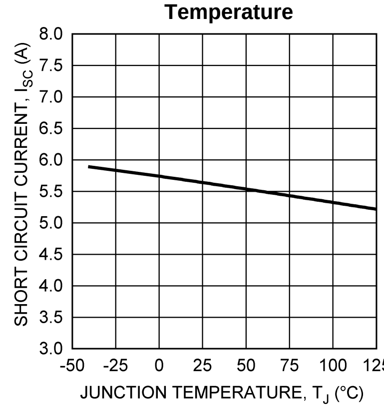



**Figure 10.**

**Load Transient, 10mA to 3A**
**$V_{OUT}$ = $V_{ADJ}$, $C_{OUT}$ = 10 µF Ceramic**

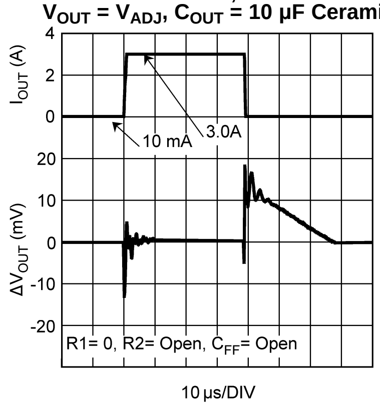



**Figure 11.**

**Load Transient, 10 mA to 3A**
**$V_{OUT}$ = 1.20V, $C_{OUT}$ = 10 µF Ceramic**

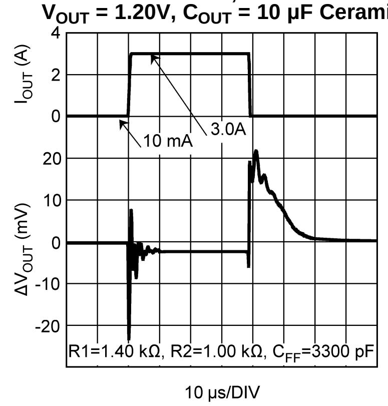



**Figure 12.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = 2.50V, $V_{OUT}$ = $V_{ADJ}$, $V_{EN}$ = 2.0V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 10 mA.

**Load Transient, 1A to 3A**
**$V_{OUT}$ = 1.20V, $C_{OUT}$ = 10 µF Ceramic**

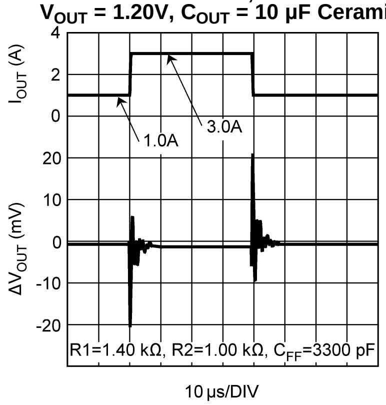



**Figure 13.**

**Line Transient**
**$V_{OUT}$ = $V_{ADJ}$, $C_{OUT}$ = 10 µF Ceramic**

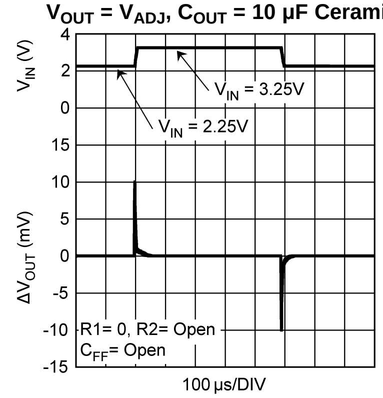



**Figure 14.**

**Line Transient**
**$V_{OUT}$ = 1.20V, $C_{OUT}$ = 10 µF Ceramic**

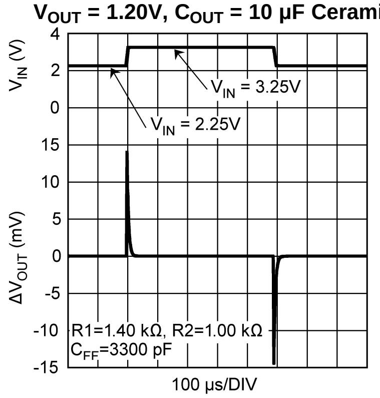



**Figure 15.**

**PSRR, $I_{OUT}$ = 100 mA**
**$V_{OUT}$ = $V_{ADJ}$, $C_{OUT}$ = 10 µF Ceramic**

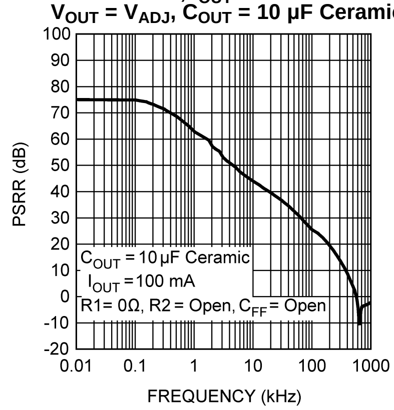



**Figure 16.**

**PSRR, $I_{OUT}$ = 3.0A**
**$V_{OUT}$ = $V_{ADJ}$, $C_{OUT}$ = 10 µF Ceramic**

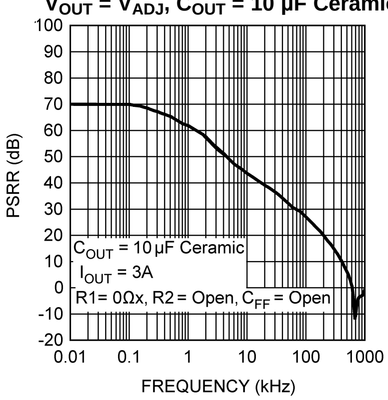



**Figure 17.**

**Output Noise Density**
**$V_{OUT}$ = $V_{ADJ}$, $C_{OUT}$ = 10 µF Ceramic**

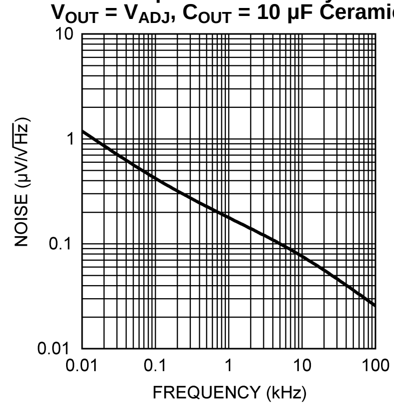
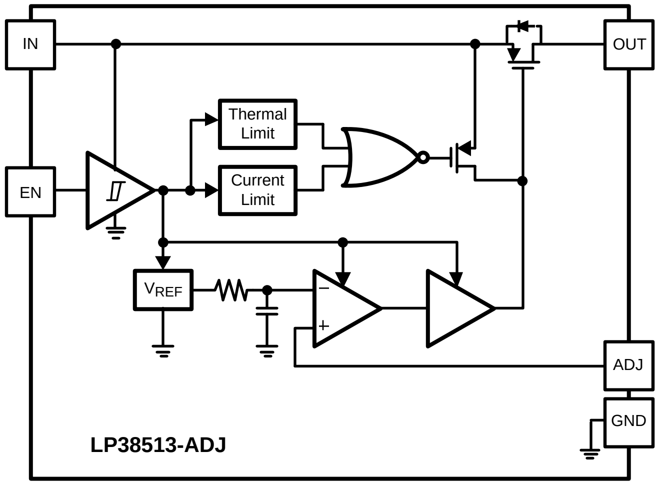



**Figure 18.**

## BLOCK DIAGRAM



## APPLICATION INFORMATION

## EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

### Input Capacitor

A ceramic input capacitor of at least 10 µF is required. For general usage across all load currents and operating conditions, a 10 µF ceramic input capacitor will provide satisfactory performance.

### Output Capacitor

A ceramic capacitor with a minimum value of 10 µF is required at the output pin for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pin using traces which have no other currents flowing through them. As long as the minimum of 10 µF ceramic is met, there is no limitation on any additional capacitance.

X7R and X5R dielectric ceramic capacitors are strongly recommended, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Z5U and Y5V dielectric ceramics are not recommended as the capacitance will drop severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

## Application Information

### REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when $V_{IN}$ is abruptly taken low and $C_{OUT}$ continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

While $V_{IN}$ is high enough to keep the control circuity alive, and the Enable pin is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. Since the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full on condition when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the Enable is low this condition will be prevented.

The internal PFET pass element in the LP38513-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output voltage to input voltage differential is more than 500 mV (typical) the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this protective clamp.

### SHORT-CIRCUIT PROTECTION

The LP38513-ADJ is short circuit protected, and in the event of a peak over-current condition the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the POWER DISSIPATION/HEAT-SINKING section for power dissipation calculations.

## SETTING THE OUTPUT VOLTAGE

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + (R1/R2)) \quad (1)$$

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of $V_{ADJ}$ is specified, the final value of $V_{OUT}$ is not. The use of low quality resistors for R1 and R2 can easily produce a $V_{OUT}$ value that is unacceptable.

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 1.00 kΩ. This is to reduce the possibility of any internal parasitic capacitances on the ADJ pin from creating an undesirable phase shift that may interfere with device stability.

$$( (R1 \times R2) / (R1 + R2) ) \leq 1.00\ k\Omega \quad (2)$$

## FEED FORWARD CAPACITOR, $C_{FF}$

When using a ceramic capacitor for $C_{OUT}$, the typical ESR value will be too small to provide any meaningful positive phase compensation, $F_Z$, to offset the internal negative phase shifts in the gain loop.

$$F_Z = 1 / (2 \times \pi \times C_{OUT} \times ESR) \quad (3)$$

A capacitor placed across the gain resistor R1 will provide additional phase margin to improve load transient response of the device. This capacitor, $C_{FF}$, in parallel with R1, will form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (4)$$

For optimum load transient response select $C_{FF}$ so the zero frequency, $F_Z$, falls between 20 kHz and 40 kHz.

$$C_{FF} = 1 / (2 \times \pi \times R1 \times F_Z) \quad (5)$$

The phase lead provided by $C_{FF}$ diminishes as the DC gain approaches unity, or $V_{OUT}$ approaches $V_{ADJ}$. This is because $C_{FF}$ also forms a pole with a frequency of:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times (R1 \parallel R2) ) \quad (6)$$

It's important to note that at higher output voltages, where R1 is much larger than R2, the pole and zero are far apart in frequency. At lower output voltages the frequency of the pole and the zero mover closer together. The phase lead provided from $C_{FF}$ diminishes quickly as the output voltage is reduced, and has no effect when $V_{OUT}$ = $V_{ADJ}$. For this reason, relying on this compensation technique alone is adequate only for higher output voltages.

Table 1 lists some suggested, best fit, standard ±1% resistor values for R1 and R2, and a standard ±10% capacitor values for $C_{FF}$, for a range of $V_{OUT}$ values. Other values of R1, R2, and $C_{FF}$ are available that will give similar results.

**Table 1.**

| $V_{OUT}$ | R1 | R2 | $C_{FF}$ | $F_Z$ |
|---|---|---|---|---|
| 0.80V | 1.07 kΩ | 1.78 kΩ | 4700 pF | 31.6 kHz |
| 1.00V | 1.00 kΩ | 1.00 kΩ | 4700 pF | 33.8 kHz |
| 1.20V | 1.40 kΩ | 1.00 kΩ | 3300 pF | 34.4 kHz |
| 1.50V | 2.00 kΩ | 1.00 kΩ | 2700 pF | 29.5 kHz |
| 1.80V | 2.94 kΩ | 1.13 kΩ | 1500 pF | 36.1 kHz |
| 2.00V | 1.02 kΩ | 340Ω | 4700 pF | 33.2 kHz |
| 2.50V | 1.02 kΩ | 255Ω | 4700 pF | 33.2 kHz |
| 3.00V | 1.00 kΩ | 200Ω | 4700 pF | 33.8 kHz |
| 3.30V | 2.00 kΩ | 357Ω | 2700 pF | 29.5 kHz |

Please refer to Application Note AN-1378 *Method For Calculating Output Voltage Tolerances in Adjustable Regulators* SNVA112 for additional information on how resistor tolerances affect the calculated $V_{OUT}$ value.

## ENABLE OPERATION

The Enable ON threshold is typically 1.2V, and the OFF threshold is typically 1.0V. To ensure reliable operation the Enable pin voltage must rise above the maximum $V_{EN(ON)}$ threshold and must fall below the minimum $V_{EN(OFF)}$ threshold. The Enable threshold has typically 200mV of hysteresis to improve noise immunity.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

If the Enable pin is driven from a single ended device (such as the collector of a discrete transistor) a pull-up resistor to $V_{IN}$, or a pull-down resistor to ground, will be required for proper operation. A 1 kΩ to 100 kΩ resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the pin should be connected directly to the adjacent $V_{IN}$ pin.

## POWER DISSIPATION/HEAT-SINKING

A heat-sink may be required depending on the maximum power dissipation ($P_{D(MAX)}$), maximum ambient temperature ($T_{A(MAX)}$)of the application, and the thermal resistance ($\theta_{JA}$) of the package. Under all possible conditions, the junction temperature ($T_J$) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ( (V_{IN} - V_{OUT}) \times I_{OUT}) + ((V_{IN}) \times I_{GND}) \quad (7)$$

where $I_{GND}$ is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise ($\Delta T_J$) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (8)$$

The maximum allowable value for junction to ambient Thermal Resistance, $\theta_{JA}$, can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)} \quad (9)$$

LP38513-ADJ is available in the TO-263 THIN surface mount package. For a comparison of the TO-263 THIN package to the standard TO-263 package see Application Note *AN-1797 TO-263 THIN Package* SNVA328. The thermal resistance depends on amount of copper area, or heat sink, and on air flow. See Application Note *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* SNVA183 for guidelines.

### *Heat-Sinking the TO-263 THIN Package*

The DAP of the TO-263 THIN package is soldered to the copper plane for heat sinking. The TO-263 THIN package has a $\theta_{JA}$ rating of 67°C/W, and a $\theta_{JC}$ rating of 2°C/W. The $\theta_{JA}$ rating of 67°C/W includes the device DAP soldered to an area of 0.055 square inches (0.22 in x 0.25 in) of 1 ounce copper on a two sided PCB, with no airflow. See JEDEC standard EIA/JESD51-3 for more information.

Figure 19 shows a curve for the $\theta_{JA}$ of TO-263 THIN package for different thermal via counts under the exposed DAP, using a four layer PCB for heat sinking. The thermal vias connect the copper area directly under the exposed DAP to the first internal copper plane only. See JEDEC standards EIA/JESD51-5 and EIA/JESD51-7 for more information.

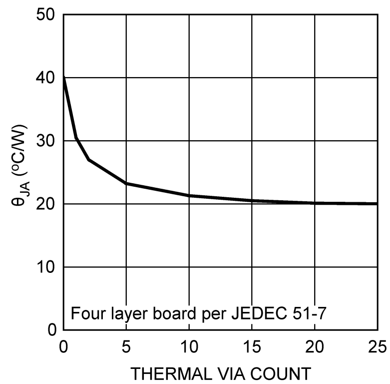



**Figure 19. $\theta_{JA}$ vs Thermal Via Count for the TO-263 THIN Package on 4–Layer PCB**

Figure 20 shows the thermal performance when the Thin TO-263 is mounted to a two layer PCB where the copper area is predominately directly under the exposed DAP. .As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement.

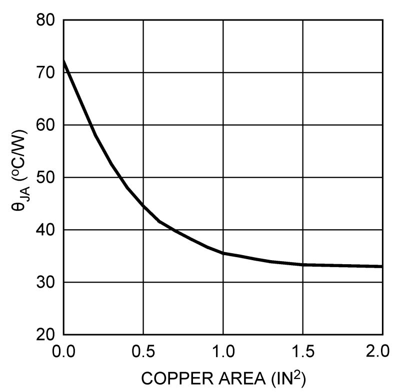



**Figure 20. $\theta_{JA}$ vs Copper Area for the TO-263 THIN Package**

# REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 12 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP38513TJ-ADJ/NOPB | ACTIVE | TO-263 | NDQ | 5 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LP38513<br>TJ-ADJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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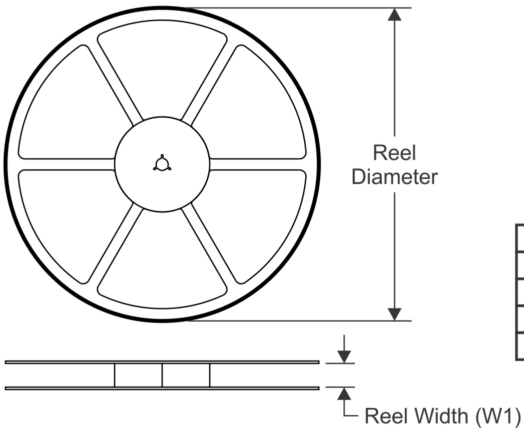
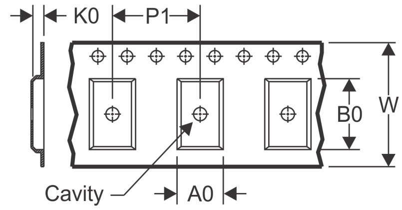
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

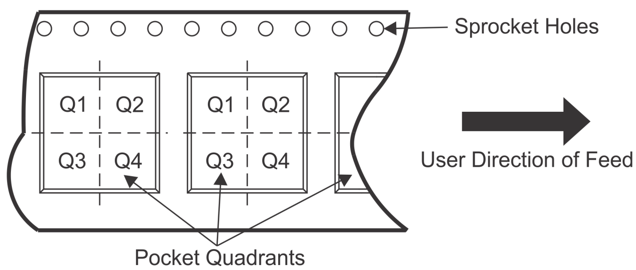



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

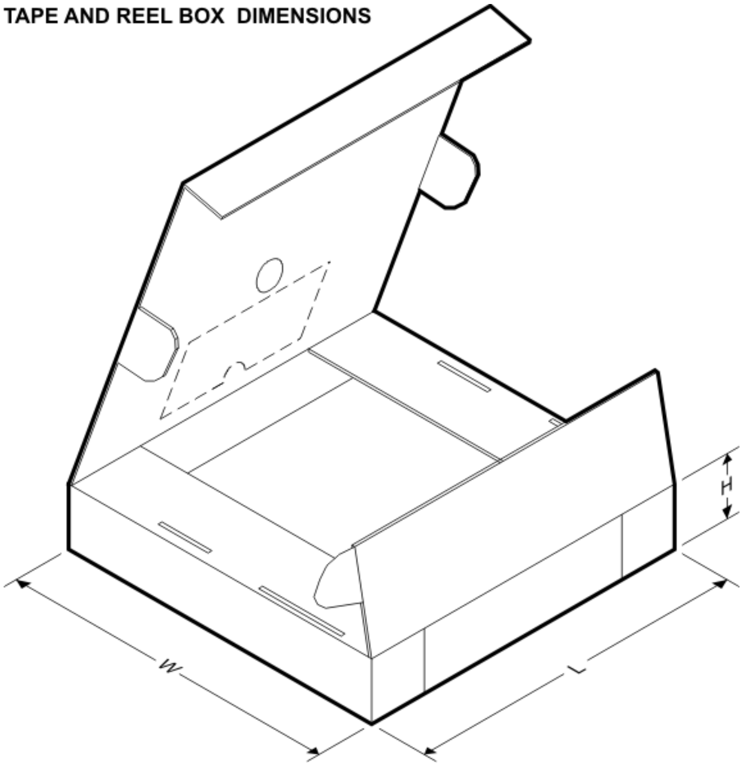
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP38513TJ-ADJ/NOPB | TO-263 | NDQ | 5 | 1000 | 330.0 | 24.4 | 10.6 | 15.4 | 2.45 | 12.0 | 24.0 | Q2 |

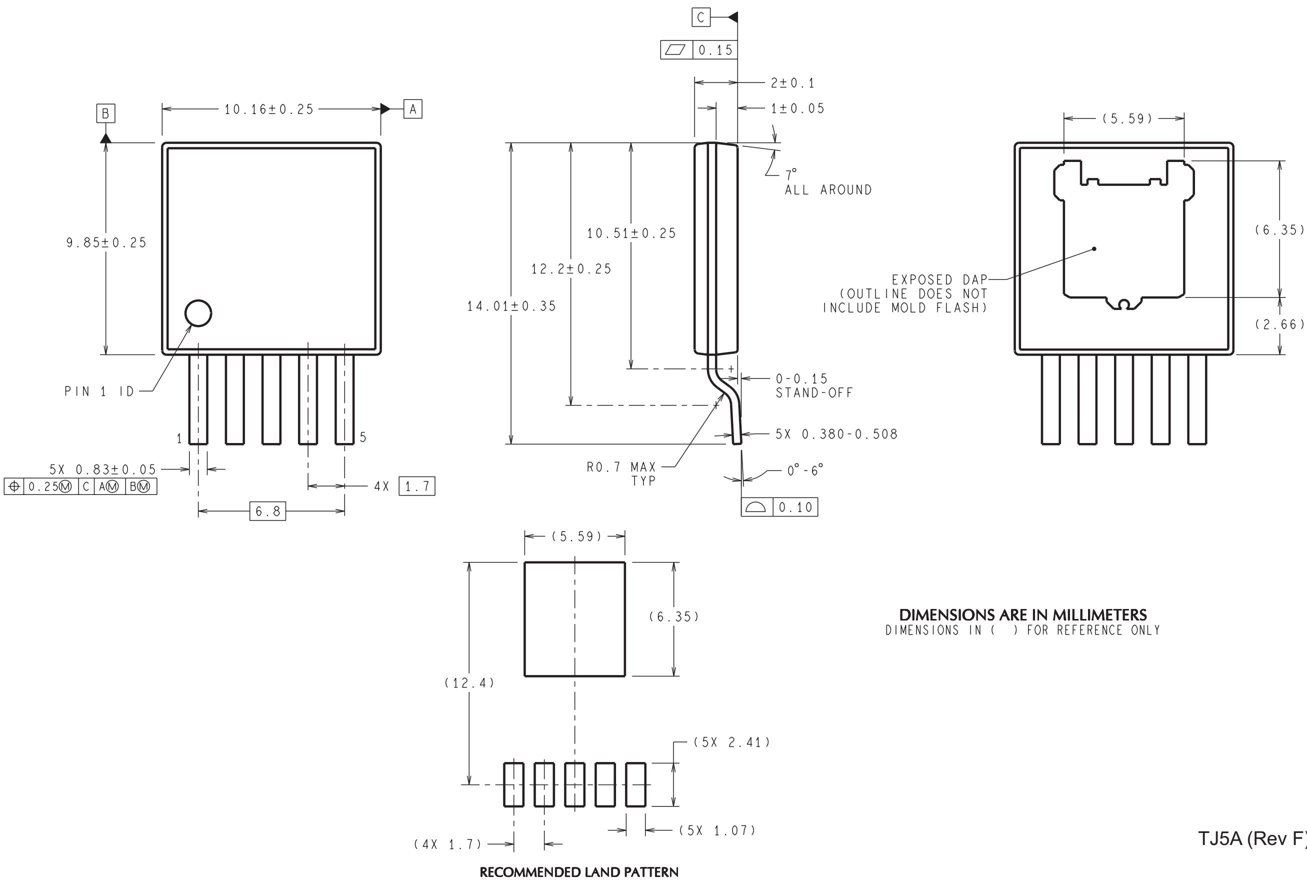
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP38513TJ-ADJ/NOPB | TO-263 | NDQ | 5 | 1000 | 367.0 | 367.0 | 35.0 |

# NDQ0005A




TJ5A (Rev F)

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