TPS37xx-Q1
双通道、低功耗、高精度电压检测器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 采用小型封装的双通道检测器
- 高精度阈值和滞后：1.0%
- 低静态电流：2μA（典型值）
- 可调节检测电压：最低至 1.2V
- 5% 和 10% 滞后选项
- 温度范围：-40°C 至 +125°C
- 推挽 (TPS3779-Q1) 和开漏 (TPS3780-Q1) 输出选项
- 采用 SOT-23 封装

2 应用

- 数字信号处理器 (DSP)、微控制器和微处理器
- 高级驾驶员辅助系统 (ADAS)
- 信息娱乐和仪表板
- 电源排序 应用

3 说明

TPS3779-Q1 和 TPS3780-Q1 属于高精度双通道电压检测器系列，同时拥有低功耗和小解决方案尺寸两大优势。SENSE1 和 SENSE2 输入包括滞后特性，可抑制短小毛刺脉冲，从而确保输出操作稳定而无错误触发。该器件提供了两种不同的出厂设置滞后选项：5% 或 10%。

TPS3779-Q1 和 TPS3780-Q1 配有可调节的 SENSEx 输入。这些输入可通过外部电阻分压器进行配置。当 SENSE1 和 SENSE2 输入上的电压低于下降阈值时，OUT1 和 OUT2 被分别驱动为低电平。当 SENSE1 和 SENSE2 上升到高于上升阈值时，OUT1 和 OUT2 分别变为高电平。

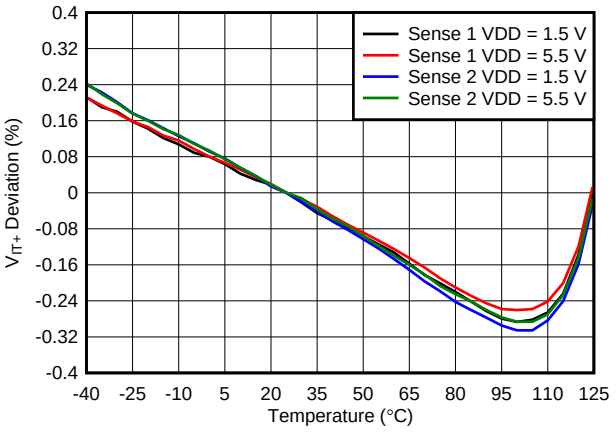
该器件的超低静态电流为 2μA（典型值），并且提供了一套精确且节省空间的电压检测解决方案，非常适合低功耗系统监视和便携式 输出电压电平信号。TPS3779-Q1 和 TPS3780-Q1 的工作电压范围为 1.5V 至 5.5V，工作温度范围为 –40°C 至 +125°C。

器件信息(1)

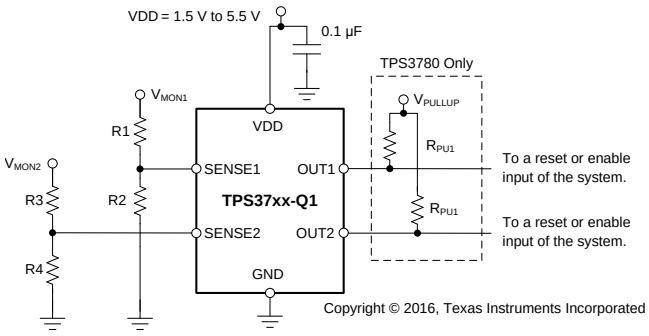
器件型号	封装	封装尺寸（标称值）
TPS37xx-Q1	SOT-23 (6)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

感测阈值 (V_{IT+}) 偏差与温度间的关系



典型电路原理图



Copyright © 2016, Texas Instruments Incorporated

目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 Device Comparison Table 3
6 Pin Configuration and Functions 3
7 Specifications 4
7.1 Absolute Maximum Ratings 4
7.2 ESD Ratings 4
7.3 Recommended Operating Conditions 4
7.4 Thermal Information 4
7.5 Electrical Characteristics 5
7.6 Timing Requirements 6
7.7 Typical Characteristics 7
8 Detailed Description 10
8.1 Overview 10
8.2 Functional Block Diagrams 10
8.3 Feature Description 11
8.4 Device Functional Modes 11
9 Application and Implementation 12
9.1 Application Information 12
9.2 Typical Applications 13
10 Power-Supply Recommendations 15
11 Layout 15
11.1 Layout Guidelines 15
11.2 Layout Example 15
12 器件和文档支持 16
12.1 器件支持 16
12.2 文档支持 16
12.3 接收文档更新通知 16
12.4 相关链接 16
12.5 社区资源 17
12.6 商标 17
12.7 静电放电警告 17
12.8 Glossary 17
13 机械、封装和可订购信息 17

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2016) to Revision A **Page**

- Added TPS3780A-Q1 row to *Device Comparison Table* 3
- Added TPS37xxA-Q1 row to V_{IT-} parameter in *Electrical Characteristics* table 5

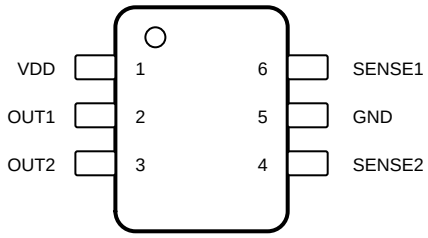
Copyright © 2016, Texas Instruments Incorporated

5 Device Comparison Table

PRODUCT	HYSTERESIS (%)	OUTPUT
TPS3779B-Q1	5	Push-pull
TPS3779C-Q1	10	Push-pull
TPS3780A-Q1	0.5	Open-drain
TPS3780B-Q1	5	Open-drain
TPS3780C-Q1	10	Open-drain

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Not to scale

Pin Functions

NAME	NO.	I/O	DESCRIPTION
GND	5	—	Ground
OUT1	2	O	OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below V_{IT-}. OUT1 is deasserted (goes high) after SENSE1 rises higher than V_{IT+}. OUT1 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.
OUT2	3	O	OUT2 is the output for SENSE2. OUT2 is asserted (driven low) when the voltage at SENSE2 falls below V_{IT-}. OUT2 is deasserted (goes high) after SENSE2 rises higher than V_{IT+}. OUT2 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.
SENSE1	6	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT1 is asserted.
SENSE2	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT2 is asserted.
VDD	1	I	Supply voltage input. Connect a 1.5-V to 5.5-V supply to VDD in order to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin (required for VDD < 1.5 V).

Copyright © 2016, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	7	V
	OUT1, OUT2 (TPS3779-Q1 only)	–0.3	VDD + 0.3	
	OUT1, OUT2 (TPS3780-Q1 only)	–0.3	7	
	SENSE1, SENSE2	–0.3	7	
Current	OUT1, OUT2		±20	mA
Temperature	Operating junction, T_J(2)	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For low-power devices, the junction temperature rise above the ambient temperature is negligible; therefore, the junction temperature is considered equal to the ambient temperature ($T_J = T_A$).

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Power-supply voltage		1.5		5.5	V
	Sense voltage	SENSE1, SENSE2	0		5.5	V
	Output voltage (TPS3779-Q1 only)	OUT1, OUT2	0		VDD + 0.3	V
	Output voltage (TPS3780-Q1 only)	OUT1, OUT2	0		5.5	V
R_{PU}	Pullup resistor (TPS3780-Q1 only)		1.5		10,000	kΩ
	Current	OUT1, OUT2	–5		5	mA
C_{IN}	Input capacitor			0.1		µF
T_J	Junction temperature		–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS3779-Q1, TPS3780-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2016, Texas Instruments Incorporated

7.5 Electrical Characteristics

all specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.5 V ≤ VDD ≤ 5.5 V (unless otherwise noted); typical values are at T_J = 25°C and VDD = 3.3 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDD	Input supply range			1.5		5.5	V
$V_{(POR)}$	Power-on-reset voltage(1)	V_{OL} (max) = 0.2 V, I_{OL} = 15 µA				0.8	V
I_{DD}	Supply current (into VDD pin)	VDD = 3.3 V, no load			2.09	5.80	µA
		VDD = 5.5 V, no load			2.29	6.50	
V_{IT+}	Positive-going input threshold voltage	$V_{(SENSEx)}$ rising			1.194		V
				–1%		1%	
$V_{IT–}$	Negative-going input threshold voltage	$V_{(SENSEx)}$ falling	TPS37xxA-Q1 (0.5% hysteresis)		1.188		V
			TPS37xxB-Q1 (5% hysteresis)		1.134		
			TPS37xxC-Q1 (10% hysteresis)		1.074		
		$V_{(SENSEx)}$ falling		–1%		1%	
$I_{(SENSEx)}$	Input current	$V_{(SENSEx)}$ = 0 V or VDD		–15		15	nA
V_{OL}	Low-level output voltage	VDD ≥ 1.5 V, I_{SINK} = 0.4 mA				0.25	V
		VDD ≥ 2.7 V, I_{SINK} = 2 mA				0.25	
		VDD ≥ 4.5 V, I_{SINK} = 3.2 mA				0.30	
V_{OH}	High-level output voltage (TPS3779-Q1 only)	VDD ≥ 1.5 V, I_{SOURCE} = 0.4 mA		0.8 VDD			V
		VDD ≥ 2.7 V, I_{SOURCE} = 1 mA		0.8 VDD			
		VDD ≥ 4.5 V, I_{SOURCE} = 2.5 mA		0.8 VDD			
$I_{lkg(OD)}$	Open-drain output leakage current (TPS3780-Q1 only)	High impedance, $V_{(SENSEx)}$ = $V_{(OUTx)}$ = 5.5 V		–250		250	nA

(1) Outputs are undetermined below $V_{(POR)}$.

Copyright © 2016, Texas Instruments Incorporated

7.6 Timing Requirements

typical values are at T_J = 25°C and VDD = 3.3 V; SENSEx transitions between 0 V and 1.3 V

		MIN	NOM	MAX	UNIT
$t_{PD(r)}$	SENSEx (rising) to OUTx propagation delay		5.5		µs
$t_{PD(f)}$	SENSEx (falling) to OUTx propagation delay		10		µs
t_{SD}	Startup delay(1)		570		µs

(1) During power-on or when a VDD transient is below VDD(min), the outputs reflect the input conditions 570 µs after VDD transitions through VDD(min).

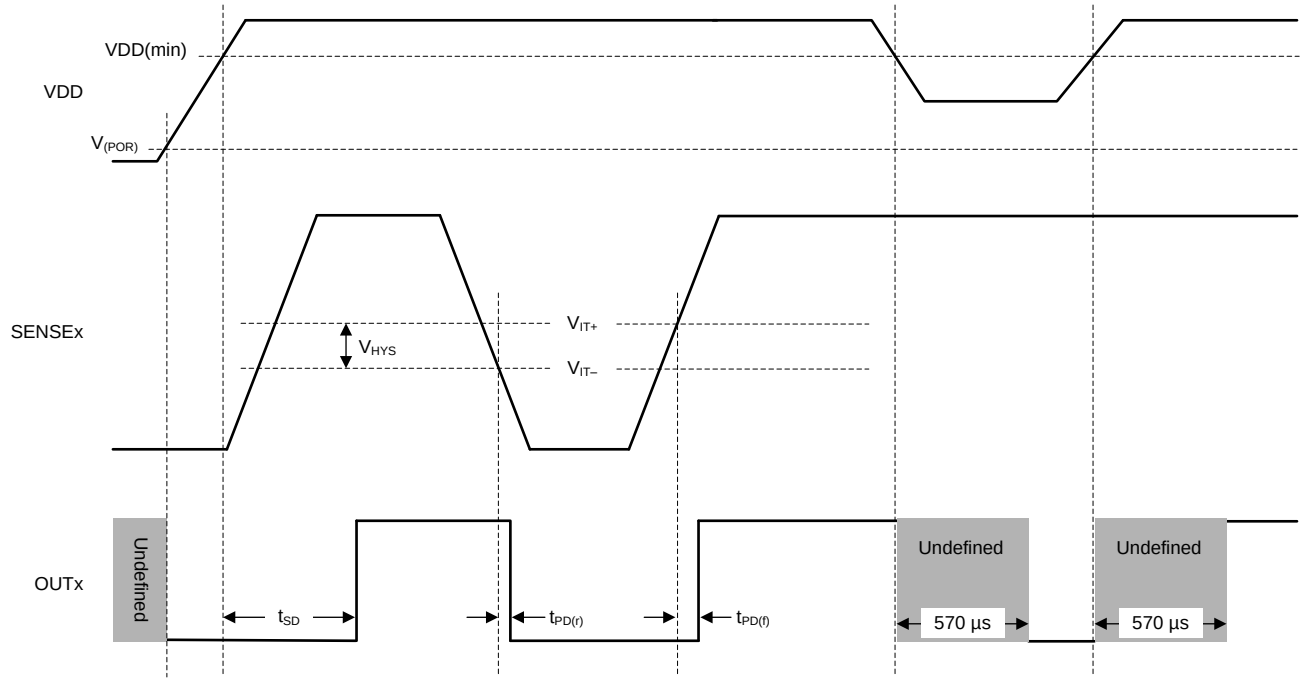


图 1. Timing Diagram

版权 © 2016, Texas Instruments Incorporated

7.7 Typical Characteristics

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)

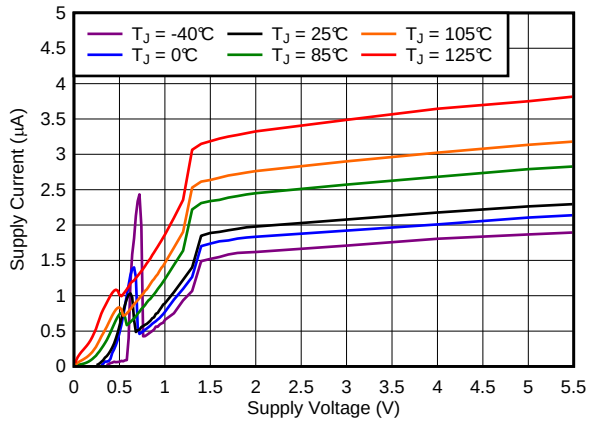


图 2. Supply Current vs Supply Voltage

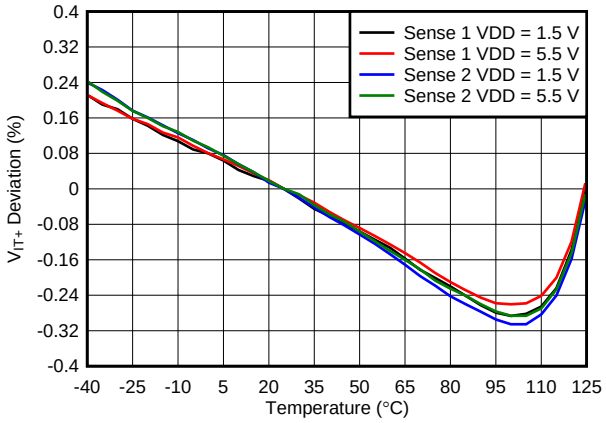


图 3. Sense Threshold (V_{IT+}) Deviation vs Temperature

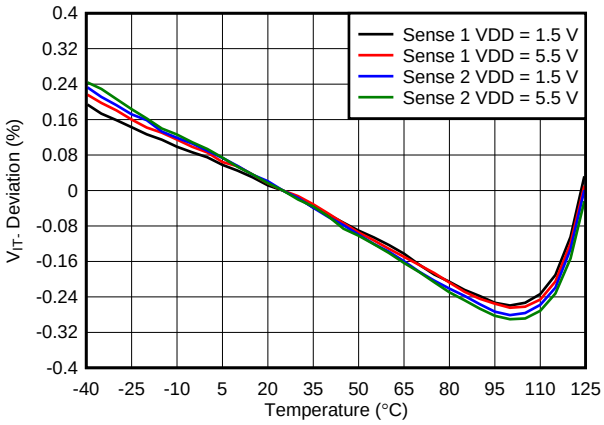


图 4. Sense Threshold (V_{IT-}) Deviation vs Temperature

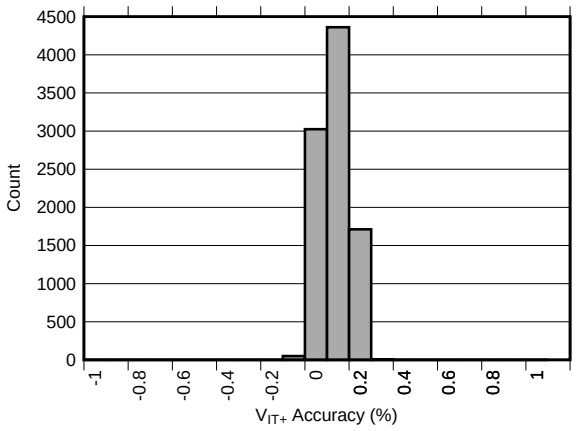


图 5. Sense Threshold (V_{IT+})

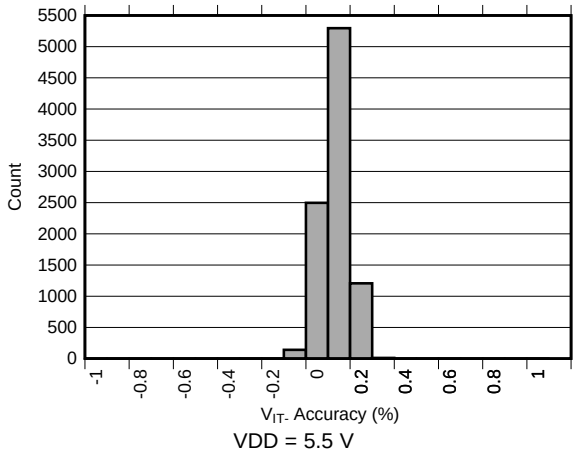


图 6. Sense Threshold (V_{IT-})

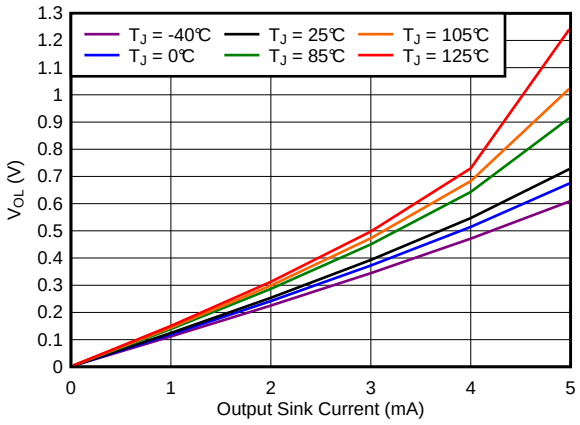


图 7. Output Voltage Low vs Output Current (VDD = 1.5 V)

Typical Characteristics (接下页)

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)

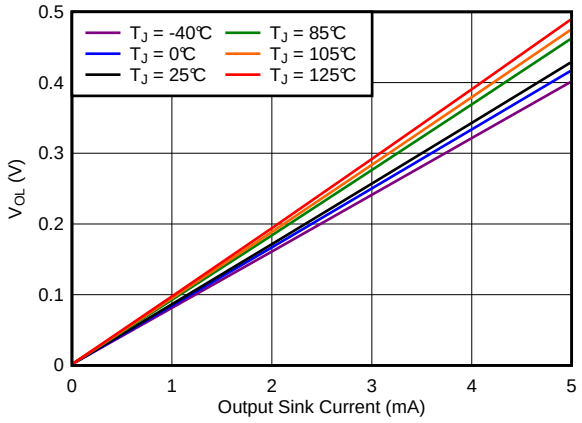


图 8. Output Voltage Low vs Output Current (VDD = 3.3 V)

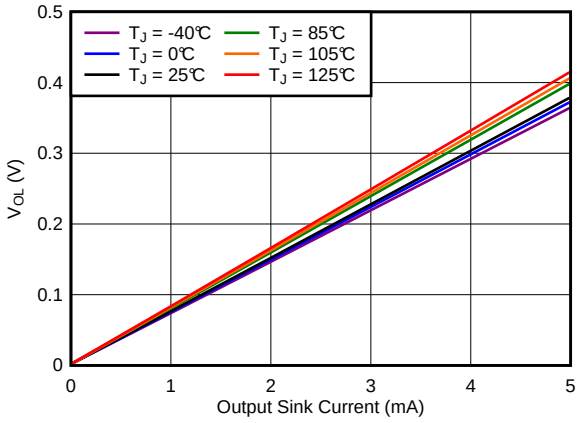


图 9. Output Voltage Low vs Output Current (VDD = 5.5 V)

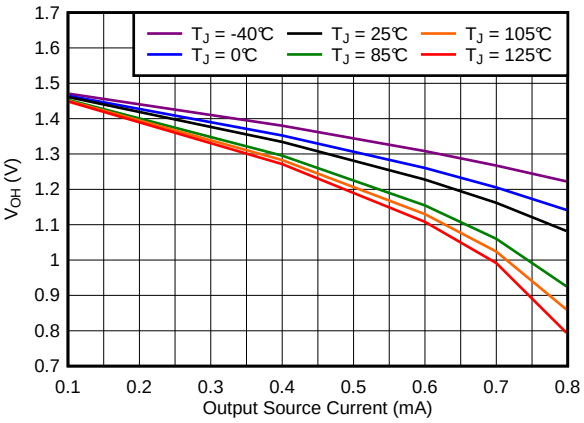


图 10. Output Voltage High vs Output Current (VDD = 1.5 V)

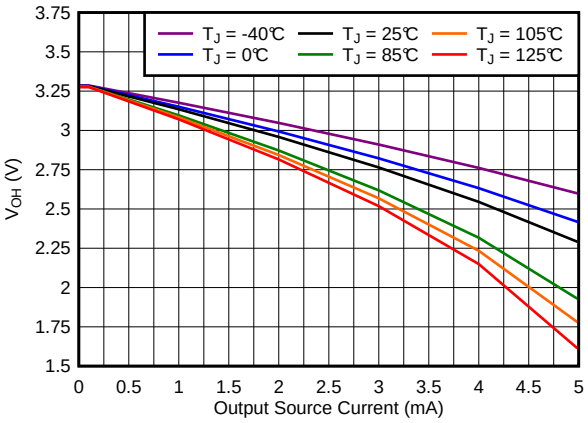


图 11. Output Voltage High vs Output Current (VDD = 3.3 V)

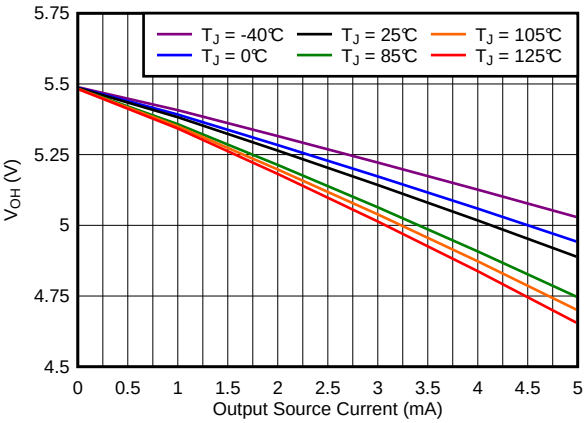
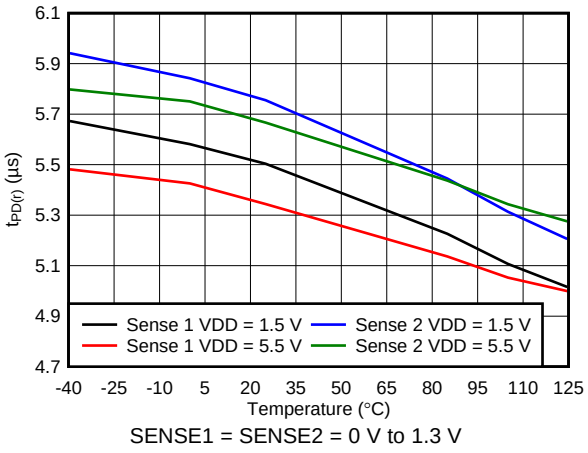


图 12. Output Voltage High vs Output Current (VDD = 5.5 V)



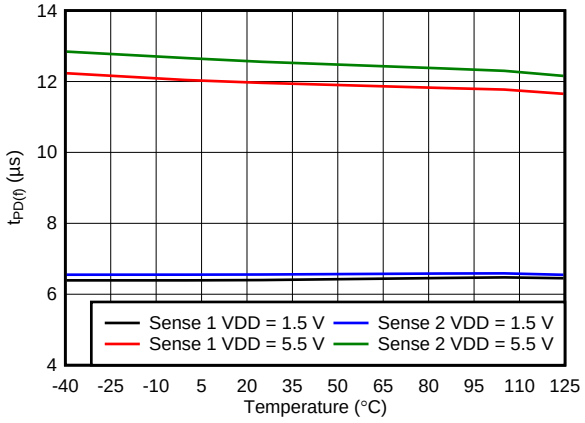
SENSE1 = SENSE2 = 0 V to 1.3 V

图 13. Propagation Delay from SENSEx High to Output High

版权 © 2016, Texas Instruments Incorporated

Typical Characteristics (接下页)

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)



SENSE1 = SENSE2 = 1.3 V to 0 V

图 14. Propagation Delay from SENSEx Low to Output Low

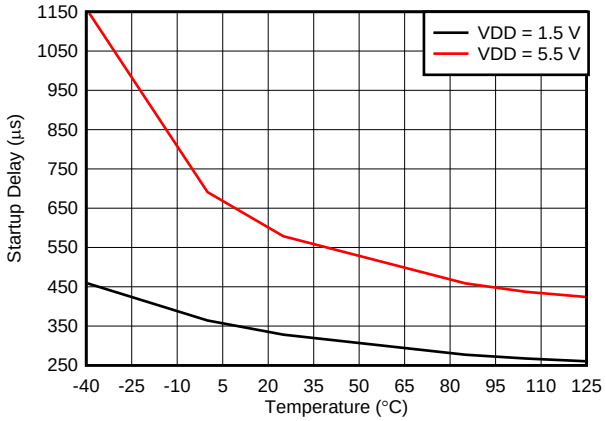
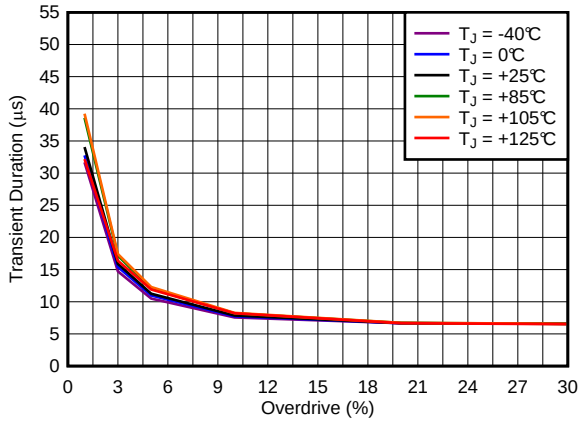
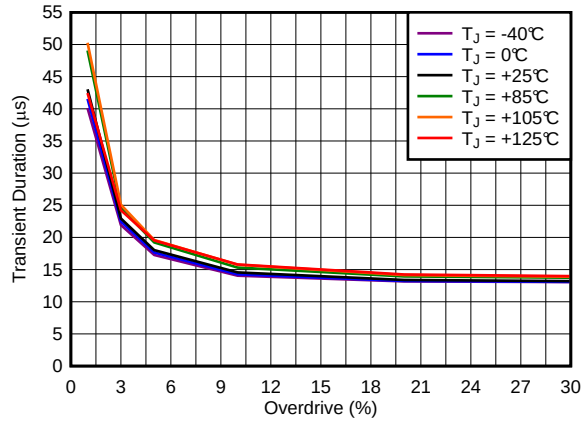


图 15. Startup Delay



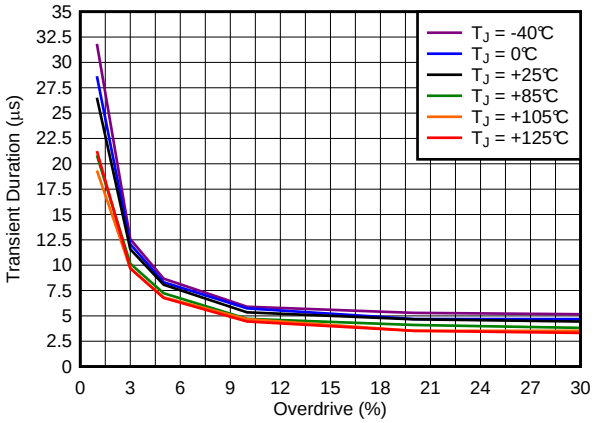
High-to-low transition occurs above the curve

图 16. Minimum Transient Duration vs Overdrive (VDD = 1.5 V)



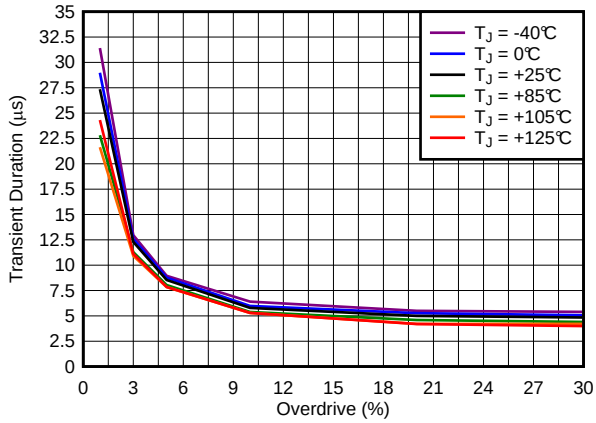
High-to-low transition occurs above the curve

图 17. Minimum Transient Duration vs Overdrive (VDD = 5.5 V)



Low-to-high transition occurs above the curve

图 18. Minimum Transient Duration vs Overdrive (VDD = 1.5 V)



Low-to-high transition occurs above the curve

图 19. Minimum Transient Duration vs Overdrive (VDD = 5.5 V)

8 Detailed Description

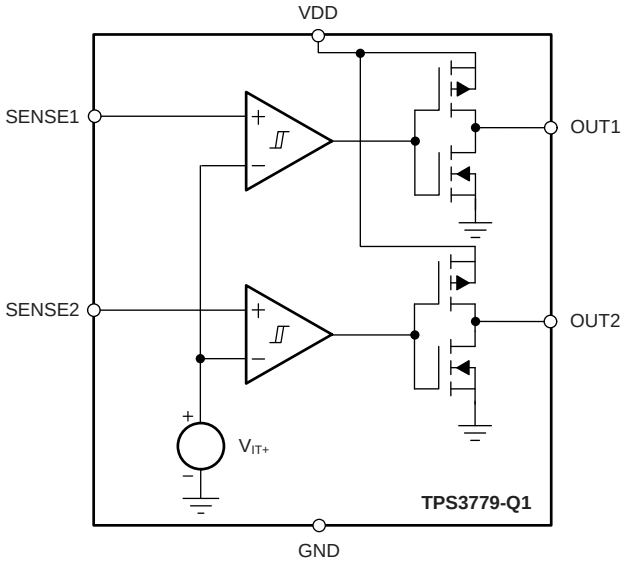
8.1 Overview

The TPS3779-Q1 and TPS3780-Q1 are small, low quiescent current (I_{DD}), dual-channel voltage detectors. These devices have high-accuracy rising and falling input thresholds, and assert the output as shown in 表 1. The output (OUTx pin) goes low when the SENSEx pin is less than V_{IT-} and goes high when the pin is greater than V_{IT+}. The TPS3779-Q1 and TPS3780-Q1 offer two hysteresis options (5% and 10%) for use in a wide variety of applications. These devices have two independent voltage-detection channels that can be used in systems where multiple voltage rails are required to be monitored, or where one channel can be used as an early warning signal and the other channel can be used as the system reset signal.

表 1. TPS3779-Q1, TPS3780-Q1 Truth Table

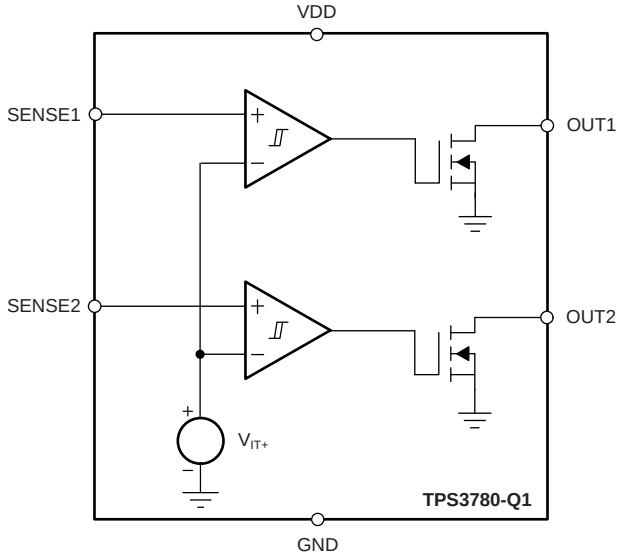
CONDITIONS	OUTPUT
SENSE1 < V_{IT-}	OUT1 = low
SENSE2 < V_{IT-}	OUT2 = low
SENSE1 > V_{IT+}	OUT1 = high
SENSE2 > V_{IT+}	OUT2 = high

8.2 Functional Block Diagrams



Copyright © 2016, Texas Instructions Incorporated

图 20. TPS3779-Q1 Block Diagram



Copyright © 2016, Texas Instructions Incorporated

图 21. TPS3780-Q1 Block Diagram

版权 © 2016, Texas Instruments Incorporated

8.3 Feature Description

8.3.1 Inputs (SENSE1, SENSE2)

The TPS3779-Q1 and TPS3780-Q1 each have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to V_{IT+}, and the falling threshold is trimmed to be equal to $V_{IT–}$. The built-in falling hysteresis options make the devices immune to supply rail noise and ensure stable operation.

The comparator inputs can swing from ground to 5.5 V, regardless of the device supply voltage used. Although not required in most cases, for extremely noisy applications, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input in order to reduce sensitivity to transients and layout parasitic.

For each SENSEx input, the corresponding output (OUTx) is driven to logic low when the input voltage drops below $V_{IT–}$. When the voltage exceeds V_{IT+}, the output (OUTx) is driven high; see 图 1.

8.3.2 Outputs (OUT1, OUT2)

In a typical device application, the outputs are connected to a reset or enable input of another device, such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC); or the outputs are connected to the enable input of a voltage regulator, such as a dc-dc or low-dropout (LDO) regulator.

The TPS3779-Q1 provides two push-pull outputs. The logic high level of the outputs is determined by the VDD pin voltage. Pullup resistors are not required with this configuration, thus saving board space. However, all interface logic levels must be examined. All OUTx connections must be compatible with the VDD pin logic level.

The TPS3780-Q1 provides two open-drain outputs (OUT1 and OUT2); pullup resistors must be used to hold these lines high when the output goes to a high-impedance condition (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The outputs can be pulled up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pullup resistor values. The pullup resistor value is determined by V_{OL}, the sink current capability, and the output leakage current ($I_{lkg(OD)}$). These values are specified in the *Electrical Characteristics* table. By using wired-AND logic, OUT1 and OUT2 can be combined into one logic signal. The *Inputs (SENSE1, SENSE2)* section describes how the outputs are asserted or deasserted. See 图 1 for a description of the relationship between threshold voltages and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation (VDD ≥ VDD(min))

When the voltage on VDD is greater than VDD(min) for t_{SD}, the output signals react to the present state of the corresponding SENSEx pins.

8.4.2 Power-On-Reset (VDD < $V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the logic low output to GND ($V_{(POR)}$), both outputs are undefined and are not to be relied upon for proper system function.

版权 © 2016, Texas Instruments Incorporated

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS3779-Q1 and TPS3780-Q1 are used as precision, dual-voltage detectors. The monitored voltage, VDD voltage, and output pullup voltage (TPS3780-Q1 only) can be independent voltages or connected in any configuration.

9.1.1 Threshold Overdrive

Threshold overdrive is how much V_{SENSE1} or V_{SENSE2} exceeds the specified threshold, and is important to know because a smaller overdrive results in a slower OUTx response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 1:

$$\text{Overdrive} = | (V_{SENSE1,2} / V_{IT} - 1) \times 100\% | \quad (1)$$

where

- V_{IT} is either V_{IT-} or V_{IT+}, depending on whether calculating the overdrive for the negative-going threshold or the positive-going threshold, respectively
- $V_{SENSE1,2}$ is the voltage at the SENSE1 or SENSE2 input

图 16 illustrates the minimum detectable pulse on the SENSEx inputs versus overdrive, and is used to visualize the relationship that overdrive has on $t_{PD(f)}$ for negative-going events.

9.1.2 Sense Resistor Divider

The resistor divider values and target threshold voltage can be calculated by using 公式 2 and 公式 3 to determine $V_{MON(UV)}$ and $V_{MON(PG)}$, respectively.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (2)$$

$$V_{MON(PG)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT+} \quad (3)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected
- $V_{MON(PG)}$ is the target voltage at which the output goes high when V_{MONx} rises

Choose R_{TOTAL} (equal to R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSEx pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, see the *Optimizing Resistor Dividers at a Comparator Input* application report (SLVA450), available for download from www.ti.com.

版权 © 2016, Texas Instruments Incorporated

9.2 Typical Applications

9.2.1 Monitoring Two Separate Rails

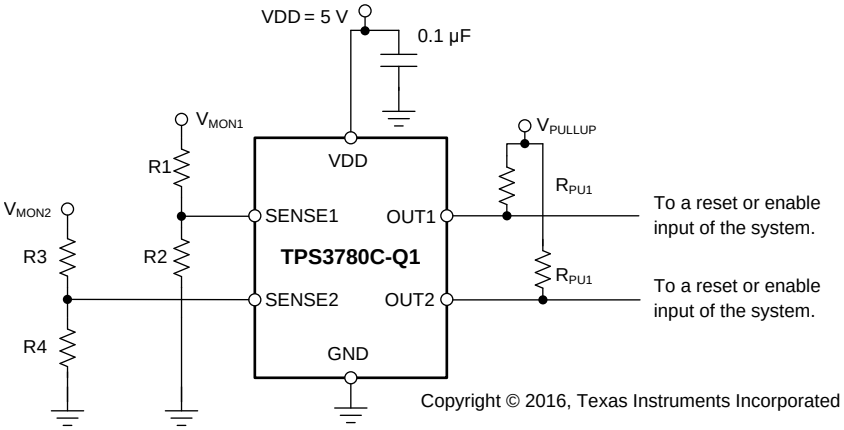


图 22. Monitoring Two Separate Rails Schematic

9.2.1.1 Design Requirements

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	5 V	5 V
Hysteresis	10%	10%
Monitored voltage 1	3.3 V nominal, $V_{MON(PG)}$ = 2.9 V, $V_{MON(UV)}$ = 2.6 V	$V_{MON(PG)}$ = 2.908 V, $V_{MON(UV)}$ = 2.618 V
Monitored voltage 2	3 V nominal, $V_{MON(PG)}$ = 2.6 V, $V_{MON(UV)}$ = 2.4 V	$V_{MON(PG)}$ = 2.606 V, $V_{MON(UV)}$ = 2.371 V
Output logic voltage	3.3-V CMOS	3.3-V CMOS

9.2.1.2 Detailed Design Procedure

1. Select the TPS3780C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3780-Q1 is selected for the output logic requirement. An open-drain output allows for the output to be pulled up to a voltage other than VDD.
2. The resistor divider values are calculated by using 公式 2 and 公式 3. For SENSE1, R1 = 1.13 MΩ and R2 = 787 kΩ. For SENSE2, R3 (R1) = 681 kΩ and R4 (R2) = 576 kΩ.

9.2.1.3 Application Curve

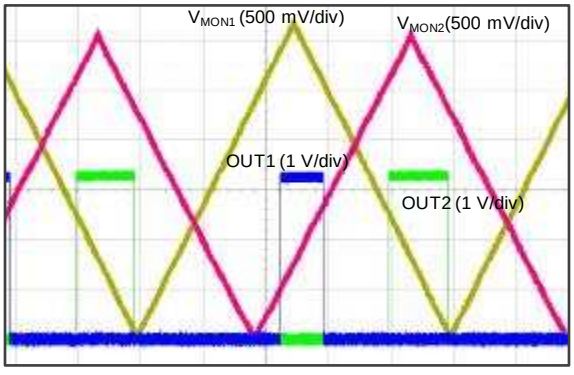
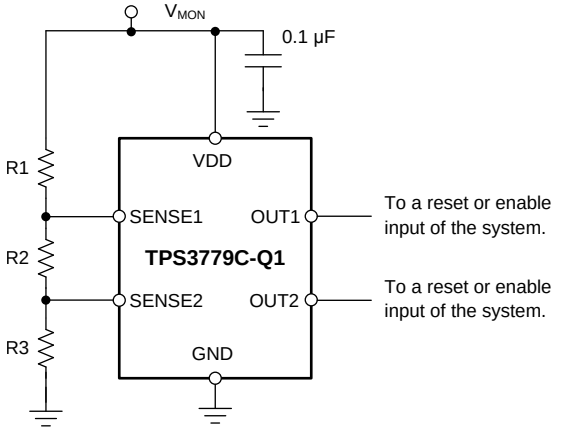


图 23. Monitoring Two Separate Rails Curve

9.2.2 Early Warning Detection



Copyright © 2016, Texas Instruments Incorporated

图 24. Early Warning Detection Schematic

9.2.2.1 Design Requirements

表 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	V_{MON}	V_{MON}
Hysteresis	10%	10%
Monitored voltage 1	$V_{MON(PG)}$ = 3.3 V, $V_{MON(UV)}$ = 3 V	$V_{MON(PG)}$ = 3.330 V, $V_{MON(UV)}$ = 2.997 V
Monitored voltage 2	$V_{MON(PG)}$ = 3.9 V, $V_{MON(UV)}$ = 3.5 V	$V_{MON(PG)}$ = 3.921 V, $V_{MON(UV)}$ = 3.529 V

9.2.2.2 Detailed Design Procedure

1. Select the TPS3779C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3779-Q1 is selected to save on component count and board space.
2. Use 公式 4 to calculate the total resistance for the resistor divider. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification. For this example, the current flow through the resistor network is chosen to be 1.41 µA. Use the key transition point for V_{MON2}. For this example, the low-to-high transition, $V_{MON(PG)}$, is considered more important.

$$R_{TOTAL} = \frac{V_{MON(PG_2)}}{I} = \frac{3.9\ V}{1.41\ \mu A} = 2.78\ M\Omega \quad (4)$$

where

- $V_{MON(PG_2)}$ is the target voltage at which OUT2 goes high when V_{MON} rises
- I is the current flowing through the resistor network

3. After R_{TOTAL} is determined, R3 can be calculated using 公式 5. Select the nearest 1% resistor value for R3. In this case, 845 kΩ is the closest value.

$$R3 = \frac{V_{IT+}}{I} = \frac{1.194\ V}{1.41\ \mu A} = 846\ k\Omega \quad (5)$$

4. Use 公式 6 to calculate R2. Select the nearest 1% resistor value for R2. In this case, 150 kΩ is the closest value. Use the key transition point for V_{MON1}. For this example, the high-to-low transition, $V_{MON(UV)}$, is considered more important.

$$R2 = \frac{R_{TOTAL}}{V_{MON(UV_1)}} \bullet V_{IT-} - R3 = \frac{2.78\ M\Omega}{3\ V} \bullet 1.074\ V - 845\ k\Omega = 149\ k\Omega \quad (6)$$

where

- $V_{MON(UV_1)}$ is the target voltage at which OUT1 goes low when V_{MON} falls

版权 © 2016, Texas Instruments Incorporated

5. Use 公式 7 to calculate R1. Select the nearest 1% resistor value for R1. In this case, 1.78 MΩ is a 1% resistor.

$$R1 = R_{TOTAL} - R2 - R3 = 2.78\ M\Omega - 150\ k\Omega - 845\ k\Omega = 1.78\ M\Omega \quad (7)$$

9.2.2.3 Application Curve

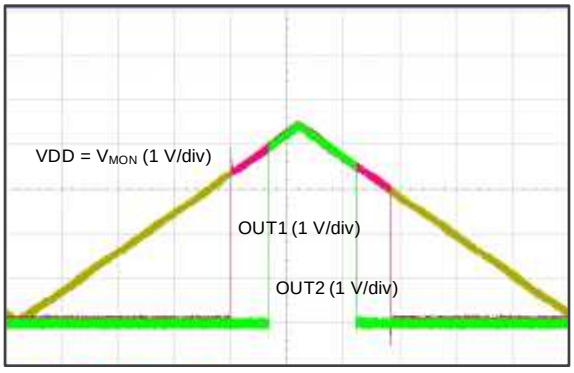


图 25. Early Warning Detection Curve

10 Power-Supply Recommendations

The TPS3779-Q1 and TPS3780-Q1 are designed to operate from an input voltage supply range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, good analog practice is to place a 0.1-µF or greater capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

For applications where SENSEx is greater than 0 V before VDD, and is subject to a startup slew rate of less than 200 mV per 1 ms, the output can be driven to logic high in error. To correct the output, cycle the SENSEx lines below V_{IT-} or sequence SENSEx after VDD.

11 Layout

11.1 Layout Guidelines

Place the VDD decoupling capacitor close to the device.

Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC tank circuit that creates ringing with peak voltages above the maximum VDD voltage.

11.2 Layout Example

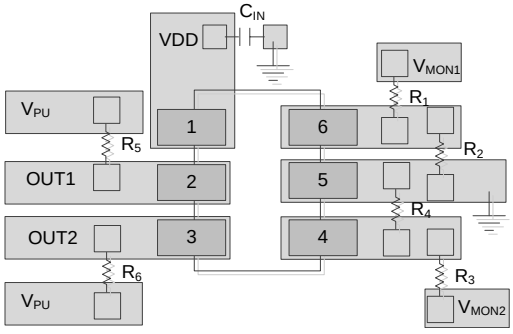


图 26. Example SOT-23 Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 评估模块

评估模块 (EVM) 可与 TPS3779-Q1 和 TPS3780-Q1 配套使用，帮助评估初始电路性能。*TPS3780EVM-154 评估模块*详细介绍了 TPS3780EVM-154 的设计套件和评估模块。

EVM 可通过德州仪器 (TI) 网站上的 TPS3779-Q1 和 TPS3780-Q1 产品文件夹获取，也可直接从 TI 网上商店购买。

12.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从相应器件产品文件夹中的*仿真模型*下获取 TPS3779-Q1 和 TPS3780-Q1 的 SPICE 模型。

12.1.2 器件命名规则

TPS3779xQyyyzQ1 和 TPS3780xQyyyzQ1 是这些器件的通用命名约定。TPS3779-Q1 和 TPS3780-Q1 代表此类器件所属系列；x 用于表示滞后版本，yyy 预留给封装标识符，z 为封装数量。

- 示例：TPS3780CDBVRQ1
- 系列：TPS3780-Q1（开漏）
- 滞后：10%
- DBV 封装：6 引脚小外形尺寸晶体管 (SOT)-23
- 封装数量：R 表示 3000 片

12.2 文档支持

12.2.1 相关文档

相关文档如下：

- *《TPS3780EVM-154 评估模块》*（文献编号：SLVU796）
- *应用报告《优化比较器输入端的电阻分压器》*（文献编号：SLVA450）

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS3779-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS3780-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

版权 © 2016, Texas Instruments Incorporated

12.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3779BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12OE	Samples
TPS3779CQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12PE	Samples
TPS3780AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12FE	Samples
TPS3780BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12GE	Samples
TPS3780CQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12HE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

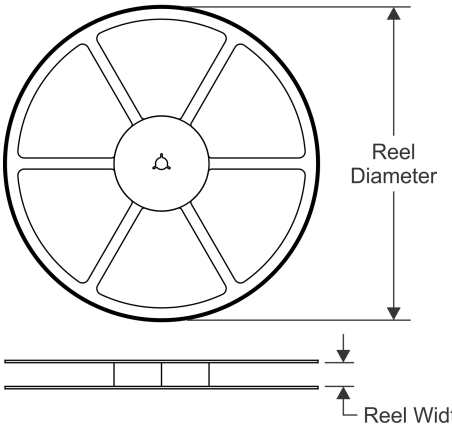
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

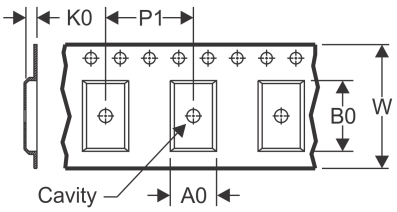
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

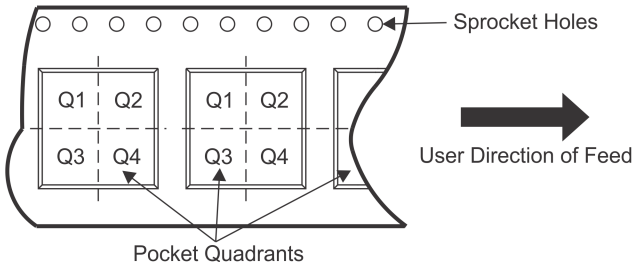


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

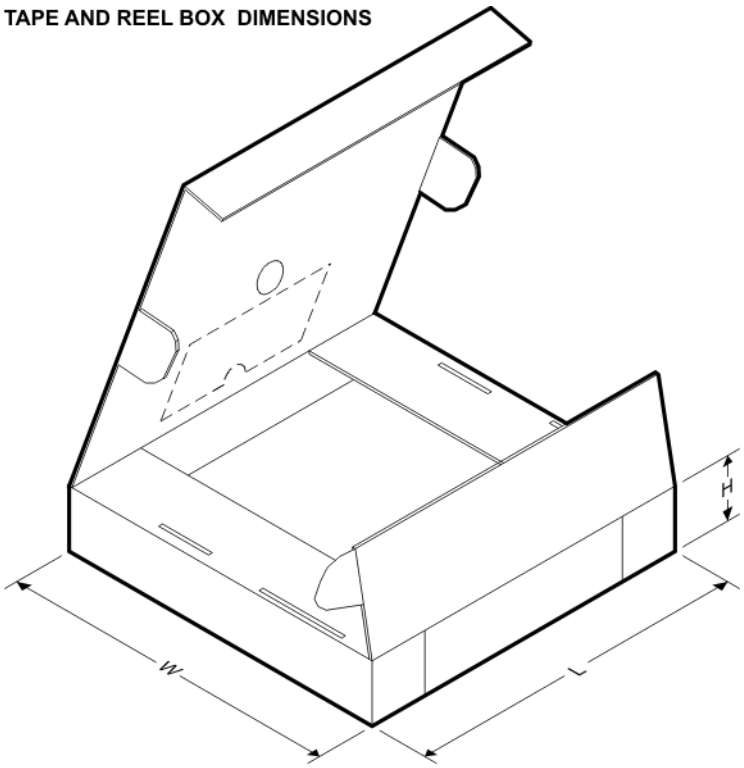
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3779BQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3779CQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780BQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780CQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

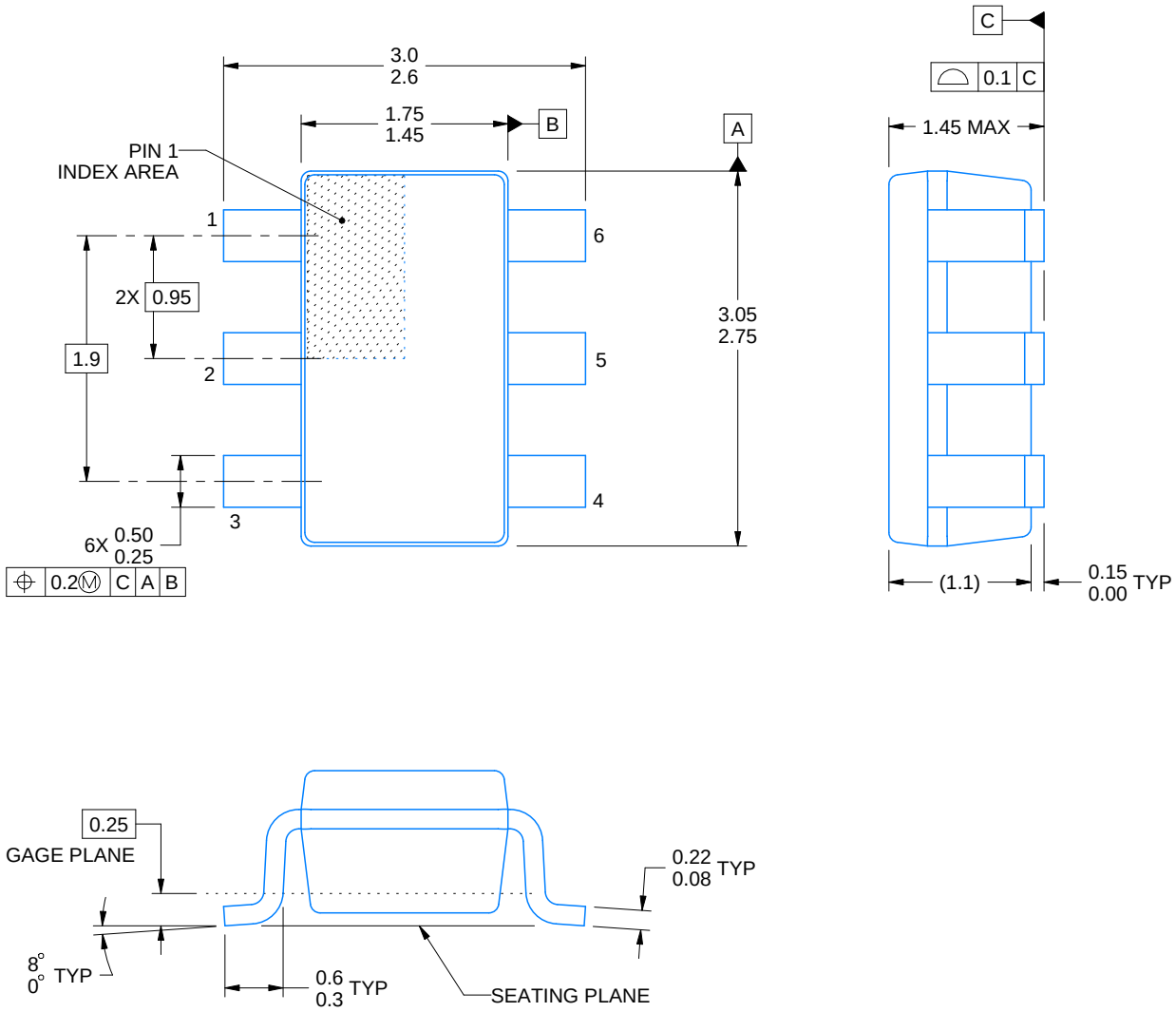
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3779BQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3779CQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780AQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780BQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780CQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

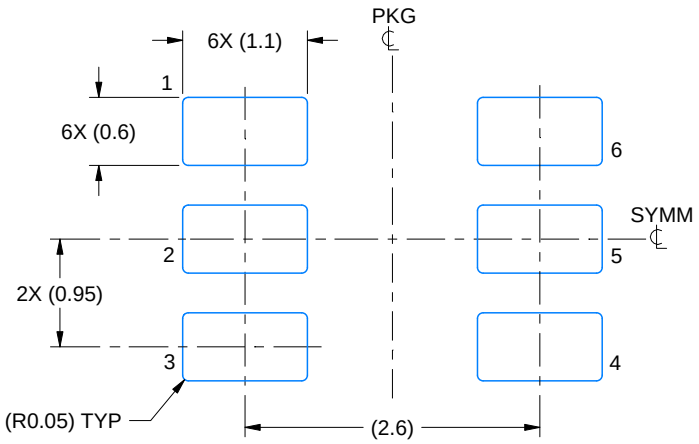
SMALL OUTLINE TRANSISTOR



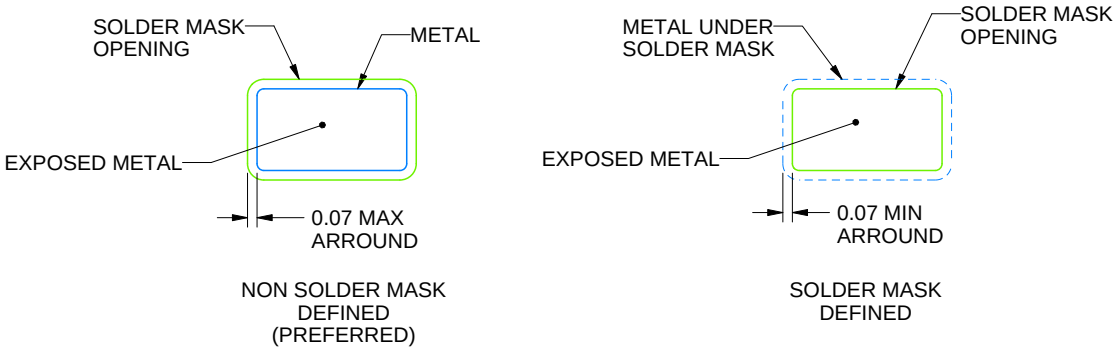
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

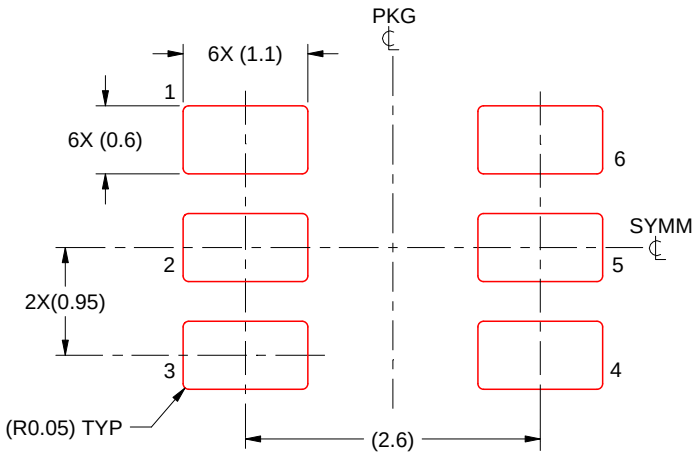


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2021 德州仪器半导体技术（上海）有限公司