LMH6739 Very Wideband, Low Distortion Triple Video Buffer

Check for Samples: LMH6739

FEATURES

- **750 MHz −3 dB small signal bandwidth (A_V = +1)**
- **−85 dBc 3rd harmonic distortion (20 MHz)**
- **2.3 nV/√Hz input noise voltage**
- **3300 V/µs slew rate**
- **32 mA supply current (10.6 mA per op amp)**
- **90 mA linear output current**
- **0.02/0.01 Diff. Gain/ Diff. Phase (R_L = 150Ω)**
- **2mA shutdown current**

APPLICATIONS

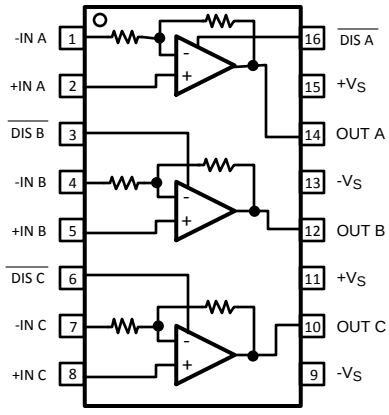
- **RGB video driver**
- **High resolution projectors**
- **Flash A/D driver**
- **D/A transimpedance buffer**
- **Wide dynamic range IF amp**
- **Radar/communication receivers**
- **DDS post-amps**
- **Wideband inverting summer**
- **Line driver**

DESCRIPTION

The LMH6739 is a very wideband, DC coupled monolithic selectable gain buffer designed specifically for ultra high resolution video systems as well as wide dynamic range systems requiring exceptional signal fidelity. Benefiting from current feedback architecture, the LMH6739 offers gains of −1, 1 and 2. At a gain of +2 the LMH6739 supports ultra high resolution video systems with a 400 MHz 2 V_{PP}3 dB Bandwidth. With 12-bit distortion level through 30 MHz (R_L = 100Ω), 2.3nV/√Hz input referred noise, the LMH6739 is the ideal driver or buffer for high speed flash A/D and D/A converters. Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the LMH6739 low input referred noise and low harmonic distortion make it an attractive solution. The LMH6739 is offered in a space saving SSOP package.

CONNECTION DIAGRAM

16-Pin SSOP
Top View



See Package Number DBQ0016A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage (V^+ - V^-)	13.2V
I_{OUT}	(3)
Common Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Information for more details.

Operating Ratings (1) (2)

Temperature Range (3)	−40°C to +85°C	
Supply Voltage (V^+ - V^-)	8V to 12V	
Thermal Resistance		
Package	**(θ_{JC})**	**(θ_{JA})**
16-Pin SSOP	36°C/W	120°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

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Electrical Characteristics (1)

T_A = 25°C, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
Frequency Domain Performance						
UGBW	−3 dB Bandwidth	Unity Gain, V_{OUT} = 200 mV_{PP}		750		MHz
SSBW	−3 dB Bandwidth	V_{OUT} = 200 mV_{PP}		480		MHz
LSBW		V_{OUT} = 2 V_{PP}		400		
	0.1 dB Bandwidth	V_{OUT} = 2 V_{PP}		150		MHz
GFR2	Rolloff	at 300 MHz, V_{OUT} = 2 V_{PP}		1.0		dB
Time Domain Response						
TRS	Rise and Fall Time (10% to 90%)	2V Step		0.9		ns
TRL		5V Step		1.7		
SR	Slew Rate	5V Step		3300		V/µs
t_s	Settling Time to 0.1%	2V Step		10		ns
t_e	Enable Time	From $\overline{\text{Disable}}$ = rising edge.		7.3		ns
t_d	Disable Time	From $\overline{\text{Disable}}$ = falling edge.		4.5		ns
Distortion						
HD2L	2nd Harmonic Distortion	2 V_{PP}, 5 MHz		−80		dBc
HD2		2 V_{PP}, 20 MHz		−71		
HD2H		2 V_{PP}, 50 MHz		−55		
HD3L	3rd Harmonic Distortion	2 V_{PP}, 5 MHz		−90		dBc
HD3		2 V_{PP}, 20 MHz		−85		
HD3H		2 V_{PP}, 50 MHz		−65		
Equivalent Input Noise						
V_N	Non-Inverting Voltage	>1 MHz		2.3		nV/√Hz
I_{CN}	Inverting Current	>1 MHz		12		pA/√Hz
N_{CN}	Non-Inverting Current	>1 MHz		3		pA/√Hz
Video Performance						
DG	Differential Gain	4.43 MHz, R_L = 150Ω		.02		%
DP	Differential Phase	4.43 MHz, R_L = 150Ω		.01		degree
Static, DC Performance						
V_{OS}	Input Offset Voltage (4)			0.5	±2.5 **±4.5**	mV
I_{BN}	Input Bias Current (4)	Non-Inverting	−16 **−21**	−8	0 **+5**	µV
I_{BI}	Input Bias Current (4)	Inverting		−2	±30 **±40**	µA
PSRR	Power Supply Rejection Ratio (4)		50 **48.5**	53		dB
CMRR	Common Mode Rejection Ratio (4)		46 **44**	50		dB
I_{CC}	Supply Current (4)	All three amps Enabled, No Load		32	35 **40**	mA
	Supply Current Disabled V^+	R_L = ∞		1.9	2.2	mA
	Supply Current Disabled V^-	R_L = ∞		1.1	1.3	mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Information for information on temperature de-rating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested on shipped production material.

(4) Parameter 100% production tested at 25° C.

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Electrical Characteristics [1] (continued)

T_A = 25°C, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
	Internal Feedback & Gain Set Resistor Value		375	450	525	Ω
	Gain Error	R_L = ∞		0.2	±1.1	%
Miscellaneous Performance						
R_{IN}+	Non-Inverting Input Resistance			1000		kΩ
C_{IN}+	Non-Inverting Input Capacitance			.8		pF
R_{IN}−	Inverting Input Impedance	Output impedance of input buffer.		30		Ω
R_O	Output Impedance	DC		0.05		Ω
V_O	Output Voltage Range [4]	R_L = 100Ω	±3.25 **±3.1**	±3.5		V
		R_L = ∞	±3.65 **±3.5**	±3.8		
CMIR	Common Mode Input Range [4]	CMRR > 40 dB	±1.9 **±1.7**	±2.0		V
I_O	Linear Output Current [5] [4]	V_{IN} = 0V, V_{OUT} < ±30 mV	80 **60**	90		mA
I_{SC}	Short Circuit Current [6]	V_{IN} = 2V Output Shorted to Ground		160		mA
I_{IH}	Disable Pin Bias Current High	$\overline{\text{Disable}}$ Pin = V^+		10		µA
I_{IL}	Disable Pin Bias Current Low	$\overline{\text{Disable}}$ Pin = 0V		−350		µA
V_{DMAX}	Voltage for Disable	$\overline{\text{Disable}}$ Pin ≤ V_{DMAX}			0.8	V
V_{DMIM}	Voltage for Enable	$\overline{\text{Disable}}$ Pin ≥ V_{DMIN}	2.0			V

(5) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Information for more details.

(6) Short circuit current should be limited in duration to no more than 10 seconds. See the Power Dissipation section of the Application Information for more details.

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Typical Performance Characteristics

A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified).

Large Signal Frequency Response

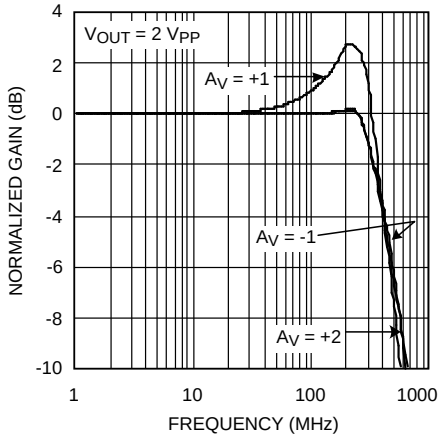

Figure 1.

Small Signal Frequency Response

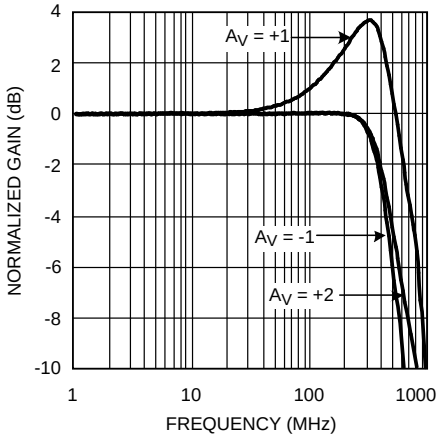

Figure 2.

Frequency Response vs. V_{OUT}

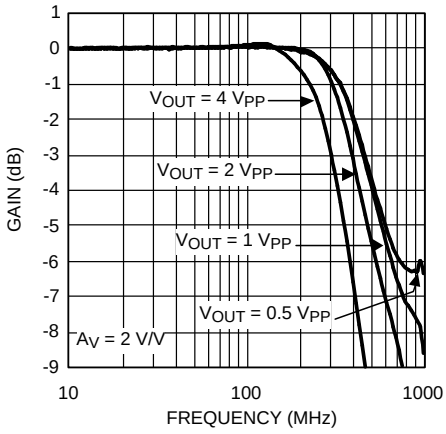

Figure 3.

Frequency Response vs. Supply Voltage

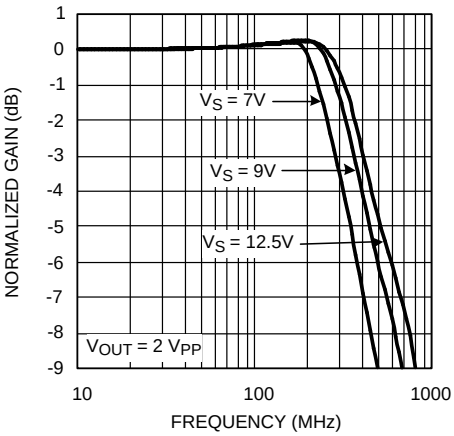

Figure 4.

Gain Flatness

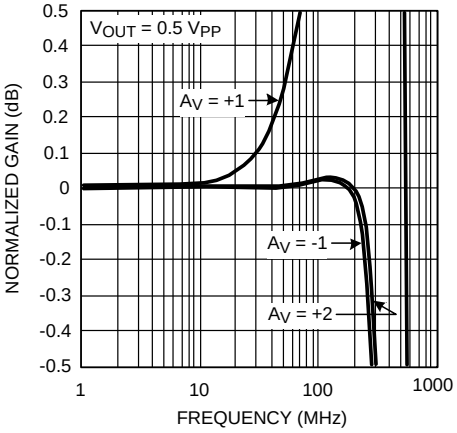

Figure 5.

Gain Flatness, Dual Input Buffer

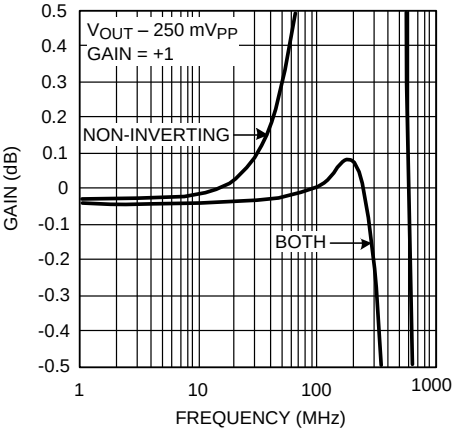

Figure 6.

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Typical Performance Characteristics (continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified).

Pulse Response

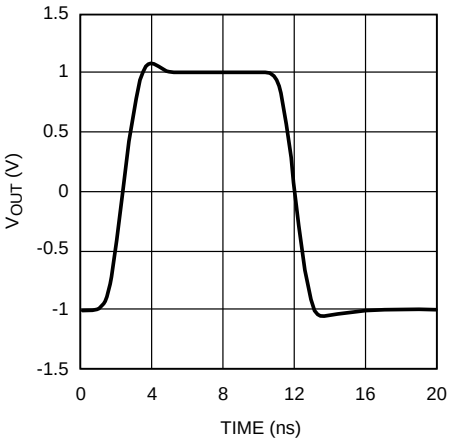

Figure 7.

Frequency Response vs. Capacitive Load

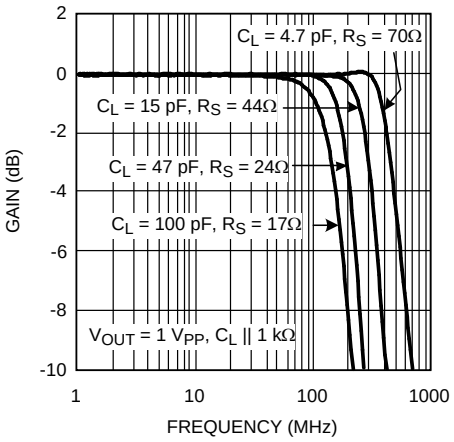

Figure 8.

Series Output Resistance vs. Capacitive Load

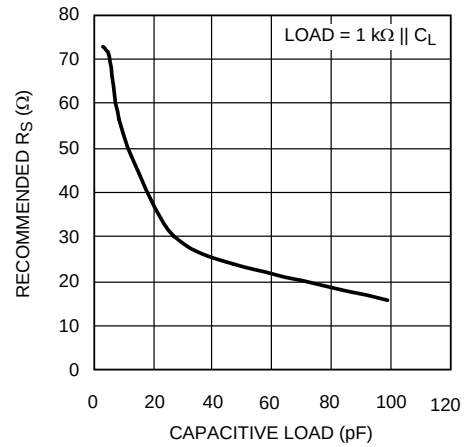

Figure 9.

Open Loop Gain and Phase

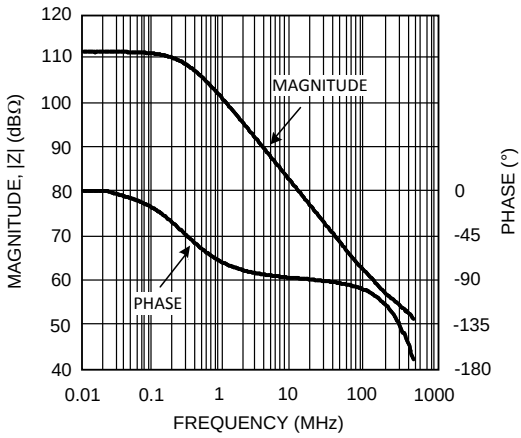

Figure 10.

Distortion vs. Frequency

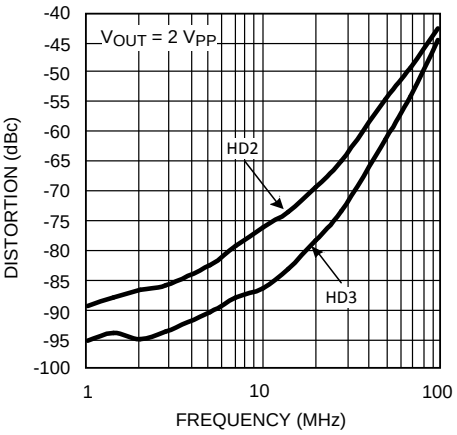

Figure 11.

10 MHz HD vs. Output Level

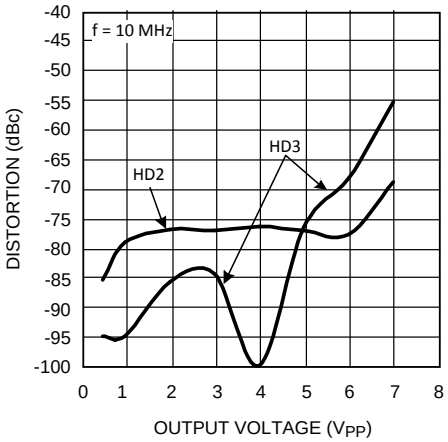

Figure 12.

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Typical Performance Characteristics (continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified).

Distortion vs. Supply Voltage

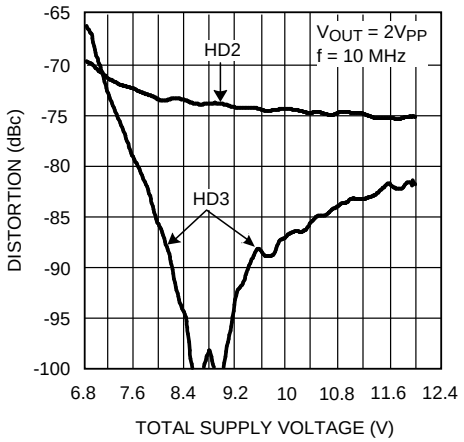

Figure 13.

CMRR vs. Frequency

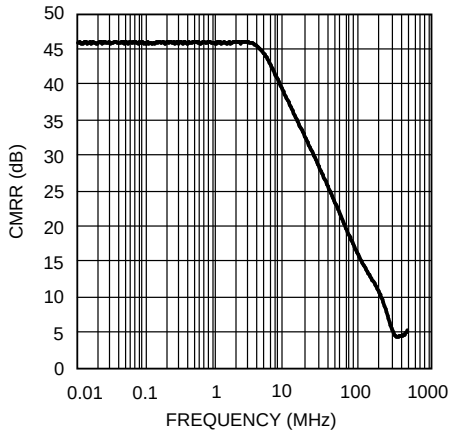

Figure 14.

PSRR vs. Frequency

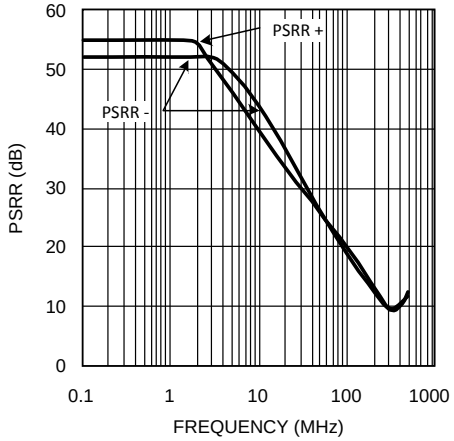

Figure 15.

Closed Loop Output Impedance |Z|

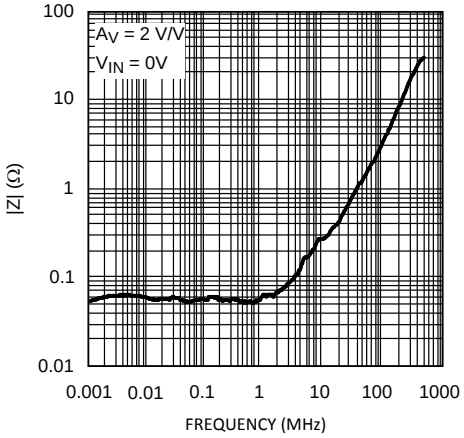

Figure 16.

Disable Timing

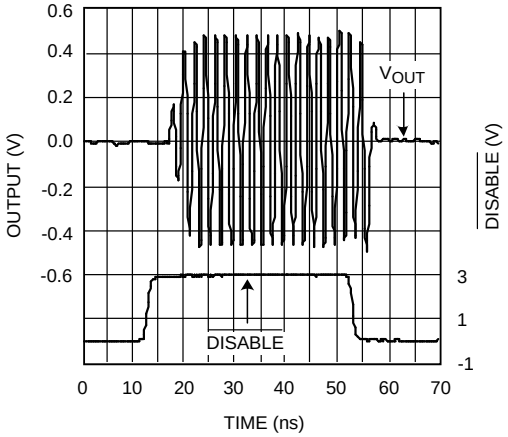

Figure 17.

DC Errors vs. Temperature

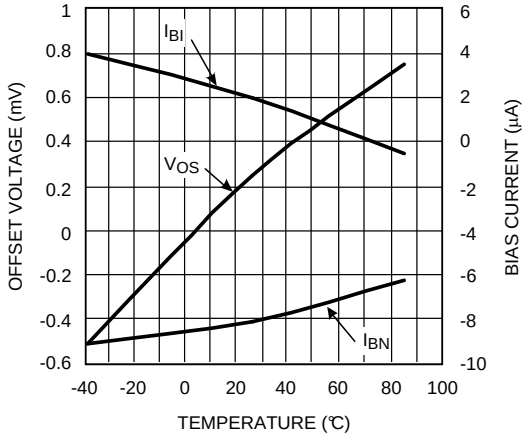

Figure 18.

Typical Performance Characteristics (continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified).

Crosstalk vs. Frequency

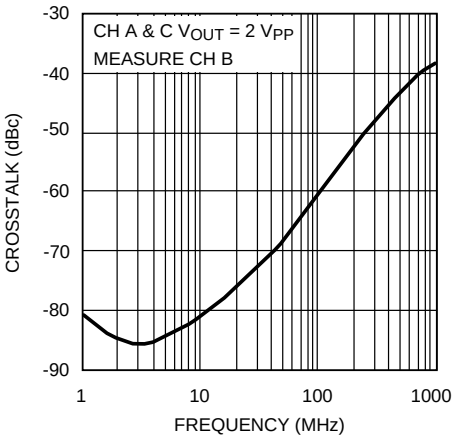

Figure 19.

Disabled Channel Isolation vs. Frequency

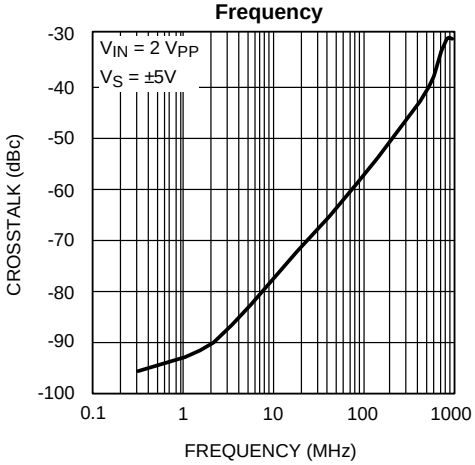

Figure 20.

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APPLICATION INFORMATION

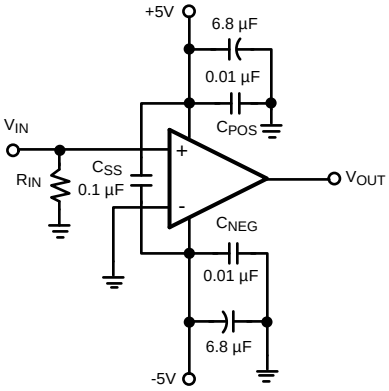

Figure 21. Recommended Non-Inverting Gain Circuit, Gain = +2

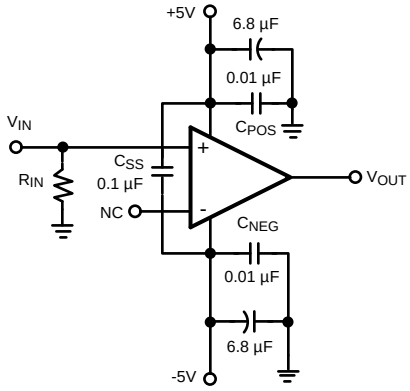

Figure 22. Recommended Non-Inverting Gain Circuit, Gain +1

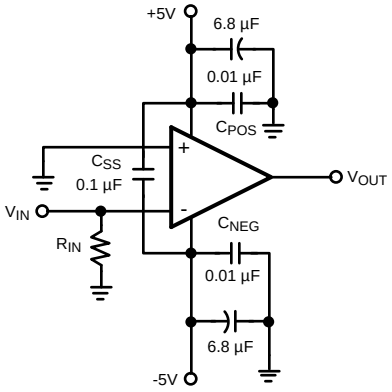

Figure 23. Recommended Inverting Gain Circuit, Gain = –1

GENERAL INFORMATION

The LMH6739 is a high speed current feedback selectable gain buffer (SGB), optimized for very high speed and low distortion. With its internal feedback and gain-setting resistors the LMH6739 offers excellent AC performance while simplifying board layout and minimizing the affects of layout related parasitic components. The LMH6739 has no internal ground reference so single or split supply configurations are both equally useful.

SETTING THE CLOSED LOOP GAIN

The LMH6739 is a current feedback amplifier with on-chip $R_F = R_G = 450\Omega$. As such it can be configured with an $A_V = +2$, $A_V = +1$, or an $A_V = -1$ by connecting pins 3 and 4 as described in Table 1.

Table 1. Input Connections for all 3 Gain Possibilities

GAIN A_V	INPUT CONNECTIONS	
	Non-Inverting	Inverting
−1 V/V	Ground	Input Signal
+1 V/V	Input Signal	NC (Open)
+2 V/V	Input Signal	Ground

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The gain of the LMH6739 is accurate to ±1% and stable over temperature. The internal gain setting resistors, R_F and R_G, match very well. However, over process and temperature their absolute value will change. Using external resistors in series with R_G to change the gain will result in poor gain accuracy over temperature and from part to part.

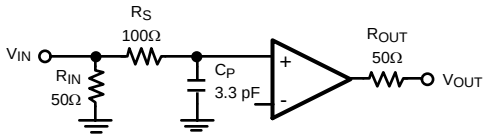

Figure 24. Correction for Unity Gain Peaking

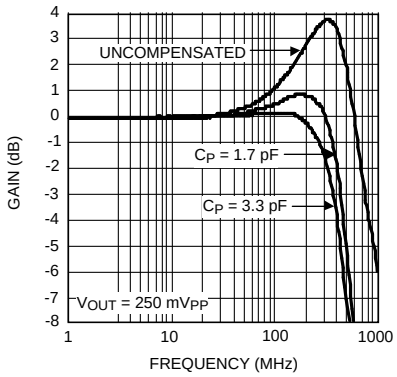

Figure 25. Frequency Response for Circuit in Figure 24

UNITY GAIN COMPENSATION

With a current feedback Selectable Gain Buffer like the LMH6739, the feedback resistor is a compromise between the value needed for stability at unity gain and the optimized value used at a gain of two. The result of this compromise is substantial peaking at unity gain. If this peaking is undesirable a simple RC filter at the input of the buffer will smooth the frequency response shown as Figure 24. Figure 25 shows the results of a simple filter placed on the non-inverting input. See Figure 26 and Figure 27 for another method for reducing unity gain peaking.

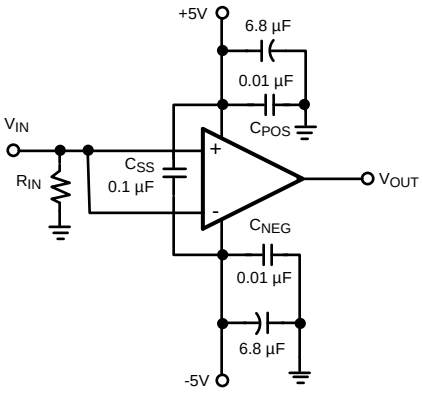

Figure 26. Alternate Unity Gain Compensation

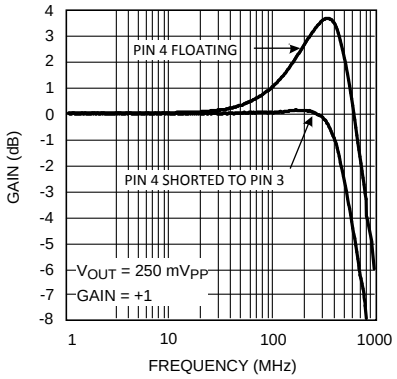

Figure 27. Frequency Response for Circuit in Figure 26

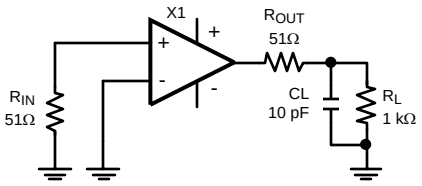

Figure 28. Decoupling Capacitive Loads

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DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Figure 28 shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The charts "Suggested R_{OUT} vs. Cap Load" give a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730275 is the evaluation board for the LMH6739.

To reduce parasitic capacitances ground and power planes should be removed near the input and output pins. Components in the feedback loop should be placed as close to the device as possible. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. The LMH6739 has multiple power and ground pins for enhanced supply bypassing. Every pin should ideally have a separate bypass capacitor. Sharing bypass capacitors may slightly degrade second order harmonic performance, especially if the supply traces are thin and /or long. In Figure 21 and Figure 22 C_{SS} is optional, but is recommended for best second harmonic distortion. Another option to using C_{SS} is to use pairs of .01 µF and 0.1 µF ceramic capacitors for each supply bypass.

VIDEO PERFORMANCE

The LMH6739 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 24 shows a typical configuration for driving a 75Ω Cable. The amplifier is configured for a gain of two to make up for the 6 dB of loss in R_{OUT}.

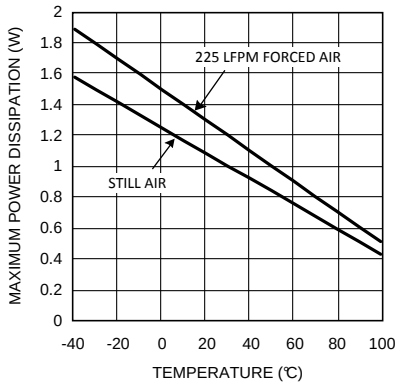

Figure 29. Maximum Power Dissipation

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POWER DISSIPATION

The LMH6739 is optimized for maximum speed and performance in the small form factor of the standard SSOP-16 package. To achieve its high level of performance, the LMH6739 consumes an appreciable amount of quiescent current which cannot be neglected when considering the total package power dissipation limit. The quiescent current contributes to about 40° C rise in junction temperature when no additional heat sink is used (V_S = ±5V, all 3 channels on). Therefore, it is easy to see the need for proper precautions to be taken in order to make sure the junction temperature's absolute maximum rating of 150°C is not violated.

To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation (all 3 channels).

With the LMH6739 used in a back-terminated 75Ω RGB analog video system (with 2 V_{PP} output voltage), the total power dissipation is around 435 mW of which 340 mW is due to the quiescent device dissipation (output black level at 0V). With no additional heat sink used, that puts the junction temperature to about 140° C when operated at 85°C ambient.

To reduce the junction temperature many options are available. Forced air cooling is the easiest option. An external add-on heat-sink can be added to the SSOP-16 package, or alternatively, additional board metal (copper) area can be utilized as heat-sink.

An effective way to reduce the junction temperature for the SSOP-16 package (and other plastic packages) is to use the copper board area to conduct heat. With no enhancement the major heat flow path in this package is from the die through the metal lead frame (inside the package) and onto the surrounding copper through the interconnecting leads. Since high frequency performance requires limited metal near the device pins the best way to use board copper to remove heat is through the bottom of the package. A gap filler with high thermal conductivity can be used to conduct heat from the bottom of the package to copper on the circuit board. Vias to a ground or power plane on the back side of the circuit board will provide additional heat dissipation. A combination of front side copper and vias to the back side can be combined as well.

Follow these steps to determine the maximum power dissipation for the LMH6739:

1. Calculate the quiescent (no-load) power:

$$P_{AMP} = I_{CC} \times (V_S)\ V_S = V^+ - V^- \quad (1)$$

2. Calculate the RMS power dissipated in the output stage:

$$P_D\ (rms) = rms\ ((V_S - V_{OUT}) * I_{OUT}) \quad (2)$$

where V_{OUT} and I_{OUT} are the voltage and current across the external load and V_S is the total supply current

3. Calculate the total RMS power:

$$P_T = P_{AMP} + P_D \quad (3)$$

The maximum power that the LMH6739 package can dissipate at a given temperature can be derived with the following equation (See Figure 29):

$P_{MAX} = (150^o - T_{AMB})/\ \theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SSOP package θ_{JA} is 120°C/W.

ESD PROTECTION

The LMH6739 is protected against electrostatic discharge (ESD) on all pins. The LMH6739 will survive 2000V Human Body model and 200V Machine model events.

Under closed loop operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6739 is driven by a large signal while the device is powered down the ESD diodes will conduct.

The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

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REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	12

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6739MQ/NOPB	ACTIVE	SSOP	DBQ	16	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH67 39MQ	Samples
LMH6739MQX/NOPB	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH67 39MQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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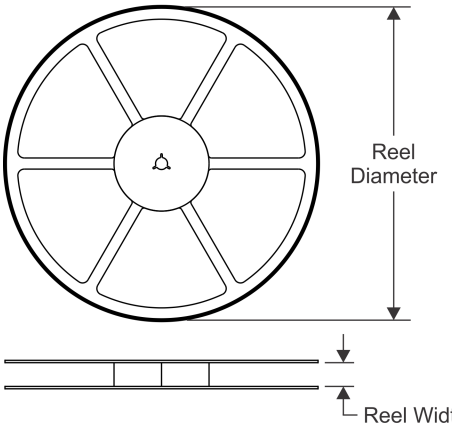
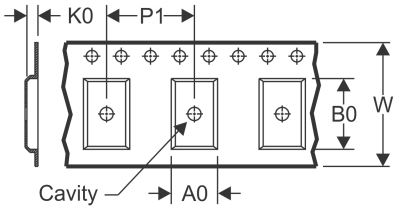
TAPE AND REEL INFORMATION

REEL DIMENSIONS

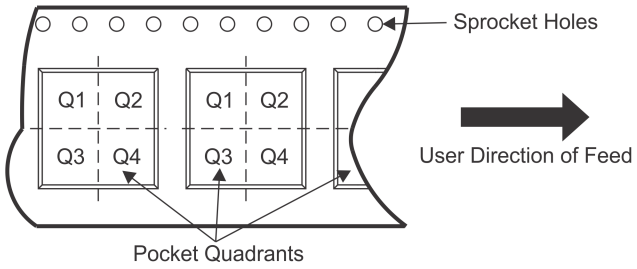


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

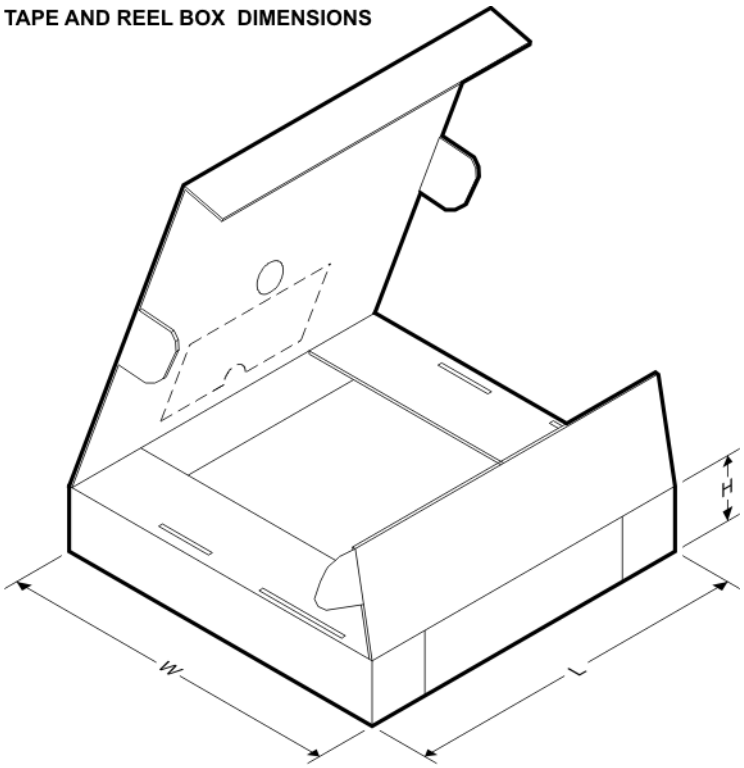
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6739MQX/NOPB	SSOP	DBQ	16	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

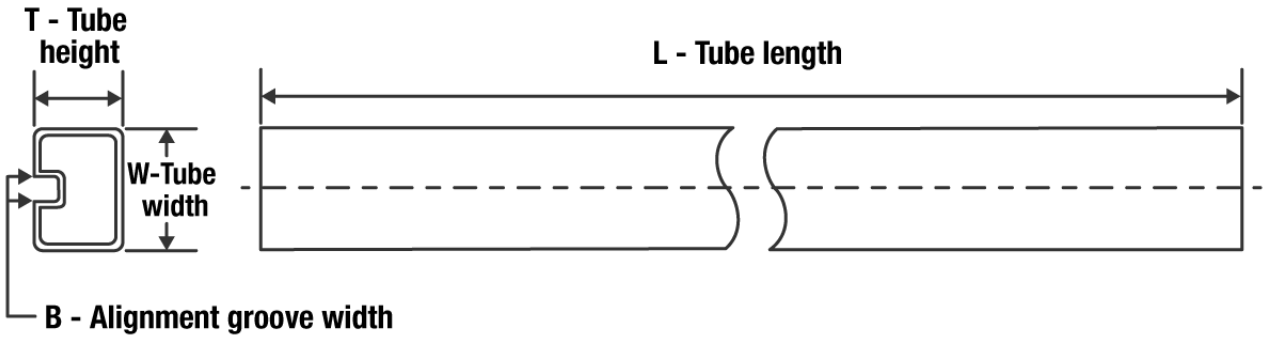
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

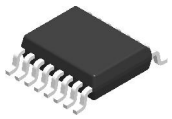
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6739MQX/NOPB	SSOP	DBQ	16	2500	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6739MQ/NOPB	DBQ	SSOP	16	95	495	8	4064	3.05

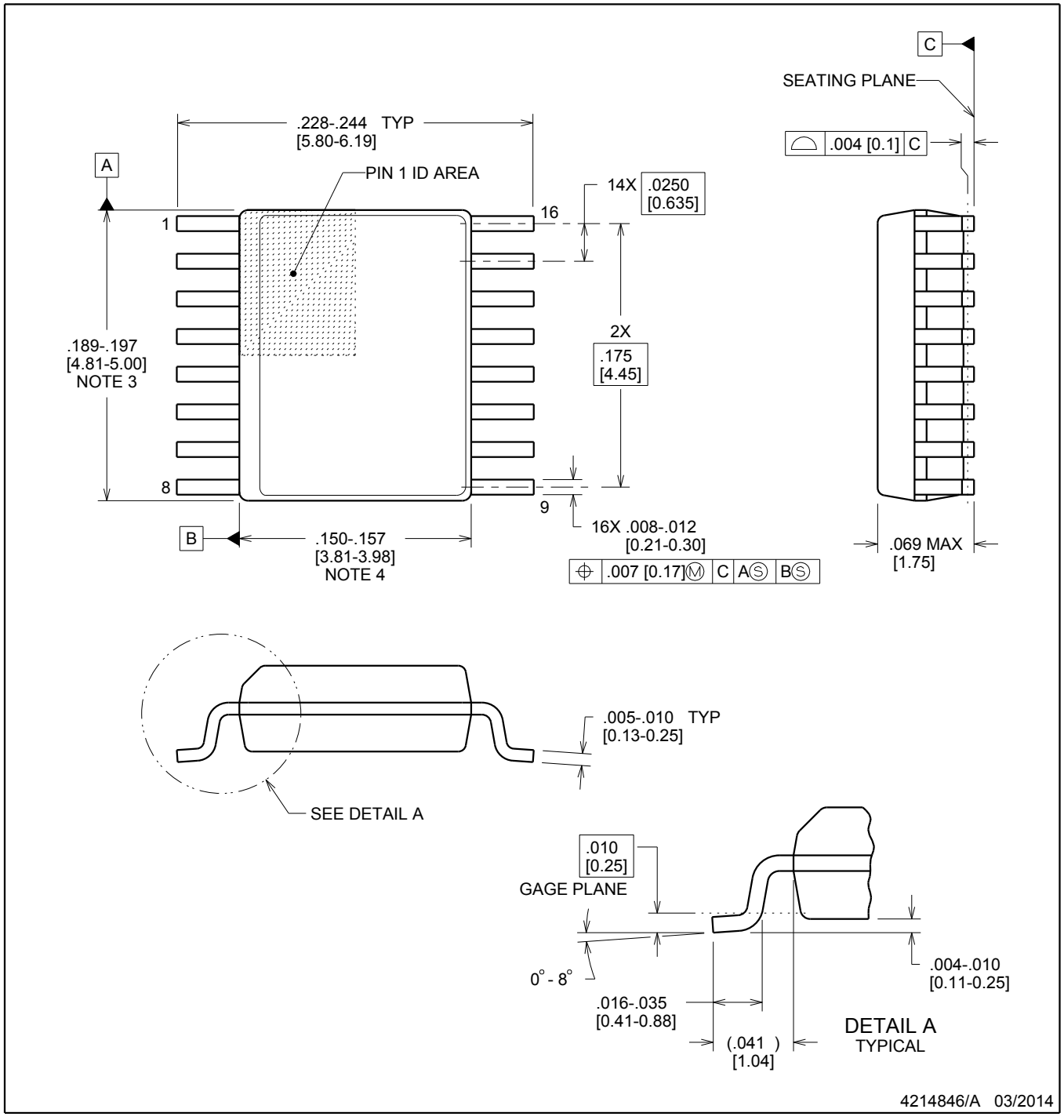


PACKAGE OUTLINE

DBQ0016A

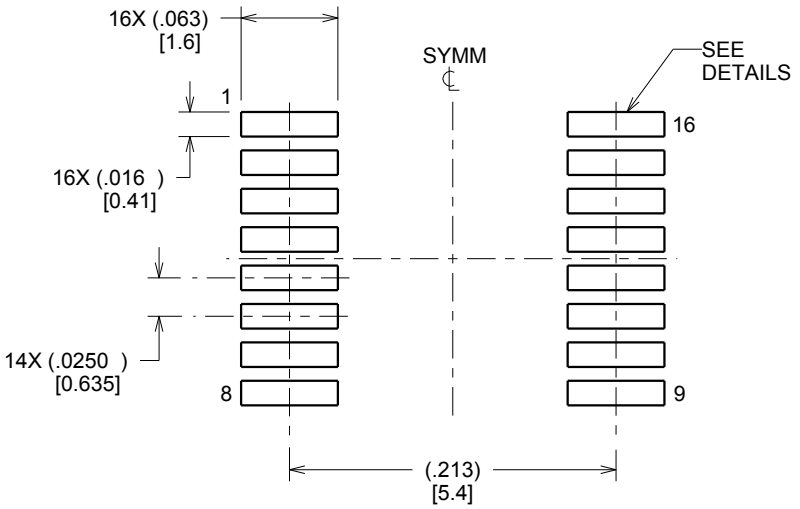
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

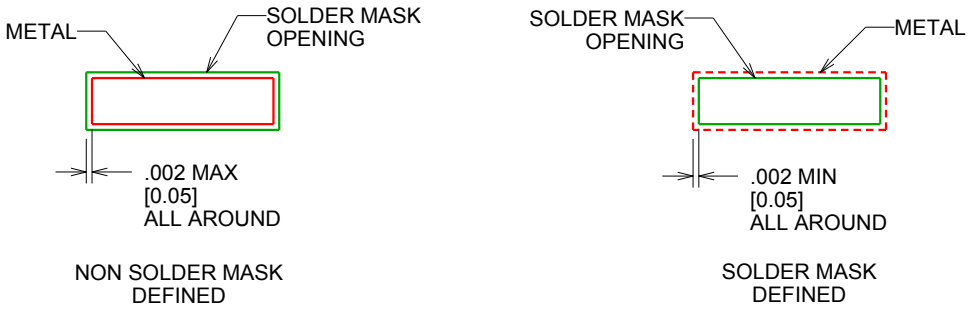


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

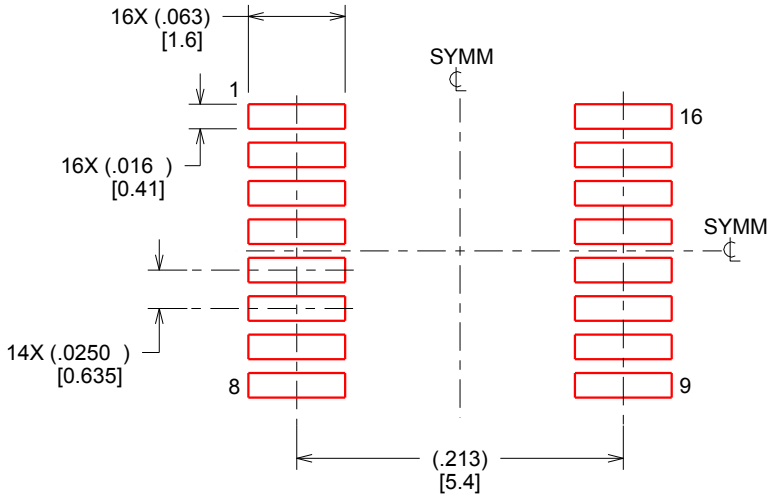
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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