TPS3702-Q1 高精度、过压和欠压监视器

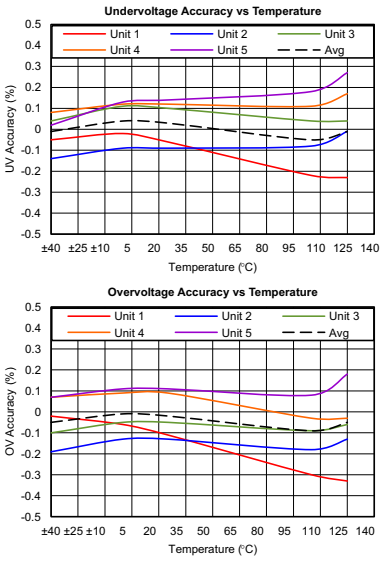
1 特性

- 符合 AEC-Q100 标准：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 输入电压范围：2V 至 18V
- 高阈值精度：
  - 0.25%（典型值）
  - 0.9%（–40°C 至 125°C）
- 已针对 1V 和 5V 之间的标称电源轨优化的固定窗口阈值
- 用于过压和欠压指示的开漏输出
- 内部毛刺抑制功能
- 可使用 SET 引脚调整阈值
- 低静态电流：7μA（典型值）
- 内部阈值滞后：0.55% 和 1.0%
- 小外形尺寸晶体管 (SOT)-6 封装

2 应用范围

- 汽车安全 应用范围
- 信息娱乐
- 现场可编程门阵列 (FPGA) 和专用集成电路 (ASIC) 应用
- 基于数字信号处理器 (DSP) 的系统
- 前置摄像头
- 后视摄像头
- 汽车雷达系统

精度与温度间的关系



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

3 说明

TPS3702-Q1 是一款集成型过压和欠压窗口比较器，其采用小型 SOT-6 封装。这款高精度电压检测器非常适合电源容限较窄且由低压电源轨供电运行的系统。该器件提供有 0.55% 和 1.0% 两个低阈值滞后选项，可防止在受监视电源电压处于其标称工作范围内时出现错误的复位信号。并且内置有毛刺抑制功能和噪声滤波器，进一步消除了错误信号所导致的错误复位。

TPS3702-Q1 无需使用任何外部电阻即可设置过压和欠压复位阈值，因此进一步提高了总体精度、减小了解决方案尺寸并降低了解决方案的成本。每款器件的两种可用阈值电压可使用 SET 引脚进行选择。独立的 SENSE 输入引脚和 VDD 引脚可满足安全关键型和高可靠性系统对于冗余的需求。该器件还 为 OV 和 UV 引脚提供了独立复位输出；可采用开漏配置将 UV 和 OV 引脚连接在一起。

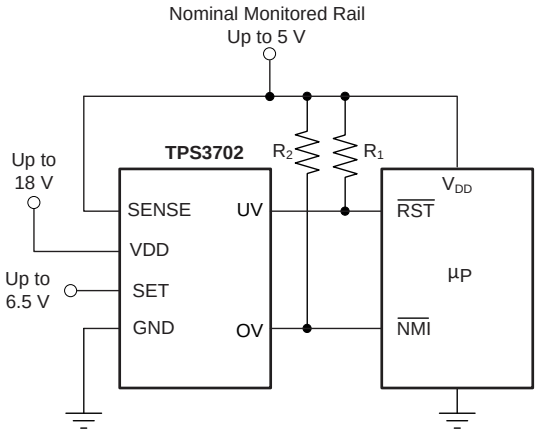
该器件的静态电流典型值低至 7μA内工作。 TPS3702-Q1 适用于汽车 应用 ，符合 AEC-Q100 1 级标准。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS3702-Q1	SOT (6)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



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4 修订历史记录

Changes from Revision A (May 2015) to Revision B **Page**

- Changed *Operating junction temperature* maximum specification in *Absolute Maximum Ratings* table ... 5

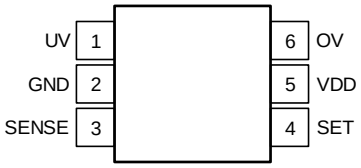
Changes from Original (April 2015) to Revision A **Page**

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5 Pin Configuration and Functions

DDC Package
SOT-6
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	UV	O	Active-low, open-drain undervoltage output. This pin goes low when the SENSE voltage falls below the internally set undervoltage threshold (V_{IT-}). See the timing diagram in 图 1 for more details. Connect this pin to a pull-up resistor terminated to the desired pull-up voltage.
2	GND	—	Ground
3	SENSE	I	Input for the monitored supply voltage rail. When the SENSE voltage goes below the undervoltage threshold, the UV pin is driven low. When the SENSE voltage goes above the overvoltage threshold, the OV pin is driven low.
4	SET	I	Use this pin to configure the threshold voltages. Refer to 表 3 for the desired configuration.
5	VDD	I	Supply voltage input pin. To power the device, connect a voltage supply (within the range of 2 V and 18 V) to VDD. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.
6	OV	O	Active-low, open-drain overvoltage output. This pin goes low when the SENSE voltage rises above the internally set overvoltage threshold (V_{IT+}). See the timing diagram in 图 1 for more details. Connect this pin to a pull-up resistor terminated to the desired pull-up voltage.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	20	V
	V_{UV}, V_{OV}	–0.3	20	V
	V_{SENSE}, V_{SET}	–0.3	7	V
Current	I_{UV}, I_{OV}		±40	mA
Continuous total power dissipation		See the *Thermal Information*		
Operating junction temperature, T_J(2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	2		18	V
V_{SENSE}	Input pin voltage	0		6.5	V
V_{SET}	SET pin voltage	0		6.5	V
V_{UV}, V_{OV}	Output pin voltage	0		18	V
I_{UV}, I_{OV}	Output pin current	0.3		10	mA
R_{PU}	Pull-up resistor	2.2		10,000	kΩ

6.4 Thermal Information

THERMAL METRIC(1)		TPS3702-Q1 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

At 2 V ≤ V_{DD} ≤ 18 V, 1 V ≤ V_{SENSE} ≤ 5 V, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		2		18	V
$V_{IT+(OV)}$	Positive-going threshold accuracy	V_{SET} ≤ $V_{IL(SET)}$, V_{SET} ≥ $V_{IH(SET)}$	–0.9%	±0.25%	0.9%	
$V_{IT–(UV)}$	Negative-going threshold accuracy	V_{SET} ≤ $V_{IL(SET)}$, V_{SET} ≥ $V_{IH(SET)}$	–0.9%	±0.25%	0.9%	
V_{HYS}	Hysteresis voltage(1)	TPS3702x**X**x	0.3%	0.55%	0.8%	
$V_{(POR)}$	Power-on reset voltage(2)	$V_{OL(max)}$ = 0.25 V, I_{OUT} = 15 µA			0.8	V
I_{DD}	Supply current	V_{DD} = 2 V		6.0	10	µA
		V_{DD} ≥ 5 V		7.0	12	
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = 5 V		1	1.5	µA
I_{SET}	Internal pull-up current, SET pin	V_{DD} = 18 V, SET pin = GND		600		nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3 V, I_{OUT} = 0.4 mA			250	mV
		V_{DD} = 2 V, I_{OUT} = 3 mA			250	
		V_{DD} = 5 V, I_{OUT} = 5 mA			250	
$V_{IL(set)}$	Low-level SET pin input voltage				250	mV
$V_{IH(set)}$	High-level SET pin input voltage		750			mV
$I_{D(leak)}$	Open-drain output leakage current	V_{PU} = V_{DD}			300	nA
$I_{LKG(od)}$		V_{DD} = 2 V, V_{PU} = 18 V			300	
UVLO	Undervoltage lockout(3)	V_{DD} falling	1.3		1.7	V

(1) Hysteresis is 0.55% of the nominal trip point.
(2) The outputs are undetermined below $V_{(POR)}$.
(3) When V_{DD} falls below UVLO, UV is driven low and OV goes to high impedance.

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6.6 Timing Requirements

At V_{DD} = 2 V, 2.5% input overdrive(1) with R_{PU} = 10 kΩ, V_{OH} = 0.9 × V_{DD}, and V_{OL} = 400 mV, unless otherwise noted. R_{PU} refers to the pull-up resistor at the UV and OV pins.

		MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay(2)		19		µs
$t_{pd(LH)}$	Low-to-high propagation delay(2)		35		µs
t_R	Output rise time(3)		2.2		µs
t_F	Output fall time(3)		0.22		µs
t_{SD}	Startup delay(4)		300		µs

(1) Overdrive = | ($V_{(VDD)}$ / V_{IT} – 1) × 100% |.
(2) High-to-low and low-to-high refers to the transition at the SENSE pin.
(3) Output transitions from 10% to 90% for rise times and 90% to 10% for fall times.
(4) During the power-on sequence, V_{DD} must be at or above 2 V for at least t_{SD} before the output is in the correct state.

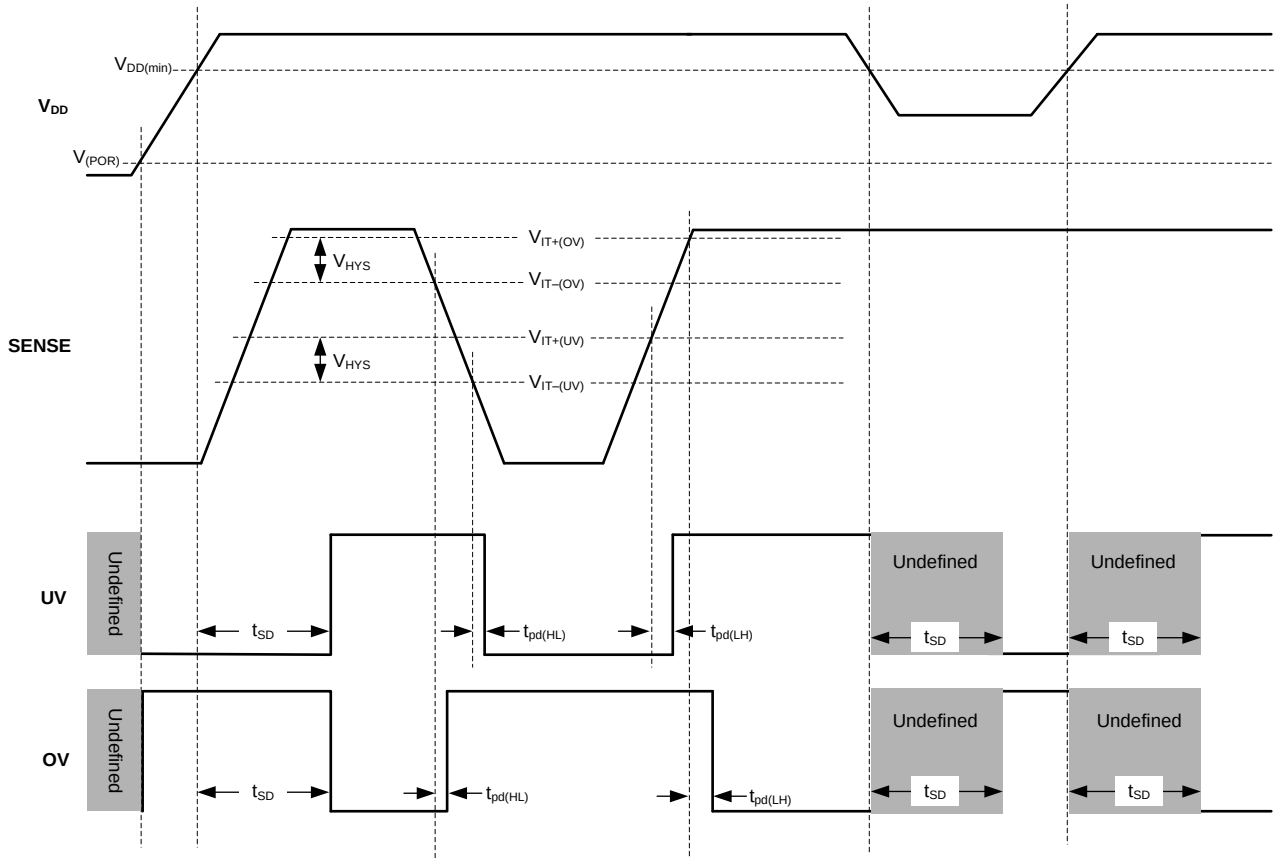
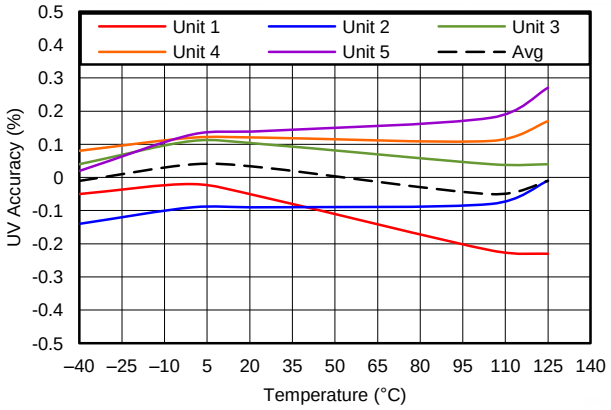


图 1. Timing Diagram

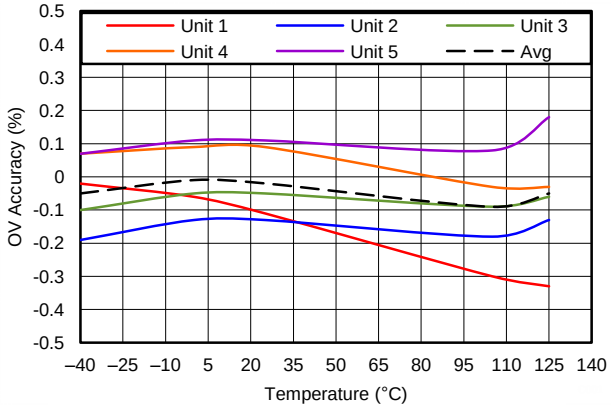
6.7 Typical Characteristics

At T_J = 25°C, V_{DD} = 3 V, and R_{PU} = 10 kΩ, unless otherwise noted.



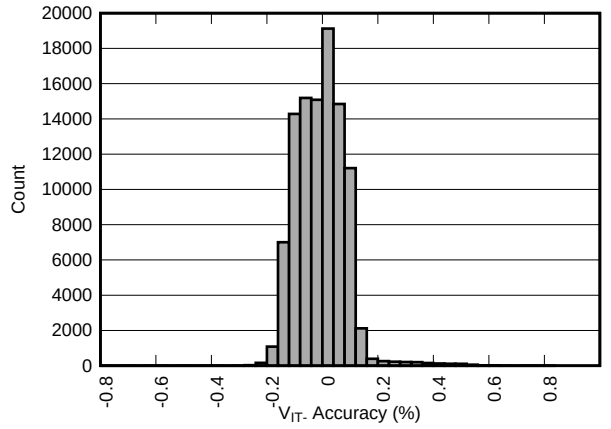
Performance is across V_{DD} with SET high or low

图 2. Undervoltage Accuracy vs Temperature



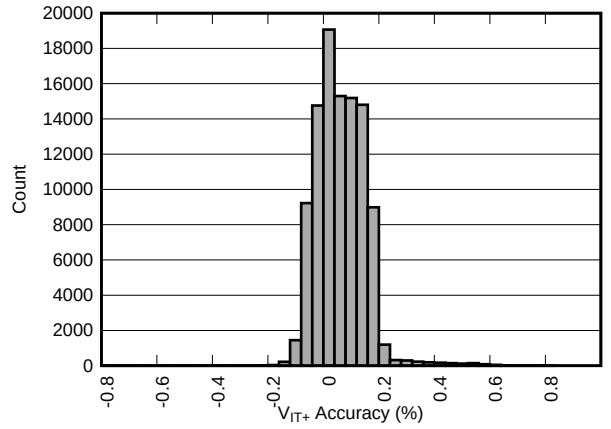
Performance is across V_{DD} with SET high or low

图 3. Overvoltage Accuracy vs Temperature



Performance is across V_{DD} with SET high or low

图 4. Undervoltage Accuracy Distribution



Performance is across V_{DD} with SET high or low

图 5. Overvoltage Accuracy Distribution

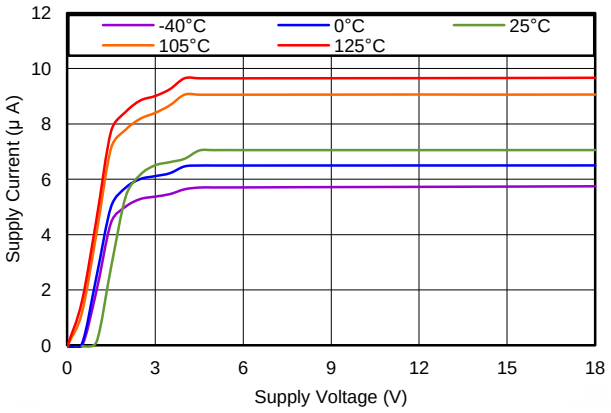


图 6. Supply Current vs Supply Voltage

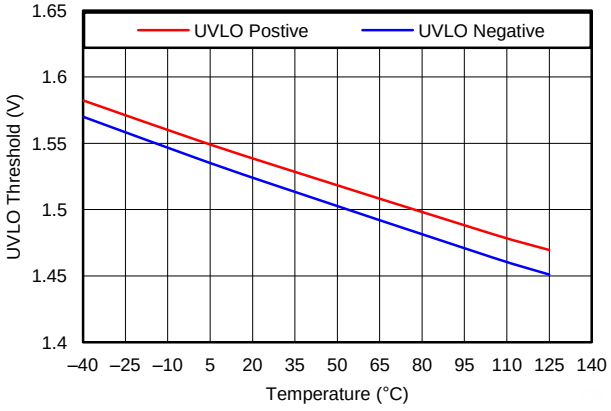


图 7. Undervoltage Lockout Threshold vs Temperature

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Typical Characteristics (接下页)

At T_J = 25°C, V_{DD} = 3 V, and R_{PU} = 10 kΩ, unless otherwise noted.

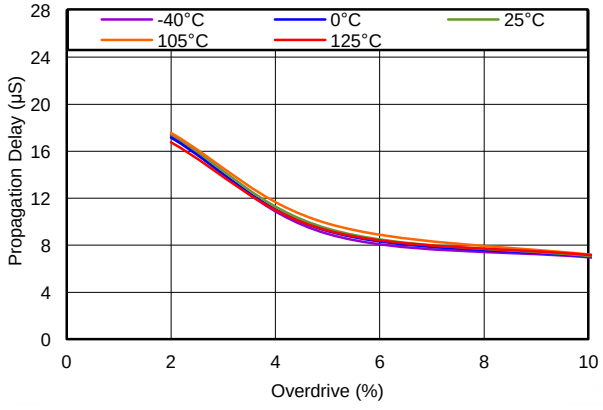


图 8. Undervoltage Propagation Delay vs Overdrive

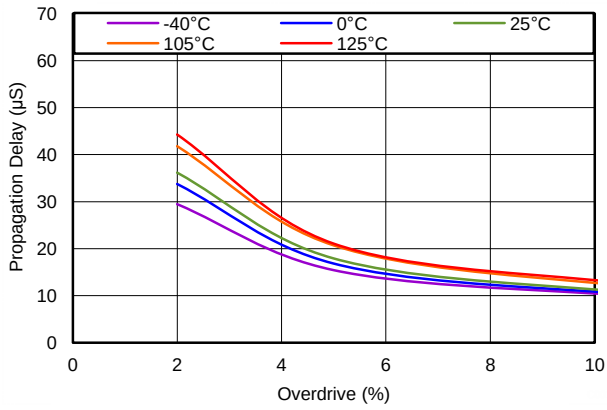


图 9. Overvoltage Propagation Delay vs Overdrive

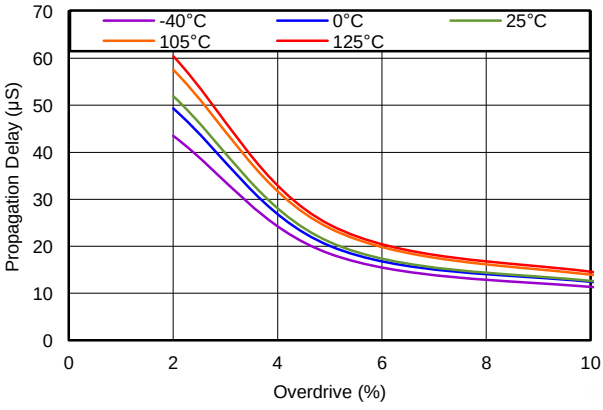


图 10. Undervoltage Propagation Delay vs Overdrive

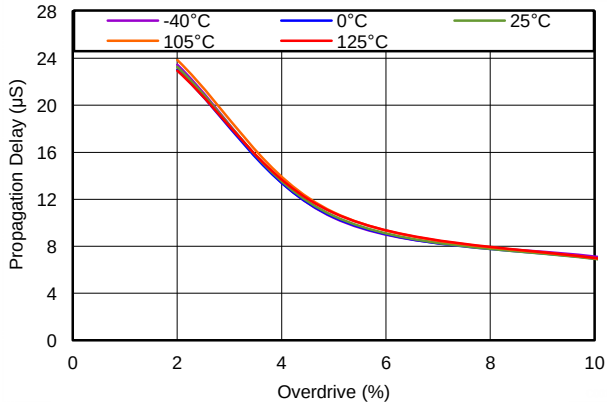


图 11. Overvoltage Propagation Delay vs Overdrive

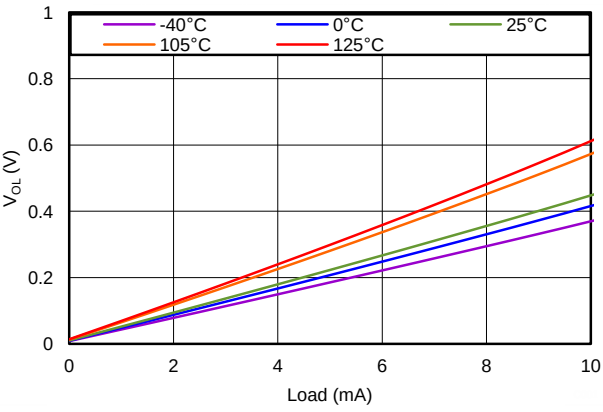


图 12. Low-Level Output Voltage vs Output Current

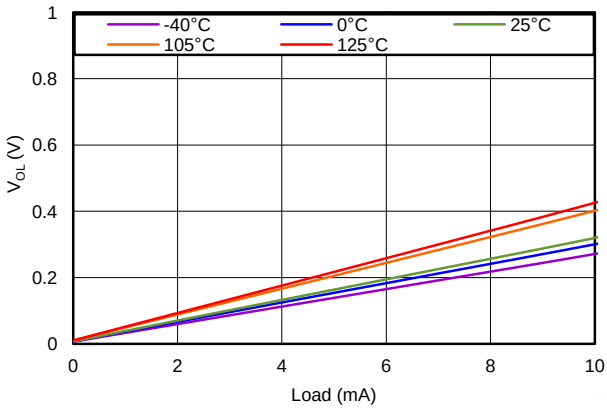


图 13. Low-Level Output Voltage vs Output Current

Typical Characteristics (接下页)

At T_J = 25°C, V_{DD} = 3 V, and R_{PU} = 10 kΩ, unless otherwise noted.

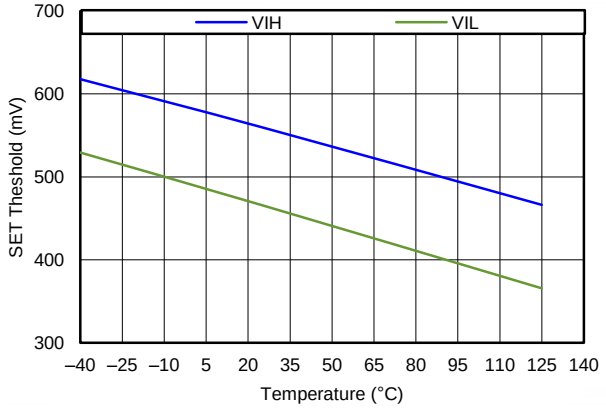


图 14. SET Threshold vs Temperature

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7 Detailed Description

7.1 Overview

The TPS3702-Q1 family of devices combines two comparators and a precision reference for overvoltage and undervoltage detection. The TPS3702-Q1 features a wide supply voltage range (2 V to 18 V) and highly accurate window threshold voltages (0.9% over temperature). The TPS3702-Q1 is designed for systems that require an active low signal if the voltage from the monitored power supply exits the accuracy band. The outputs can be pulled up to 18 V and can sink up to 10 mA.

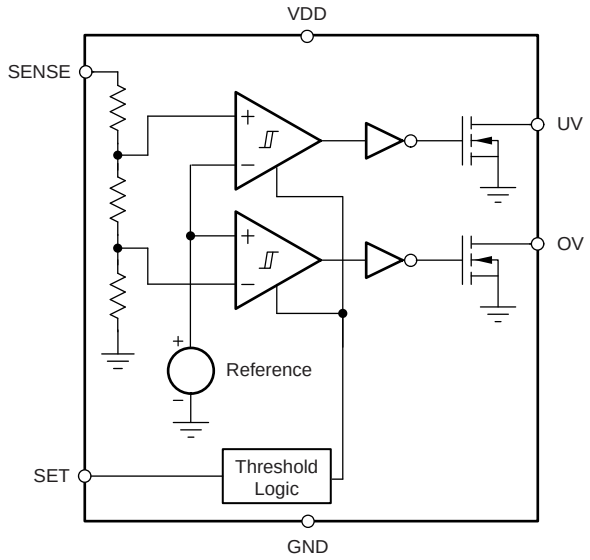
Unlike many other window comparators, the TPS3702-Q1 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

The TPS3702-Q1 is designed to assert active low output signals when the monitored voltage is outside the window band. The relationship between the monitored voltage and the states of the outputs is shown in 表 1.

表 1. Truth Table

CONDITION	OUTPUT	STATUS
SENSE < $V_{IT–(UV)}$	UV low	UV is asserted
SENSE > $V_{IT–(UV)}$ + V_{HYS}	UV high	UV is high impedance
SENSE > $V_{IT+(OV)}$	OV low	OV is asserted
SENSE < $V_{IT+(OV)}$ – V_{HYS}	OV high	OV is high impedance

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input (SENSE)

The TPS3702-Q1 combines two comparators with a precision reference voltage and a trimmed resistor divider. Only a single external input is monitored by the two comparators because the resistor divider is internal to the device. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides some noise immunity and ensures stable operation.

The SENSE input can vary from ground to 6.5 V (7.0 V, absolute maximum), regardless of the device supply voltage used. Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE input in order to reduce sensitivity to transient voltages on the monitored signal.

For the undervoltage comparator, the undervoltage output is driven to logic low when the SENSE voltage drops below the undervoltage falling threshold, $V_{IT–(UV)}$. When the voltage exceeds the undervoltage rising threshold, $V_{IT+(UV)}$ (which is $V_{IT-(UV)} + V_{HYS}$), the undervoltage output goes to a high-impedance state; see 图 1.

For the overvoltage comparator, the overvoltage output is driven to logic low when the voltage at SENSE exceeds the overvoltage rising threshold, $V_{IT+(OV)}$. When the voltage drops below the overvoltage falling threshold, $V_{IT–(OV)}$ (which is $V_{IT+(OV)} – V_{HYS}$), the overvoltage output goes to a high-impedance state; see 图 1. Together, these two comparators form a window-detection function as described in the *Window Comparator Considerations* section. Also see the *器件命名规则* section.

7.3.2 Outputs (UV, OV)

In a typical TPS3702-Q1 application, the outputs are connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the outputs are connected to the enable input of a voltage regulator [such as a dc-dc converter or low-dropout regulator (LDO)].

The TPS3702-Q1 provides two open-drain outputs (UV and OV) and uses pull-up resistors to hold these lines high when the output goes to a high-impedance state. Connect the pull-up resistors to the proper voltage rails to enable the outputs to be connected to other devices at the correct interface voltage levels. The TPS3702-Q1 outputs can be pulled up to 18 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current ($I_{D(leak)}$). These values are specified in the *Electrical Characteristics* table. Use wired-OR logic to merge the undervoltage and overvoltage signals into one logic signal that goes low if either outputs are asserted because of a fault condition.

表 1 describes how the outputs are either asserted low or high impedance. See 图 1 for a timing diagram that describes the relationship between the threshold voltages and the respective output.

7.3.3 User-Configurable Accuracy Band (SET)

The TPS3702-Q1 has an innovative feature allowing each device to be set for one of two accuracy bands, 表 3 describes the available accuracy bands with nominal thresholds ranging from ±2% to ±10% of the monitored rail nominal voltage. Forcing the voltage on the SET pin above the high-level SET pin input voltage, $V_{IH(SET)}$, sets the thresholds for the tighter window whereas forcing the voltage on the SET pin below the low-level SET pin input voltage, $V_{IL(SET)}$, sets the thresholds for the wider window.

Using the TPS3702Cxxx-Q1 as an example, when $V_{SET} \geq V_{IH(SET)}$ the nominal thresholds are set to ±4% (see 图 15). Thus, when the positive-going and negative-going threshold accuracy is accounted for, the device outputs an active low signal for voltage excursions outside a ±4.9% band (worst case), which is calculated by taking the nominal threshold percentage for that given part number and adding that value to the threshold accuracy found in the *Specifications* section. Similarly, when $V_{SET} \leq V_{IL(SET)}$, the nominal thresholds are set to ±9% and the device outputs an active low signal for voltage excursions outside the ±9.9% band (worst case).

The ability for the user to change the accuracy band allows a system to programmatically change the accuracy band during certain conditions. One example is during system start up when the monitored voltage can be slightly outside its typical accuracy specifications but a reset signal is not desired. In this case, V_{SET} can be set below $V_{IL(SET)}$ to detect voltage excursions outside the 10% band and, after the system is fully started up, V_{SET} can be pulled higher than $V_{IH(SET)}$, thus tightening the band to ±5%.

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Feature Description (接下页)

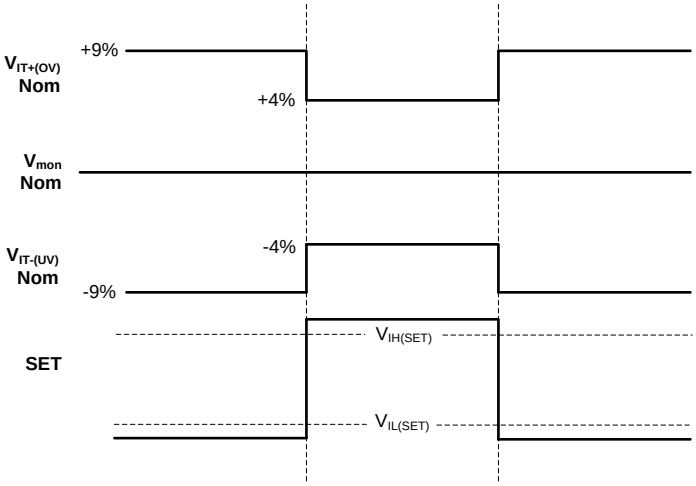


图 15. TPS3702Cxxx User-Configurable Accuracy Bands

Another benefit of allowing the user to change the accuracy band is the reduction in qualification costs. Users who have multiple rail monitoring needs (such as some rails that must be within ±5% of the nominal voltage and other rails that must be within ±10% of the same nominal voltage) benefit by only having to spend the time and money qualifying one device instead of two.

7.4 Device Functional Modes

7.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on VDD is greater than UVLO for approximately 300 µs (t_{SD}), the undervoltage and overvoltage signals correspond to the voltage on the SENSE pin; see 表 1.

7.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} <$ UVLO)

When the voltage on VDD is less than the device UVLO voltage but greater than the power-on reset voltage ($V_{(POR)}$), the undervoltage output is asserted and the overvoltage output is high impedance, regardless of the voltage on SENSE.

7.4.3 Power-On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are undefined and are not to be relied upon for proper device function.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS3702-Q1 is a precision window comparator that can be used in several different configurations. The supply voltage (V_{DD}), the monitored voltage, and the output pullup voltage can be independent voltages or connected in many configurations. 图 16 shows how the outputs operate with respect to the voltage on the SENSE pin.

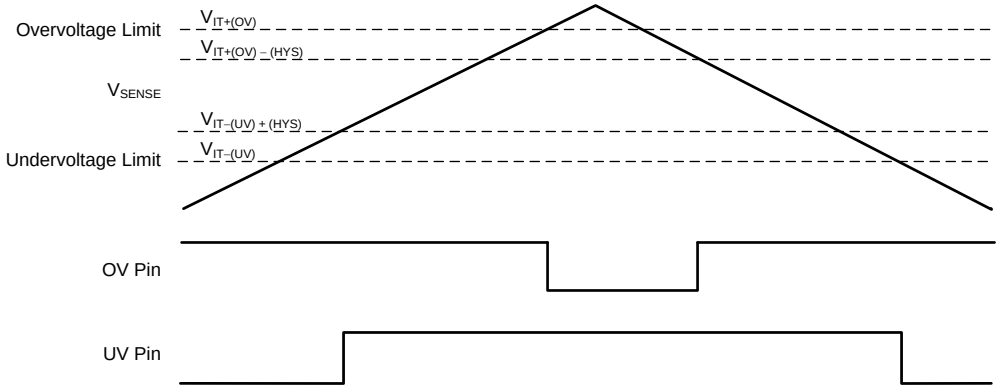


图 16. Window Comparator Operation

The following sections show the connection configurations and the voltage limitations for each configuration.

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Application Information (接下页)

8.1.1 Window Comparator Considerations

The inverting and noninverting configurations of the comparators form a window-comparator detection circuit by using the internal resistor divider. The internal resistor divider allows for set voltage thresholds that already account for the tolerances of the resistors in the resistor divider. The UV and OV pins signal undervoltage and overvoltage conditions, respectively, on the SENSE pin, as shown in 图 17.

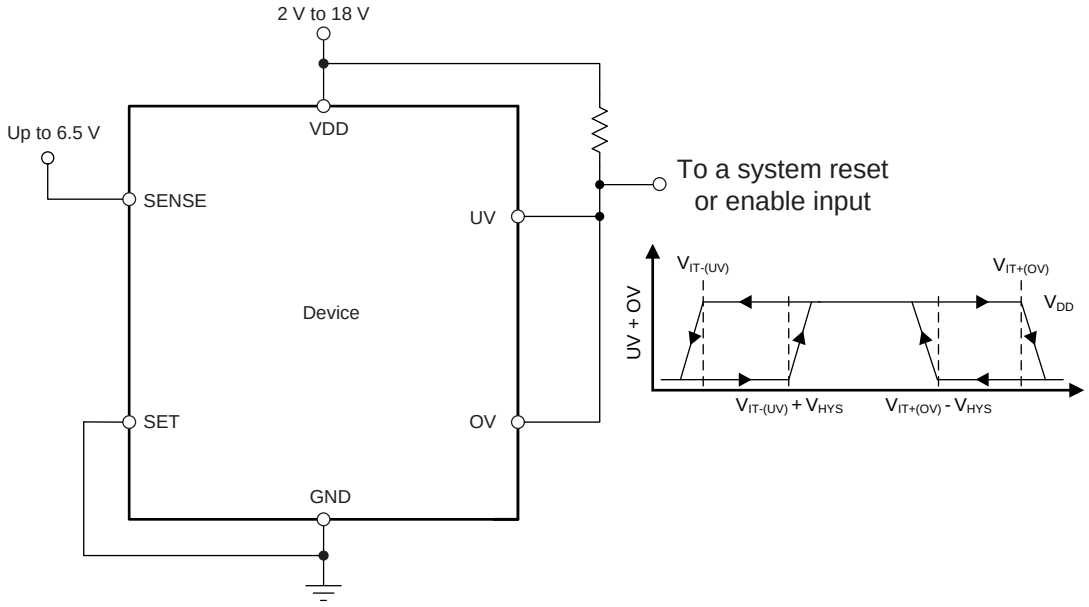


图 17. Window Comparator Schematic

The TPS3702-Q1 flags the overvoltage or undervoltage conditions with the most accuracy in order to ensure proper system operation. The highest accuracy threshold voltages are $V_{IT–(UV)}$ and $V_{IT+(OV)}$, and correspond with the falling SENSE undervoltage flag and the rising SENSE overvoltage flag, respectively. These thresholds represent the accuracy when the monitored voltage changes from being within the desired window (when both the undervoltage and overvoltage outputs are high) to when the monitored voltage goes outside the desired window, indicating a fault condition. If the monitored voltage is outside of the valid window (V_{SENSE} is less than the undervoltage limit, $V_{IT–(UV)}$, or greater than overvoltage limit, $V_{IT+(OV)}$), then the SENSE threshold voltages to enter into the valid window are $V_{IT+(UV)} = V_{IT–(UV)} + V_{HYS}$ or $V_{IT–(OV)} = V_{IT+(OV)} – V_{HYS}$.

Application Information (接下页)

8.1.2 Input and Output Configurations

图 18 to 图 20 illustrate examples of the various input and output configurations.

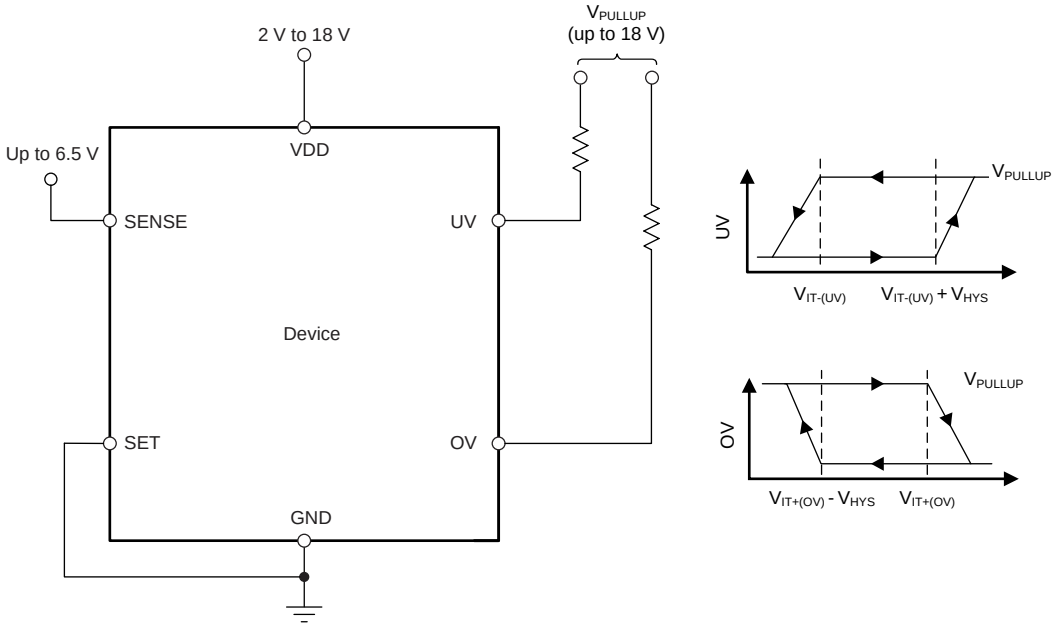


图 18. Interfacing to Voltages Other Than V_{DD}

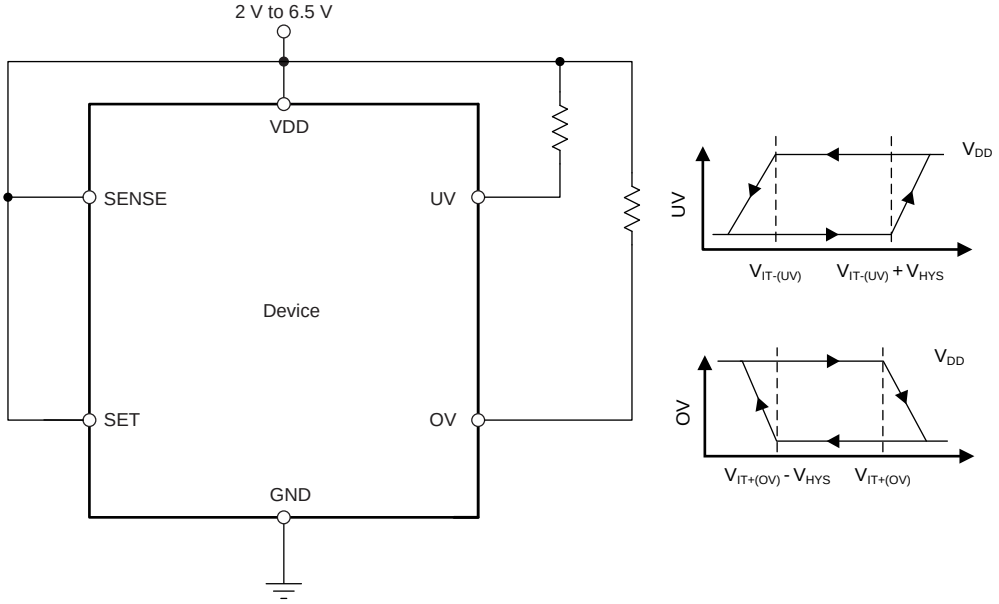


图 19. Monitoring the Same Voltage as V_{DD} with Wired-OR Logic

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Application Information (接下页)

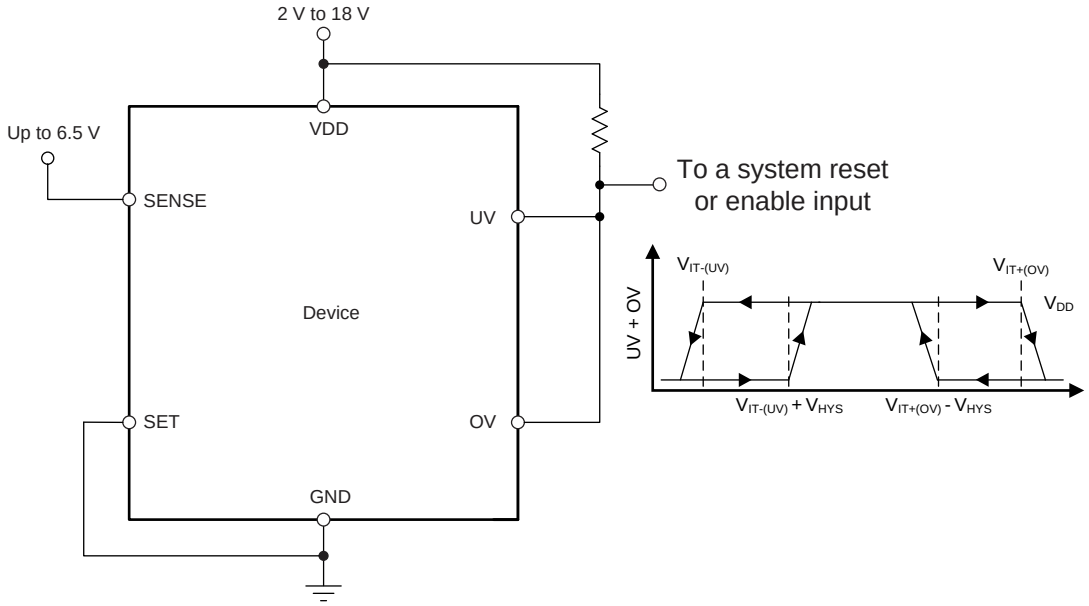


图 20. Monitoring a Voltage Other Than V_{DD} with Wired-OR Logic

Note that the SENSE input can also monitor voltages that are higher than $V_{SENSE\ (max)}$ or that may not be designed for rail voltages with the use of an external resistor divider network. If a resistor divider is used to reduce the voltage on the SENSE pin, ensure that the I_{SENSE} current is accounted for so the accuracy is not unexpectedly affected. As a general approximation, the current flowing through the resistor divider to ground must be greater than 100 times the current going into the SENSE pin. See application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for a more in-depth discussion on setting an external resistor divider.

8.1.3 Immunity to SENSE Pin Voltage Transients

The TPS3702-Q1 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient.

Overdrive is defined by how much the V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs (UV and OV). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 1:

$$\text{Overdrive} = | (V_{SENSE} / V_{IT} - 1) \times 100\% | \quad (1)$$

where:

- V_{IT} is either V_{IT-} or V_{IT+} for UV or OV.

图 8 to 图 11 illustrate the V_{SENSE} minimum detectable pulse versus overdrive, and can be used to visualize the relationship that overdrive has on propagation delay.

8.2 Typical Application

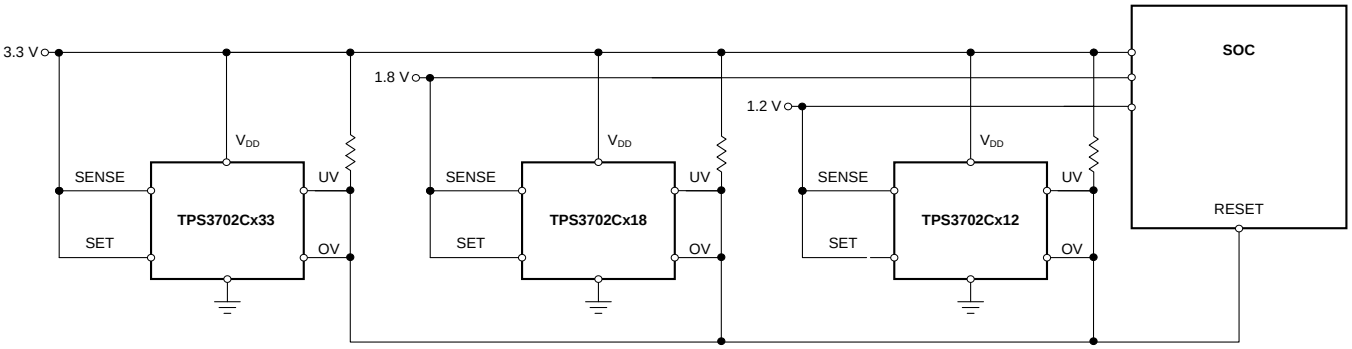


图 21. ±5% Window Monitoring for SOC Power Rails

8.2.1 Design Requirements

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3-V nominal, with alerts if outside of ±5% of 3.3 V (including device accuracy)	Worst case $V_{IT+(OV)}$ = 3.463 V (4.94%), Worst case $V_{IT-(UV)}$ = 3.139 V (4.86%)
	1.8-V nominal, with alerts if outside of ±5% of 1.8 V (including device accuracy)	Worst case $V_{IT+(OV)}$ = 1.889 V (4.94%), Worst case $V_{IT-(UV)}$ = 1.712 V (4.86%)
	1.2-V nominal, with alerts if outside of ±5% of 1.2 V (including device accuracy)	Worst case $V_{IT+(OV)}$ = 1.259 V (4.94%), Worst case $V_{IT-(UV)}$ = 1.142 V (4.86%)
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum device current consumption	50 µA	40.5 µA (max), 24 µA (typ)

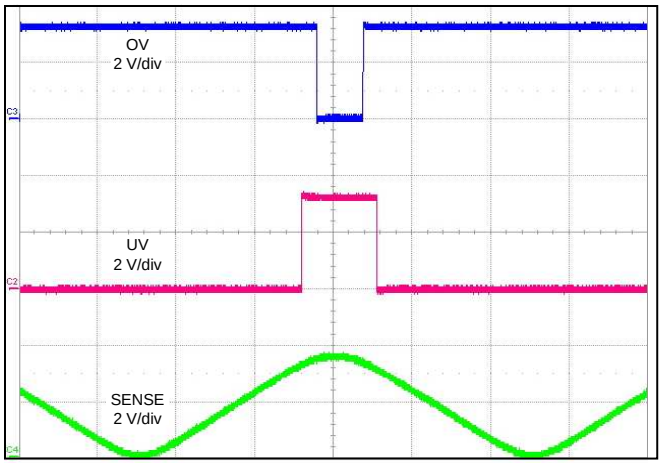
8.2.2 Detailed Design Procedure

Determine which version of the TPS3702-Q1 best suits the application nominal rail and window tolerances. See 表 3 for selecting the appropriate device number for the application needs. If the nominal rail voltage to be monitored is not listed as an option, a resistor divider can be used to reduce the voltage to a nominal voltage that is available. The current I_{SENSE} causes an error in the voltage detected at the SENSE pin because the SENSE current only flows through the resistor at the top of the resistor divider. The larger the current through the resistor divider to ground, the smaller this error will be. To optimize this resistor divider, refer to application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for more information.

When the outputs switch to the high-Z state, the rise time of the UV or OV node depends on the pull-up resistance and the capacitance on that node. Choose pull-up resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 10-kΩ to 1-MΩ resistors are a good choice for low-capacitive loads.

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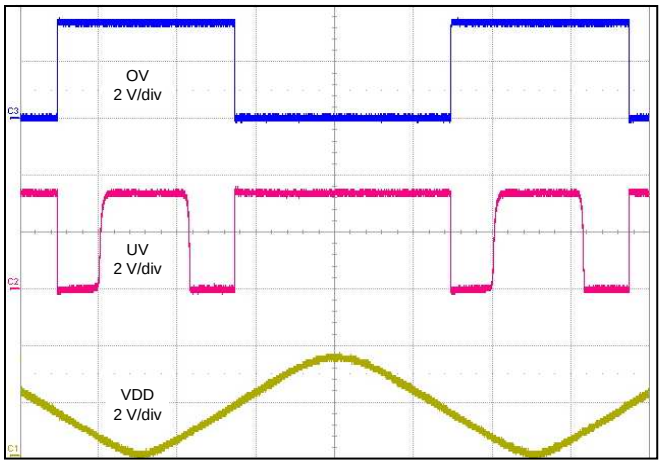
8.2.3 Application Curves



Time (1 ms/div)

V_{SENSE} goes from 0 V to 3.47 V ($V_{IT+(OV)}$), V_{DD} = 3.3 V, V_{PULLUP} = 3.3 V

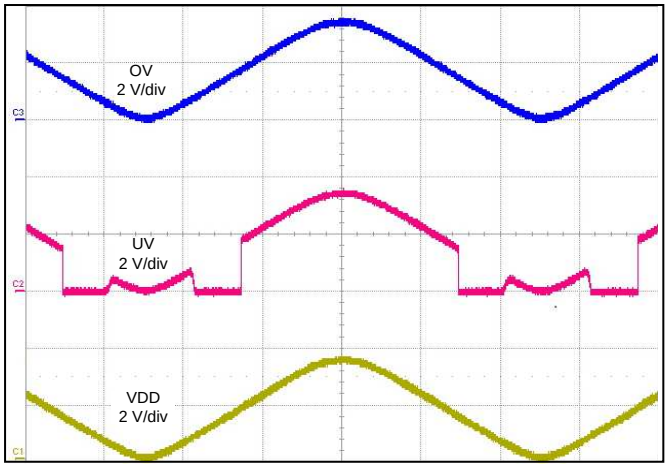
图 22. TPS3702CX33-Q1 Window Comparator Function



Time (1 ms/div)

V_{DD} goes from 0 V to 3.3 V, V_{SENSE} = 3.47 V (above $V_{IT+(OV)}$)

图 23. TPS3702CX33-Q1 Startup with V_{PULLUP} = 3 V



Time (1 ms/div)

V_{DD} goes from 0 V to 3.3 V, V_{SENSE} = 3.3 V

图 24. TPS3702CX33-Q1 Startup with V_{PULLUP} = V_{DD}

9 Power Supply Recommendations

The TPS3702-Q1 is designed to operate from an input voltage supply range between 2 V and 18 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin. This device has a 20-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 20 V, additional precautions must be taken.

10 Layout

10.1 Layout Guidelines

- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum VDD voltage.

10.2 Layout Example

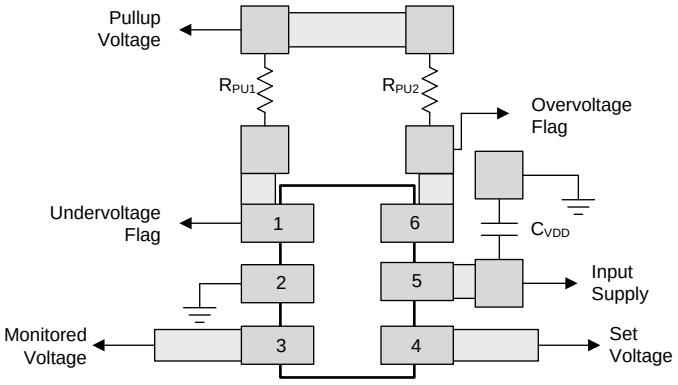


图 25. Recommended Layout

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11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TPS3702 配套使用，帮助评估初始电路性能。TPS3702CX33EVM-683 评估模块（和相关的用户指南）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI 网上商店购买。

11.1.2 器件命名规则

表 3 以 TPS3702CX33-Q1 为例，介绍如何根据器件部件号确定器件的功能。

表 3. 器件命名约定

说明	命名规则	值
TPS3702 （高精度窗口比较器系列）	—	—
C （标称阈值，受监视电压标称值的百分比）	A	SET 引脚高电平 = ±2%，SET 引脚低电平 = ±6%
	B	SET 引脚高电平 = ±3%，SET 引脚低电平 = ±7%
	C	SET 引脚高电平 = ±4%，SET 引脚低电平 = ±9%
	D	SET 引脚高电平 = ±5%，SET 引脚低电平 = ±10%
X （滞后选项）	X	0.55%
	Y	1.0%
33 （受监视电压标称值选项）	10	1.0V
	12	1.2V
	18	1.8V
	33	3.3V
	50	5.0V
Q1 （汽车版本）	—	—

表 4 列出了 TPS3702 系列的已发布版本，其中包括标称欠压和过压阈值。有关表 3 中所列的其他选项的详细信息和可用性，请联系制造商；最低订购量适用。

表 4. 已发布器件的阈值

产品	标称电源 (V)	滞后 (%)	UV 阈值 (V) SET ≤ $V_{IL(SET)}$	UV 阈值 (V) SET ≥ $V_{IH(SET)}$	OV 阈值 (V) SET ≤ $V_{IL(SET)}$	OV 阈值 (V) SET ≥ $V_{IH(SET)}$
TPS3702CX10	1.0	0.5	0.91	0.96	1.09	1.04
TPS3702CX12	1.2	0.5	1.09	1.15	1.31	1.25
TPS3702AX18	1.8	0.5	1.69	1.76	1.91	1.84
TPS3702CX18	1.8	0.5	1.64	1.73	1.96	1.87
TPS3702AX33	3.3	0.5	3.10	3.23	3.50	3.37
TPS3702CX33	3.3	0.5	3.00	3.17	3.60	3.43
TPS3702CX50	5.0	0.5	4.55	4.80	5.45	5.20

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11.2 文档支持

11.2.1 相关文档

优化比较器输入上的电阻分压器，SLVA450

《*TPS3702CX33EVM-683 评估模块*》，SBVU026

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
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接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
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OMAP应用处理器	www.ti.com/omap		
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3702AX18QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFIO	Samples
TPS3702AX33QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFEO	Samples
TPS3702CX10QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFGO	Samples
TPS3702CX12QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFFO	Samples
TPS3702CX18QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFJO	Samples
TPS3702CX33QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFHO	Samples
TPS3702CX50QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFWO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

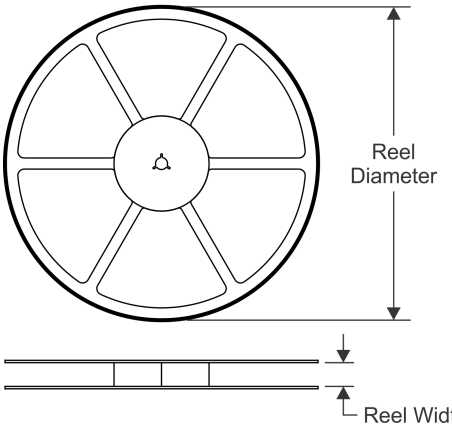
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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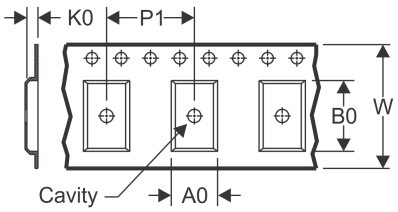
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

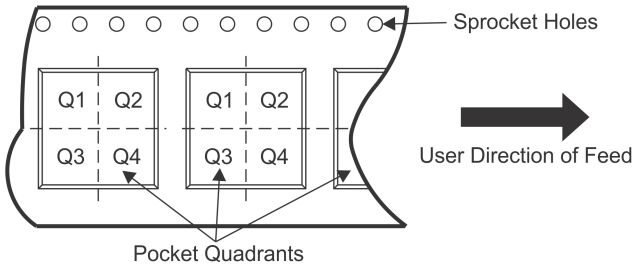


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

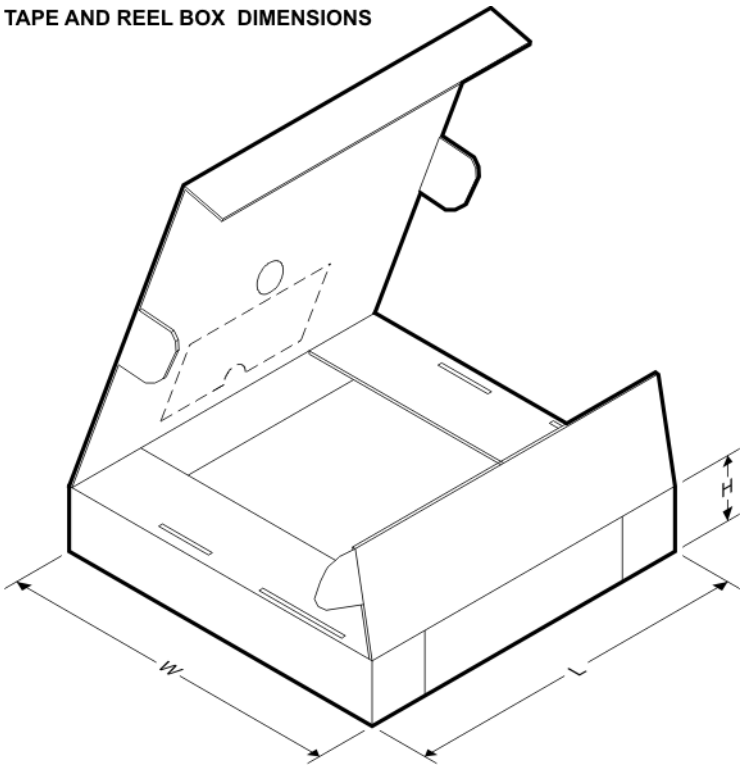
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3702AX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702AX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX10QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX12QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX50QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

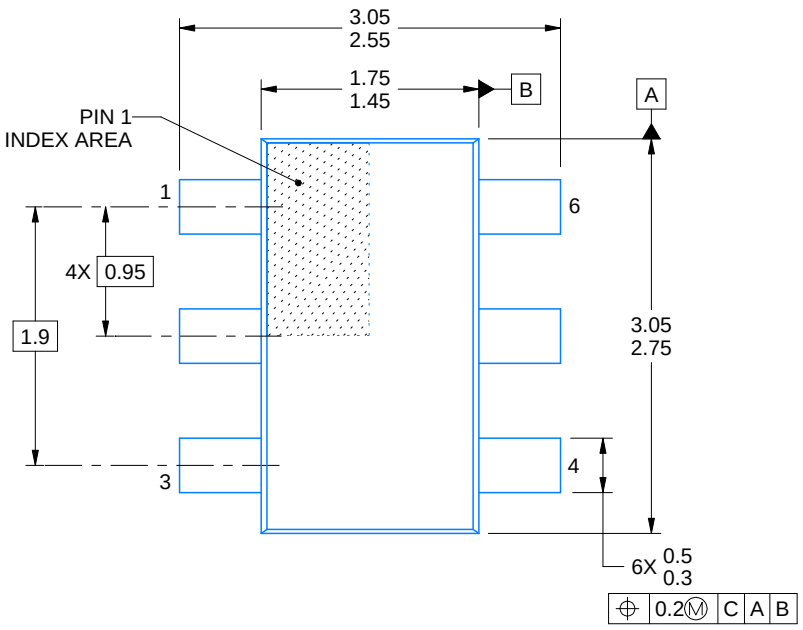
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3702AX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702AX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX10QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX12QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX50QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0

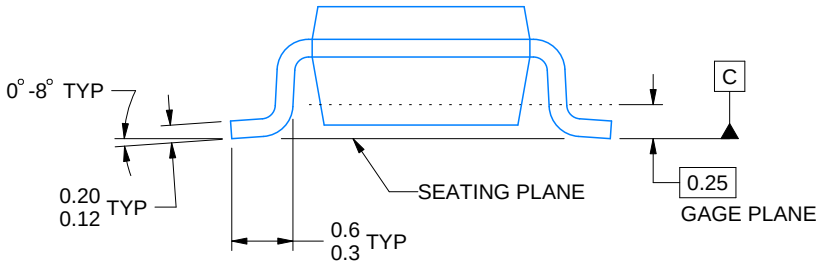
PACKAGE OUTLINE

DDC0006A

SOT - 1.1 max height

SOT

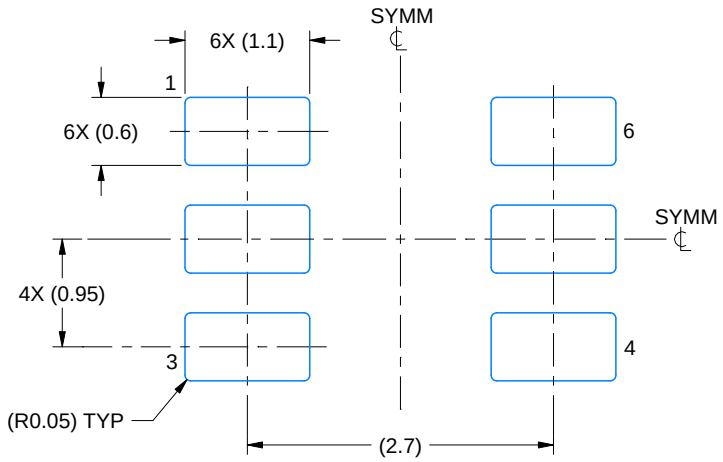




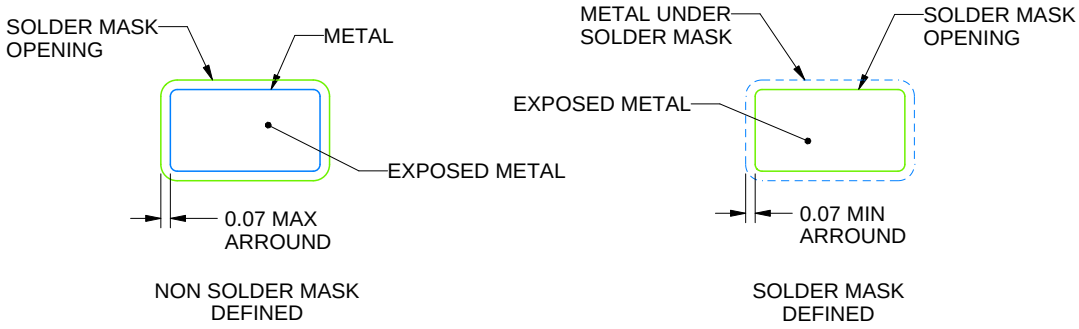
4214841/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

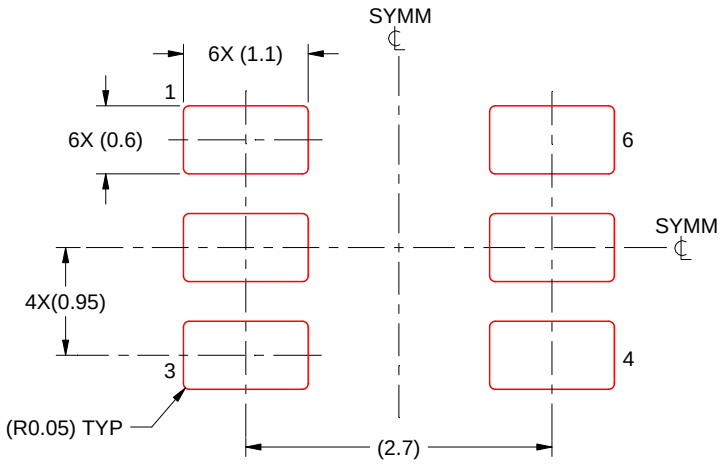


SOLDERMASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/B 11/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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