SINGLE-CHIP CHARGER AND DC/DC CONVERTER IC FOR PORTABLE APPLICATIONS

FEATURES

- **Li-Ion Or Li-Pol Charge Management and Synchronous DC-DC Power Conversion In a Single Chip**
- **Charges and Powers the System from Either the AC Adapter or USB with Autonomous Power Source Selection**
- **Integrated USB Charge Control with Selectable 100 mA and 500 mA Charge Rates**
- **Integrated Power FET and Current Sensor for Up to 500 mA Charge Applications AND 300 mA DC-DC Controller with Integrated FETs**
- **Reverse Leakage Protection Prevents Battery Drainage**
- **Automatic Power Save Mode For High Efficiency at Low Current, or Forced PWM for Frequency Sensitive Applications**

APPLICATIONS

- **MP3 Players**
- **PDAs, Smartphones**
- **Digital Cameras**

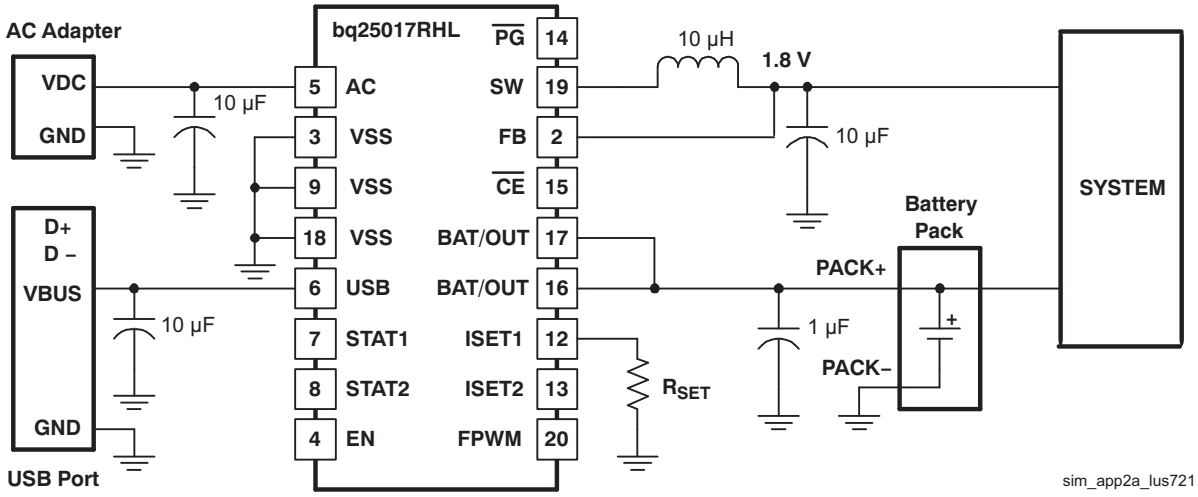
DESCRIPTION

The bq25015/7 are highly integrated charge and power management devices targeted at space-limited bluetooth applications. The bq25015/7 devices offer integrated power FET and current sensor for charge control, reverse blocking protection, high accuracy current and voltage regulation, charge status, charge termination, and a highly efficient and low-power dc-dc converter in a small package.

The bq25015/7 devices charge the battery in three phases: conditioning, constant current and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety feature for charge termination. The bq25015/7 automatically re-starts the charge if the battery voltage falls below an internal threshold. The bq25015/7 automatically enters sleep mode when V_{CC} supply is removed.

The integrated low-power high-efficiency dc-dc converter is designed to operate directly from a single-cell Li-ion or Li-Pol battery pack. The output voltage is either adjustable from 0.7 V to VBAT, or fixed at 1.8 V (bq25017) and is capable of delivering up to 300-mA of load current. The dc-dc converter operates at a synchronized 1 MHz switching frequency allowing for the use of small inductors.

TYPICAL APPLICATION



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	OUTPUT VOLTAGE (V)	PART NUMBER(2)(3)	STATUS	PACKAGE MARKING
-40°C to 125°C	Adjustable	bq25015RHLR	Production	BZL
	Adjustable	bq25015RHLT	Production	BZL
	1.8 V	bq25017RHLR	Production	BZM
	1.8 V	bq25017RHLT	Production	BZM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com
(2) The RHL package is available taped and reeled only in quantities of 3,000 devices per reel.
(3) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		bq25015/7
Supply voltage	AC, USB (wrt VSS)	–0.3 V to 7 V
Input voltage	$\overline{PG}$, OUT, ISET1, ISET2, STAT1, STAT2, TS (wrt VSS)	–0.3 V to 7 V
	EN, FB, FPWM, SW (wrt VSS)	V_{OUT} + 0.3 V
Output sink/source current	$\overline{PG}$, STAT1, STAT2	15 mA
	TS	200 µA
Output source current	OUT	1.5 A
Storage temperature range, T_{stg}		–65°C to 150°C
Junction temperature range, T_J		–40°C to 125°C
Lead temperature (solderig, 10 seconds)		260°C
ESD rating (human body model, HBM)		1500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage (from AC input)	4.5	6.5	V
V_{CC}	Supply voltage (from USB input)	4.35	6.5	
T_A	Operating temperature range	0	85	°C
I_{OUT_L}	Maximum DC-DC output current		300	mA

DISSIPATION RATINGS

PACKAGE	T_A < 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 40°C	θ_{JA}
20-pin RHL(1)	1.81 W	21 mW/°C	46.87°C/W

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2×3 via matrix.

ELECTRICAL CHARACTERISTICS

over operating temperature range (T_A = 0°C to 125°C) and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
$I_{CC(VCC)}$	Supply current 1, VCC	$V_{VCC} > V_{VCC(min)}$		1.2	2.0	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into OUT/BAT, $V_{VCC} < V_{(SLP)}$		2	5	µA
$I_{CC(STDBY)}$	Standyby current	$\overline{CE}$ = High, 0°C ≤ T_J ≤ 85°C			150	µA
$I_{IB(OUT)}$	Input current, OUT	Charge DONE, $V_{VCC} > V_{VCC(min)}$, $I_{OUT(SW)}$ = 0 mA, Converter not switching		15	35	µA
$I_{IB(CE)}$	Input current, $\overline{CE}$				1	µA
CHARGE VOLTAGE REGULATION ($V_{BAT(REG)}$ + $V_{(DO-MAX)}$ ≤ V_{VCC}, $I_{(TERM)}$ < $I_{OUT(BAT)}$ ≤ 0.5 A)						
$V_{REG(BAT)}$	Charger regulation voltage			4.2		V
	Charge voltage regulation accuracy	T_A = 25°C	–0.35%		0.35%	
			–1%		1%	
($V_{(AC)}$ – $V_{(OUT)}$)	AC dropout voltage	$V_{OUT\ (BAT)} = V_{REG\ (BAT)}$, $I_{OUT(BAT)}$ = 0.5 A		175	250	mV
($V_{(USB)}$ – $V_{(OUT)}$)	USB dropout voltage	$V_{OUT\ (BAT)} = V_{REG\ (BAT)}$, ISET2 = High		350	500	mV
		$V_{OUT\ (BAT)} = V_{REG\ (BAT)}$, ISET2 = Low		60	100	mV
CHARGE CURRENT REGULATION						
$I_{OUT\ (BAT)}$	AC output current range	V_{VCC} ≥ 4.5 V, $V_{OUT\ (BAT)} = V_{(LOWV)}$, $V_{VCC} - V_{OUT\ (BAT)} > V_{(DO-MAX)}$, $I_{OUT(BAT)} = (K_{(SET)} \times V_{(SET)} / R_{SET})$	50		500	mA
$I_{OUT\ (BAT)}$	USB output current range	$V_{VCC(min)}$ ≥ 4.5 V, $V_{OUT\ (BAT)} = V_{(LOWV)}$, $V_{VCC} - V_{OUT\ (BAT)} > V_{(DO-MAX)}$, ISET2= Low	80		100	mA
		$V_{VCC(min)}$ ≥ 4.5 V, $V_{OUT\ (BAT)} = V_{(LOWV)}$, $V_{VCC} - V_{OUT\ (BAT)} > V_{(DO-MAX)}$, ISET2 = High	400		500	mA
$V_{(SET)}$	Output current set voltage	Voltage on ISET1, V_{VCC} ≥ 4.5 V, $V_{OUT\ (BAT)} = V_{(LOWV)}$, $V_{VCC} - V_{OUT\ (BAT)} > V_{(DO-MAX)}$, ISET2 = High	2.436	2.500	2.538	V
$K_{(SET)}$	Output current set factor	50 mA ≤ $I_{OUT(OUT)}$ ≤ 1000 mA	307	322	337	
		10 mA ≤ $I_{OUT(OUT)}$ ≤ 50 mA	296	320	346	
		10 mA ≤ $I_{OUT(OUT)}$ ≤ 10 mA	246	320	416	
PRECHARGE and SHORT-CIRCUIT CURRENT REGULATION						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold	Voltage on OUT/BAT	2.8	3.0	3.2	V
t_{PRECHG_DG}	Deglitch time for fast-charge to precharge transition	$V_{VCC(min)}$ ≥ 4.5 V, t_{FALL} = 100 ns, 10 mV overdrive, $V_{IN(BAT)}$ decreasing below threshold	250	375	500	ms
$I_{OUT(PRECHG)}$	Precharge range	0 V < $V_{IN(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$, $I_{OUT(PRECHG)} = (K_{(SET)} \times V_{(PRECHG)}) / R_{SET}$	5		100	mA
$V_{(PRECHG)}$	Precharge set voltage	Voltage on ISET1, $V_{REG(BAT)}$ = 4.2 V, 0 V < $V_{IN(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$	240	255	270	mV
CHARGE TAPER and TERMINATION DETECTION						
$I_{(TAPER)}$	Charge taper detection range	$V_{IN(BAT)} > V_{(RCH)}$, t < $t_{(PRECHG)}$, $I_{(TAPER)} = (K_{(SET)} \times V_{(TAPER)}) / R_{SET}$	5		100	mA
$V_{(TAPER)}$	Charge taper detection set voltage	Voltage on ISET1, $V_{REG(BAT)}$ = 4.2 V, $V_{IN(BAT)} > V_{(RCH)}$, t < $t_{(PRECHG)}$	235	250	265	mV
$V_{(TERM)}$	Charge termination detection set voltage	Voltage on ISET1, $V_{REG(BAT)}$ = 4.2 V, $V_{IN(BAT)} > V_{(RCH)}$, t < $t_{(PRECHG)}$, $I_{(TERM)} = (K_{(SET)} \times V_{(TERM)}) / R_{SET}$	11	18	25	mV

ELECTRICAL CHARACTERISTICS (continued)

over operating temperature range (T_A = 0°C to 125°C) and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TPRDET_DG}	Deglitch time for taper detection	$V_{VCC(min)} \geq$ 4.5 V, t_{FALL} = 100 ns, 10 mV overdrive, I_{CHG} increasing above or decreasong below threshold	250	375	500	ms
$t_{TERMDET_DG}$	Deglitch time for termination detection	$V_{VCC(min)} \geq$ 4.5 V, t_{FALL} = 100 ns, 10 mV overdrive, I_{CHG} decreasing below threshold	350	375	500	
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge threshold voltage		$V_{REG(BAT)}$ – 0.115	$V_{REG(BAT)}$ – 0.10	$V_{REG(BAT)}$ – 0.085	V
t_{RCHDET}	Deglitch time for recharge detect	$V_{VCC(min)} \geq$ 4.5 V, t_{FALL} = 100 ns, 10 mV overdrive, I_{CHG} decreasing below or increasing above threshold	250	375	500	ms
STAT1, STAT2 and $\overline{PG}$ OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 5 mA			0.25	V
ISET2 and $\overline{CE}$ INPUTS						
V_{IL}	Low-level input voltage	I_{IL}= 10 µA	0		0.4	V
V_{IH}	High-level input voltage	I_{IL}= 20 µA	1.4			
I_{IL}	Low-level input current, $\overline{CE}$		–1			µA
I_{IH}	High-level input current, $\overline{CE}$				1	
I_{IL}	Low-level input current, ISET2	V_{ISET2} = 0 V	–20			
I_{IH}	High-level input current, ISET2	$V_{ISET2} = V_{CC}$			40	
I_{IHZ}	High-Z input current, ISET2	V_{ISET2} = High-Z			1	
TIMERS						
$t_{(PRECHG)}$	Precharge time limit		1620	1800	1930	s
$t_{(TAPER)}$	Taper time limit		1620	1800	1930	
$t_{(CHG)}$	Charge time limit		16200	18000	19300	
$I_{(FAULT)}$	Timer fault recovery current			200		µA
SLEEP COMPARATOR for CHARGER						
$V_{(SLP)}$	Sleep mode entry threshold	2.3 V ≤ $V_{IN(BAT)} \leq V_{REG(BAT)}$			$V_{VCC} \leq V_{IN(BAT)}$ +80 mV	V
$V_{(SLP_DG)}$	Sleep mode exit threshold	2.3 V ≤ $V_{IN(BAT)} \leq V_{REG(BAT)}$	$V_{VCC} \geq V_{IN(BAT)}$ +190 mV			
$t_{(DEGL)}$	Deglitch time for sleep mode	V_{CC} decreasing below threshold, t_{FALL} = 100 ns, 10 mV overdrive,	250	375	500	ms
THERMAL SHUTDOWN						
$T_{(SHTDWN)}$	Thermal trip threshold temperature			165		°C
	Thermal hysteresis			15		
UNDERVOLTAGE LOCKOUT AND POR						
$V_{(UVLO_CHG)}$	Undervoltage lockout threshold voltage	Decreasing V_{CC}	2.4	2.5	2.6	V
	Hysteresis			27		mV
V_{POR}	POR threshold voltage(1)		2.3	2.4	2.5	V
DC-DC INPUT						
$V_{(BAT)}$	Input voltage range	Input power absent	$V_{(LOWV)}$		4.2	V
		Input power present	$V_{(UVLO)}$		4.2	
$V_{(UVLO)}$	Undervoltage lockout				2.0	

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating temperature range (T_A = 0°C to 125°C) and recommended supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
FPWM – bq25015							
$V_{IH(FPWM)}$	High-level input voltage			2.0			
$V_{IL(FPWM)}$	Low-level input voltage					0.4	
FPWM – bq25017							
$V_{IH(FPWM)}$	High-level input voltage			1.3			V
$V_{IL(FPWM)}$	Low-level input voltage					0.4	
I_{FPWM}	Input bias current		V_{EN} = GND or V_{BAT}, V_{FPWM} = GND or V_{BAT}		0.01	0.1	µA
ENABLE							
$V_{IH(EN)}$	High-level input voltage			1.3			V
$V_{IL(EN)}$	Low-level input voltage					0.4	
I_{EN}	Input bias current		V_{EN} = GND or V_{BAT}, V_{FPWM} = GND or V_{BAT}		0.01	0.1	µA
POWER SWITCH							
$R_{DS(on)}$	Internal P-channel MOSFET on-resistance		V_{IN} = V_{GS} = 3.6 V		530	790	mΩ
			V_{IN} = V_{GS} = 2.5 V		670	930	
	Internal N-channel MOSFET on-resistance		V_{IN} = V_{GS} = 3.6 V		430	620	
			V_{IN} = V_{GS} = 2.5 V		530	740	
$I_{LEAK(P)}$	P-channel leakage current		V_{DS} = 6.0 V		0.1	1.0	µA
$I_{LEAK(N)}$	N-channel leakage current		V_{DS} = 6.0 V		0.1	1.0	
$I_{(LIM)}$	P-channel current limit		2.5 V < V_{BAT} < 4.2 V	380	480	670	mA
OSCILLATOR							
f_{SW}	Switching frequency			0.65	1.00	1.50	MHz
OUTPUT							
V_{REF}	Reference voltage	bq25015			0.5		V
V_{FB}	Feedback voltage(2)	bq25015	3.6 V ≤ V_{BAT}≤ 4.2 V, 0 mA ≤ I_{OUT}≤ 150 mA	–3%		+3%	
V_{DC-DC}	Adjustable output voltage range	bq25015		0.7		V_{BAT}	
	Fixed output voltage	bq25017	3.6 V ≤ V_{BAT}≤ 4.2 V, 0 mA ≤ I_{OUT}≤ 150 mA	1.746	1.8	1.854	

(2) For output voltages ≤ 1.2 V a 22-µF output capacitor value is required to achieve a maximum output voltage accuracy of +3% while operating in power save mode (PFM).

TYPICAL OPERATING CHARACTERISTICS

EFFICIENCY vs LOAD CURRENT

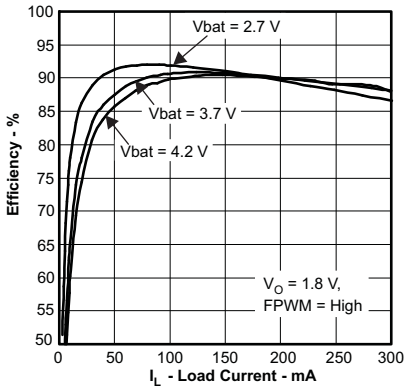


Figure 1.

EFFICIENCY vs LOAD CURRENT

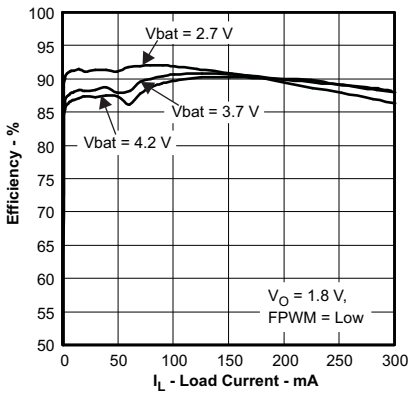


Figure 2.

EFFICIENCY vs LOAD CURRENT

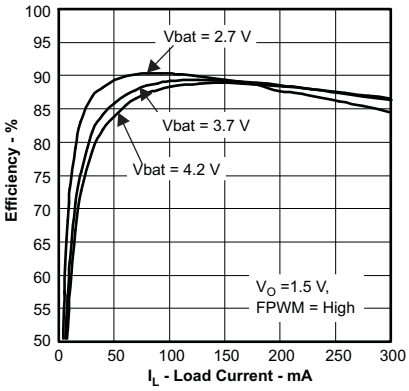


Figure 3.

EFFICIENCY vs LOAD CURRENT

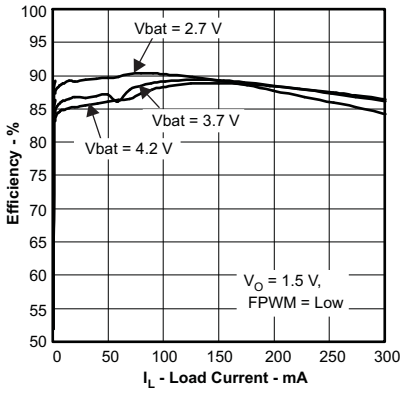


Figure 4.

SHORT CIRCUIT INDUCTOR CURRENT

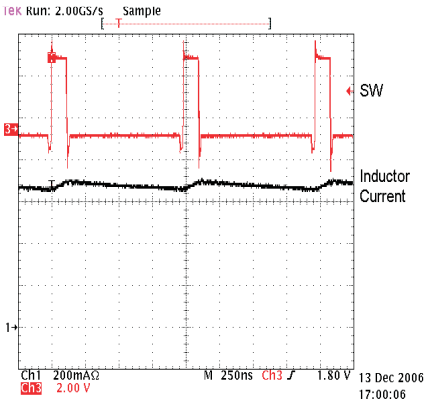


Figure 5.

TYPICAL OPERATING CHARACTERISTICS (continued)

**LOAD TRANSIENT, 3 mA TO 300 mA,
Vbat = 3.7 V, Vo = 1.8 V
FPWM = HIGH, FORCE PWM**

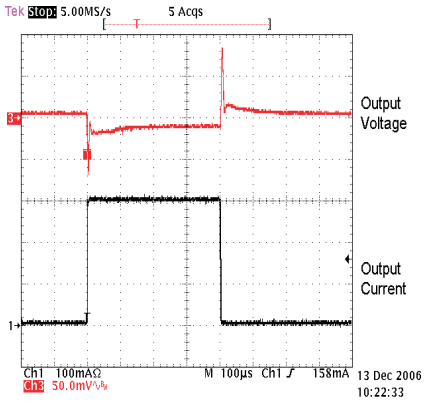


Figure 6.

**LOAD TRANSIENT, 3 mA TO 300 mA,
Vbat = 3.7 V, Vo = 1.8 V
FPWM = LOW, POWER SAVE MODE**

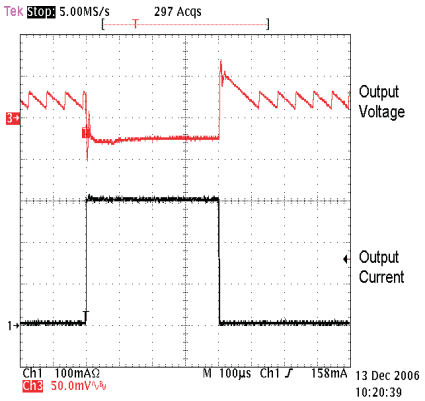


Figure 7.

**LIGHT LOAD WAVEFORM, Vbat = 3.7 V, Vo = 1.8 V
LOAD CURRENT = 36 mA,
FPWM = HIGH, FORCE PWM**

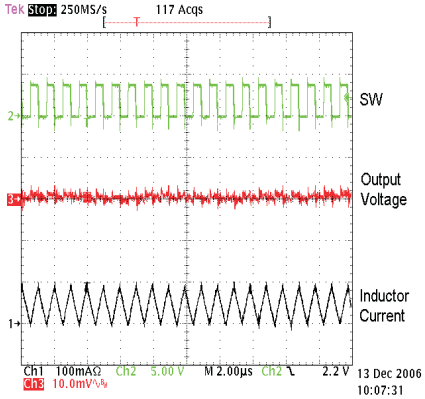


Figure 8.

**LIGHT LOAD WAVEFORM, Vbat = 3.7 V, Vo = 1.8 V
LOAD CURRENT = 36 mA,
FPWM = LOW, FORCE PWM**

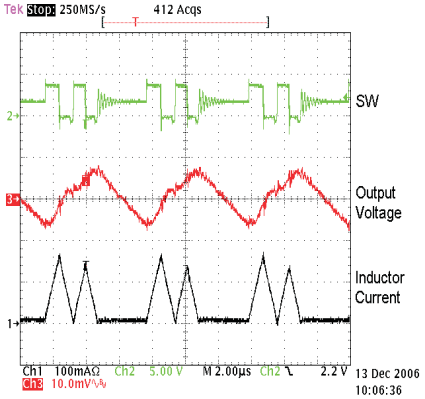


Figure 9.

**START-UP AND SHUT-DOWN, Vbat = 3.7 V, Vo = 1.8 V
LOAD CURRENT = 300 mA,
FPWM = HIGH, FORCE PWM**

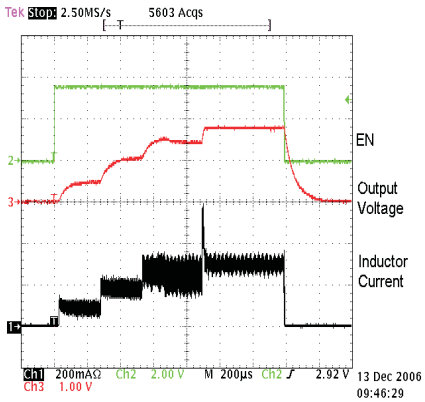


Figure 10.

**START-UP AND SHUT-DOWN, Vbat = 3.7 V, Vo = 1.8 V
LOAD CURRENT = 300 mA,
FPWM = LOW, POWER SAVE MODE**

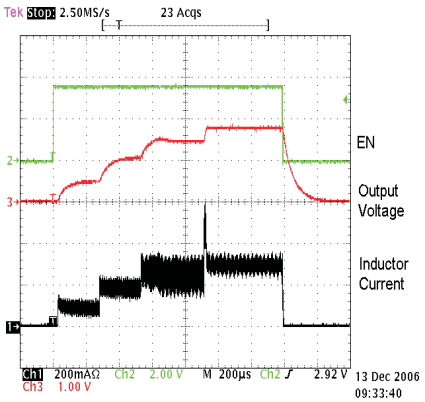
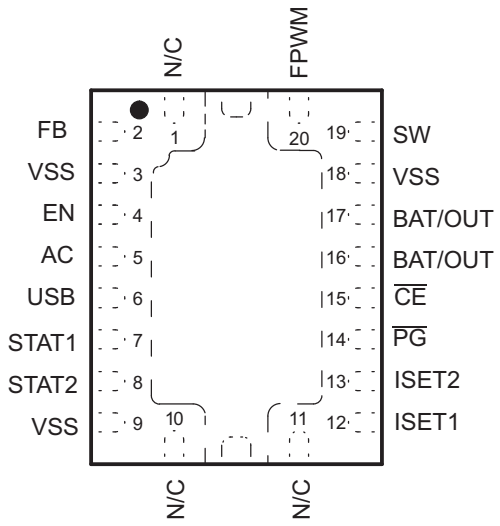


Figure 11.

DEVICE INFORMATION

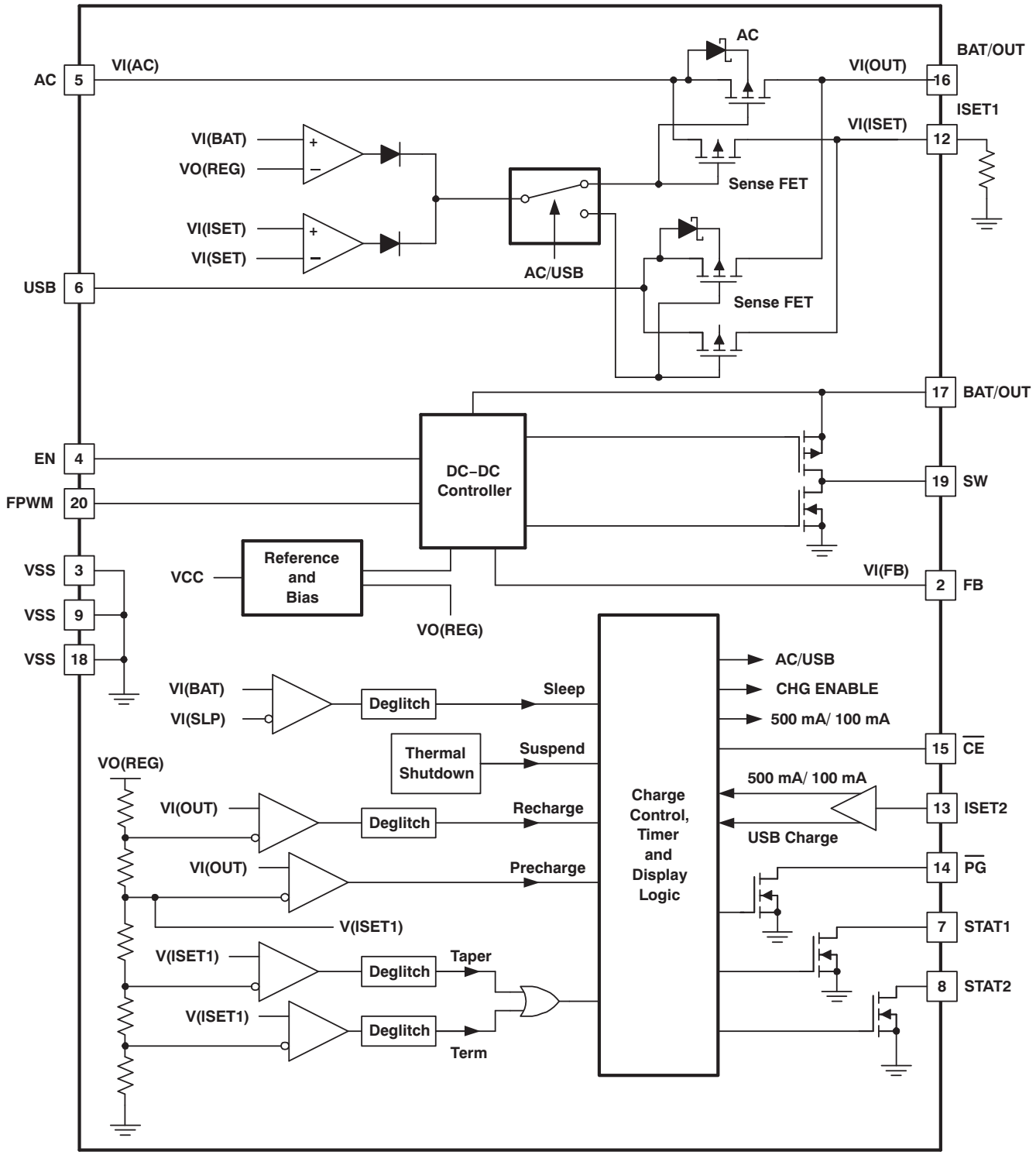
bq25015, bq25017
RHL PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AC	5	I	Charge input voltage from AC adapter, connect 10 µF capacitor to ground
BAT/OUT	16	I/O	Charge current output
BAT/OUT	17	I	Battery input to DC-DC converter
$\overline{CE}$	15	I	Charge enable input (active low)
EN	4	I	Enable input for DC-DC converter; EN=HIGH for device enable
FB	2	I	Feedback pin for DC-DC converter; connect to voltage divider for bq25015, or connect to system OUT voltage for bq25017
FPWM	20	I	PWM control input for the DC-DC converter. A high on FPWM = forced PWM mode. A low = power save mode.
ISET1	12	I	Charge current set point for AC input and precharge and taper set point for both AC and USB
ISET2	13	I	Charge current set point for USB port (High = 500 mA, Low = 100 mA, High-Z = disable USB charge)
NC	1, 10, 11	–	No connect. These pins must be left floating.
$\overline{PG}$	14	O	Power good status output (active low, open-drain)
STAT1	7	O	Charge status output 1 (open-drain)
STAT2	8	O	Charge status output 2 (open-drain)
SW	19	O	Phase node of the DC/DC converter; connect series inductor and capacitor to ground
USB	6	I	Charge input voltage from USB adapter; connect to 10 µF capacitor to ground
VSS	3, 9, 18	–	Ground Input. Also note that there is an internal electrical connection between the exposed thermal pad and VSS pins of the device. The exposed thermal pad must be connected to the same potential as the Vss pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. All VSS pins must be connected to ground at all times.

FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTIONS

BATTERY CHARGER

The bq2501x supports a precision Li-Ion or Li-Pol charging system suitable for single-cell battery packs and a low-power DC-DC converter for providing power to system processor. See a typical charge profile, application circuit and an operational flow chart in Figure 12 through Figure 14 respectively. Figure 13 is the typical application circuit for a high-current application (300 mA). Here the battery charge current is 500 mA, input voltage range of 4.5V – 6.5V.

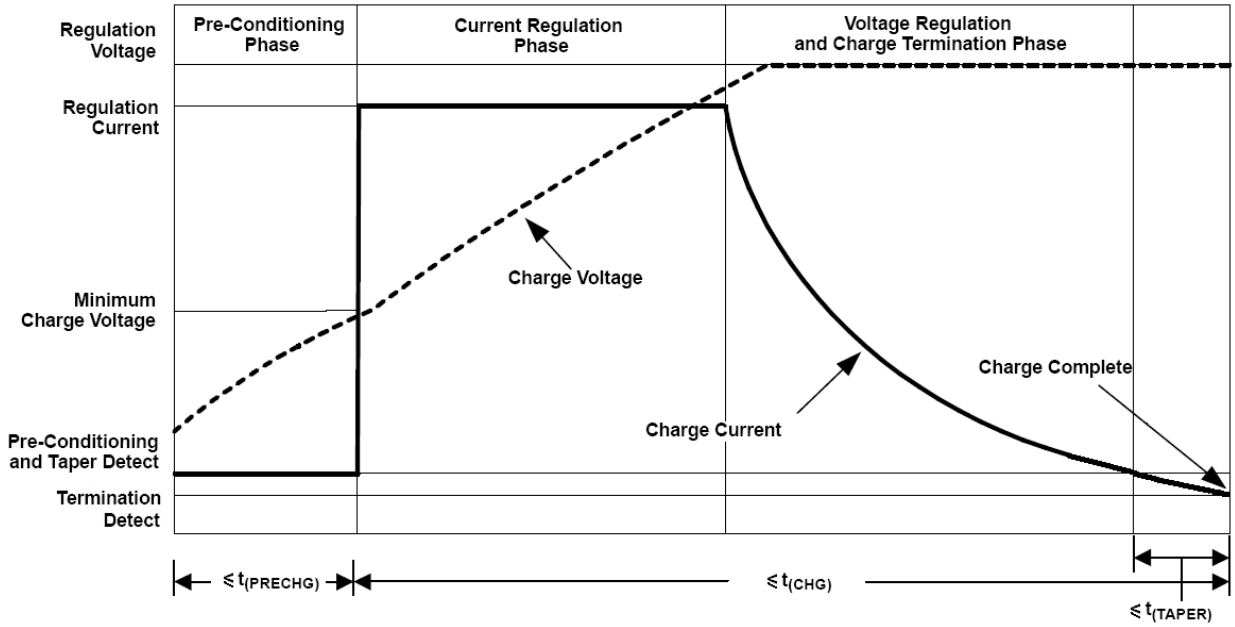

Figure 12. Typical Charger Profile

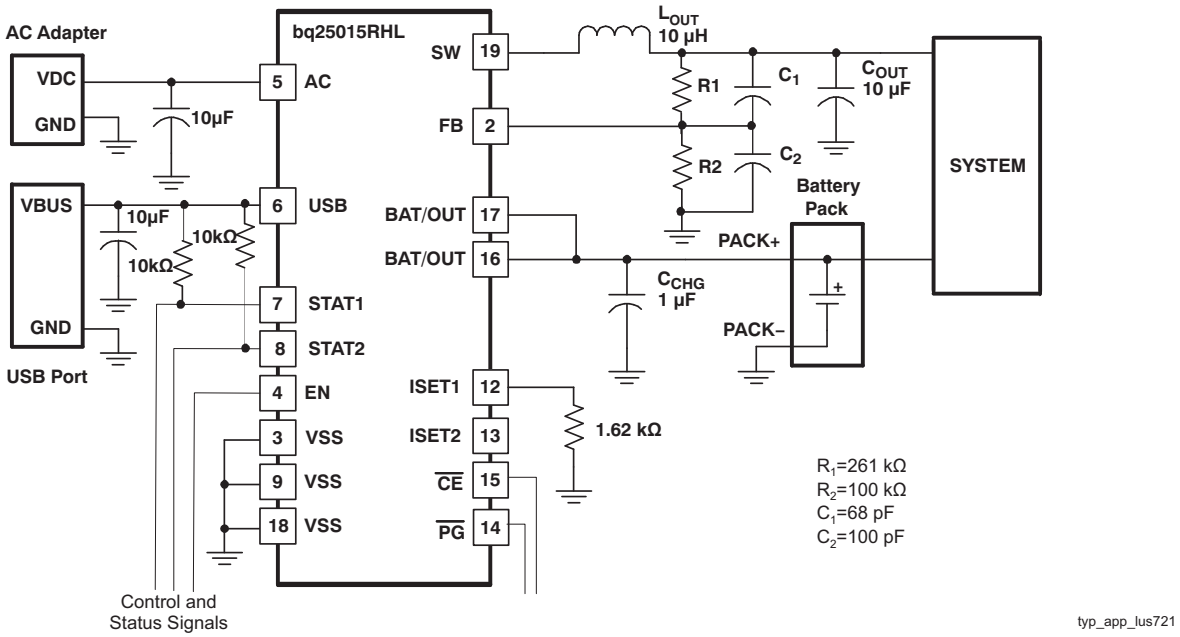

Figure 13. Typical Application Circuit

FUNCTIONAL DESCRIPTIONS (continued)

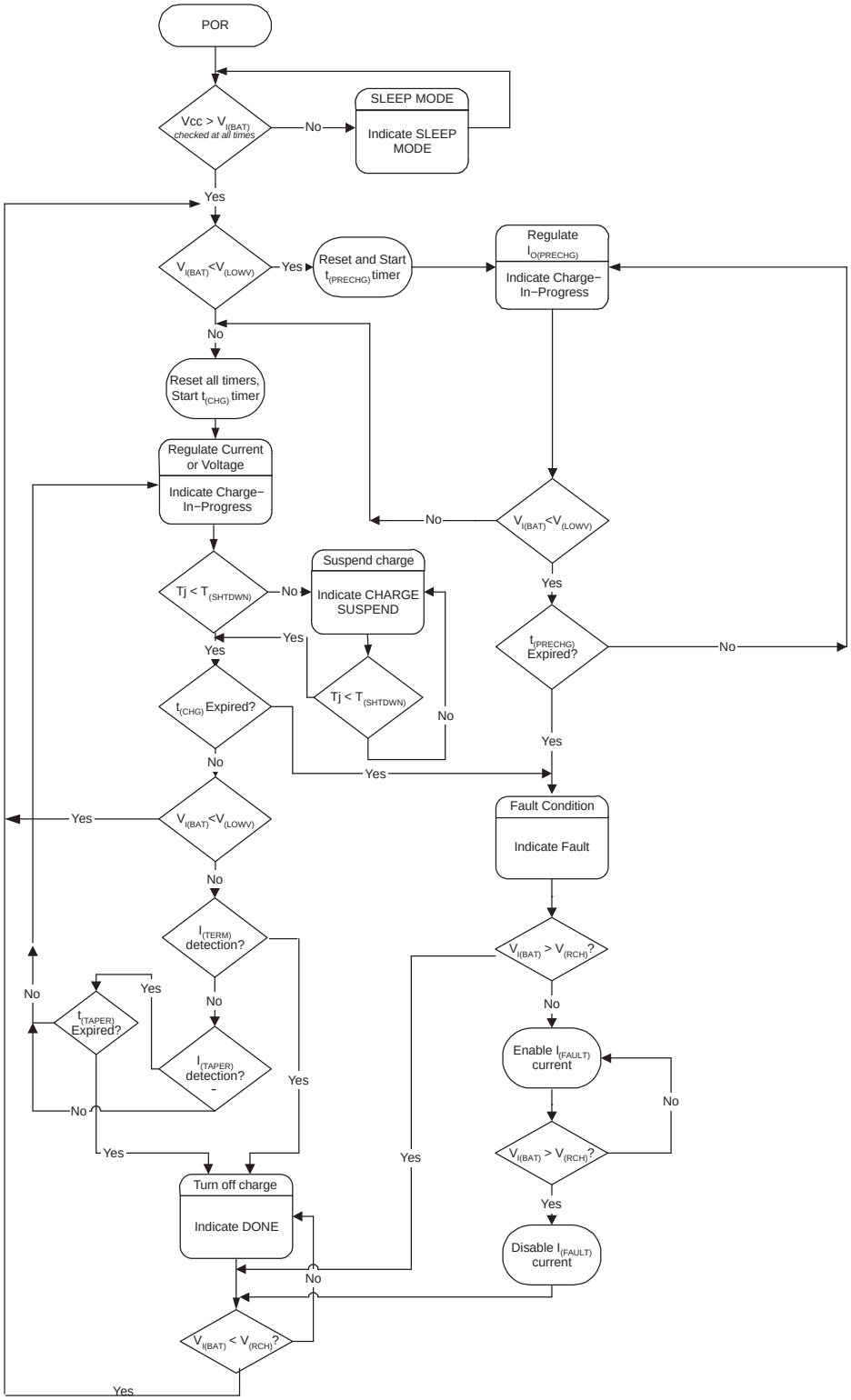

Figure 14. Operational Flow Chart

FUNCTIONAL DESCRIPTIONS (continued)

Autononous Power Source Selection

As default, the bq25015/7 attempts to charge the battery from the AC input. If AC input is not present, the USB input is selected. If both inputs are available, the AC adapter has the priority. Refer to Figure 15 for details.

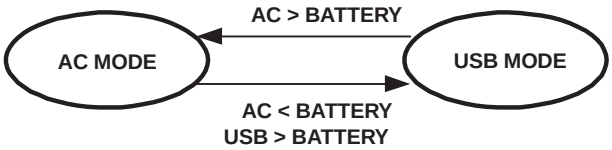

Figure 15. Power Source Selection

Battery Pre-Conditioning

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold, the bq25015/7 applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET1 and VSS pins, R_{SET}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}} \tag{1}$$

The bq25015/7 activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bq25015/7 turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. Please refer to *Timer Fault Recovery* section for additional details.

Battery Charge Current

The bq25015/7 offers on-chip current regulation with programmable set point. The resistor connected between the ISET1 and VSS pins, R_{SET}, determines the charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \tag{2}$$

When charging from a USB port, the host controller has the option of selecting either 100 mA or 500 mA charge rate using the ISET2 pin. A low-level signal sets the current at 100 mA and a high-level signal sets the current at 500 mA. A high-Z input disables USB charging.

Battery Voltage Regulation

The voltage regulation feedback is through the BAT/OUT pin. This input is tied directly to the positive side of the battery pack. The bq25015/7 monitors the battery-pack voltage between the BAT/OUT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the bq25015/7 also monitors the charge time in the charge mode. If taper threshold is not detected within this time period, $t_{(CHG)}$, the bq25015/7 turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. Please refer to section titled *Timer Fault Recovery*section for additional details.

Charge Taper Detection, Termination and Regharge

The bq25015/7 monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bq25015/7 initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The resistor connected between the ISET1 and VSS pins, R_{SET}, determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TAPER)} = \frac{V_{(TAPER)} \times K_{(SET)}}{R_{SET}} \tag{3}$$

FUNCTIONAL DESCRIPTIONS (continued)

The bq25015/7 resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$.

In addition to the taper current detection, the bq25015/7 terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition or insertion of a fully charged battery. Note that taper timer is not activated. The resistor connected between the ISET1 and VSS pins, R_{SET}, determines the taper detection level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (4)$$

After charge termination, the bq25015/7 restarts the charge once the voltage on the BAT/OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

Sleep Mode for Charger

The bq25015/7 enters the low-power sleep mode if both AC and USB are removed from the circuit. This feature prevents draining the battery during the absence of V_{CC}.

Operation Modes

Operational modes of the bq25015/7 are summarized in Table 1. Operation of DC-DC is not recommended while charger is in precharge mode.

Table 1. Operation Modes

BATTERY VOLTAGE	AC or USB ADAPTER STATUS	CHARGER STATUS	DC-DC STATUS
$V_{I(BAT)} > V_{(LOWV)}$	Present	Fast	EN
$0\ V < V_{I(BAT)} < V_{(LOWV)}$	Present	Precharge	EN
$V_{I(BAT)} < V_{(UVLO)}$	Both absent	Off	Off

Status Outputs

The STAT1 and STAT2 open-drain outputs indicate various charger and battery conditions as shown in Table 2. These status pins can be used to communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

Table 2. Status Pins Summary

CHARGE STATE	INPUT POWER STATE	STAT1	STAT2
Precharge in progress	Present	ON	ON
Fast charge in progress	Present	ON	OFF
Charge done	Not reported	OFF	ON
Timer fault	Not reported	OFF	OFF
Speel mode	Absent	OFF	OFF

$\overline{PG}$ Output (Power Good)

The open-drain $\overline{PG}$ output indicates when the AC adapter is present. The output turns ON when a valid voltage is detected. This output is turned off in the sleep mode. The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor.

$\overline{CE}$ Input (Charge Enable)

The $\overline{CE}$ digital input is used to enable or disable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge and places the device into a low-power mode. A high-to-low transition on this pin also resets all timers and timer fault conditions. Note that this applies to both AC and USB charging.

Thermal Shutdown and Protection

The bq25015/7 monitors the junction temperature, T_J, of the die and suspends charging if T_J exceeds $T_{(SHTDWN)}$. Charging resumes when T_J falls below $T_{(SHTDWN)}$ by approximately 15°C.

TImer Fault Recovery

As shown in Figure 14, bq25015/7 provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery method: bq25015/7 waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bq25015/7 clears the fault and starts a new charge cycle. A POR or $\overline{CE}$ toggle also clears the fault.

Condition 2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery method: Under this scenario, the bq25015/7 applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bq25015/7 disables the $I_{(FAULT)}$ current and executes the recovery method described for Condition 1. Once the battery falls below the recharge threshold, the bq25015/7 clears the fault and starts a new charge cycle. A POR or $\overline{CE}$ toggle also clears the fault.

DC-DC CONVERTER

The bq25015/7 provides a low quiescent-current synchronous DC-DC converter. The internally compensated converter is designed to operate over the entire voltage range of a single-cell Li-Ion or Li-Pol battery. Under nominal load current, the device operates with a fixed PWM switching frequency of typically 1 MHz. At light load currents, the device enters the power save mode of operation; the switching frequency is reduced and the quiescent current drawn by the converter from the BAT/OUT pin is typically only 15 µA.

During PWM operation the converter uses a unique fast-response voltage mode controller scheme with input voltage feedforward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channnel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through the N-channnel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the on the P-channel switch. The g_M amplifier as well as the input voltage determines the rise time of the saw-tooth generator and therefore any change in input voltage or output voltage directly controls the duty cycle of the converter giving a very good line and load transient regulation.

Power Save Mode Operation

As the load current decreases the converter enters the power save mode operation. During power save mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

Two conditions allow the converter to enter the power save mode operation. One is the detection of discontinuous conduction mode. The other is when the peak switch current in the P-channel switch goes below the skip current limit. The typical skip current limit can be calculated as:

$$I_{SKIP} = 66\ \text{mA} + \frac{V_{IN}}{160\ \Omega} \tag{5}$$

During the power save mode the output voltage is monitored with the comparator by the thresholds comp low and comp high. As the output voltage falls below the comp low threshold (set to typically 0.8% above VOUT nominal) the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The typical peak switch current can be calculated as:

$$I_{PEAK} = 66\ \text{mA} + \frac{V_{IN}}{80\ \Omega} \tag{6}$$

The N-channel rectifier is turned on and the inductor current ramps down. As the inductor current approaches zero the N-channel rectifier is turned off and the P-channel switch is turned on again starting the next pulse. The converter continues these pulses until the comp high threshold (set to typically 1.6% above VOUT nominal) is reached. The converter enters a sleep mode, reducing the quiescent current to a minimum. The converter wakes up again as the output voltage falls below the comp low threshold again. This control method reduces the quiescent current to typically to 15 µA and the switching frequency to a minimum, thereby achieving high converter efficiency. Setting the skip current thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic output voltage achieving lower absolute voltage drops during heavy load transient changes. This allows the converter to operate with a small output capacitor of only 10 µF and still have a low absolute voltage drop during heavy load transient changes. Refer to Figure 16 as well for detailed operation of the power save mode.

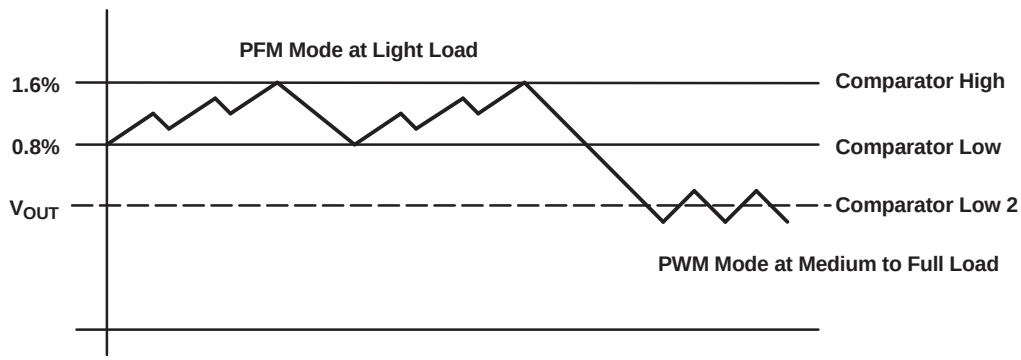

Figure 16. Power Save Mode Thresholds and Dynamic Voltage Positioning

The converter enters the fixed-frequency PWM mode again as soon as the output voltage drops below the comp low 2 threshold.

Dynamic Voltage Positioning

As described in the power save mode operation section and as detailed in Figure 16, the output voltage is typically 0.8% above the nominal output voltage at light load currents as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load the voltage overshoot is also minimized due to active regulation turning on the N-Channel rectifier switch.

Soft-Start

The bq25015/7 has an internal soft-start circuit that limits the inrush current during startup. This soft-start is implemented as a digital circuit increasing the switch current in steps of typically 60 mA, 120 mA, 240 mA and then the typical switch current limit of 480 mA. Therefore the starup time depends mainly on the output capacitor and load current. Typical startup time with a 10-µF output capacitor and a 100-mA load current is 1.6 ms.

100% Duty Cycle Low Dropout Operation

The bq2501 offers a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as:

$$V_{IN(min)} = V_{OUT(max)} + I_{OUT(max)} \times \left(R_{DS(on)MAX} + R_L\right) \quad (7)$$

where

$I_{OUT(max)}$ = maximum output current plus indicator ripple current
$R_{DS(on)MAX}$ = maximum P-channel switch $R_{DS(on)}$
R_L = DC resistance of the inductor
$V_{OUT(max)}$ = nominal output voltage plus maximum output voltage tolerance

Enable

Pulling the enable pin (EN) low forces the DC-DC converter into shutdown mode, with a shutdown quiescent current of typically 0.1 µA. In this mode the P-channel switch and N-channel rectifier are turned off, the internal resistor feedback divider is disconnected, and the converter enters shutdown mode. If an output voltage, which could be an external voltage source or a super capacitor, is present during shut down, the reverse leakage current is specified under electrical characteristics. For proper operation the EN pin must be terminated and should not be left floating.

Pulling the EN pin high starts up the DC-DC converter with the soft-start as previously described.

Undervoltage Lockout

The undervoltage lockout circuit prevents the converter from turning on the switch or rectifier MOSFET at low input voltages or under undefined conditions.

Forced PWM Mode

The FPWM input pin allows the host system to override the power save mode by driving the FPWM pin high. In this state, the DC-DC converter remains in the PWM mode of operation with continuous current conduction regardless of the load conditions. Tying the FPWM pin low allows the device to enter power save mode automatically as previously described.

APPLICATION INFORMATION

ADJUSTABLE OUTPUT VOLTAGE VERSION (bq25015)

When the adjustable output voltage version is being used (bq25015), the output is set by the external resistor divider, as shown in Figure 13.

The output voltage can be calculated as:

$$V_{OUT} = 0.5\ V \times \left(1 + \frac{R1}{R2}\right) \tag{8}$$

where

R1 + R2 ≤ 1 MΩ

Internal reference voltage $V_{REF(typ)}$ = 0.5 V

C1 and C2 should be selected as:

$$C1 = \frac{1}{2\pi \times 10\ kHz \times R1} \tag{9}$$

where

R1 = upper resistor of the voltage divider

C1 = upper capacitor of the voltage divider

For C1, a value should be chosen that comes closest to the calculated result.

$$C2 = \frac{R1}{R2} \times C1 \tag{10}$$

where

R2 = lower resistor of the voltage divider

C2 = lower capacitor of the voltage divider

For C2, the selected capacitor value should always be selected larger than the calculated result. For example, in Figure 13, a 100-pF capacitor is selected for a calculated result of C2 = 86.17 pF.

If quiescent current is not a key design parameter, C1 and C2 can be omitted and a low-impedance feedback divider must be used with R1 + R2 < 100 kΩ. This design reduces the noise available on the feedback pin (FB) as well, but increases the overall quiescent current during operation.

FIXED OUTPUT VOLTAGE VERSION (bq25017)

When a fixed output voltage version of the device is being used, no external resistive divider network is necessary. In this case, the output of the inductor should be connected directly the FB pin, as shown in Figure 13.

INPUT CAPACITOR SELECTION

In most applications, all that is needed is a high-frequency decoupling capacitor. A 0.1-µF ceramic, placed in close proximity to AC/USB and VSS pins, works fine. The bq2501x is designed to work with both regulated and unregulated external DC supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance has to be added to the input of the charger.

CHARGER OUTPUT CAPACITOR (DC-DC CONVERTER INPUT CAPACITOR) SELECTION

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizes the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients.

For good input voltage filtering, usually a 4.7-µF input capacitor is sufficient and can be increased without any limit for better input voltage filtering.

APPLICATION INFORMATION (continued)

If ceramic output capacitors are used, the capacitor RMS ripple current rating ensures the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{RMS} = I_{OUT(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{11}$$

The worst case RMS ripple current occurs at D=0.5 and is calculated as:

$$I_{RMS} = \frac{I_{OUT}}{2} \tag{12}$$

Ceramic capacitors perform well because of the low ESR value, and they are less sensitive to voltage transients and spikes compared to tantalum capacitors. The input capacitor should be placed as close as possible to the BAT/OUT pin of the device for best performance. Refer to Table 1for recommended components.

DC-DC CONVERTER OUTPUT CAPACITOR SELECTION

The advanced fast response voltage mode control scheme of the bq25015/7 allows the use of tiny ceramic capacitors without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are therefore recommended. If required, tantalum capacitors may be used as well (refer to Table 1 for recommended components). If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{RMS(Cout)} = V_{OUT} \times \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{13}$$

At nominal load current the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR\right) \tag{14}$$

where the output voltage ripple occurs at the highest input voltage V_{IN}.

At light load currents the device operates in power save mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the output voltage V_{OUT}.

APPLICATION INFORMATION (continued)

DC-DC CONVERTER OUTPUT INDUCTOR SELECTION

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Although the inductor core material has less effect on efficiency than its DC resistance, an appropriate inductor core material must be used. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current, and the lower the conduction losses of the converter. On the other hand, larger inductor values causes a slower load transient response. Usually the inductor ripple current, as calculated below, should be around 30% of the average output current.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current that is calculated as:

$$\Delta I_L = V_{OUT} \times \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f} \tag{15}$$

where

f = switching frequency (1 MHz typical, 650 kHz minimal)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(max)}$ = maximum inductor current

The highest inductor current occurs at maximum V_{IN}. A more conservative approach is to select the inductor current rating just for the maximum switch current of 350 mA. The internal compensator is designed in such a way that the optimized resonant frequency of the output inductor and capacitor is approximately 16kHz. The recommended inductor and capacitor values for various output current are given in Table 3.

Table 3. Recommended Inductor and Capacitor Values

TYPICAL OUTPUT CURRENT (mA)	INDUCTOR VALUE (µH)	CAPACITOR VALUE (µF)	APPLICATION
30	100	1	For low current, smallest capacitor
60	47	2.2	For low current, small capacitor
80	33	3.3	For medium current, small capacitor
150	22	4.7	For medium current
300	10	10	For highest current, smallest inductor

CHARGING WHILE UNDER LOAD

The bq25015/7 are designed such that maximum charging safety and efficiency can be obtained by suspending normal operation while the device is actively charging the battery. In this mode of operation, the timeout function prevents a defective battery from being charged indefinitely. If charging does not terminate normally within five hours, the device annunciates a fault condition on the STAT1 and STAT2 pins as indicated in Table 2.

If a load is applied to the device while it is being used to charge a battery, a false fault condition may result due to a slower rate of charge being applied to the battery. For this reason it is recommended that the load be disconnected from the bq25015/7 while it is charging a battery.

THERMAL CONSIDERATIONS

The bq25015/7 devices are packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note *QFN/SON PCB Attachment* (SLUA271). The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{16}$$

where

T_J = chip junction temperature

T_A = ambient temperature

P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation (P) is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from the following equation:

$$P = \left(V_{IN} - V_{IN(BAT)}\right) \times I_{OUT(OUT)} \tag{17}$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest.

PCB LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done the regulator could exhibit stability problems as well as EMI problems. With this in mind, one should lay out the PCB using wide, short traces for the main current paths. The input capacitor, as well as the inductor and output capacitors, should be placed as close as possible to the IC pins.

The feedback resistor network must be routed away from the inductor and switch node to minimize noise and magnetic interference. To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces must be used for shielding. This becomes very important especially at high switching frequencies.

The following are some additional guidelines that should be observed:

- To obtain optimal performance, the decoupling capacitor from AC to VSS (and from USB to VSS) and the output filter capacitors from BAT/OUT to VSS should be placed as close as possible to the bq25015/7, with short trace runs to both signal and VSS pins.
- All low-current VSS connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The BAT/OUT pin provides voltage feedback to the IC for the charging function and should be connected with its trace as close to the battery pack as possible.
- The high current charge paths into AC and USB and from the BAT/OUT and SW pins must be sized appropriately for the maximum charge or output current in order to avoid voltage drops in these traces.
- The bq25015/7 deviecs are packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note *QFN/SON PCB Attachment* (SLUA271).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25015RHLR	ACTIVE	VQFN	RHL	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BZL	Samples
BQ25015RHLT	ACTIVE	VQFN	RHL	20	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BZL	Samples
BQ25015RHLTG4	ACTIVE	VQFN	RHL	20	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BZL	Samples
BQ25017RHLR	ACTIVE	VQFN	RHL	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BZM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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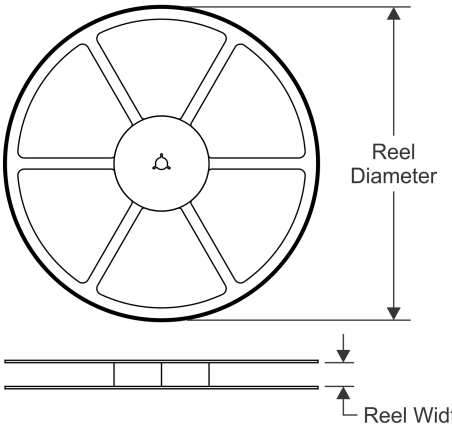
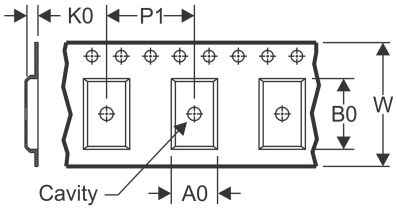
TAPE AND REEL INFORMATION

REEL DIMENSIONS

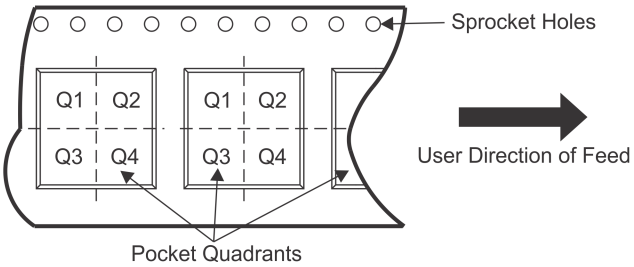


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

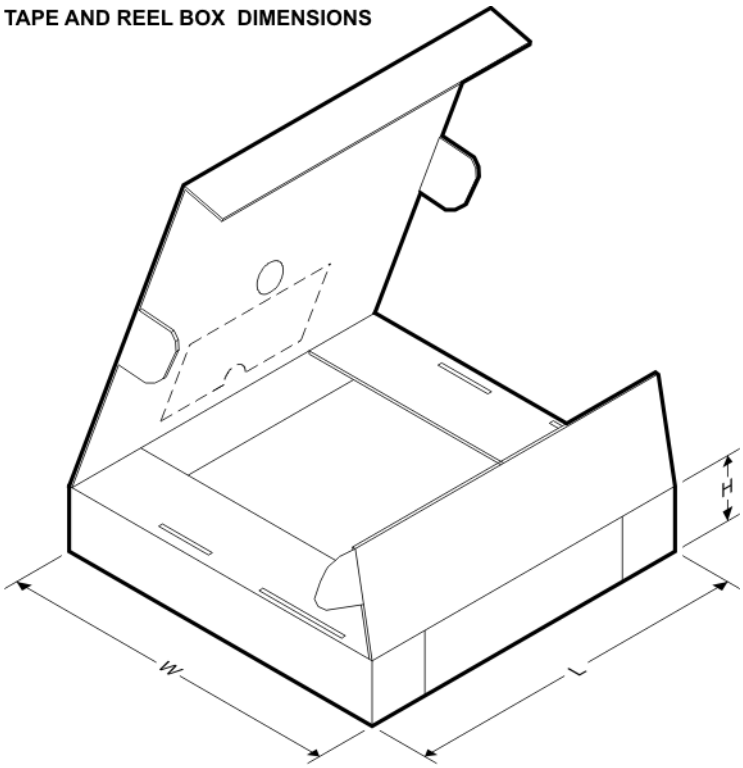
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25015RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ25015RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ25017RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

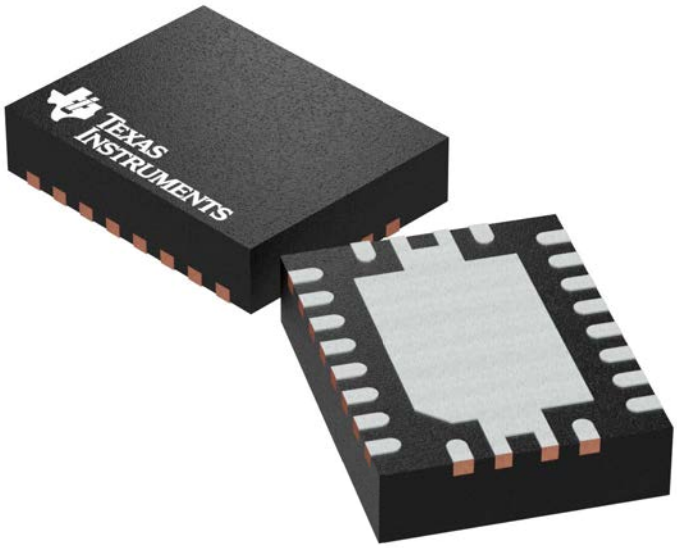
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25015RHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ25015RHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ25017RHLR	VQFN	RHL	20	3000	367.0	367.0	35.0

RHL 20

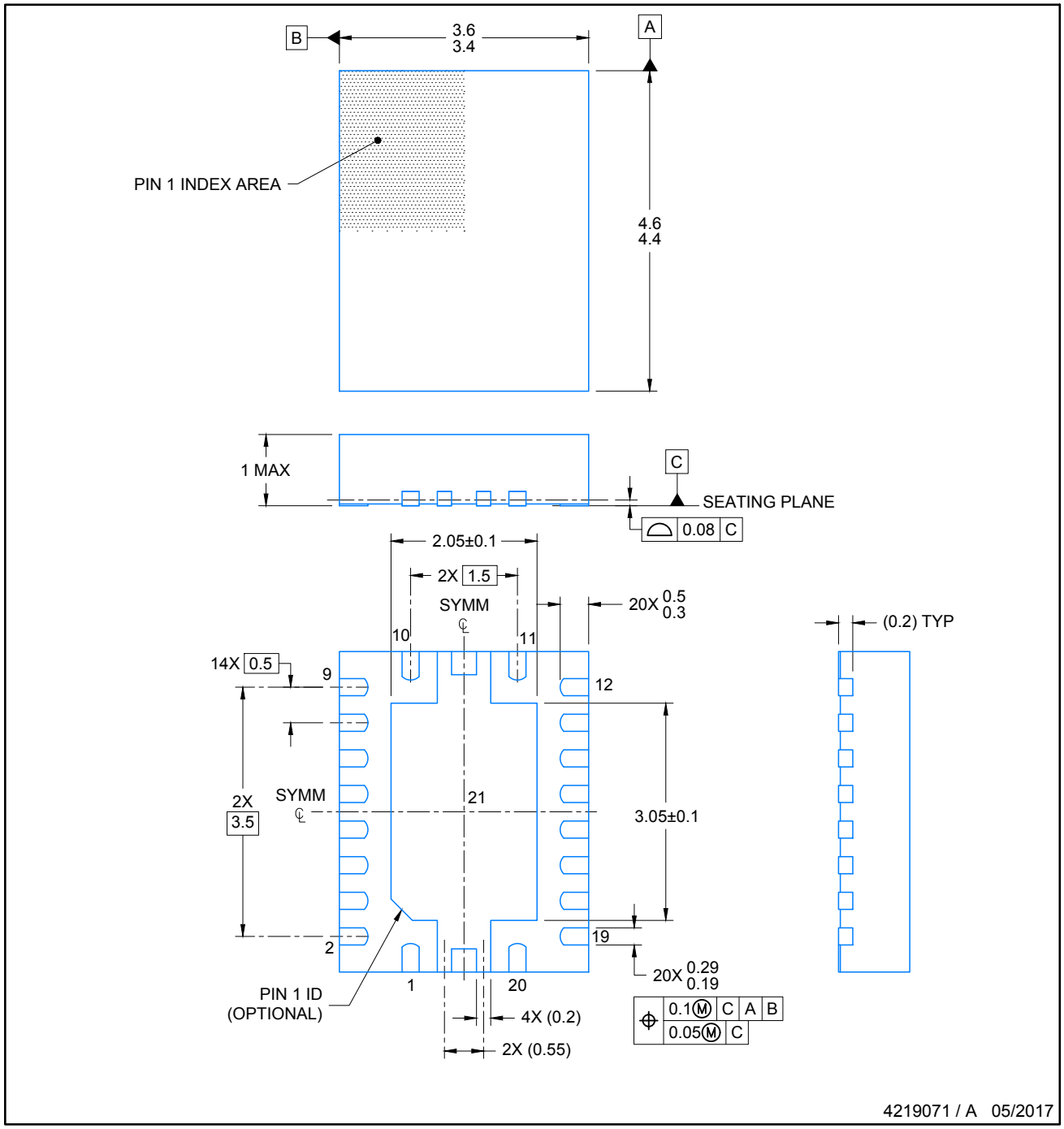
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

3.5 x 4.5 mm, 0.5 mm pitch

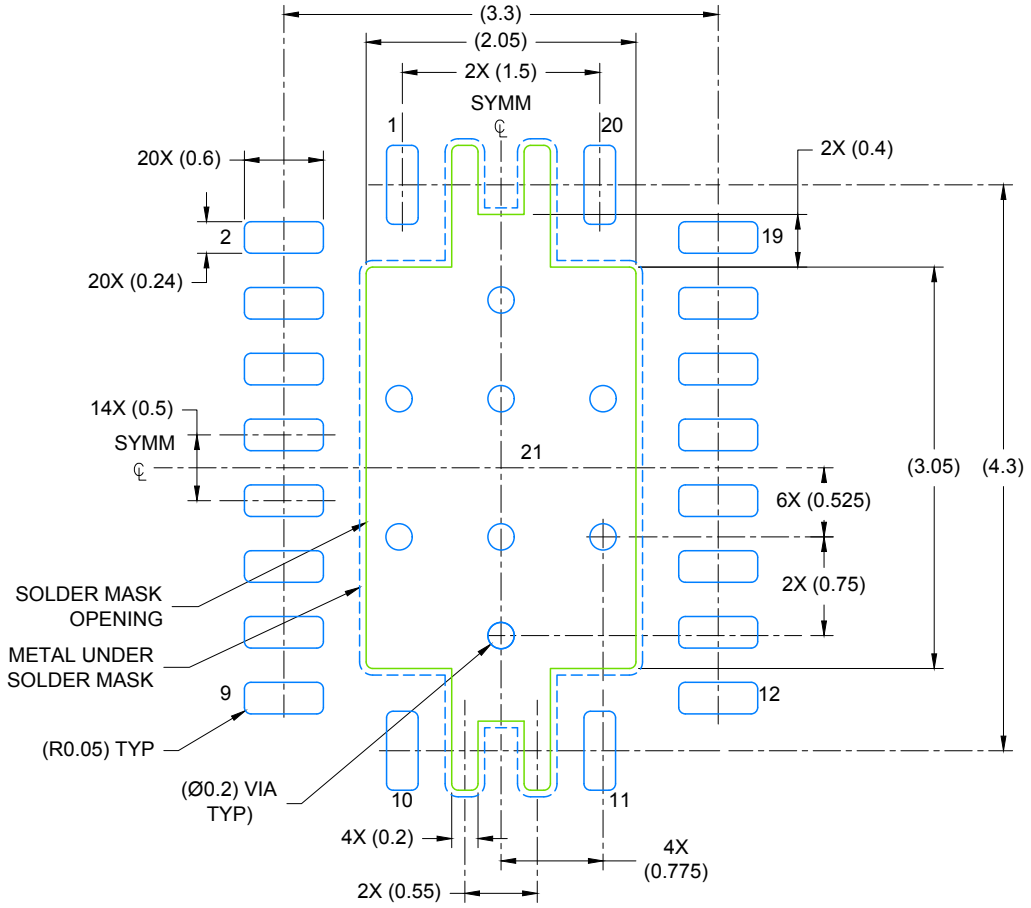


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

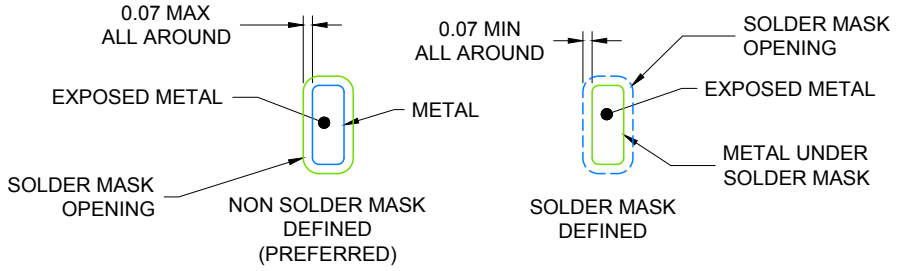


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

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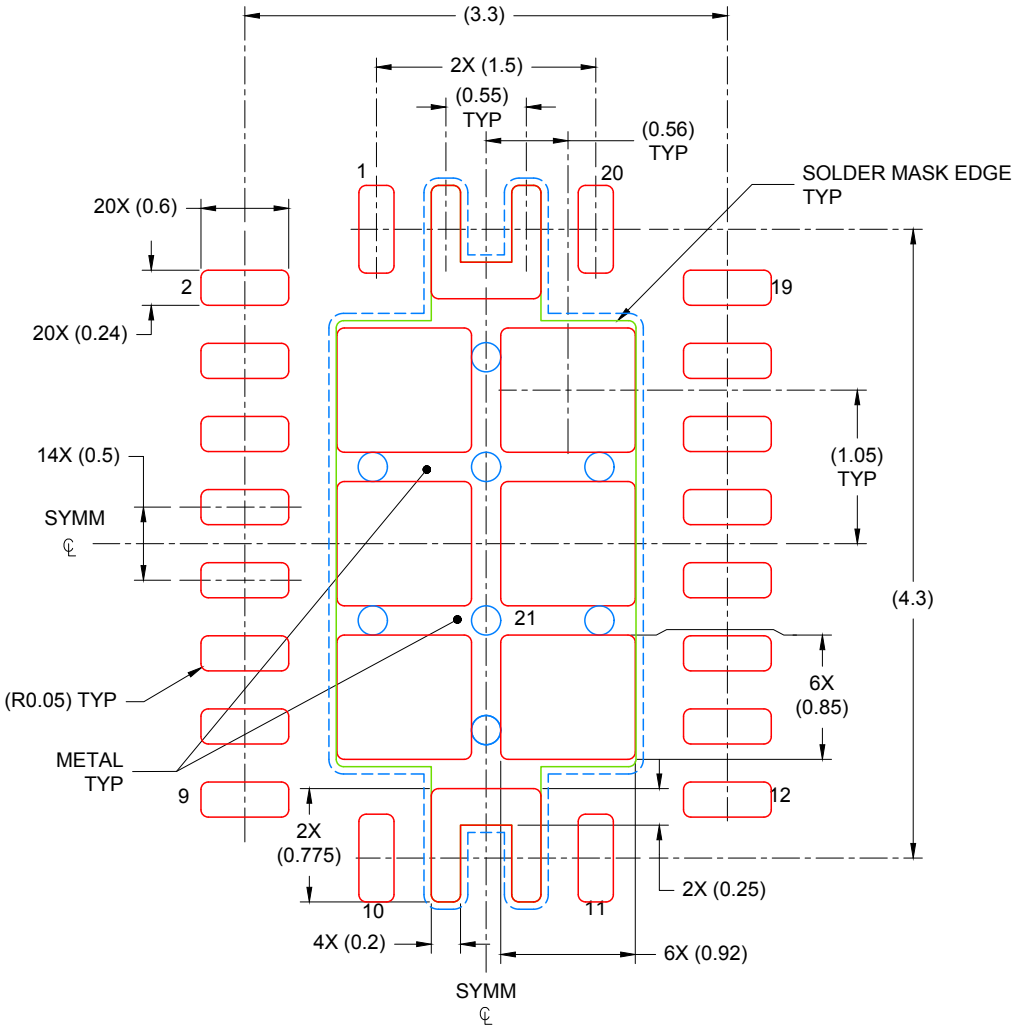
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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