LMH0384 3-Gbps HD - SD SDI Extended Reach and Configurable Adaptive Cable Equalizer

1 Features

- Compliant With ST 424, ST 292, ST 344, and ST 259
- Supports DVB-ASI at 270 Mbps
- Wide Range of Data Rates: 125 Mbps to 2.97 Gbps
- Equalizes up to 140 Meters of Belden 1694A at 2.97 Gbps, up to 200 Meters of Belden 1694A at 1.485 Gbps, or Up to 400 Meters of Belden 1694A at 270 Mbps
- Power Save Mode With Auto Sleep Control (35 mW Typical Power Consumption in Power Save Mode)
- Optional SPI Register Access
- Manual Bypass and Output Mute With a Programmable Threshold
- Internally Terminated 100-Ω LVDS Outputs With SPI Programmable Output Common-Mode Voltage and Swing
- Programmable Launch Amplitude Optimization in SPI Mode
- Cable Length Indicator in SPI Mode
- Single 3.3-V Supply Operation
- 16-Pin WQFN Package
- Industrial Temperature Range: −40°C to +85°C
- Footprint Compatible With the LMH0344, LMH0044, and LMH0074 in Pin Mode

2 Applications

- ST 424, ST 292, ST 344, and ST 259 Serial Digital Interfaces
- Serial Digital Data Equalization and Reception
- Data Recovery Equalization (1)

(1) Due to SMPTE naming convention, all SMPTE Engineering Documents will be numbered as a 2-letter prefix and a number. Documents and references with the same root number and year are functionally identical; for example ST 424-2006 and SMPTE 424M-2006 refer to the same document.

3 Description

The LMH0384 3-Gbps HD - SD SDI Extended Reach and Configurable Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports ST 424, ST 292, ST 344, and ST 259 standards.

The LMH0384 device includes active sensing features and design enhancements including longer cable equalization, lower output jitter, configurable pin mode and SPI modes, a power-saving sleep mode, and programmable output common-mode voltage and swing. The LMH0384 implements DC restoration to correctly handle pathological data conditions.

The LMH0384 includes an auto sleep mode to power down the device when no input signal is detected. Other features include separate carrier detect and output mute pins which may be tied together to mute the output when no input signal is present, and a programmable mute reference which may be used to mute the output at a selectable level of signal degradation.

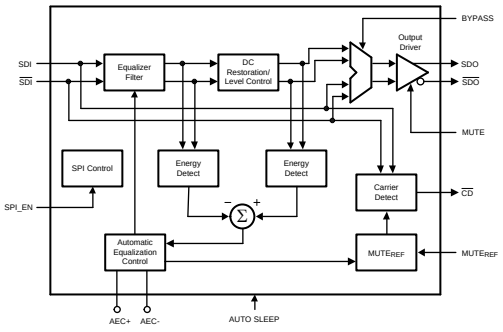
The LMH0384 supports two modes of operation. In pin mode (non-SPI mode) the LMH0384 is footprint compatible with the LMH0344 and legacy SDI equalizers. In the optional SPI mode, the LMH0384 provides register access to all of its features along with a cable length indicator, programmable output common-mode voltage and swing, and launch amplitude optimization.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH0384	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 DC Electrical Characteristics ... 5
6.6 AC Electrical Characteristics ... 6
6.7 Timing Requirements ... 7
6.8 Switching Characteristics ... 7
6.9 Typical Characteristics ... 9
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 12
7.5 Programming ... 13
7.6 Register Maps ... 16
8 Application and Implementation ... 18
8.1 Application Information ... 18
8.2 Typical Application ... 18
8.3 Dos and Don'ts ... 20
9 Power Supply Recommendations ... 21
10 Layout ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Example ... 22
11 Device and Documentation Support ... 23
11.1 Documentation Support ... 23
11.2 Community Resources ... 23
11.3 Trademarks ... 23
11.4 Electrostatic Discharge Caution ... 23
11.5 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2013) to Revision G — **Page**

- Added, updated, or renamed the following sections: Device Information Table, *Pin Configuration and Functions*; *Specifications*; *Applications and Implementation*; *Detailed Description*; *Layout*;*Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1
- Added "(logic zero)" to Pin 14 - MUTE - in *Pin Descriptions – Pin Mode (non-SPI) / SPI_EN = GND / LMH0344 Compatible* table. ... 3
- Added note "Typical pullup or pulldown for digital pin is 100 kΩ. The tolerance is between 69K to 131K" to *DC Electrical Characteristics* ... 5

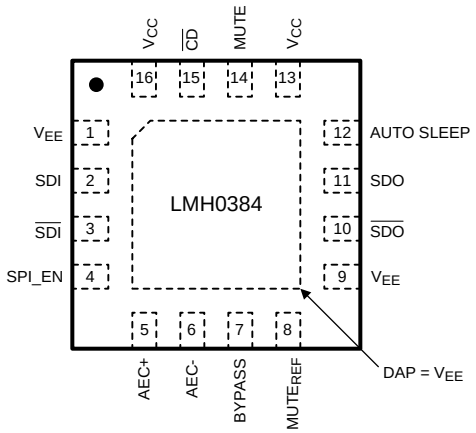
Changes from Revision E (April 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 17

Copyright © 2009–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

RUM Package
16-Pin WQFN
Top View



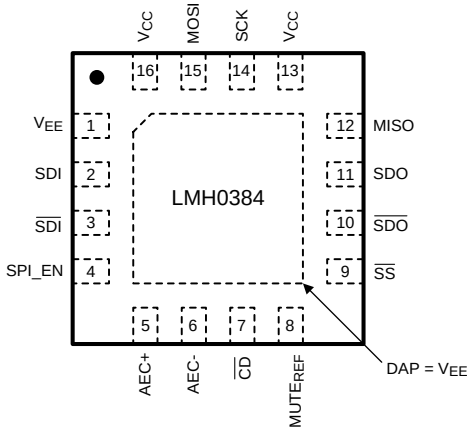
NOTE: The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

Pin Functions – Pin Mode (non-SPI) / SPI_EN = GND / LMH0344 Compatible

PIN		I/O, TYPE	DESCRIPTION
NO.	NAME		
1	V_{EE}	Ground	Negative power supply (ground).
2	SDI	I, SDI	Serial data true input.
3	$\overline{SDI}$	I, SDI	Serial data complement input.
4	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
5	AEC+	I/O, Analog	AEC loop filter external capacitor (1-µF) positive connection.
6	AEC-	I/O, Analog	AEC loop filter external capacitor (1-µF) negative connection.
7	BYPASS	I, LVCMOS	Equalization bypass. This pin has an internal pulldown. H = Equalization is bypassed (no equalization occurs). L = Normal operation.
8	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
9	V_{EE}	I, LVCMOS	Connect this pin to ground or drive it logic low.
10	$\overline{SDO}$	O, LVDS	Serial data complement output.
11	SDO	O, LVDS	Serial data true output.
12	AUTO SLEEP	I, LVCMOS	Auto Sleep. AUTO SLEEP has precedence over MUTE and BYPASS. This pin has an internal pullup. H = Device will power down when no input is detected. L = Normal operation (device will not enter auto power down).
13	V_{CC}	Power	Positive power supply (+3.3 V).
14	MUTE	I, LVCMOS	Output mute. $\overline{CD}$ may be tied to this pin to inhibit the output when no input signal is present. MUTE has precedence over BYPASS. This pin has an internal pulldown. H = Outputs forced to a muted state (logic zero). L = Outputs enabled.
15	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
16	V_{CC}	Power	Positive power supply (+3.3 V).
—	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground).

Copyright © 2009–2015, Texas Instruments Incorporated

RUM Package
16-Pin WQFN
Top View



NOTE: The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

Pin Functions – SPI Mode / SPI_EN = V_{CC}

PIN		I/O, TYPE	DESCRIPTION
NO.	NAME		
1	V_{EE}	Ground	Negative power supply (ground).
2	SDI	I, SDI	Serial data true input.
3	$\overline{SDI}$	I, SDI	Serial data complement input.
4	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
5	AEC+	I/O, Analog	AEC loop filter external capacitor (1 µF) positive connection.
6	AEC-	I/O, Analog	AEC loop filter external capacitor (1 µF) negative connection.
7	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
8	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
9	$\overline{SS}$ (SPI)	I, LVCMOS	SPI slave select. This pin has an internal pullup.
10	$\overline{SDO}$	O, LVDS	Serial data complement output.
11	SDO	O, LVDS	Serial data true output.
12	MISO (SPI)	O, LVCMOS	SPI Master Input / Slave Output. LMH0384 data transmit.
13	V_{CC}	Power	Positive power supply (+3.3 V).
14	SCK (SPI)	I, LVCMOS	SPI serial clock input.
15	MOSI (SPI)	I, LVCMOS	SPI Master Output / Slave Input. LMH0384 data receive.
16	V_{CC}	Power	Positive power supply (+3.3 V).
—	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground).

Copyright © 2009–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage		4.0	V
Input voltage (all inputs)	−0.3	V_{CC}+0.3	V
Junction temperature		125	°C
Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	
		Machine model (MM)	±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±6500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC} – V_{EE}$	Supply Voltage	3.135	3.3	3.465	V
	Input Coupling Capacitance		1		µF
	AEC Capacitor (Connected between AEC+ and AEC-)		1		µF
T_A	Operating Free Air Temperature	−40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH0384 WQFN (RUM) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input Voltage High Level (Logic Inputs)		2		V_{CC}	V
V_{IL}	Input Voltage Low Level		V_{EE}		0.8	V
V_{SDI}	Input Voltage Swing (SDI, $\overline{SDI}$)	0 m cable length(5)	720	800	950	mV_{P-P}
V_{CMIN}	Input Common-Mode Voltage (SDI, $\overline{SDI}$)			1.75		V

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3 V and T_A = +25°C.
(3) Typical pullup or pulldown for digital pin is 100 kΩ.
(4) Due to SMPTE naming convention, all SMPTE Engineering Documents will be numbered as a two-letter prefix and a number. Documents and references with the same root number and year are functionally identical; for example ST 424-2006 and SMPTE 424M-2006l refer to the same document.
(5) The LMH0384 can be optimized for different launch amplitudes through the SPI.

Copyright © 2009–2015, Texas Instruments Incorporated

DC Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SSP-P}	Differential Output Voltage, P-P (SDO, $\overline{SDO}$)	100-Ω load, default values(6), see Figure 1	500	700	900	mV_{P-P}
V_{OD}	Differential Output Voltage (SDO, $\overline{SDO}$)		250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States (SDO, $\overline{SDO}$)				50	mV
V_{OS}	Offset Voltage (SDO, $\overline{SDO}$)		1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States (SDO, $\overline{SDO}$)				50	mV
I_{OS}	Output Short Circuit Current (SDO, $\overline{SDO}$)				30	mA
$MUTE_{REF}$	$MUTE_{REF}$ DC Voltage (floating)			1.3		V
	$MUTE_{REF}$ Range			0.8		V
V_{OH}	Output Voltage High Level ($\overline{CD}$, MISO)	I_{OH} = -2 mA	2.4			V
V_{OL}	Output Voltage Low Level ($\overline{CD}$, MISO)	I_{OL} = +2 mA			0.4	V
I_{CC}	Supply Current	Normal operation, equalizing cable < 140m (Belden 1694A)(7)		70	85	mA
		Normal operation, equalizing cable > 140 m (Belden 1694A)		90	110	mA
		Power save mode		10	14	mA

(6) The differential output voltage and offset voltage are adjustable through the SPI.
(7) The equalizer automatically shifts equalization stages at cable lengths less than 140 m (Belden 1694A) to reduce power consumption. This power savings is also achieved by setting Extended 3G Reach Mode = 1 through the SPI.

6.6 AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BR_{MIN}	Minimum Input Data Rate (SDI, $\overline{SDI}$)		125			Mbps
BR_{MAX}	Maximum Input Data Rate (SDI, $\overline{SDI}$)				2970	Mbps
TJ_{RAW}	Jitter for Various Cable Lengths	270 Mbps, Belden 1694A, 0 to 350 meters(2)			0.2	UI
		270 Mbps, Belden 1694A, 350 to 400 meters		0.2		
		1.485 Gbps, Belden 1694A, 0 to 170 meters(2)			0.25	
		1.485 Gbps, Belden 1694A, 170 to 200 meters		0.3		
		2.97 Gbps, Belden 1694A, 0-110 meters(2)			0.3	
		2.97 Gbps, Belden 1694A, 110 to 140 meters		0.35		
t_r,t_f	Output Rise Time, Fall Time (SDO, $\overline{SDO}$)	20% to 80%, 100-Ω load(3), see Figure 1		80	130	ps
	Mismatch in Rise/Fall Time (SDO, $\overline{SDO}$)	See (3)		2	15	ps
t_{OS}	Output Overshoot (SDO, $\overline{SDO}$)	See (3)		1%	5%	

(1) Typical values are stated for V_{CC} = +3.3 V and T_A = +25°C.
(2) Based on design and characterization data over the full range of recommended operating conditions of the device. Jitter is measured in accordance with ST RP 184, ST RP 192, and the applicable serial data transmission standard: ST 424, ST 292, or ST 259.
(3) Specification is ensured by characterization.

Copyright © 2009–2015, Texas Instruments Incorporated

AC Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL_{IN}	Input Return Loss (SDI, $\overline{SDI}$)	5 MHz to 1.5 GHz(4)	15			dB
		1.5 GHz to 3.0 GHz(4)	10			dB
R_{IN}	Input Resistance (SDI, $\overline{SDI}$)	single-ended		1.3		kΩ
C_{IN}	Input Capacitance (SDI, $\overline{SDI}$)	single-ended		0.7		pF

(4) Input return loss is dependent onboard design. The LMH0384 exceeds this specification on the SD384 evaluation board with a return loss network consisting of a 5.6 nH inductor in parallel with the 75-Ω series resistor on the input.

6.7 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
f_{SCK}	SCK Frequency				20	MHz
t_{PH}	SCK Pulse Width High	See Figure 2 and Figure 3	40			% SCK period
t_{PL}	SCK Pulse Width Low		40			% SCK period
t_{SU}	MOSI Setup Time	See Figure 2 and Figure 3	4			ns
t_H	MOSI Hold Time		4			ns
t_{SSSU}	$\overline{SS}$ Setup Time	See Figure 2 and Figure 3	4			ns
t_{SSH}	$\overline{SS}$ Hold Time		4			ns
t_{SSOF}	$\overline{SS}$ Off Time		10			ns

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
t_{ODZ}	MISO Driven-to-Tristate Time	See Figure 3			15	ns
t_{OZD}	MISO Tristate-to-Driven Time				15	ns
t_{OD}	MISO Output Delay Time				15	ns

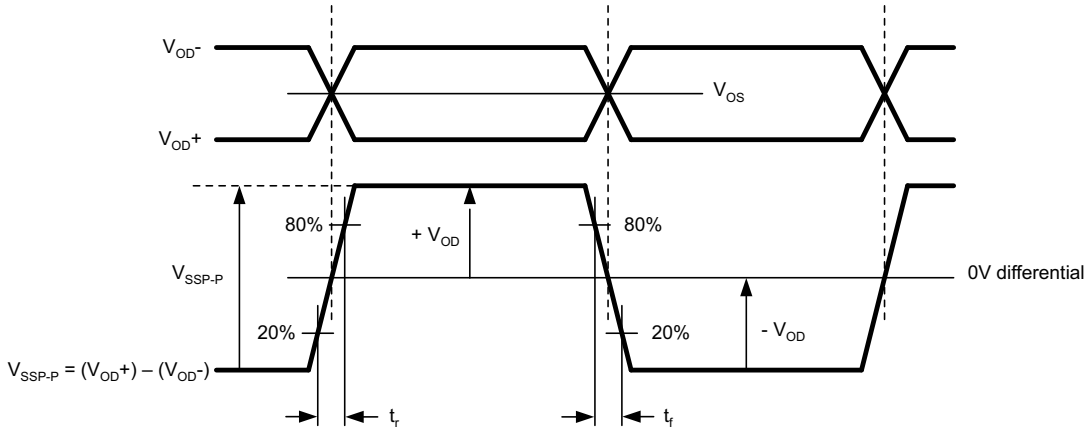


Figure 1. LVDS Output Voltage, Offset, and Timing Parameters

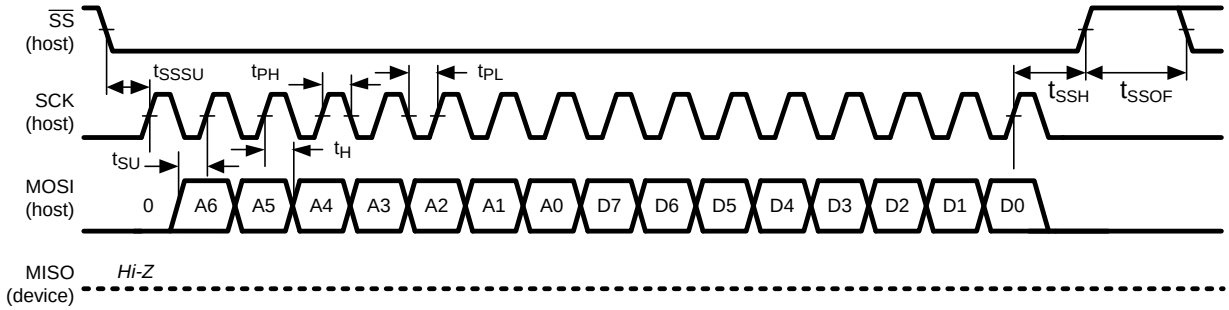


Figure 2. SPI Write

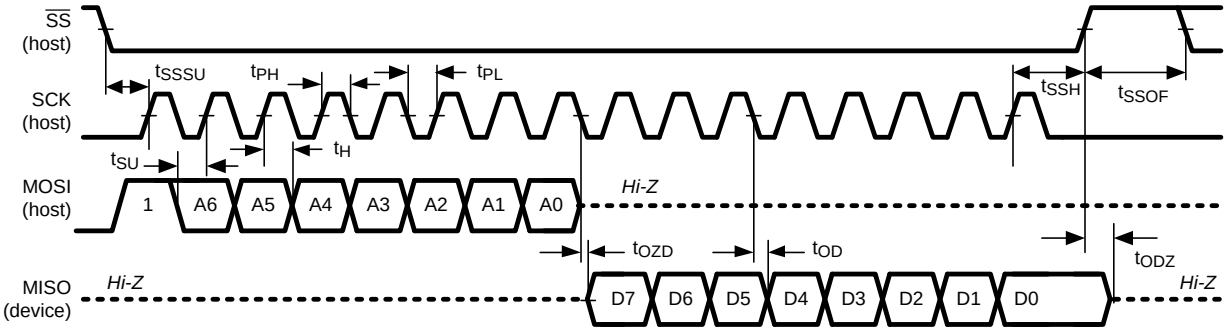


Figure 3. SPI Read

Copyright © 2009–2015, Texas Instruments Incorporated

6.9 Typical Characteristics

Typical device characteristics at TA = +25°C and VDD = 3.3 V, unless otherwise noted.

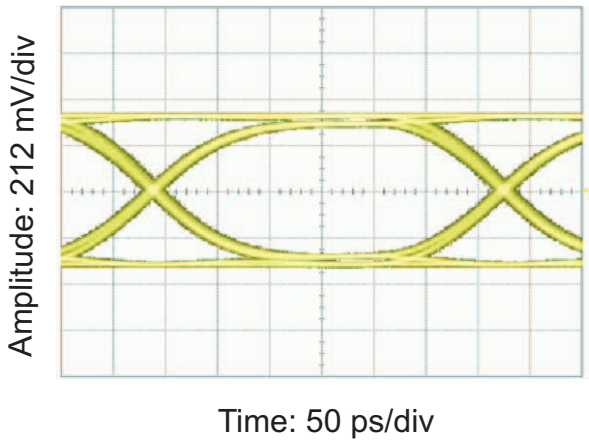


Figure 4. 20-M B1694A PRBS10 2.97 Gbps

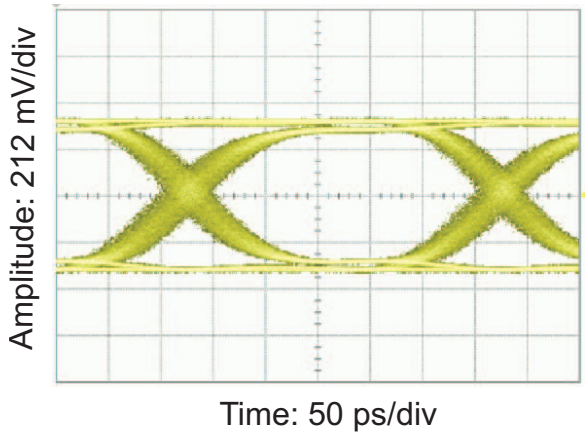


Figure 5. 100-M B1694A PRBS10 2.97 Gbps

Copyright © 2009–2015, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The LMH0384 3-Gbps HD - SD SDI Extended Reach and Configurable Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports ST 424, ST 292, ST 344, and ST 259 standards. The LMH0384 includes active sensing features and design enhancements including longer cable equalization, lower output jitter, configurable pin mode and SPI modes, a power-saving sleep mode, and programmable output common-mode voltage and swing. The LMH0384 implements DC restoration to correctly handle pathological data conditions.

7.2 Functional Block Diagram

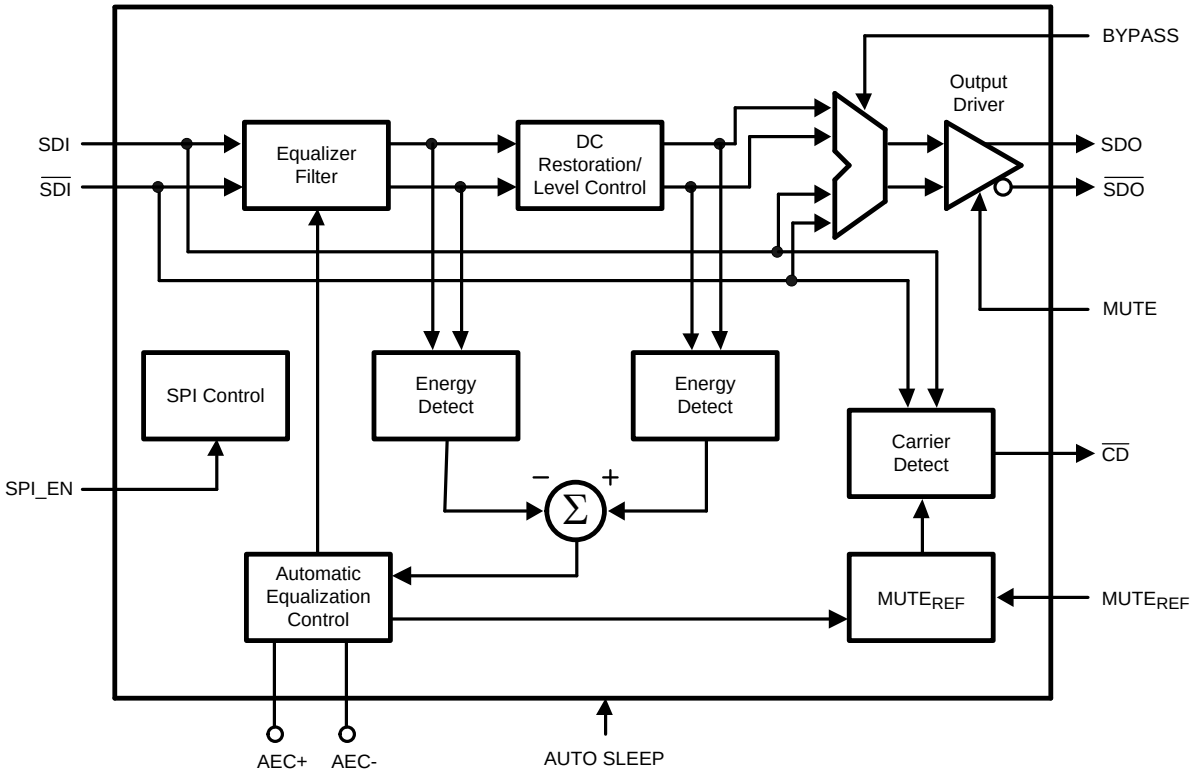


Figure 6. Pin Mode

7.3 Feature Description

7.3.1 Block Description

The **Equalizer Filter** block is a multistage adaptive filter. If BYPASS is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If BYPASS is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1-µF capacitor placed across the AEC+ and AEC- pins.

The **Carrier Detect** block generates the carrier detect signal based on the SDI input and an adjustment from the **Mute Reference** block.

Copyright © 2009–2015, Texas Instruments Incorporated

Feature Description (continued)

The **SPI Control** block uses the MOSI, MISO, SCK, and $\overline{SS}$ signals in SPI mode to control the SPI registers. SPI_EN selects between SPI mode and pin mode. In pin mode, SPI_EN is driven logic low.

The **Output Driver** produces SDO and $\overline{SDO}$.

7.3.2 Mute Reference ($MUTE_{REF}$)

The mute reference sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. The applied voltage must be greater than the $MUTE_{REF}$ floating voltage (typically 1.3 V) in order to change the $\overline{CD}$ threshold. As the applied $MUTE_{REF}$ voltage is increased, the amount of cable that can be equalized before carrier detect is deasserted and the outputs are muted is decreased. $MUTE_{REF}$ may be left unconnected or connected to ground for normal $\overline{CD}$ operation.

7.3.3 Carrier Detect ($\overline{CD}$) and Mute

Carrier detect $\overline{CD}$ indicates if a valid signal is present at the LMH0384 input. If $MUTE_{REF}$ is used, the carrier detect threshold will be altered accordingly. $\overline{CD}$ provides a high voltage when no signal is present at the LMH0384 input. $\overline{CD}$ is low when a valid input signal is detected.

MUTE can be used to manually mute or enable SDO and $\overline{SDO}$. Applying a high input to MUTE will mute the LMH0384 outputs by forcing the output to a logic zero. Applying a low input will force the outputs to be active.

$\overline{CD}$ and MUTE may be tied together to automatically mute the output when no input signal is present.

7.3.4 Auto Sleep

The auto sleep mode allows the LMH0384 to power down when no input signal is detected. If the AUTO SLEEP pin is set high, the LMH0384 goes into a deep power save mode when no signal is detected. The device powers on again once an input signal is detected. The auto sleep functionality can be turned off by setting AUTO SLEEP low or tying this pin to ground. An additional auto sleep setting available in SPI mode can be used to force the equalizer to power down regardless of whether there is an input signal or not. Auto sleep has precedence over mute and bypass modes.

In auto sleep mode, the time to power down the equalizer when the input signal is removed is less than 200 µs and should not have any impact on the system timing requirements. The device will wake up automatically once an input signal is detected (within 1 µs). The overall system will be limited only by the settling time constant of the equalizer adaptation loop.

7.3.5 Input Interfacing

The LMH0384 accepts either differential or single-ended input. The input must be AC-coupled. *Functional Block Diagram* shows the typical configuration for a single-ended input. The unused input must be properly terminated as shown.

The LMH0384 can be optimized for different launch amplitudes through the SPI (see *Launch Amplitude Optimization* in *Programming*).

The LMH0384 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

7.3.6 Output Interfacing

SDO and $\overline{SDO}$ together are internally terminated 100-Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

The default output common-mode voltage (V_{OS}) is 1.25 V. The output common-mode voltage may be adjusted through the SPI in 200-mV increments, from 1.05 V to 1.85 V (see *Output Driver Adjustments* in *Programming*). This adjustable output common-mode voltage offers flexibility for interfacing to many types of receivers.

The default differential output swing (V_{SSP-P}) is 700 mV_{P-P}. The differential output swing may be adjusted through the SPI in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P} (see *Output Driver Adjustments* in *Programming*).

Copyright © 2009–2015, Texas Instruments Incorporated

Feature Description (continued)

The LMH0384 output should be DC coupled to the input of the receiving device as long as the common-mode ranges of both devices are compatible. 100-Ω differential transmission lines should be used to connect between the LMH0384 outputs and the input of the receiving device where possible. Figure 7 shows an example of a DC-coupled interface between the LMH0384 and LMH0346 SDI reclocker. All that is required is the 100-Ω differential termination as shown. The resistor should be placed as close as possible to the LMH0346 input. If desired, this network may be terminated with two 50-Ω resistors and a center tap capacitor to ground in place of the signal 100-Ω resistor.

Figure 8 shows an example of a DC-coupled interface between the LMH0384 and LMH0356 SDI reclocker. The LMH0356 inputs have 50-Ω internal terminations (100-Ω differential) to terminate the transmission line, so no additional components are required.

The LMH0384 allows flexibility when interfacing to low voltage crosspoint switches (that is, 1.8 V) and other devices with limited input ranges. The LMH0384 outputs can be DC coupled to these devices in most cases, avoiding the need to AC couple.

The LMH0384 may be AC-coupled to the receiving device when necessary. For example, the LMH0384 outputs are not strictly compatible with 3.3 V CML and thus should not be connected through 50-Ω resistors to 3.3 V. If the input common-mode range of the receiving device is not compatible with the output common-mode range of the LMH0384, then AC coupling is required. Following the AC-coupling capacitors, the signal may have to be biased at the input of the receiving device.

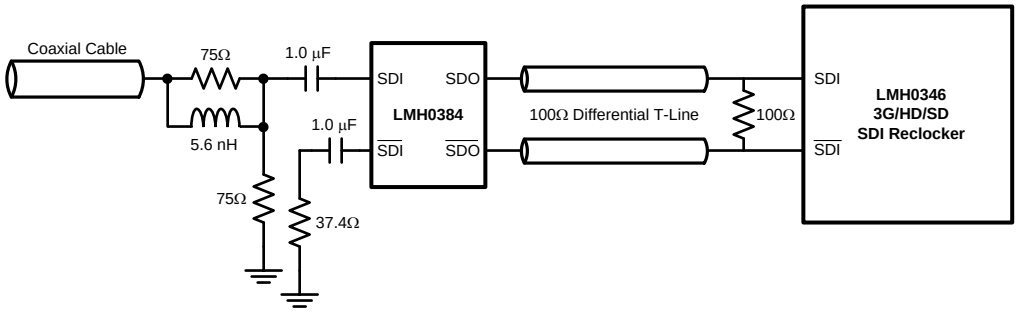


Figure 7. DC Output Interface to LMH0346 Reclocker

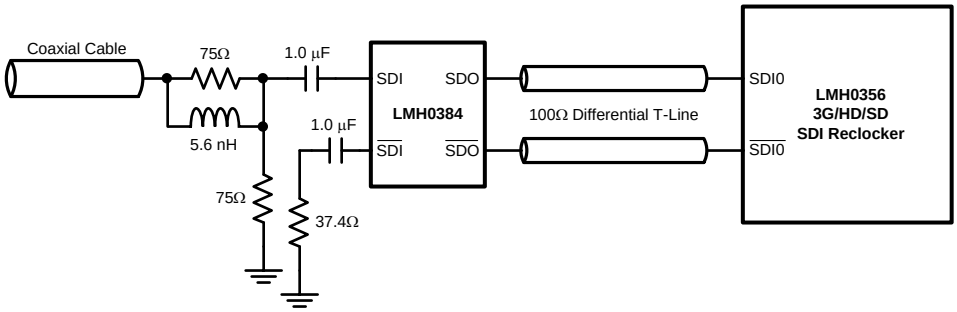


Figure 8. DC Output Interface to LMH0356 Reclocker

7.4 Device Functional Modes

The LMH0384 supports two modes of operation: Pin and SPI Mode. In pin mode the LMH0384 is footprint compatible with the LMH0344 and legacy SDI equalizers. In the optional SPI mode, the LMH0384 provides register access to all of its features along with a cable length indicator, programmable output common-mode voltage and swing, and launch amplitude optimization.

Copyright © 2009–2015, Texas Instruments Incorporated

7.5 Programming

Setting SPI_EN high enables the optional SPI register access mode. In SPI mode, the LMH0384 provides register access to all of its features along with a cable length indicator, programmable output common-mode voltage and swing, and launch amplitude optimization. There are five supported 8-bit registers in the device (see Table 1). With SPI_EN set low, the device operates in pin mode and is footprint compatible with the LMH0344, LMH0044, and LMH0074.

7.5.1 SPI Write

The SPI write is shown in Figure 2. The MOSI payload consists of a “0” (write command), seven address bits, and eight data bits. The $\overline{SS}$ signal is driven low, and the 16 bits are sent to the LMH0384's MOSI input. Data is latched on the rising edge of SCK. The MISO output is normally tri-stated during this operation. After the SPI write, $\overline{SS}$ must return high.

7.5.2 SPI Read

The SPI read is shown in Figure 3. The MOSI payload consists of a “1” (read command) and seven address bits. The $\overline{SS}$ signal is driven low, and the eight bits are sent to the LMH0384's MOSI input. The addressed location is accessed immediately after the rising edge of the 8th clock and the eight data bits are shifted out on MISO starting with the falling edge of the 8th clock. MOSI must be tri-stated immediately after the rising edge of the 8th clock. After the SPI read, $\overline{SS}$ must return high.

7.5.3 Output Driver Adjustments

The output driver swing (amplitude) and offset voltage (common-mode voltage) are adjustable through SPI register 01h.

The output swing is adjustable through bits [7:5] of SPI register 01h. The default value for these register bits is “011” for a peak to peak differential output voltage of 700 mV_{P-P}. The output swing can be adjusted in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P}.

The offset voltage is adjustable through bits [4:2] of SPI register 01h. The default value for these register bits is “001” for an output offset of 1.25 V. The output common-mode voltage may be adjusted in 200-mV increments, from 1.05 V to 1.85 V. It can also be set to “101” for the maximum offset voltage. At this maximum offset voltage setting, the outputs are referenced to the positive supply and the offset voltage is around 2.1 V.

7.5.4 Launch Amplitude Optimization

The LMH0384 can compensate for attenuation of the input signal prior to the equalizer. This compensation is useful for applications with a passive splitter at the equalizer input or a non-ideal input termination network, and is controlled by SPI register 02h.

Bit 7 of SPI register 02h is used for coarse control of the launch amplitude setting. At the default setting of “0”, the LMH0384 operates normally and expects a launch amplitude of 800 mV_{P-P}. Bit 7 may be set to “1” to optimize the LMH0384 for input signals with 6 dB of attenuation (400 mV_{P-P}).

Once the coarse control is set, the LMH0384 input compensation may be further fine tuned by bits [6:3] of SPI register 02h. These bits may be used to tweak the input gain stage -22% to +40% around the coarse control setting.

Copyright © 2009–2015, Texas Instruments Incorporated

Programming (continued)

7.5.5 Cable Length Indicator (CLI)

The Cable Length Indicator (CLI) provides an indication of the length of cable attached to the input. CLI is accessible through bits [7:3] of SPI register 03h. The 5-bit CLI ranges in decimal value from 0 to 25 (“00000” to “11001” binary) and increases as the cable length is increased. Figure 9 shows typical CLI values vs. Belden 1694A cable length. CLI is valid for Belden 1694A cable lengths of up to 140 m at 2.97 Gbps, 200 m at 1.485 Gbps, and 400 m at 270 Mbps.

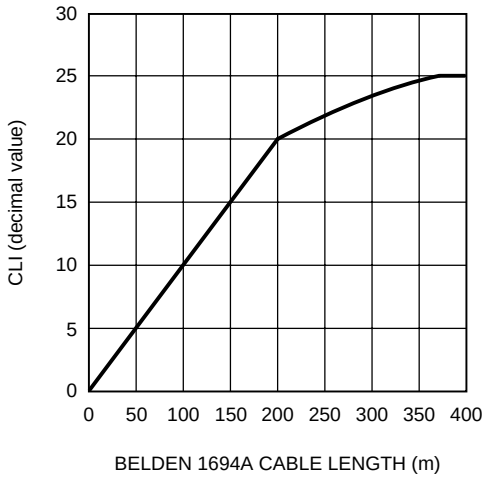


Figure 9. CLI vs. Belden 1694A Cable Length

7.5.6 Application of CLI: Extending 3G Reach

An application of CLI is to extend the 3G reach in systems which have margin in the jitter budget. This allows for additional cable reach at 2.97 Gbps at the expense of slightly higher output jitter. The extended 3G reach mode provides 15m of additional Belden 1694A cable reach, with an increase of output jitter at this longer cable length of 0.05 to 0.1 UI.

The extended 3G reach mode is accessible through bit 2 of SPI register 00h. In order to achieve longer 3G cable reach while still maintaining the performance at HD and SD data rates, a state machine can be implemented as shown in Figure 10. (Note: If this procedure is not followed, the maximum equalizable cable lengths for HD and SD data rates will be limited to less than what can be achieved in normal mode).

Copyright © 2009–2015, Texas Instruments Incorporated

Programming (continued)

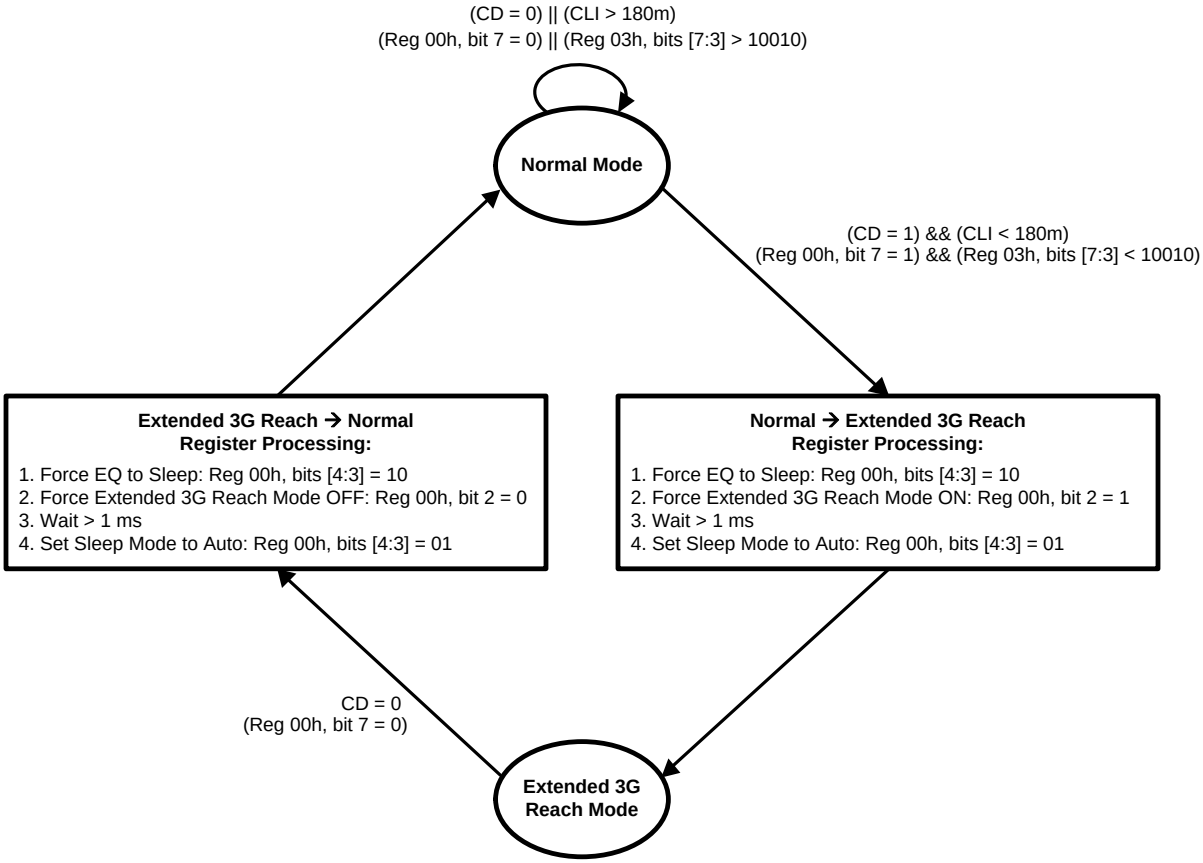


Figure 10. Extended 3G Reach Mode State Machine Example

7.5.7 Explanation of Extended 3G Reach Mode State Machine (Figure 10)

When the LMH0384 is powered on, it will be in normal mode. If there is no input signal (register 00h, bit 7 = 0) or if the input cable is longer than a user programmable cable length (that is 180m, which means register 03h, bits [7:3] > 10010), then the device should remain in normal mode.

Once an input signal is detected (register 00h, bit 7 = 1) AND the detected cable length is shorter than the user programmed cable length of 180m (register 03h, bits [7:3] < 10010), then the equalizer can enter the extended 3G reach mode to allow for longer cable lengths at 2.97 Gbps. This requires the following procedure:

1. Force the equalizer to sleep by writing “10” to bits [4:3] of register 00h.
2. Turn on the extended 3G reach mode by writing “1” to bit 2 of register 00h.
3. Wait at least 1ms.
4. Set the sleep mode to auto by writing “01” to bits [4:3] of register 00h. Alternately, sleep mode may be set to off by writing “00” to bits [4:3] of register 00h.

The equalizer remains in extended 3G reach mode until the cable length is changed. If the cable length is changed, the input signal drops out momentarily. Once this happens (register 00h, bit 7 = 0), then the following procedure must be used to set the device back to normal mode:

1. Force the equalizer to sleep by writing “10” to bits [4:3] of register 00h.
2. Turn off the extended 3G reach mode by writing “0” to bit 2 of register 00h.
3. Wait at least 1ms.
4. Set the sleep mode to auto by writing “01” to bits [4:3] of register 00h. Alternately, sleep mode may be set to off by writing “00” to bits [4:3] of register 00h.

Copyright © 2009–2015, Texas Instruments Incorporated

7.6 Register Maps

Table 1. SPI Registers

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
00h	R/W	General Control	7	Carrier Detect		0: No carrier detected. 1: Carrier detected.
			6	Mute	0	Mute has precedence over Bypass. 0: Normal operation. 1: Outputs muted.
			5	Bypass	0	0: Normal operation. 1: Equalizer bypassed.
			4:3	Sleep Mode	01	Sleep mode control. Sleep has precedence over Mute and Bypass. 00: Disable sleep mode (force equalizer to stay enabled). 01: Sleep mode active when no input signal detected. 10: Force equalizer into sleep mode (powered down) regardless of whether there is an input signal or not. 11: Reserved.
			2	Extended 3G Reach Mode	0	Extended 3G reach mode to extend the cable length for 2.97 Gbps applications. 0: Normal operation. 1: Extended 3G reach mode.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.
01h	R/W	Output Driver	7:5	Output Swing	011	Output driver swing (V_{SSP-P}). 000: V_{SSP-P} = 400 mV_{P-P}. 001: V_{SSP-P} = 500 mV_{P-P}. 010: V_{SSP-P} = 600 mV_{P-P}. 011: V_{SSP-P} = 700 mV_{P-P}. 100: V_{SSP-P} = 800 mV_{P-P}. 101, 110, 111: Reserved.
			4:2	Offset Voltage	001	Output driver offset voltage (common-mode voltage). 000: V_{OS} = 1.05V. 001: V_{OS} = 1.25V. 010: V_{OS} = 1.45V. 011: V_{OS} = 1.65V. 100: V_{OS} = 1.85V. 101: V_{OS} referenced to positive supply. 110, 111: Reserved.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.

Copyright © 2009–2015, Texas Instruments Incorporated

Register Maps (continued)

Table 1. SPI Registers (continued)

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
02h	R/W	Launch Amplitude	7	Coarse Control	0	Coarse launch amplitude optimization. 0: Normal optimization with no external attenuation (800 mV_{P-P} launch amplitude). 1: Optimized for 6 dB external attenuation (400 mV_{P-P} launch amplitude).
			6:3	Fine Control	0000	Launch amplitude optimization fine tuning. 0000: Nominal. 0001: -4% from nominal. 0010: -8% from nominal. 0011: -11% from nominal. 0100: -14% from nominal. 0101: -17% from nominal. 0110: -20% from nominal. 0111: -22% from nominal. 1000: Nominal. 1001: +4% from nominal. 1010: +9% from nominal. 1011: +14% from nominal. 1100: +20% from nominal. 1101: +26% from nominal. 1110: +33% from nominal. 1111: +40% from nominal.
			2:0	Reserved	000	Reserved as 000. Always write 000 to these bits.
03h	R	CLI	7:3	CLI		Cable Length Indicator. Provides an indication of the length of cable attached to the input. CLI increases as the cable length increases.
			2:0	Reserved	000	Reserved.
04h	R	Device ID	7:0	Die Revision	00000010	Die revision.

Copyright © 2009–2015, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH0384 is a single-channel, 3-Gbps HD - SD SDI Adaptive Cable Equalizer designed to equalize data transmitted over cable or any media with similar dispersive loss characteristics. The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports ST 424, ST 292, ST 344, and ST 259. Additional features include separate carrier detect and output mute pins which may be tied together to mute the output when no signal is present. A programmable mute reference is provided to mute the output at a selectable level of signal degradation. The bypass pin allows the adaptive equalizer to be bypassed. The LMH0384 accepts either a differential or single-ended input. The input must be AC-coupled.

The LMH0384 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in ST RP 178 and RP 198, respectively.

8.1.1 Replacing the LMH0344

In pin mode, the LMH0384 is a drop-in replacement for the LMH0344SQ SDI cable equalizer. When replacing an LMH0344 with an LMH0384, it is important to consider the following points:

1. The LMH0384 auto sleep function is mapped to pin 12 which is a ground pin on the LMH0344SQ. When this pin is grounded on the LMH0384, the auto sleep function is disabled. To enable auto sleep mode on the LMH0384, pin 12 must be pulled high.
2. Pin 4 and pin 9 on the LMH0344SQ are true ground pins. For the LMH0384, pin 4 and pin 9 may be driven logic low in pin mode (they do not require a true ground connection).
3. The LMH0384 has lower input capacitance than the LMH0344 which allows for improved input return loss. The input return loss network may need to be modified. In most cases, the LMH0384 should provide superior input return loss.
4. The LMH0384 default output common-mode voltage is different than that of the LMH0344. In most cases, this should not cause an issue. The LMH0384 and LMH0344 outputs can both be DC coupled to TI's SDI reclockers and cable drivers. In addition, the LMH0384 output can be DC coupled to LVDS and other inputs that require lower input common-mode voltages than the LMH0344. The LMH0384 output common-mode voltage is adjustable through the SPI.

8.2 Typical Application

Figure 11 and Figure 12 show the application circuit for the LMH0384 in SPI mode and Pin mode.

Copyright © 2009–2015, Texas Instruments Incorporated

Typical Application (continued)

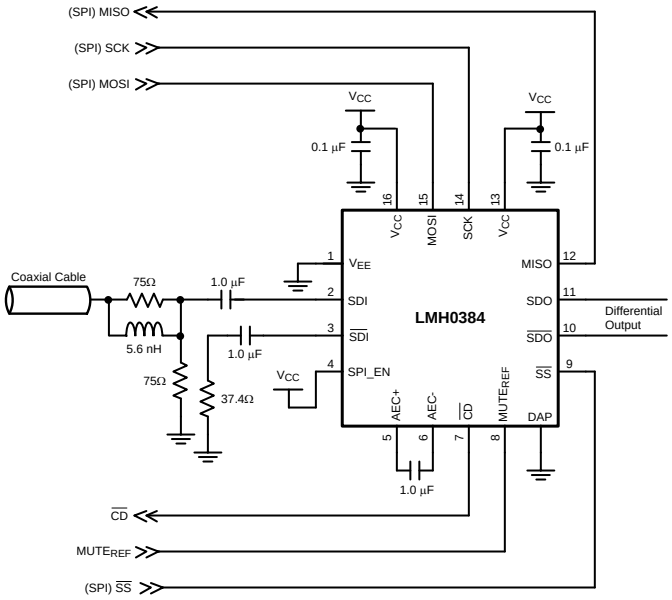


Figure 11. Application Circuit (SPI Mode)

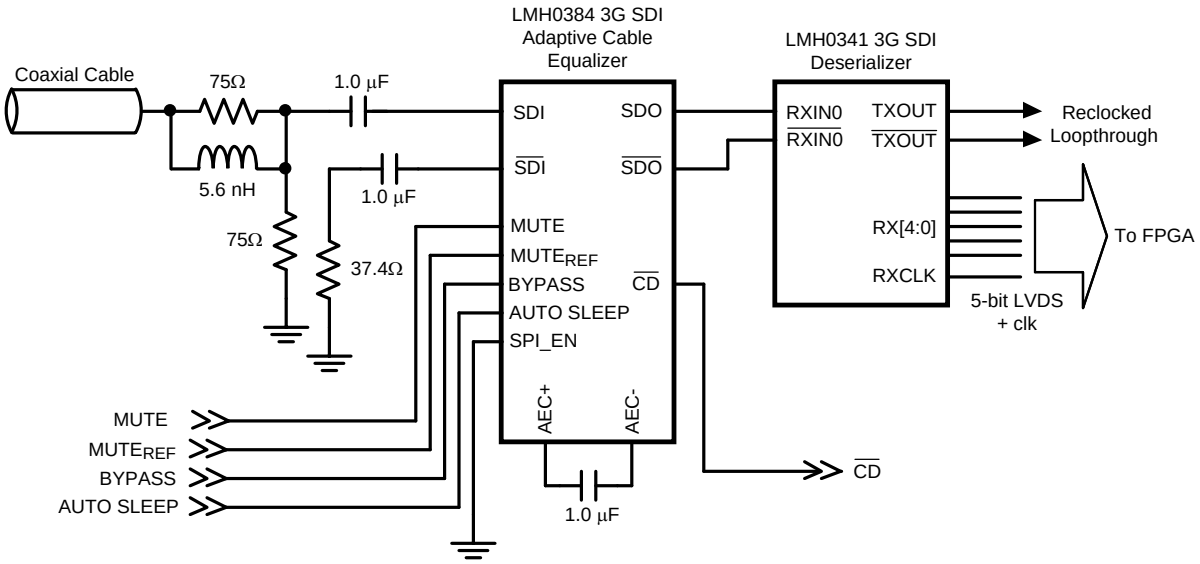


Figure 12. Typical Application (Pin Mode)

8.2.1 Design Requirements

Table 2 lists the design parameters for the LMH0384.

Table 2. LMH0384 Design Parameters

DESIGN PARAMETER	REQUIREMENT
Input AC-coupling capacitors	Required. A common type of AC-coupling capacitor is 1 µF ±10% X7R ceramic capacitor (0402 or 0201 size). Capacitors may be implemented on the PCB or in the connector.

Copyright © 2009–2015, Texas Instruments Incorporated

Typical Application (continued)

Table 2. LMH0384 Design Parameters (continued)

DESIGN PARAMETER	REQUIREMENT
Output AC-coupling capacitors	The user should check input common mode voltage. If AC coupling capacitor is required, SDO AC-coupling capacitor is expected to be 4.7 µF ±10%.
Distance from Device to BNC	Keep this distance as short as possible to minimize parasitic
Input launch amplitude	Refer to *DC Electrical Characteristics*

8.2.2 Detailed Design Procedure

1. Maximum power draw for PCB regulator selection. For this use maximum power consumption in the data sheet.
2. Closely compare schematic against typical connection diagram in the data sheet.
3. Plan out the PCB layout and component placement to minimize parasitic.
4. Consult the BNC vendor for optimum BNC landing pattern.

8.2.3 Application Curves

Figure 13 and Figure 14 depict the differential output eye diagrams for SDO, $\overline{\text{SDO}}$ at 2.97 Gbps. Measurements were done at default operating conditions.

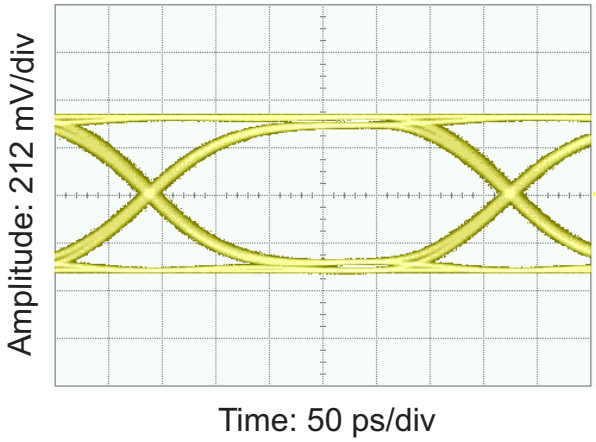


Figure 13. 1-M B1694A PRBS10 2.97 Gbps

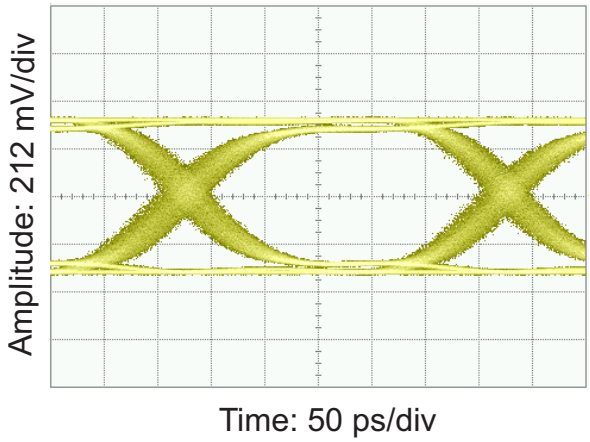


Figure 14. 100-M B1694A PRBS10 2.97 Gbps

8.3 Dos and Don'ts

Pay special attention to the PCB layout for the high speed signals. The SMPTE specifies the requirements for the Serial Digital Interface to transport digital video at SD, HD, and 3 Gbps data rates over coaxial cables. One of the requirements is meeting the required Return Loss. This requirement specifies how closely the port resembles 75-Ω impedance across a specified frequency band. The SMPTE specifications also defines the use of AC-coupling capacitors for transporting uncompressed serial data streams with heavy low frequency content. This specification requires the use of a 1-µF AC-coupling capacitors on the input of the LMH0384 to avoid low frequency DC wander.

Copyright © 2009–2015, Texas Instruments Incorporated

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the recommended operating conditions in terms of DC voltage, and maximum current consumption.
2. The maximum current draw for the LMH0384 is provided in the data sheet. This figure can be used to calculate the maximum current the supply must provide. Current consumption can be derived from the typical power consumption specification in the data sheet.
3. The LMH0384 does not require any special power supply filtering, provided the recommended operating conditions are met. Only standard supply decoupling is required.

10 Layout

10.1 Layout Guidelines

For information on layout and soldering of the WQFN package, please refer to the following application note: *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

The ST 424, 292, and 259 standards have stringent requirements for the input return loss of receivers, which essentially specify how closely the input must resemble a 75-Ω network. Any non-idealities in the network between the BNC and the equalizer will degrade the input return loss. Take care to minimize impedance discontinuities between the BNC and the equalizer to ensure that the characteristic impedance of this trace is 75 Ω.

Please consider the following PCB recommendations:

- Use surface-mount components, and use the smallest components available. In addition, use the smallest size component pads.
- Select trace widths that minimize the impedance mismatch between the BNC and the equalizer.
- Select a board stack up that supports both 75-Ω single-ended traces and 100-Ω loosely-coupled differential traces.
- Place return loss components closest to the equalizer input pins.
- Maintain symmetry on the complementary signals.
- Route 100-Ω traces uniformly (keep trace widths and trace spacing uniform along the trace).
- Avoid sharp bends in the signal path; use 45° or radial bends.
- Place bypass capacitors close to each power pin, and use the shortest path to connect equalizer power and ground pins to the respective power or ground planes.

Copyright © 2009–2015, Texas Instruments Incorporated

10.2 Layout Example

Figure 15 and Figure 16 demonstrate the LMH0384EVM PCB layout. Ground and supply relief under the return loss passive components and pads reduces parasitic - improving return loss performance. Note 5 vias without solder paste are located between 4 squares solder paste mainly for thermal as well as to improve soldering during board assembly.

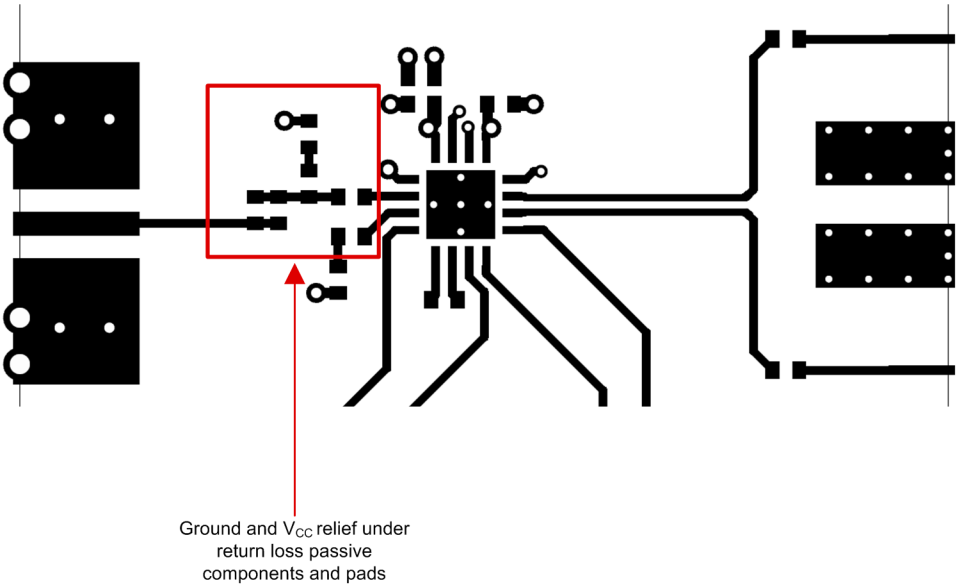


Figure 15. LMH0384EVM Top Etch Layout Example

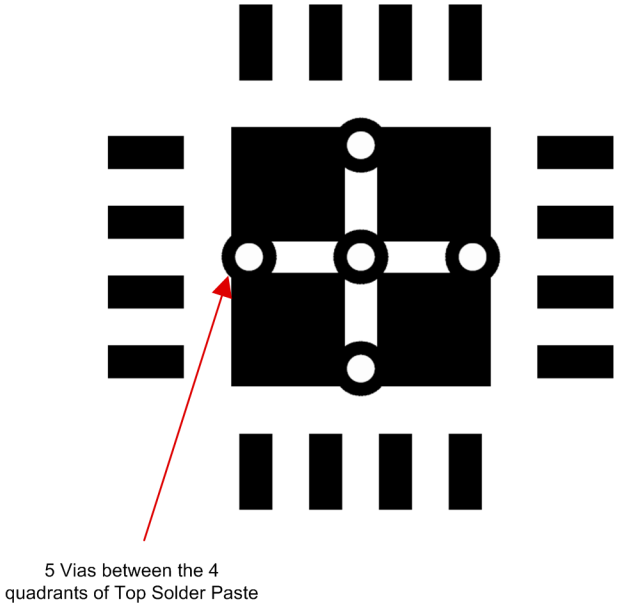


Figure 16. LMH384EVM Top Solder Paste Mask

Copyright © 2009–2015, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For additional information, see the following:

Application Note AN- 1187, *Leadless Leadframe Package (LLP)* (SNOA401).

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2009–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0384SQ/NOPB	ACTIVE	WQFN	RUM	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L0384	Samples
LMH0384SQE/NOPB	ACTIVE	WQFN	RUM	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L0384	Samples
LMH0384SQX/NOPB	ACTIVE	WQFN	RUM	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L0384	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

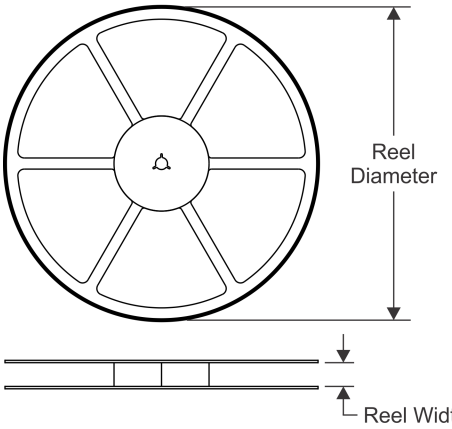
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

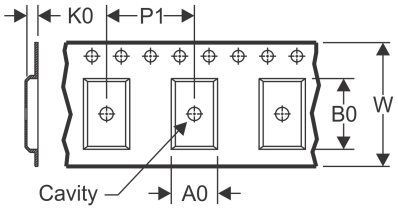
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

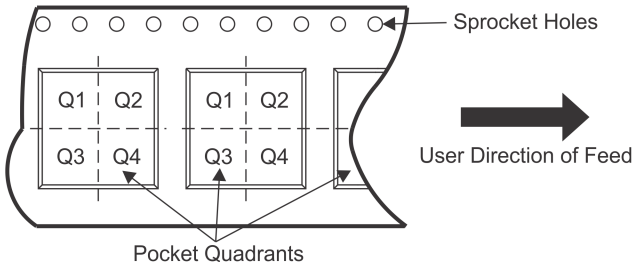


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

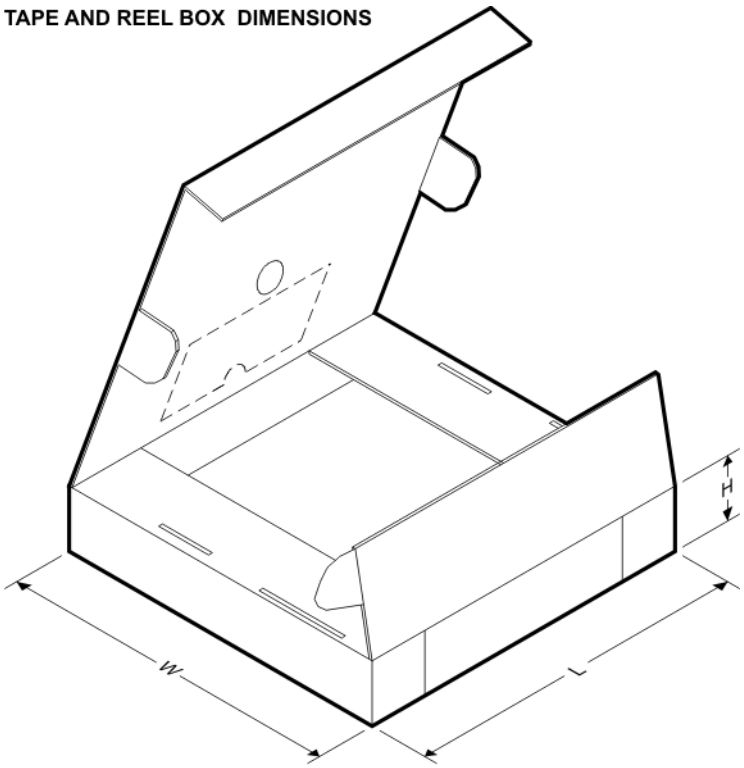
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0384SQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0384SQE/NOPB	WQFN	RUM	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0384SQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

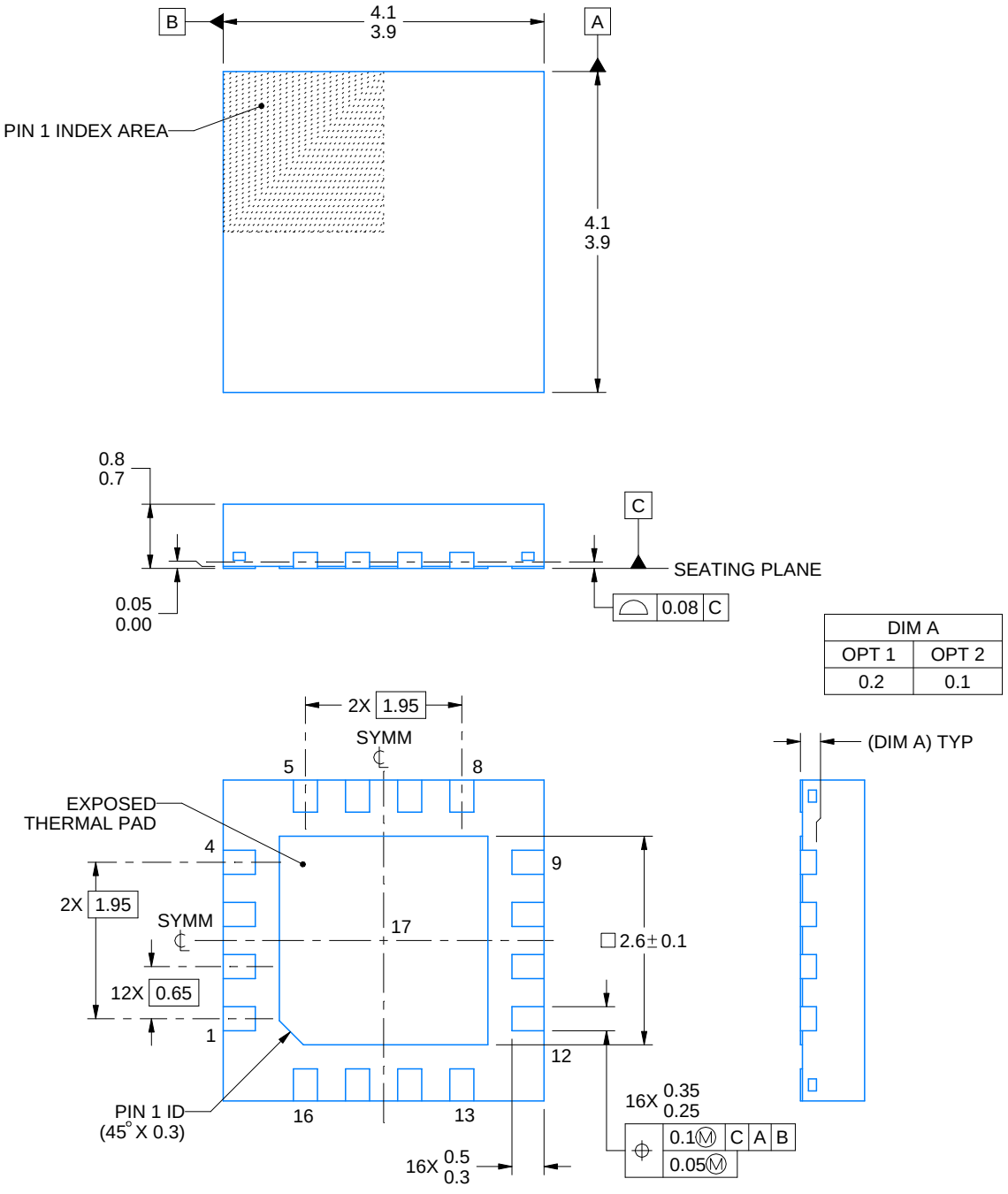
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0384SQ/NOPB	WQFN	RUM	16	1000	208.0	191.0	35.0
LMH0384SQE/NOPB	WQFN	RUM	16	250	208.0	191.0	35.0
LMH0384SQX/NOPB	WQFN	RUM	16	4500	853.0	449.0	35.0

RUM0016A

PACKAGE OUTLINE

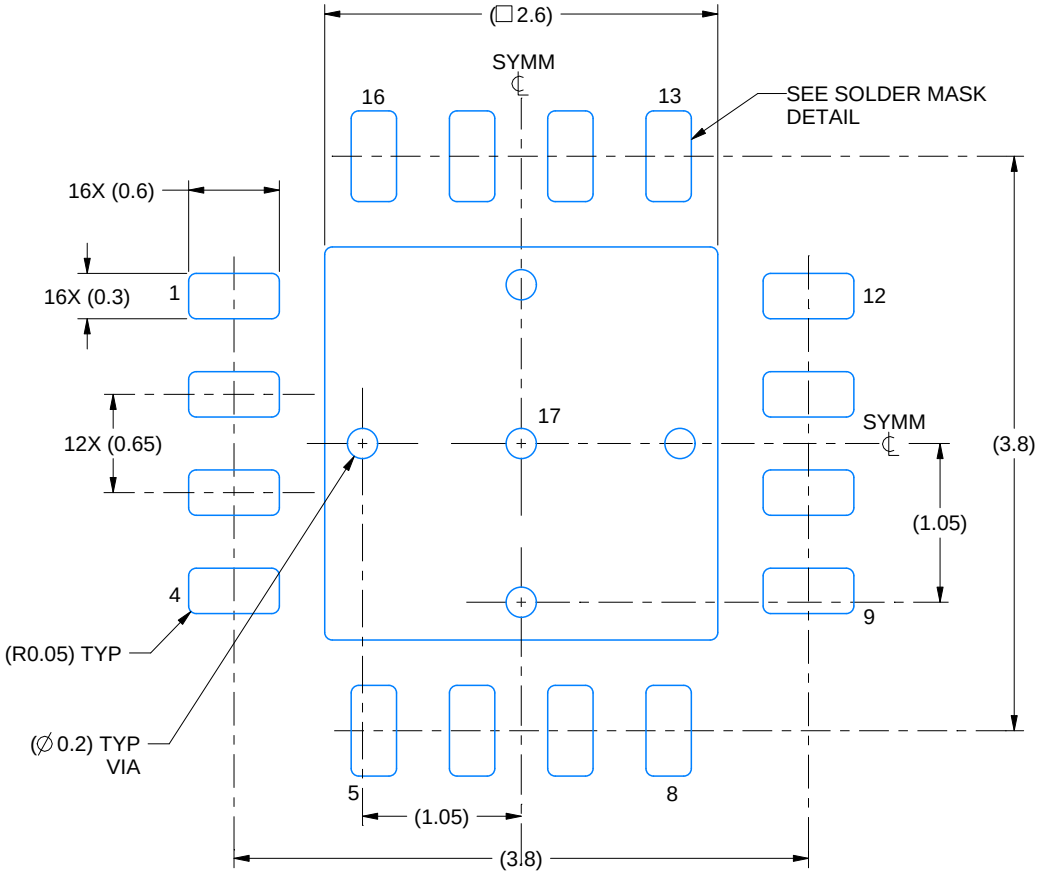
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

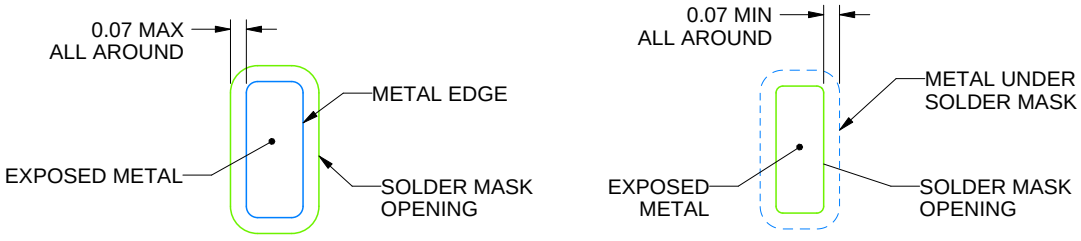


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214998/A 11/2021

NOTES: (continued)

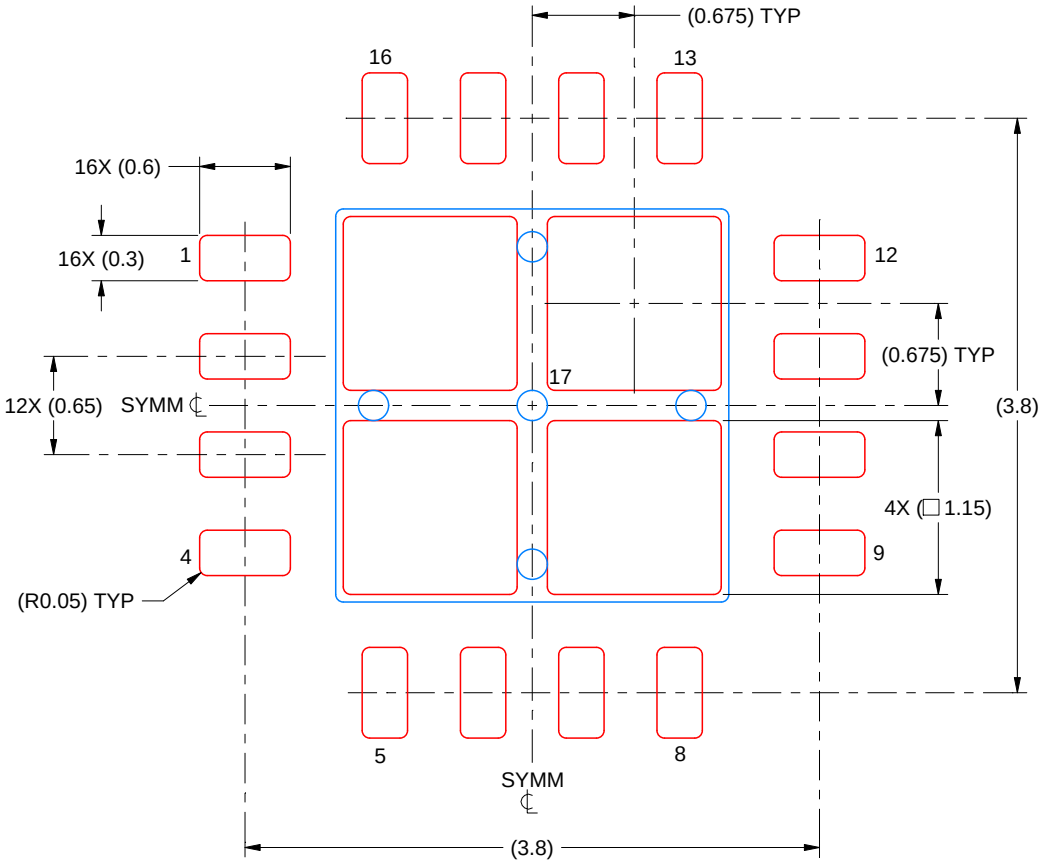
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4214998/A 11/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated