脱离电池运行的 TPS7B81-Q1 150mA、超低 I_Q (3µA) 低压降稳压器

1 特性

- 符合面向汽车 应用的 AEC-Q100 标准：
  - 温度等级 1：-40°C 至 125°C，T_A
- 器件结温范围：
  -40°C 至 150°C
- 3V 至 40V 宽 V_{IN} 输入电压范围，瞬态电压高达 45V
- 最大输出电流：150mA
- 低静态电流 I_Q：
  - EN = 低电平时典型值为 300nA（关断模式）
  - 轻负载时典型值为 2.7µA
  - 轻负载时最大值为 4.5µA
- 线路、负载和温度范围内的输出电压精度为 1.5%
- 最大压降电压：对于固定 5V 输出电压版本，150mA 负载电流下为 540mV
- 与低 ESR（0.001Ω 至 5Ω）陶瓷输出稳定电容器（1µF 至 200µF）搭配使用时可保持稳定
- 5V、3.3V 和 2.5V 固定输出电压
- 集成故障保护：
  - 热关断
  - 短路和过流保护
- 封装：
  - DGN（8 引脚 HVSSOP），$R_{\theta JA}$ = 63.9°C/W
  - DRV（6 引脚 WSON），$R_{\theta JA}$ = 72.8°C/W
  - KVU（5 引脚 TO-252），$R_{\theta JA}$ = 38.8°C/W
    添加了项目符号

2 应用

- 汽车音响主机
- 前照灯
- 电池管理系统 (BMS)
- 逆变器和电机控制

3 说明

在汽车电池连接 应用中，低静态电流 (I_Q) 对于省电和延长电池寿命而言非常重要。始终开启的系统必须在扩展温度范围内实现超低 I_Q，以便在车辆点火开关关闭时也能实现持久运行。

TPS7B81-Q1 是一款低压降 (LDO) 线性稳压器，专为高达 40V V_{IN} 的 这些领域而设计。此器件在轻负载时的典型静态电流仅为 2.7µA，是用于为待机系统中的微控制器以及控制器局域网和本地互联网络 (CAN/LIN) 收发器供电的最佳解决方案。

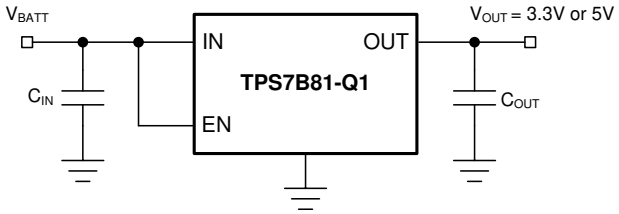
此器件 具有 集成式短路和过流保护。此器件可在 -40°C 至 +125°C 的环境温度下运行，结温范围为 -40°C 至 +150°C。此外，此器件提供多种具有不同尺寸和热导率的封装选项。小型 WSON 封装有助于实现最紧凑的 PCB 设计，即使整个器件散热较多，TO-252 封装也能让器件实现持久运行。这些 特性 使得此器件非常适合用作各种电池连接汽车 这些领域。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7B81-Q1	HVSSOP (8)	3.00mm × 3.00mm
	WSON (6)	2.00mm × 2.00mm
	TO-252 (5)	6.10mm × 6.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Typical Characteristics ... 7
7 **Detailed Description** ... 11
7.1 Overview ... 11
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 12
8 **Application and Implementation** ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 17
9 **Power Supply Recommendations** ... 18
10 **Layout** ... 19
10.1 Layout Guidelines ... 19
10.2 Layout Example ... 19
11 器件和文档支持 ... 20
11.1 接收文档更新通知 ... 20
11.2 支持资源 ... 20
11.3 商标 ... 20
11.4 静电放电警告 ... 20
11.5 Glossary ... 20
12 机械、封装和可订购信息 ... 20

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2019) to Revision C **Page**

- 已更改 将 KVU 封装从“预览”更改为“生产数据” ... 1
- 已更改 *应用* 部分 ... 1

Changes from Revision A (June 2019) to Revision B **Page**

- 已更改 将 DGN 封装从“预览”更改为“生产数据” ... 1
- 已更改 将 *525mV* 更改为 *540mV*（在*最大压降电压* 特性 项目符号） ... 1
- 已添加 $R_{\theta JA}$ *versus Cu Area for the HVSSOP (DGN) Package* through ψ_{JB} *versus Cu Area for the TO-252 (KVU) Package* figures to *Power Dissipation* section ... 15
- Deleted values from capacitors C_{IN} and C_{OUT} in 图 31 ... 17

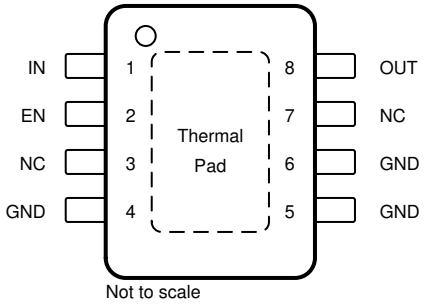
Changes from Original (May 2019) to Revision A **Page**

- 已更改 将“预告信息”更改为“生产数据” ... 1

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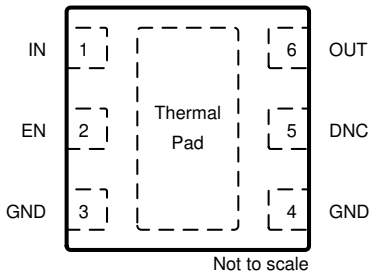
5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP PowerPAD™
Top View



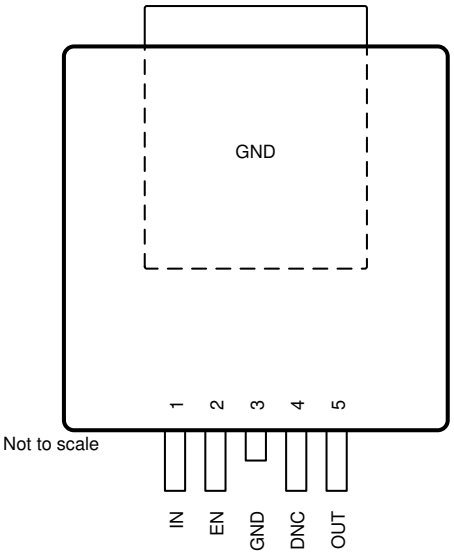
Not to scale

DRV Package
6-Pin WSON PowerPAD™
Top View



Not to scale

KVU Package
5-Pin TO-252
Top View



Not to scale

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Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	DGN	DRV	KVU		
DNC	—	5	4	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	I	Enable input pin. Drive EN greater than V_{IH} to turn on the regulator. Drive EN less than V_{IL} to put the low-dropout (LDO) into shutdown mode.
GND	4, 5, 6	3,4	3, TAB	—	Ground reference
IN	1	1	1	I	Input power-supply pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input Capacitor* section. Place the input capacitor as close to the output of the device as possible.
NC	3, 7	—	—	—	Not internally connected
OUT	8	6	5	O	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Output Capacitor* section. Place the output capacitor as close to output of the device as possible.
Thermal pad				—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Unregulated input(3)	–0.3	45	V
V_{EN}	Enable input(3)	–0.3	V_{IN}	V
V_{OUT}	Regulated output	–0.3	7	V
T_J	Junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, can withstand 45 V for 200 ms.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	3	40	V
V_{EN}	Enable input voltage	0	V_{IN}	V
C_{OUT}	Output capacitor requirements(1)	1	200	µF
ESR	Output capacitor ESR requirements(2)	0.001	5	Ω
T_A	Ambient temperature range	–40	125	°C
T_J	Junction temperature range	–40	150	°C

(1) The output capacitance range specified in the table is the effective value.
(2) Relevant ESR value at f = 10 kHz

6.4 Thermal Information

THERMAL METRIC(1)		TPS7B81-Q1			UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	31.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

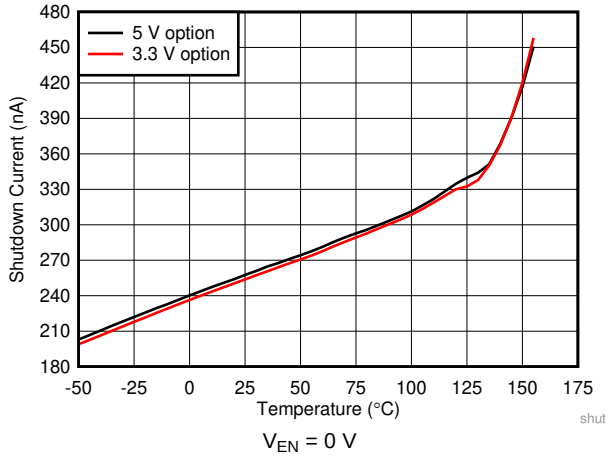
over operating ambient temperature range, T_J = –40°C to +150°C, V_{IN} = 14 V, and 10-µF ceramic output capacitor (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)								
V_{IN}	Input voltage				$V_{OUT(Nom)}$ + $V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	EN = 0 V				0.3	1	µA
$I_{(Q)}$	Quiescent current	V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0 mA				1.9	3.5	µA
		V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0.2 mA		DGN package		2.7	6.5	
				DRV and KVU packages		2.7	4.5	
$V_{(IN, UVLO)}$	V_{IN} undervoltage detection	Ramp V_{IN} down until the output turns off					2.7	V
		Hysteresis				200		mV
ENABLE INPUT (EN)								
V_{IL}	Logic-input low level						0.7	V
V_{IH}	Logic-input high level				2			V
I_{EN}	Enable current					10		nA
REGULATED OUTPUT (OUT)								
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1 mA to 150 mA			–1.5%		1.5%	
$V_{(Line-Reg)}$	Line regulation	V_{IN} = 6 V to 40 V, I_{OUT} = 10 mA					10	mV
$V_{(Load-Reg)}$	Load regulation	V_{IN} = 14 V, I_{OUT} = 1 mA to 150 mA		DGN package			20	mV
				DRV and KVU packages			10	
$V_{(Dropout)}$	Dropout voltage	V_{OUT} = 5 V	I_{OUT} = 150 mA	DGN package		270	540	mV
				DRV and KVU packages		325	585	
			I_{OUT} = 100 mA	DGN package		180	350	
				DRV and KVU packages		200	390	
		V_{OUT} = 3.3 V	I_{OUT} = 150 mA	DGN package			650	
				DRV and KVU packages		345	675	
			I_{OUT} = 100 mA			255	450	
		V_{OUT} = 2.5 V, DGN package	I_{OUT} = 150 mA				750	
			I_{OUT} = 100 mA				500	
I_{OUT}	Output current	V_{OUT} in regulation, V_{IN} = 7 V for the fixed 5-V option, V_{IN} = 5.8 V for the fixed 3.3-V option			0		150	mA
$I_{(CL)}$	Output current limit	V_{OUT} short to 90% × V_{OUT}			180	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)}$ = 0.5 V_{PP}, I_{OUT} = 10 mA, frequency = 100 Hz, C_{OUT} = 2.2 µF				60		dB
OPERATING TEMPERATURE RANGE								
$T_{(SD)}$	Junction shutdown temperature					175		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown					20		°C

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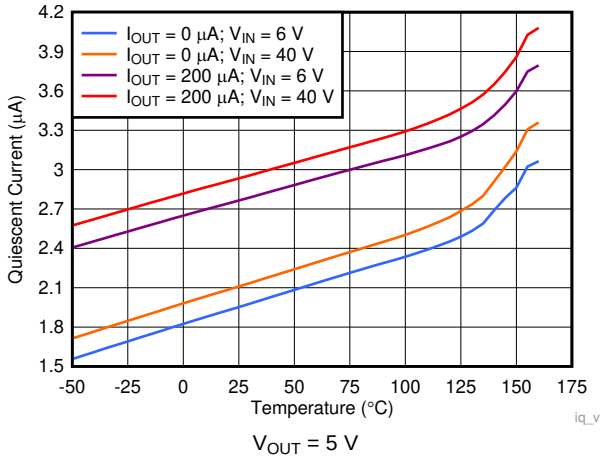
6.6 Typical Characteristics

at T_J = –40°C to +150°C, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



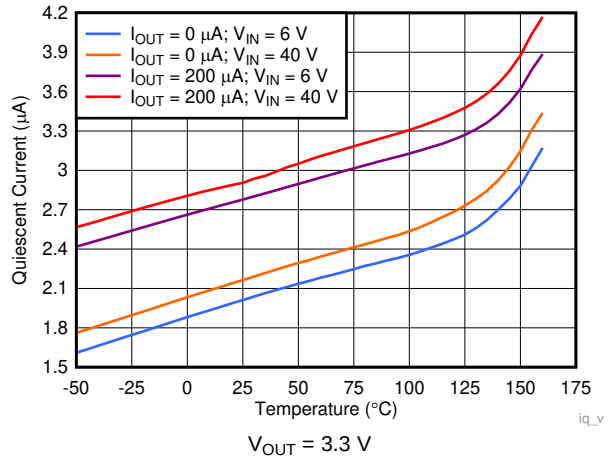
V_{EN} = 0 V

图 1. Shutdown Current vs Ambient Temperature



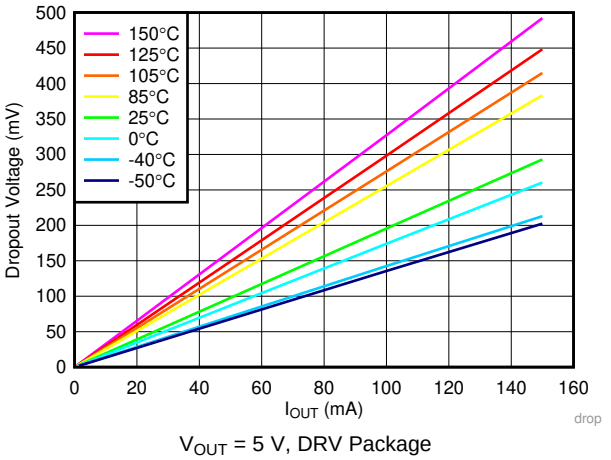
V_{OUT} = 5 V

图 2. Quiescent Current vs Ambient Temperature



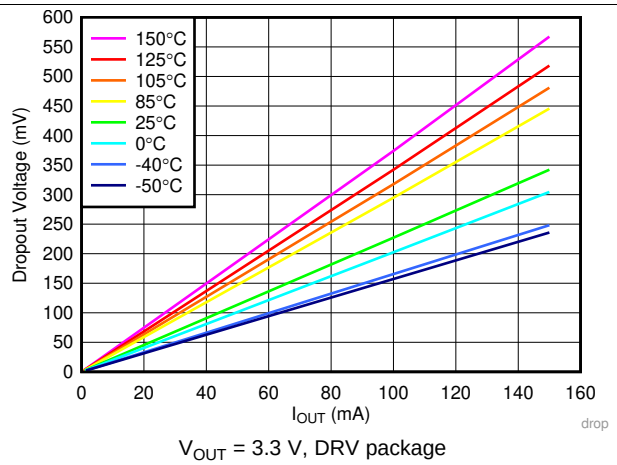
V_{OUT} = 3.3 V

图 3. Quiescent Current vs Ambient Temperature



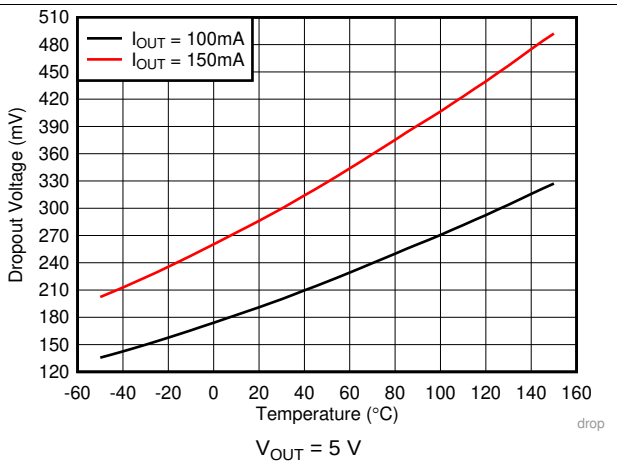
V_{OUT} = 5 V, DRV Package

图 4. Dropout Voltage vs Output Current



V_{OUT} = 3.3 V, DRV package

图 5. Dropout Voltage vs Output Current

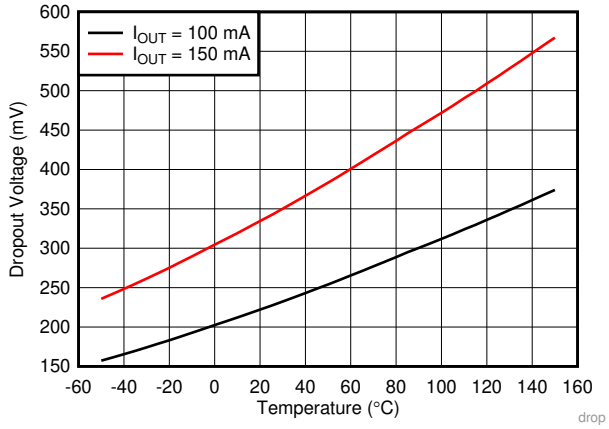


V_{OUT} = 5 V

图 6. Dropout Voltage vs Ambient Temperature

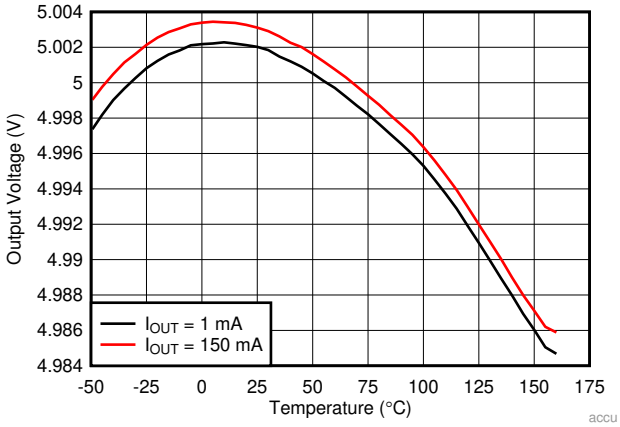
Typical Characteristics (接下页)

at T_J = –40°C to +150°C, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



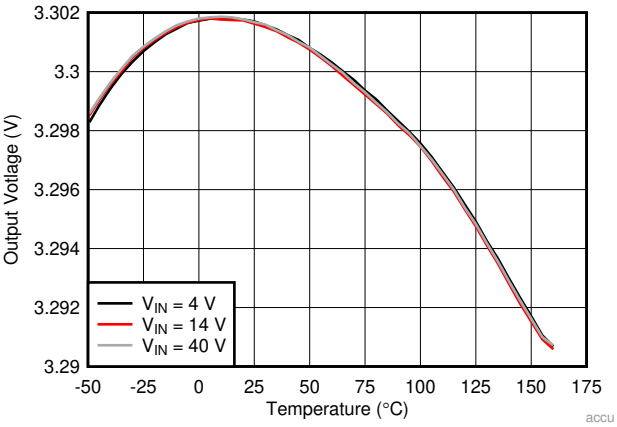
V_{OUT} = 3.3 V

图 7. Dropout Voltage vs Ambient Temperature



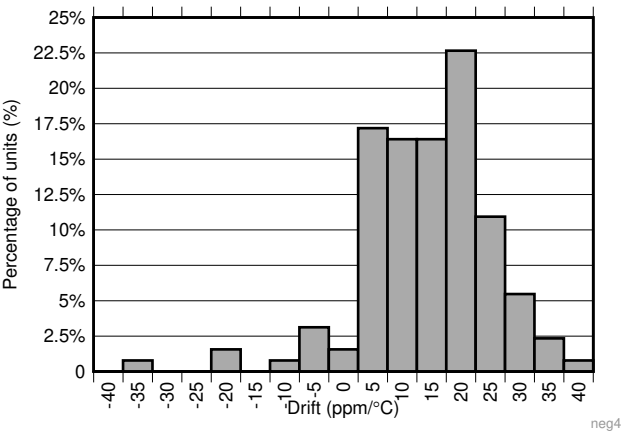
V_{OUT} = 5 V

图 8. Output Voltage vs Ambient Temperature



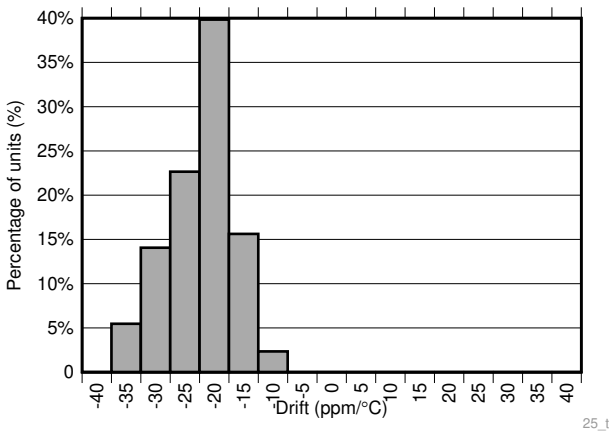
V_{OUT} = 3.3 V, I_{OUT} = 1 mA

图 9. Output Voltage vs Ambient Temperature



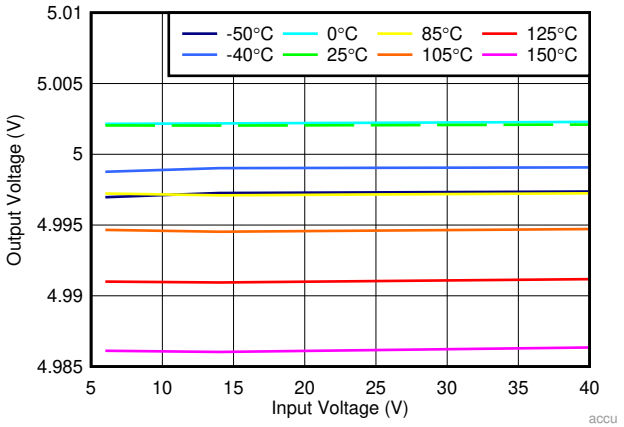
3.3-V and 5-V options, I_{OUT} = 1 mA

图 10. Temperature Drift Histogram (–40°C to +25°C)



3.3-V and 5-V options, I_{OUT} = 1 mA

图 11. Temperature Drift Histogram (25ºC to 150ºC)



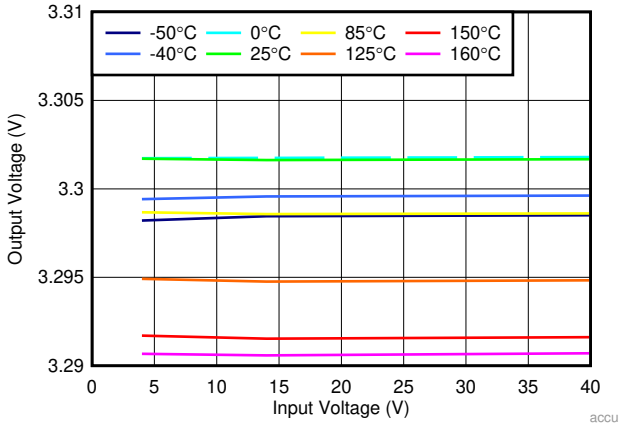
V_{OUT} = 5 V, I_{OUT} = 1 mA

图 12. Output Voltage vs Input Voltage

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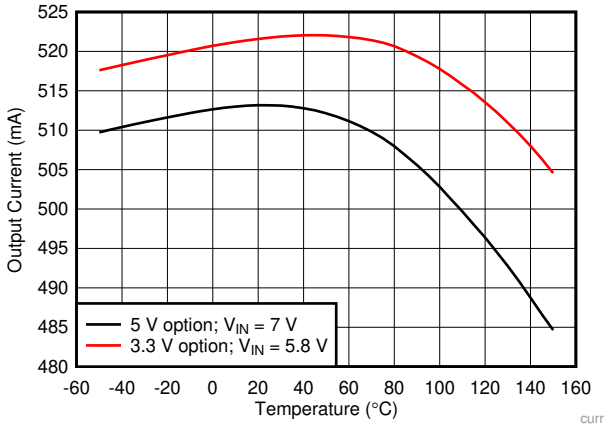
Typical Characteristics (接下页)

at T_J = –40°C to +150°C, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



V_{OUT} = 3.3 V, I_{OUT} = 1 mA

图 13. Output Voltage vs Input Voltage



V_{OUT} is shorted to 90% × $V_{OUT(NOM)}$

图 14. Output Current Limit vs Ambient Temperature

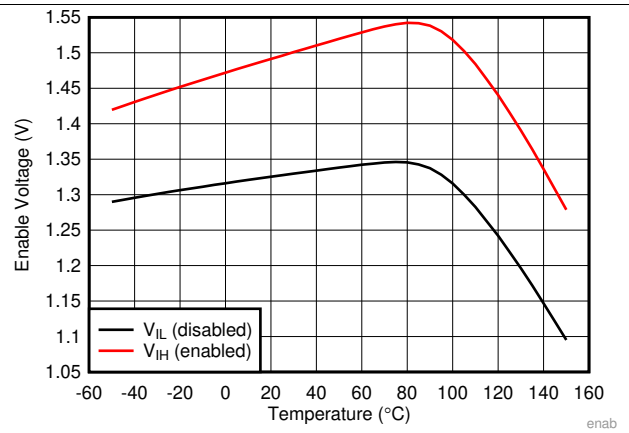


图 15. Enable Voltage vs Ambient Temperature

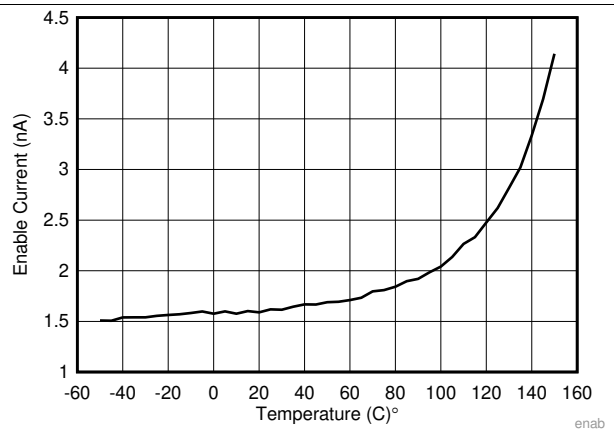


图 16. Enable Current vs Ambient Temperature

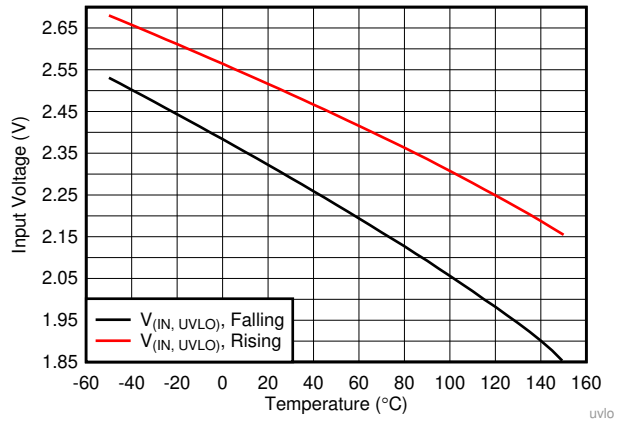
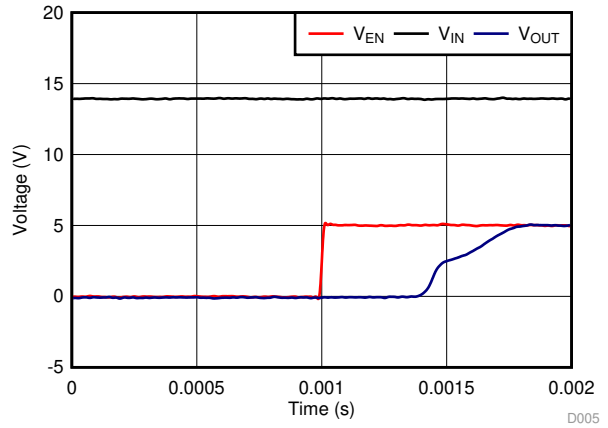


图 17. UVLO vs Ambient Temperature

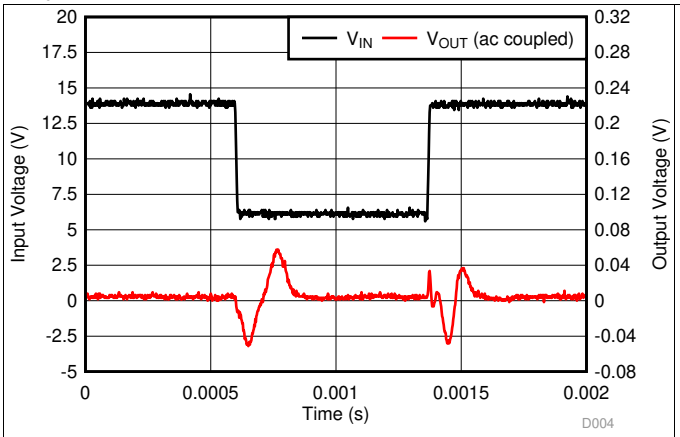


V_{OUT} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1 µF

图 18. Startup with enable

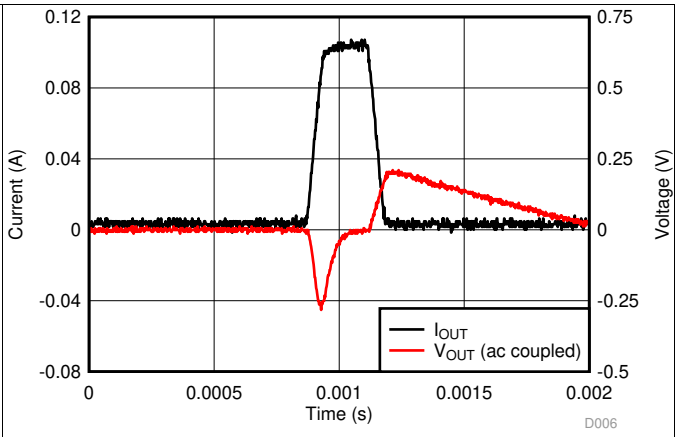
Typical Characteristics (接下页)

at T_J = –40°C to +150°C, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



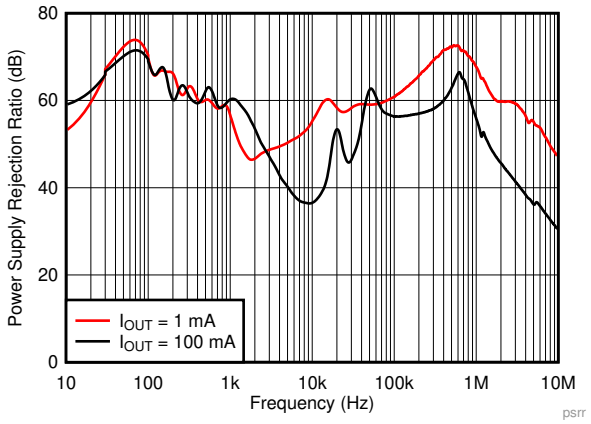
V_{OUT} = 3.3 V, C_{IN} = 0 µF, C_{OUT} = 1 µF,
I_{OUT} = 100 mA, Slew rate = 1 V/µs

图 19. Line Transient



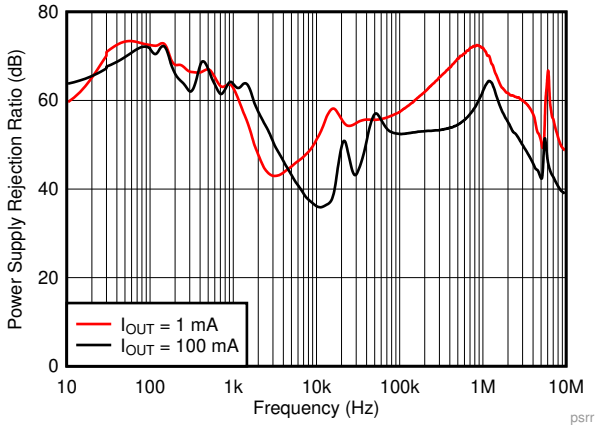
V_{OUT} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1 µF,
I_{OUT} = 1 mA → 100 mA → 1 mA, Slew rate = 1 mA/µs

图 20. Load Transient



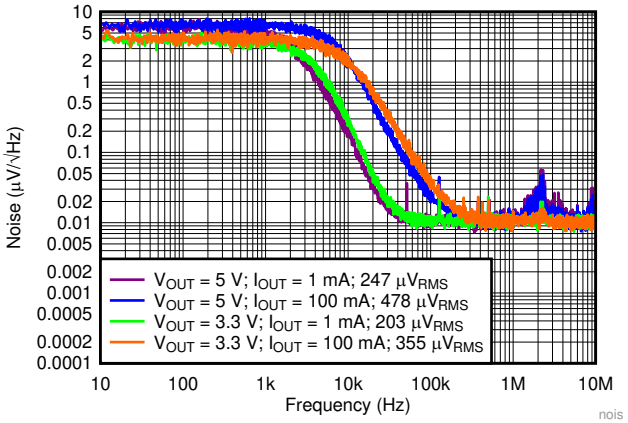
V_{OUT} = 5 V, C_{IN} = 0 µF, C_{OUT} = 10 µF

图 21. PSRR vs Frequency



V_{OUT} = 3.3 V, C_{IN} = 0 µF, C_{OUT} = 10 µF

图 22. PSRR vs Frequency



C_{IN} = 0.1 µF, C_{OUT} = 10 µF

图 23. Noise vs Frequency

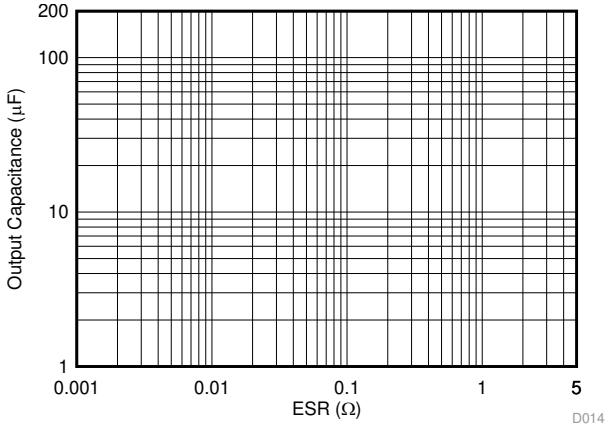


图 24. Output Capacitance vs ESR Stability

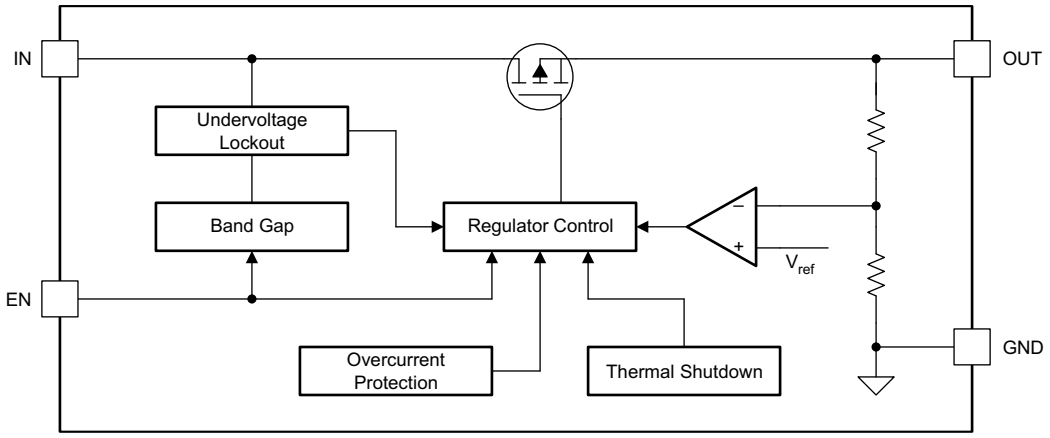
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7 Detailed Description

7.1 Overview

The TPS7B81-Q1 is a 40-V, 150-mA, low-dropout (LDO) linear regulator with ultralow quiescent current. This voltage regulator consumes only 3 µA of quiescent current at light load, and is quite suitable for the automotive always-on application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation on. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold ($V_{(UVLO)}$). This feature ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the thermal shutdown hysteresis, the output turns on again.

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7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. The device does not operate at input voltages below the actual UVLO voltage.

7.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{(Dropout)}$ and $V_{IN} \geq 3$ V	$V_{EN} > V_{IH}$	$I_{OUT} < I_{CL}$	$T_J < 160°C$
Dropout mode	$3V \leq V_{IN} < V_{OUT(nom)} + V_{(Dropout)}$	$V_{EN} > V_{IH}$	$I_{OUT} < I_{CL}$	$T_J < 160°C$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{(IN, UVLO)}$	$V_{EN} < V_{IL}$	—	$T_J > 160°C$

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8 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B81-Q1 is a 150-mA, 40-V, low-dropout (LDO) linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.1.1 Power Dissipation

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be approximated using 公式 1:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air (T_A), according to 公式 2. The equation is rearranged for output current in 公式 3.

$$T_J = T_A + R_{\theta JA} \times P_D \quad (2)$$

$$I_{OUT} = (T_J – T_A) / [R_{\theta JA} \times (V_{IN} – V_{OUT})] \quad (3)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the v table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. Note that for a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

图 25 through 图 30 show the functions of $R_{\theta JA}$ and ψ_{JB} vs. copper area and thickness. These plots are generated with a 101.6 mm x 101.6 mm x 1.6mm PCB of two and four layers. For the four layer board, inner planes use 1 oz copper thickness. Outer layers are simulated with both 1 oz and 2 oz copper thickness. A 2 x 1 array of thermal vias of 300 µm drill diameter and 25 µm Cu plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

Application Information (接下页)

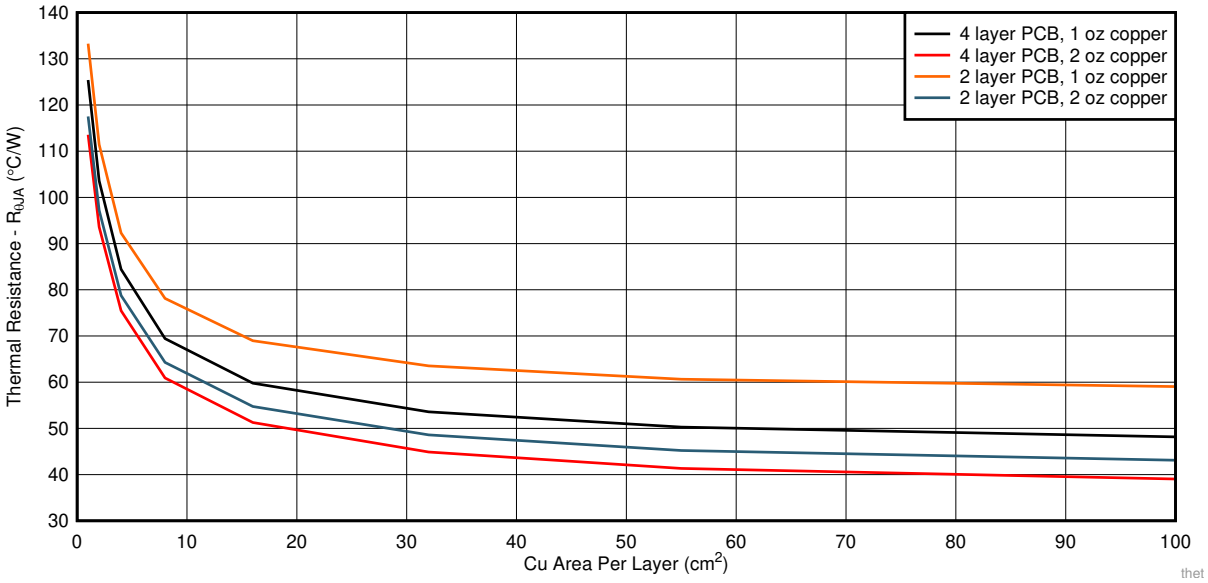


图 25. $R_{\theta JA}$ versus Cu Area for the WSON (DRV) Package

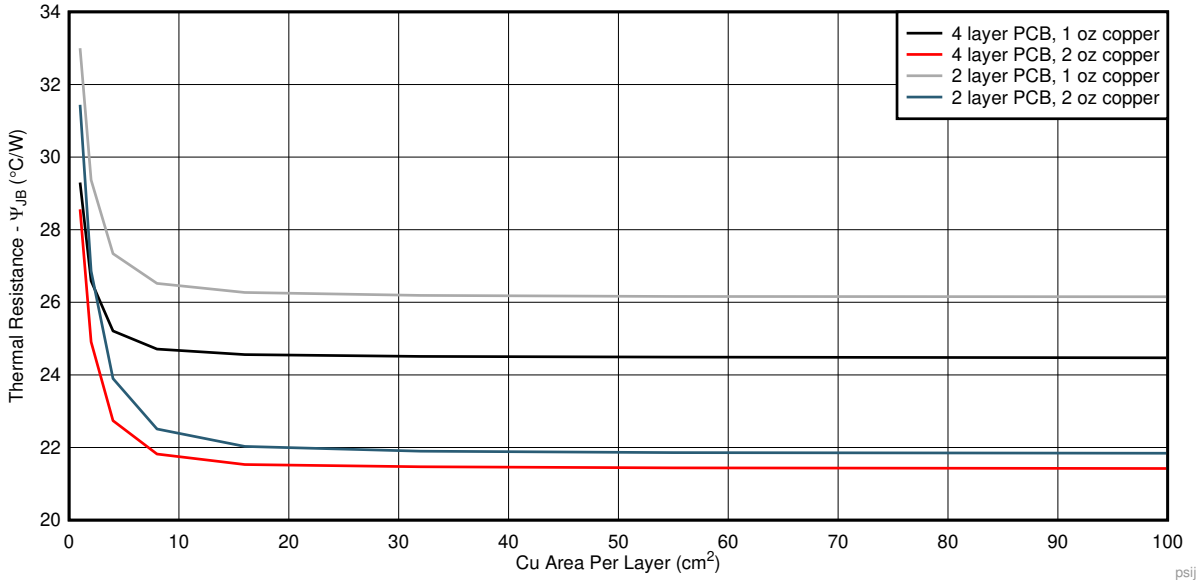


图 26. Ψ_{JB} versus Cu Area for the WSON (DRV) Package

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Application Information (接下页)

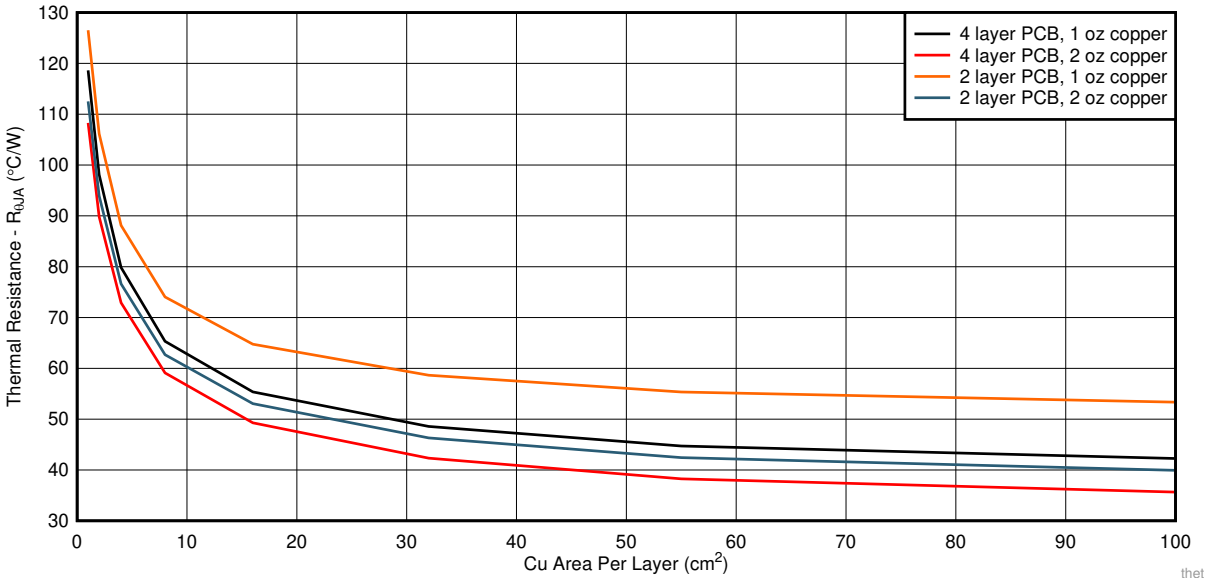


图 27. $R_{\theta JA}$ versus Cu Area for the HVSSOP (DGN) Package

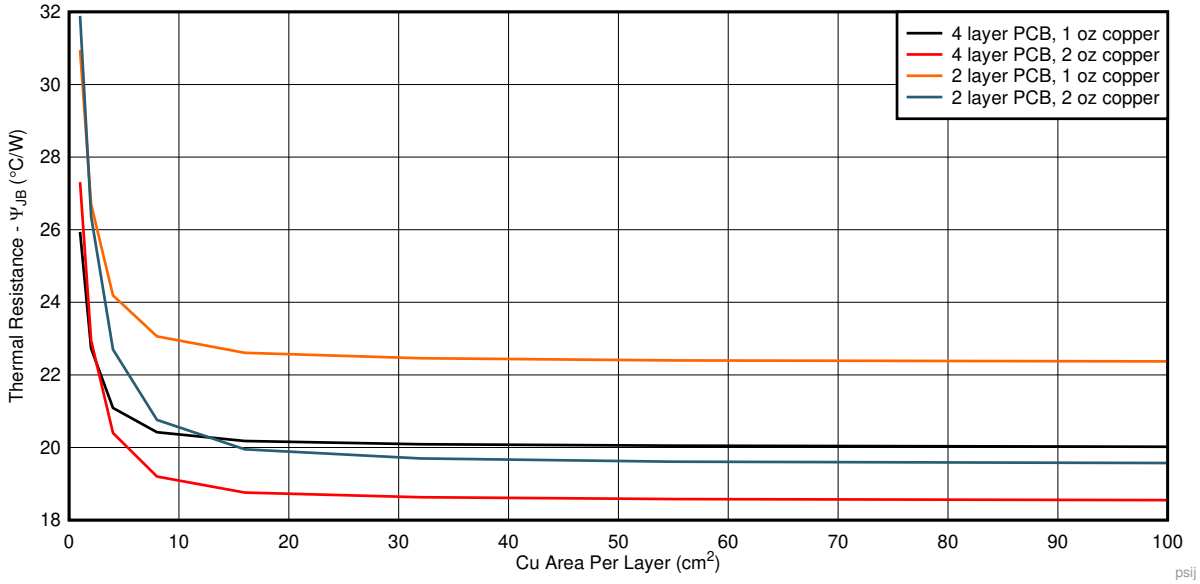


图 28. ψ_{JB} versus Cu Area for the HVSSOP (DGN) Package

Application Information (接下页)

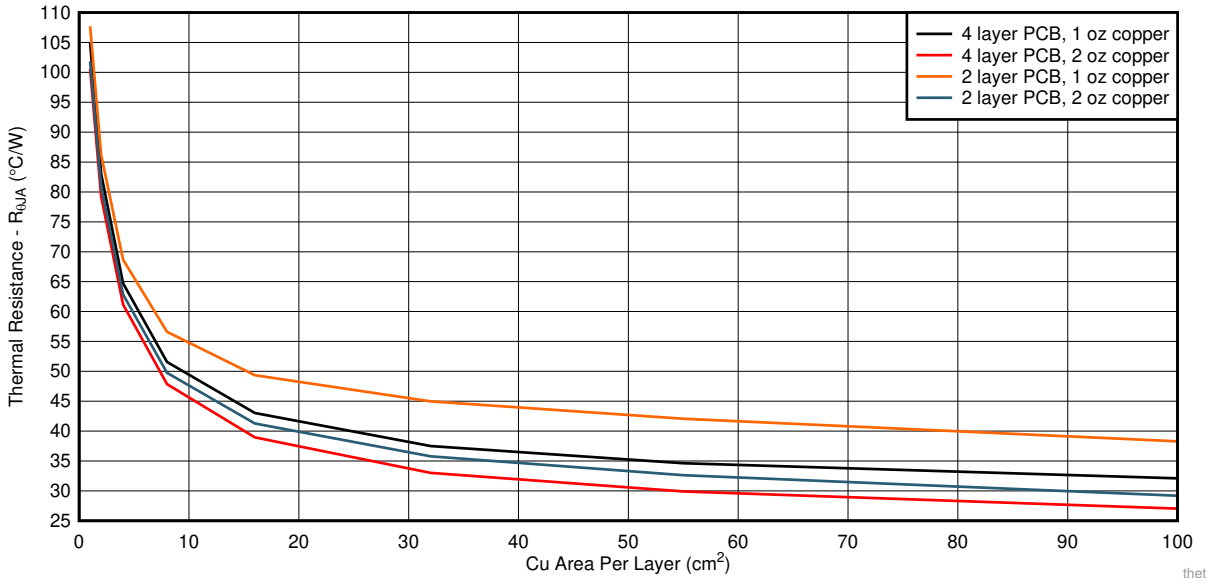


图 29. $R_{\theta JA}$ versus Cu Area for the TO-252 (KVU) Package

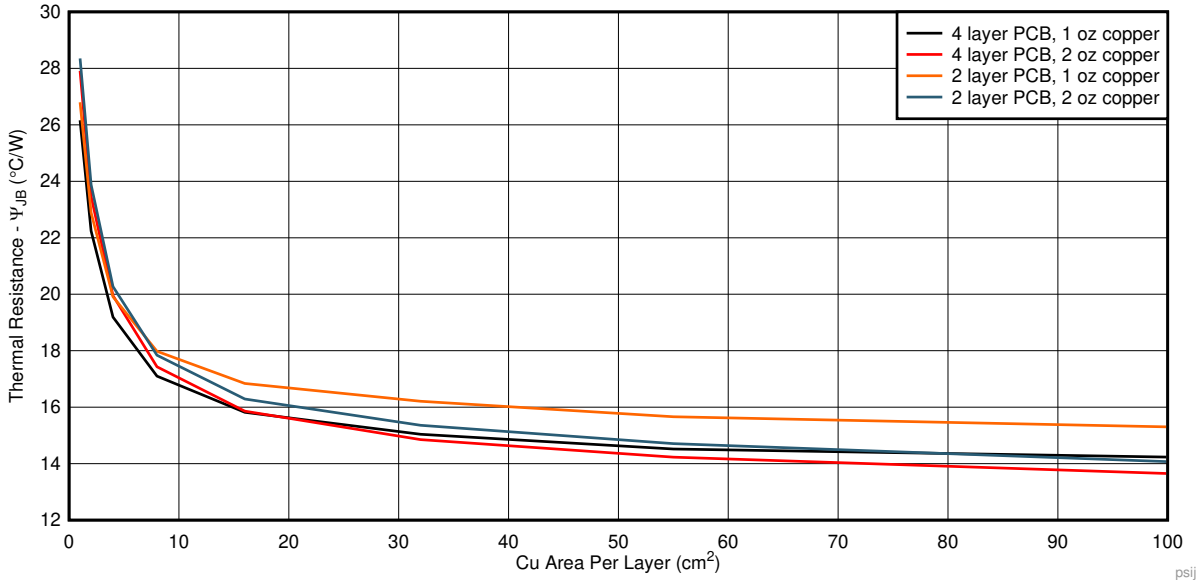


图 30. Ψ_{JB} versus Cu Area for the TO-252 (KVU) Package

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Application Information (接下页)

8.1.1.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with 公式 4.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in 公式 1
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (4)

8.2 Typical Application

图 31 shows a typical application circuit for the TPS7B81-Q1. Different external component values can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-equivalent series resistance (ESR) ceramic capacitor with an X5R- or X7R-type dielectric.

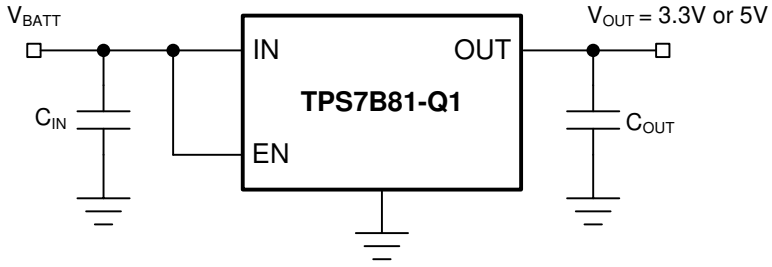


图 31. TPS7B81-Q1 Typical Application Schematic

8.2.1 Design Requirements

Use the parameters listed in 表 2 for this design example.

表 2. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	150 mA maximum

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-µF to 22-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B81-Q1, the device requires an output capacitor with a value in the range from 1 µF to 200 µF and with an ESR range between 0.001 Ω and 5 Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.3 Application Curve

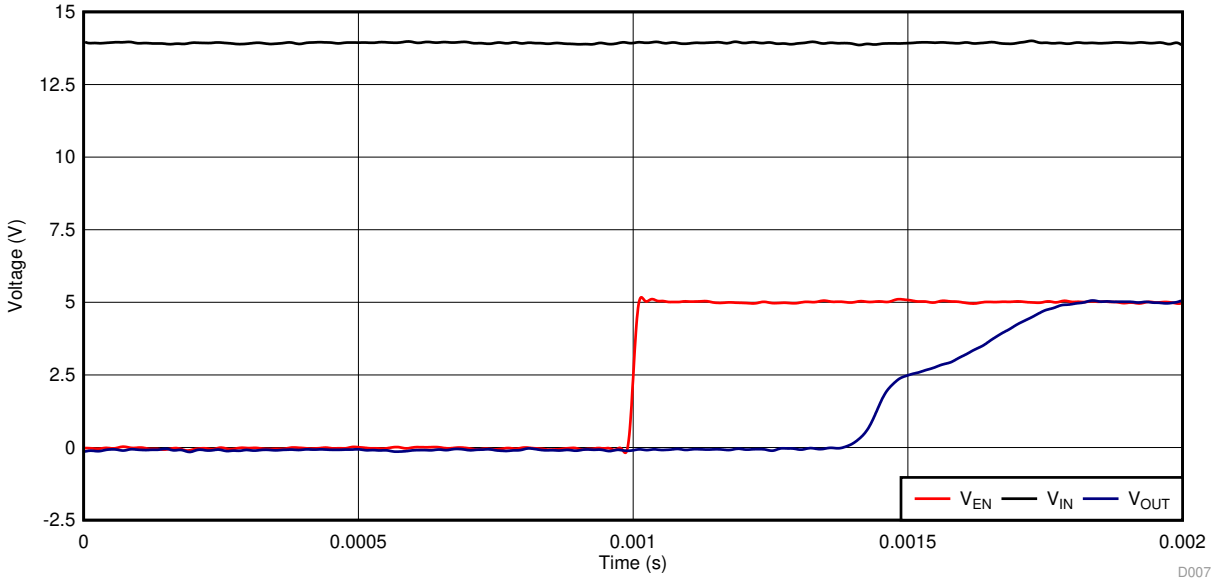


图 32. TPS7B81-Q1 Power-Up Waveform (5 V)

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 3 V to 40 V. The input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B81-Q1, TI recommends adding a capacitor with a value greater than or equal to 10 µF with a 0.1-µF bypass capacitor in parallel at the input.

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10 Layout

10.1 Layout Guidelines

Layout is an important step for LDO power supplies, especially for high-voltage and large-output-current supplies. If the layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitations. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and put enough thermal vias on the copper under the thermal pad. 图 33 shows an example layout.

10.2 Layout Example

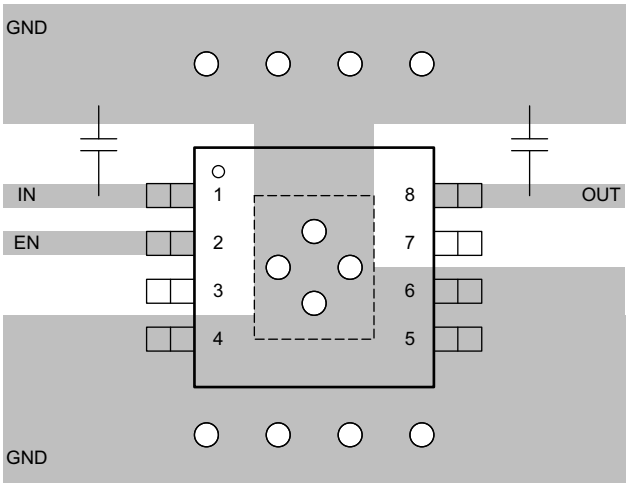


图 33. TPSB81-Q1 Example Layout Diagram

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8125QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	26GX	Samples
TPS7B8133QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1VTX	Samples
TPS7B8133QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1X2H	Samples
TPS7B8133QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8133Q1	Samples
TPS7B8150QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1VUX	Samples
TPS7B8150QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1WNH	Samples
TPS7B8150QKVURQ1	ACTIVE	TO-252	KVU	5	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	7B8150Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS7B81-Q1 :

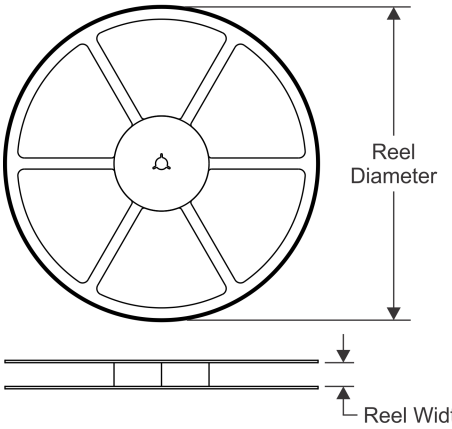
- Catalog : TPS7B81

NOTE: Qualified Version Definitions:

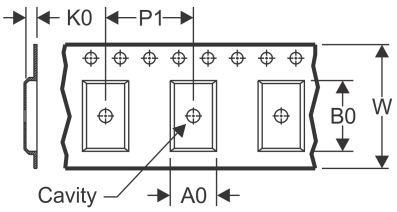
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

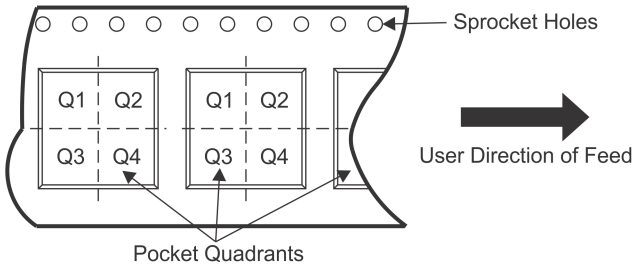


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

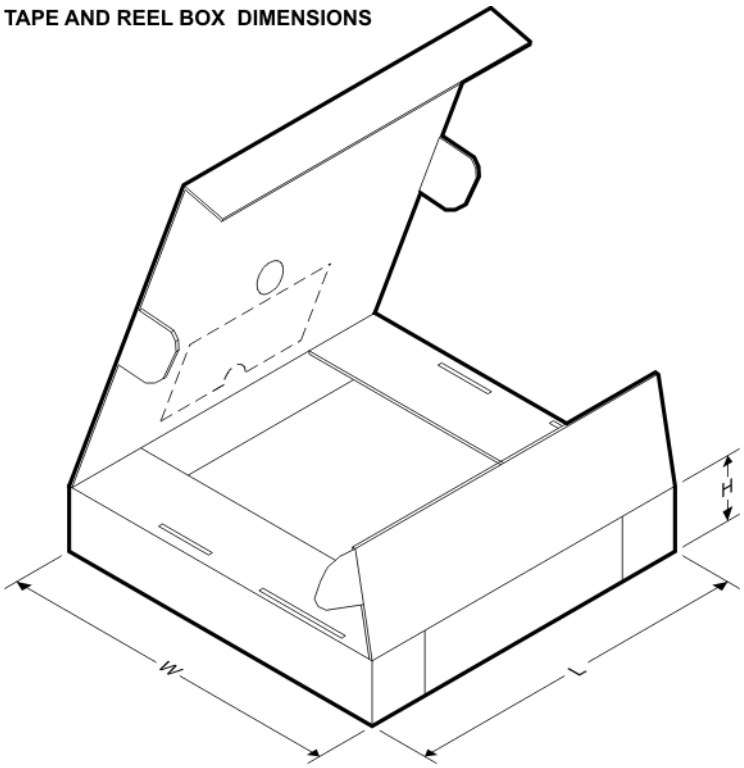
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8125QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8133QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8133QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8133QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8150QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8150QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8150QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

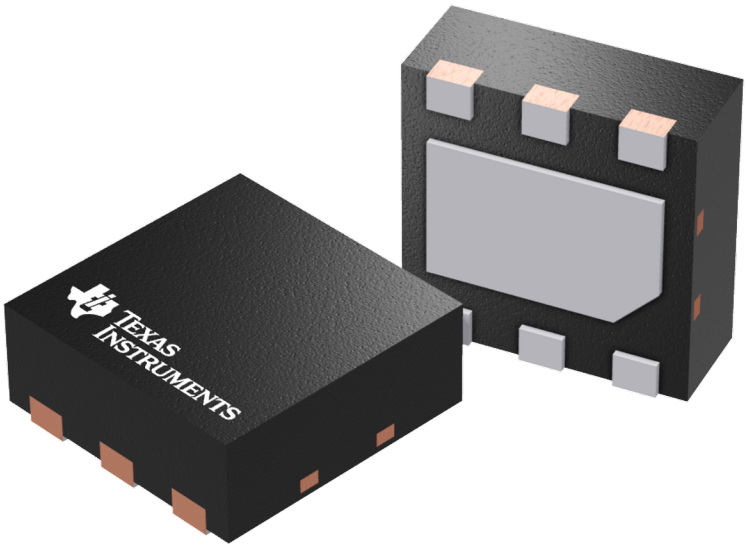


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8125QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8133QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8133QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8133QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8150QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8150QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8150QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



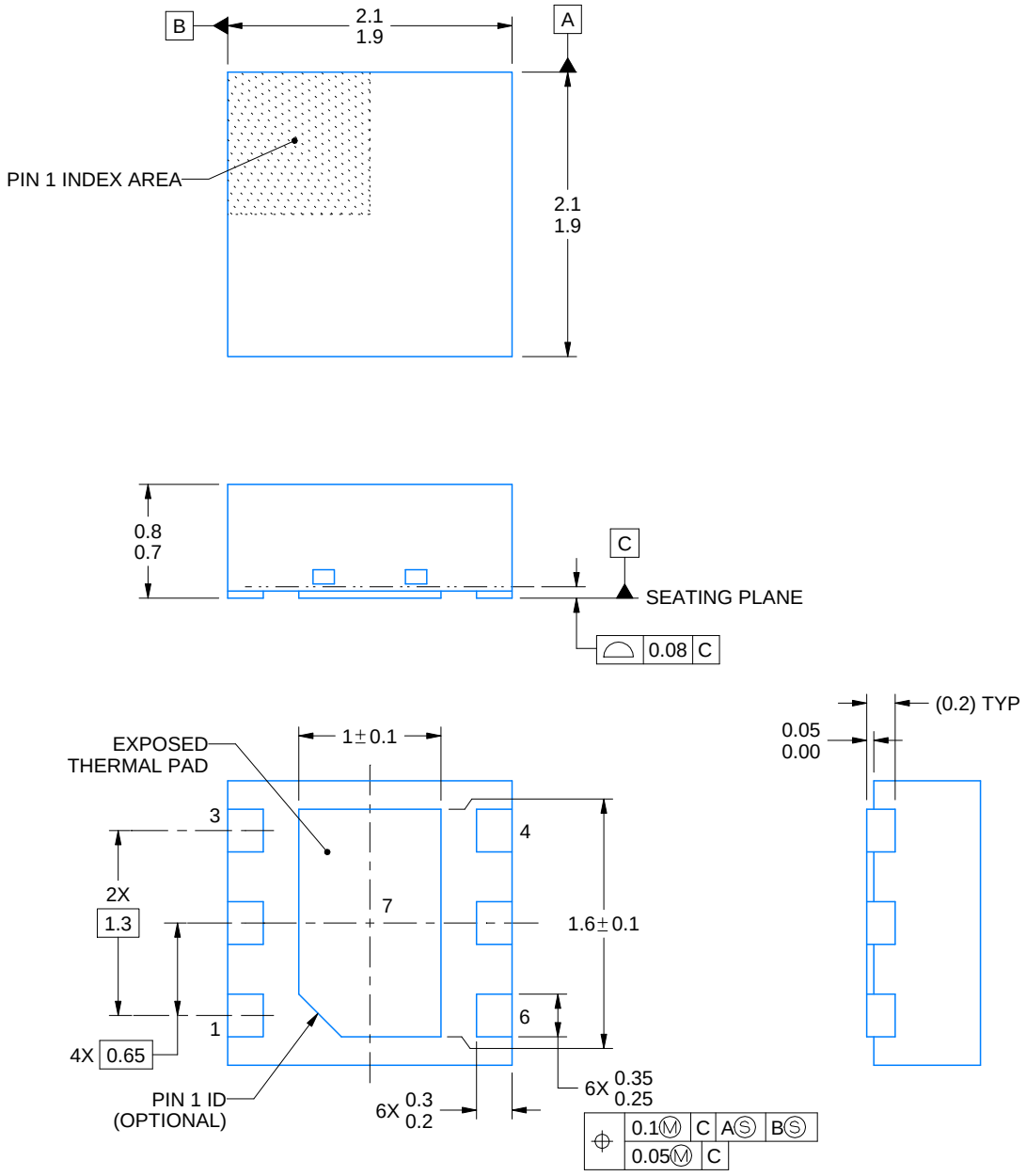
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

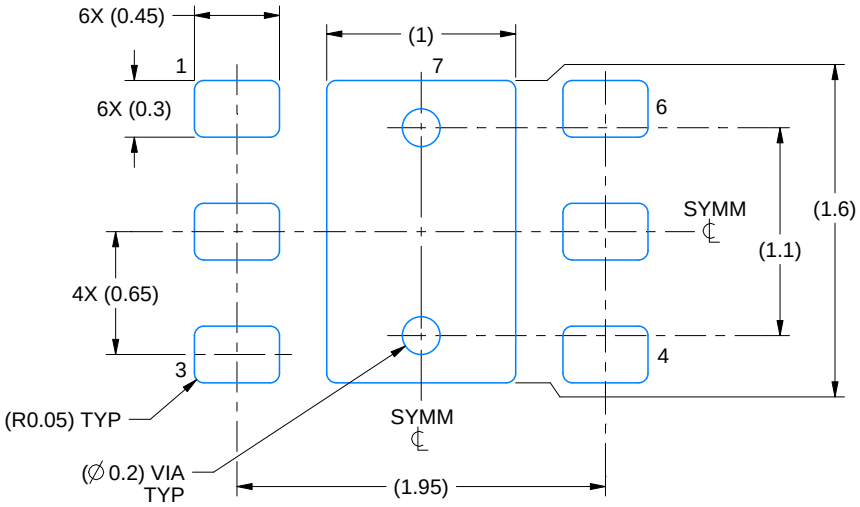
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

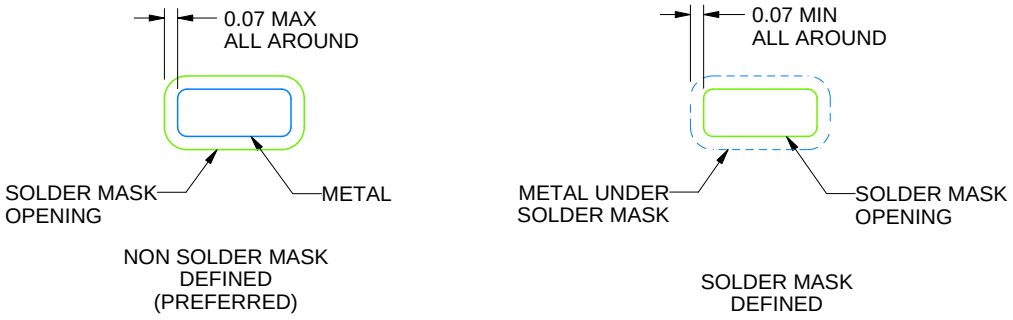


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

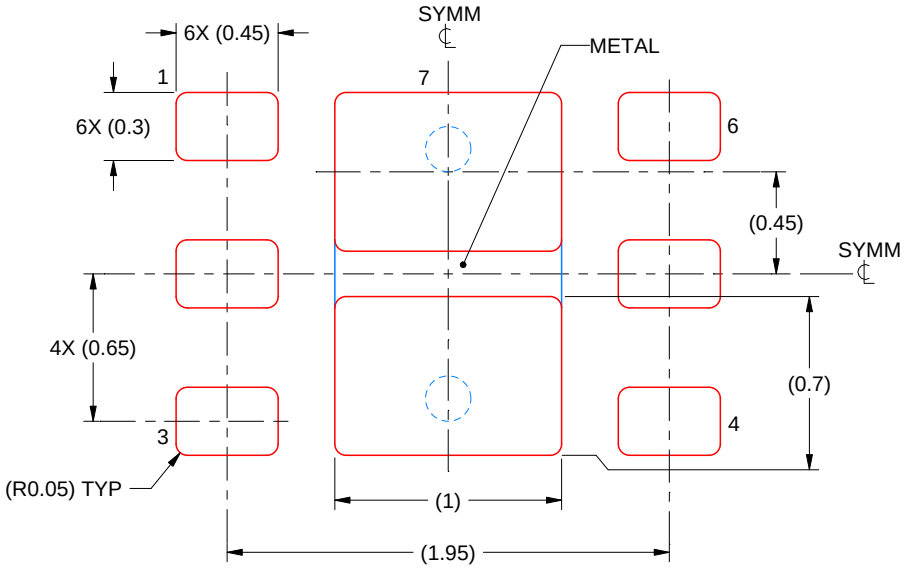
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

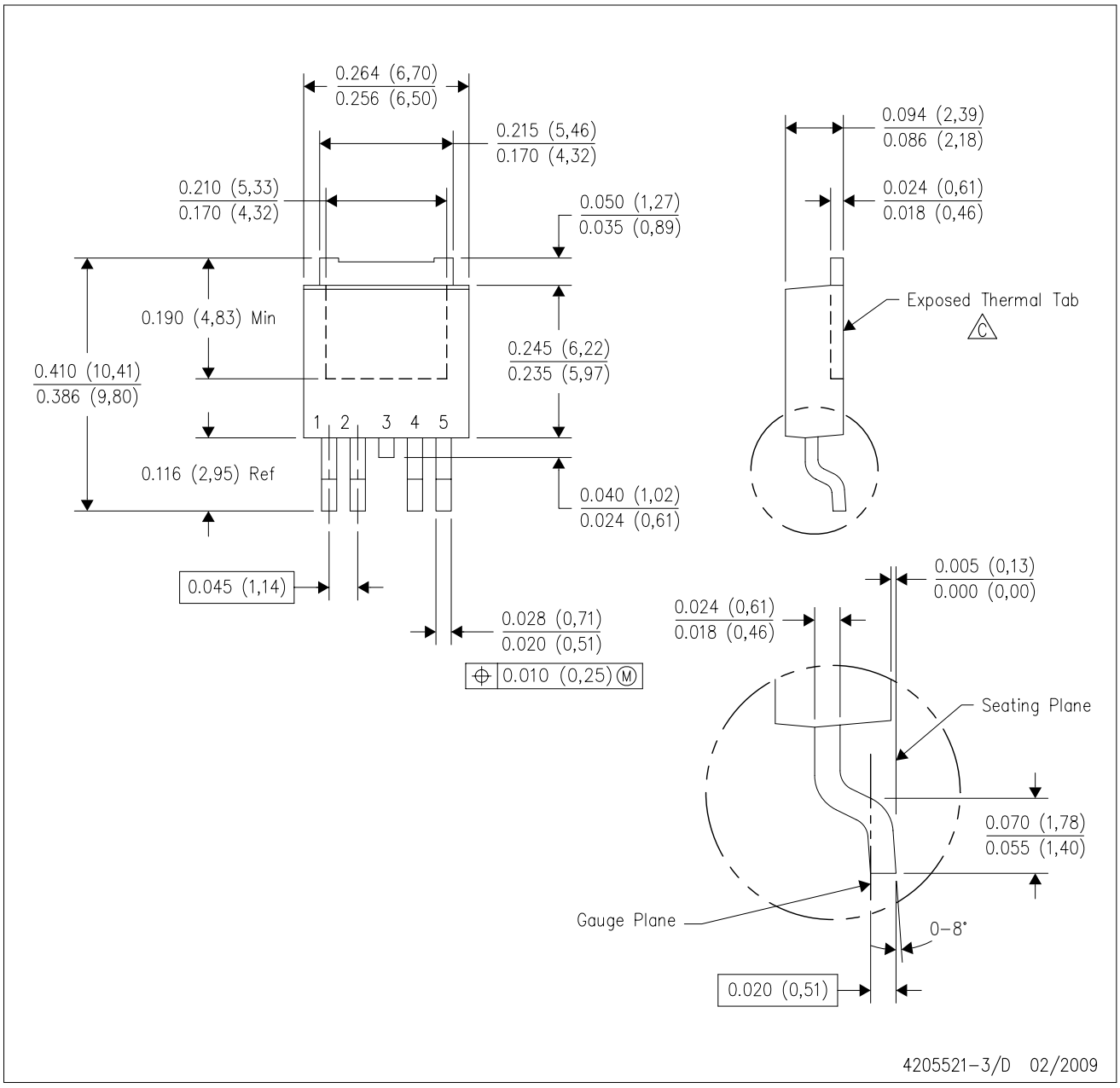
EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

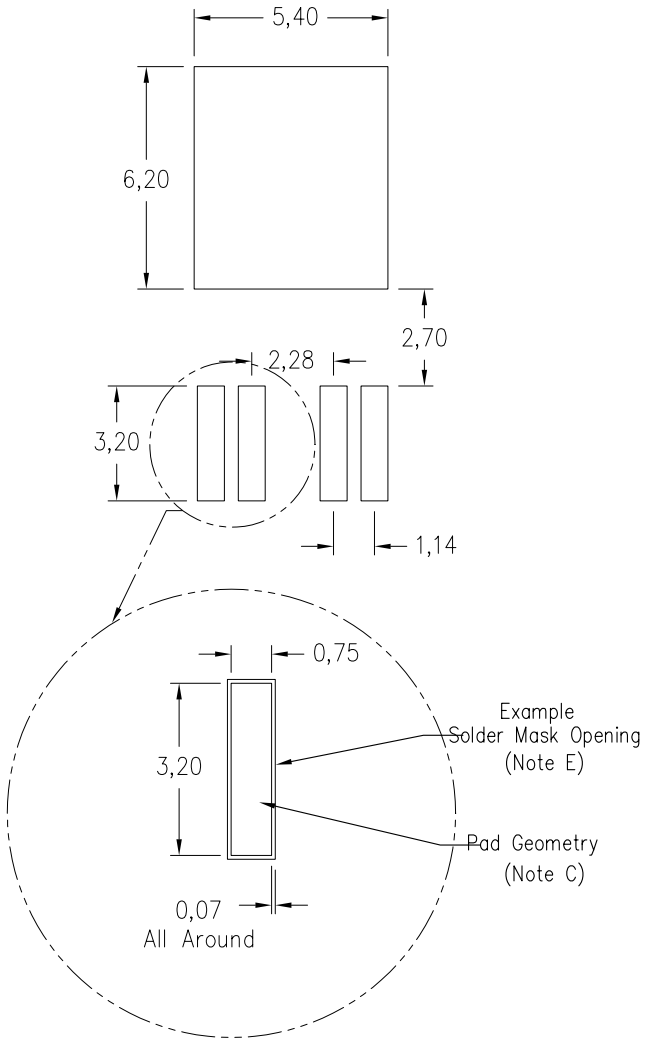
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



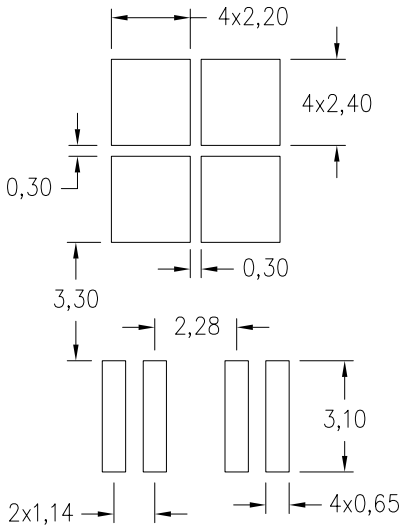
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

GENERIC PACKAGE VIEW

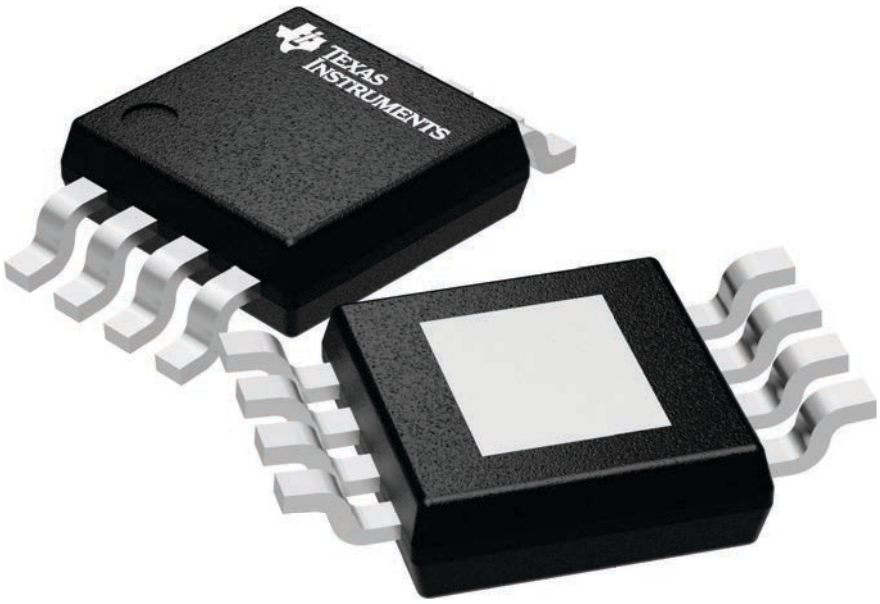
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

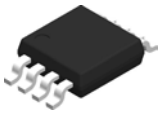
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

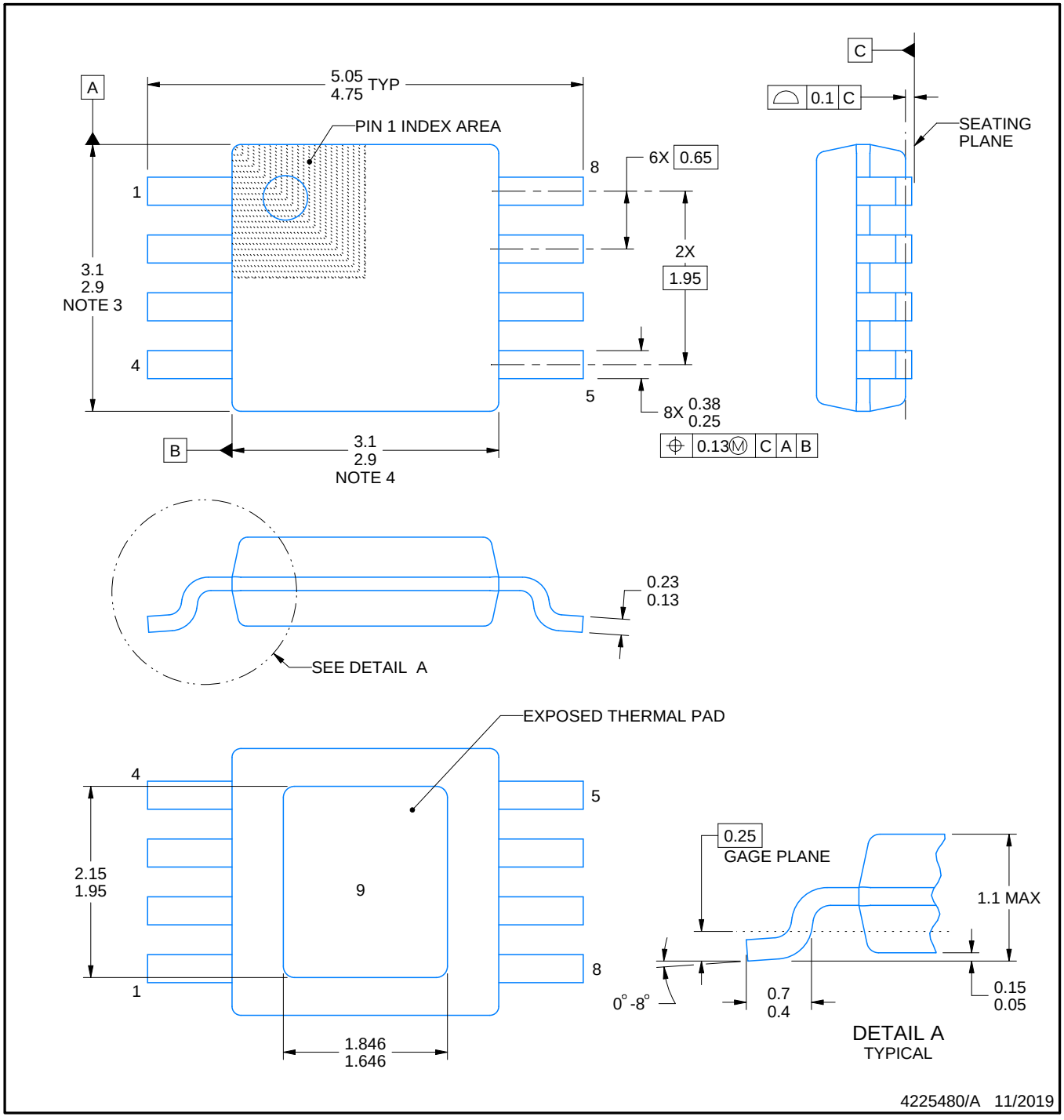
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

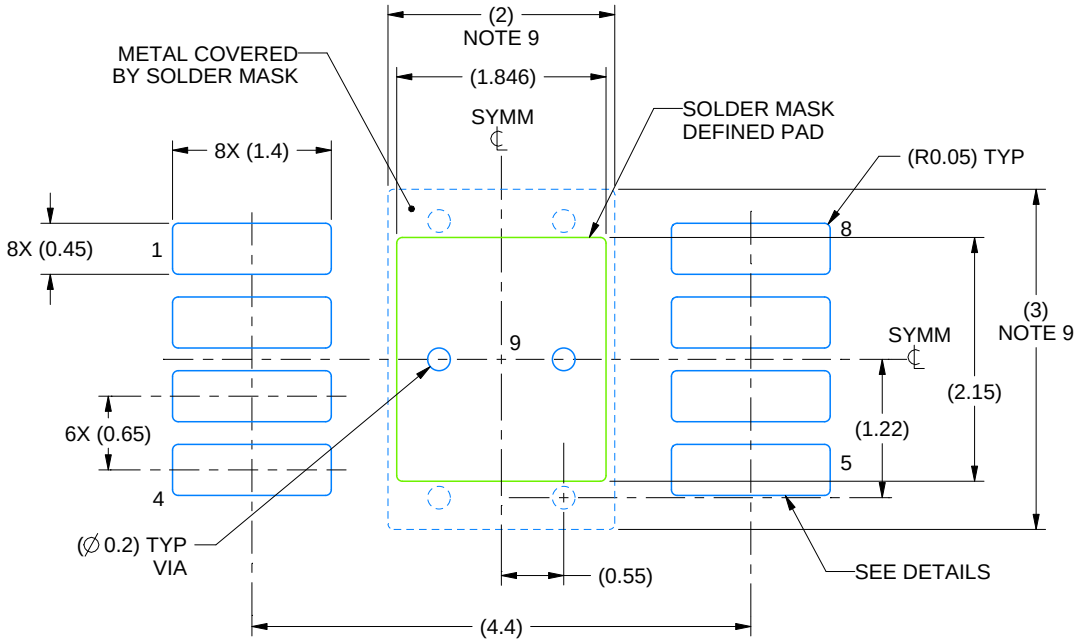
SMALL OUTLINE PACKAGE



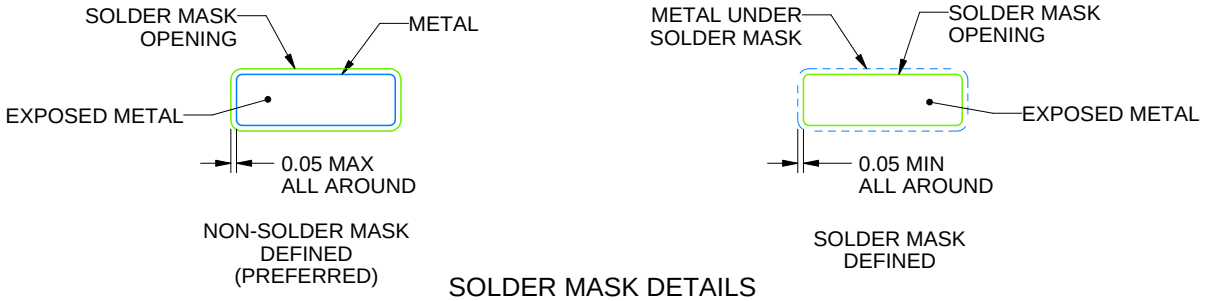
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

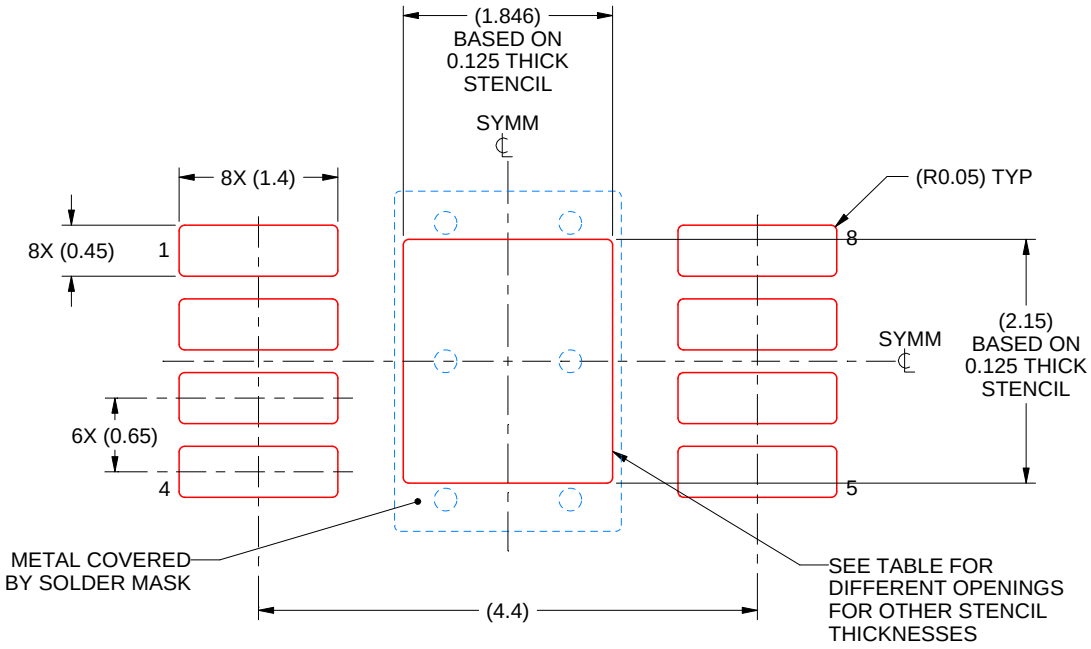


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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