

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DESCRIPTION

This 20-bit bus-interface D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{1OE}$ or $\overline{2OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{OE}$ does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16841 is characterized for operation from -40°C to 85°C.

**DGG OR DL PACKAGE
(TOP VIEW)**

$\overline{1OE}$	1	56	1LE
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
V_{CC}	7	50	V_{CC}
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V_{CC}	22	35	V_{CC}
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
$\overline{2OE}$	28	29	2LE



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SN74ALVCH16841

20-BIT BUS-INTERFACE D-TYPE LATCH

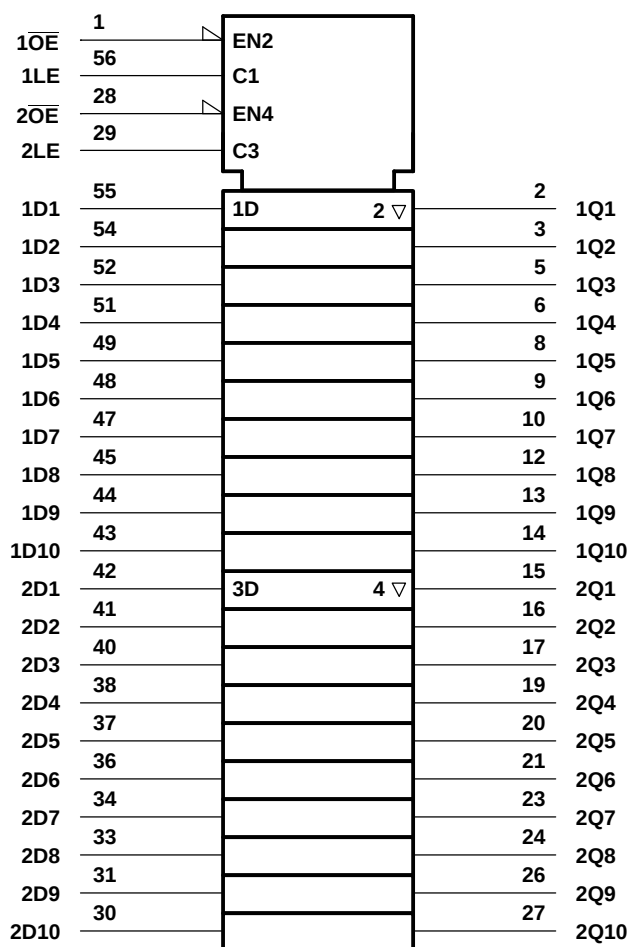
WITH 3-STATE OUTPUTS

SCES043E—JULY 1995—REVISED SEPTEMBER 2004

FUNCTION TABLE
(each 10-bit latch)

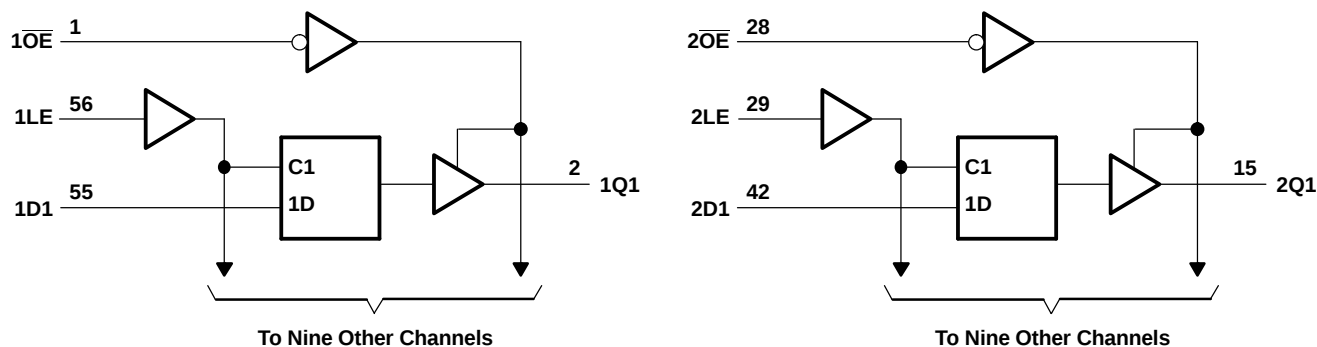
INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC SYMBOL⁽¹⁾



⁽¹⁾ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
V _I	Input voltage range ⁽²⁾		-0.5	4.6	V
V _O	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through each V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package		81	°C/W
		DL package		74	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

SN74ALVCH16841
20-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCES043E–JULY 1995–REVISED SEPTEMBER 2004

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-12	
		V _{CC} = 2.7 V		-12	
		V _{CC} = 3 V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		12	
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V
		I _{OH} = -4 mA	1.65 V	1.2			
		I _{OH} = -6 mA	2.3 V	2			
	I _{OH} = -12 mA	2.3 V	1.7				
		2.7 V	2.2				
		3 V	2.4				
		I _{OH} = -24 mA	3 V	2			
V _{OL}		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 6 mA	2.3 V			0.4	
	I _{OL} = 12 mA	2.3 V			0.7		
		2.7 V			0.4		
		I _{OL} = 24 mA	3 V			0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{I(hold)}		V _I = 0.58 V	1.65 V	25			μA
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V	2.3 V	-45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		V _I = 0 to 3.6 V ⁽²⁾	3.6 V			±500	
I _{OZ}		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4.5			pF
	Data inputs			6.5			
C _o	Outputs	V _O = V _{CC} or GND	3.3 V	7			pF

(1) All typical values are at $V_{CC} = 3.3\ V$, $T_A = 25^\circ C$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		$V_{CC} = 1.8\ V$		$V_{CC} = 2.5\ V \pm 0.2\ V$		$V_{CC} = 2.7\ V$		$V_{CC} = 3.3\ V \pm 0.3\ V$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low	(1)		3.3		3.3		3.3		ns
t_{su}	Setup time, data before $LE\uparrow$	(1)		0.9		0.7		1.1		ns
t_h	Hold time, data after $LE\uparrow$	(1)		1.2		1.5		1.1		ns

(1) This information was not available at the time of publication.

SN74ALVCH16841

20-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCES043E–JULY 1995–REVISED SEPTEMBER 2004

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D	Q	(1)	1	5	4.7		1.2	3.9	ns
	LE		(1)	1	5.6	5.1		1	4.3	
t _{en}	$\overline{OE}$	Q	(1)	1	6.2	6		1	4.9	ns
t _{dis}	$\overline{OE}$	Q	(1)	1.1	5.3	4.3		1.3	4.1	ns

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

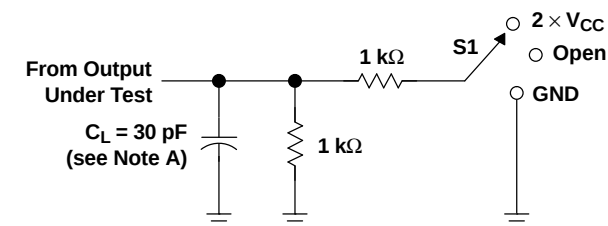
T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	(1)	12	20	pF
		Outputs disabled		(1)	1	3	

(1) This information was not available at the time of publication.

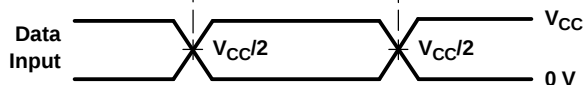
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8 \text{ V}$

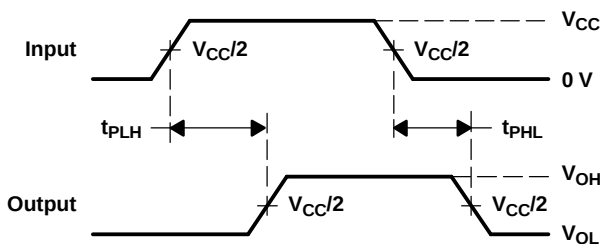


LOAD CIRCUIT

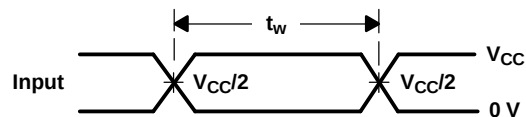
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



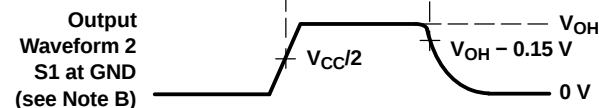
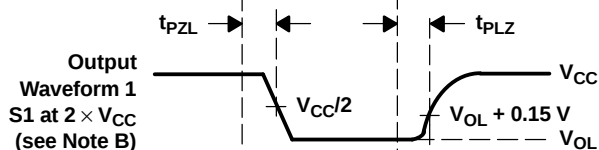
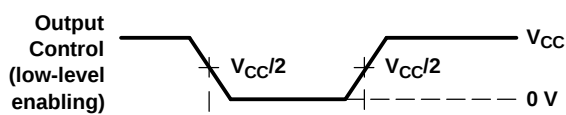
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

SN74ALVCH16841

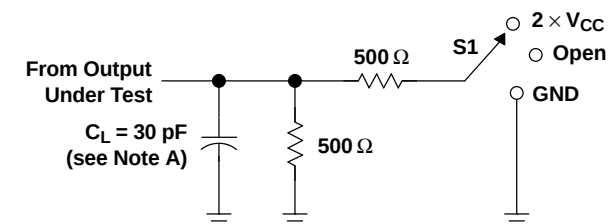
20-BIT BUS-INTERFACE D-TYPE LATCH

WITH 3-STATE OUTPUTS

SCES043E—JULY 1995—REVISED SEPTEMBER 2004

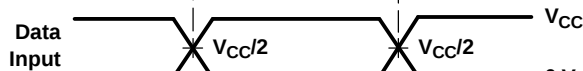
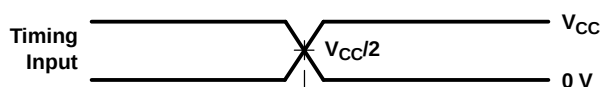
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

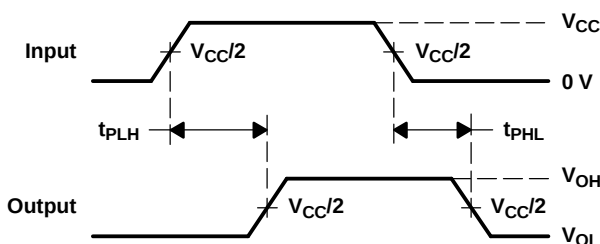


LOAD CIRCUIT

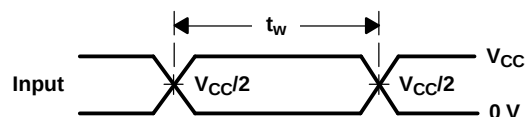
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



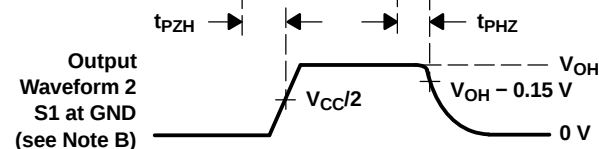
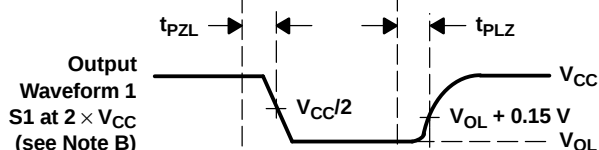
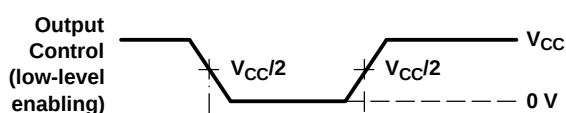
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



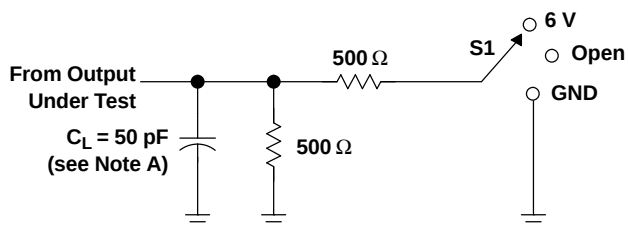
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

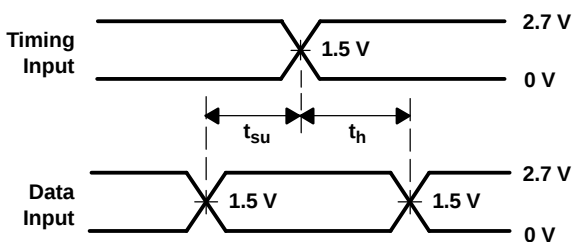
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

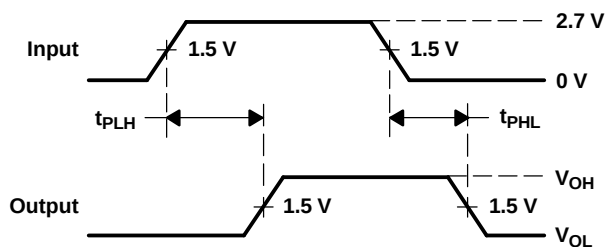
$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

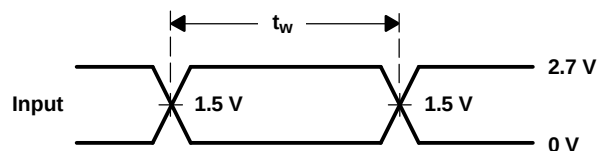


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

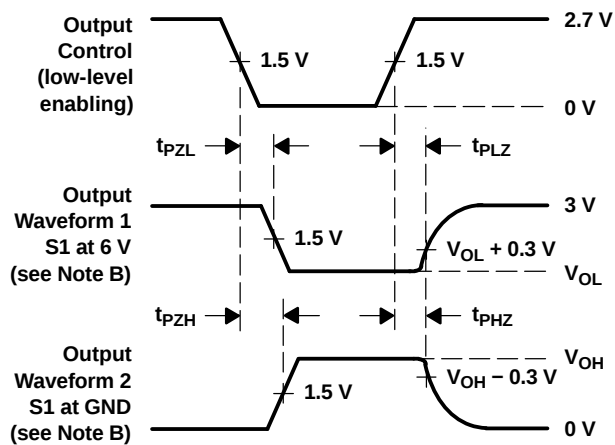


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCH16841DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16841	Samples
SN74ALVCH16841DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16841	Samples
SN74ALVCH16841DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16841	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

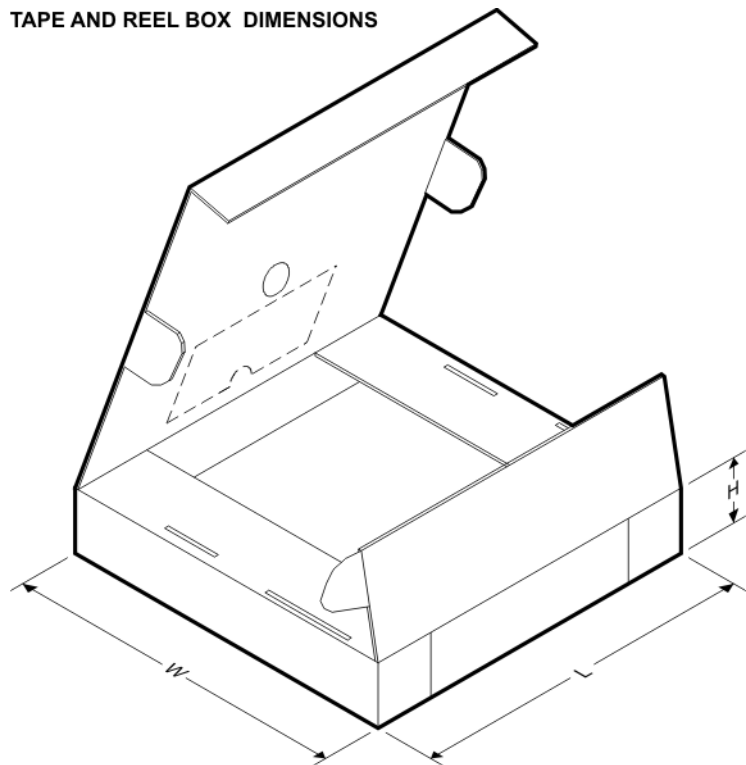
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16841DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16841DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16841DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ALVCH16841DLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE

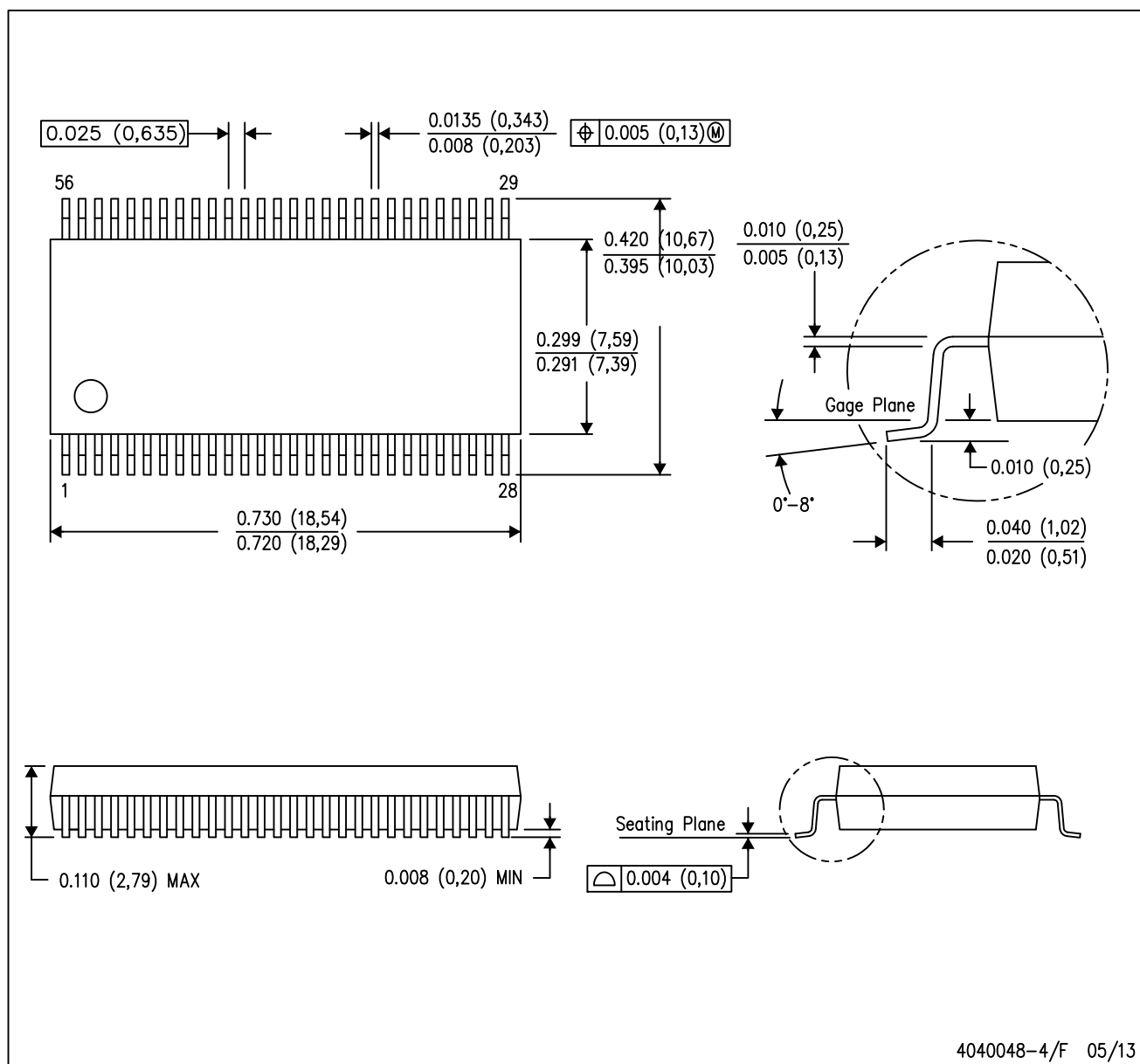


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALVCH16841DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

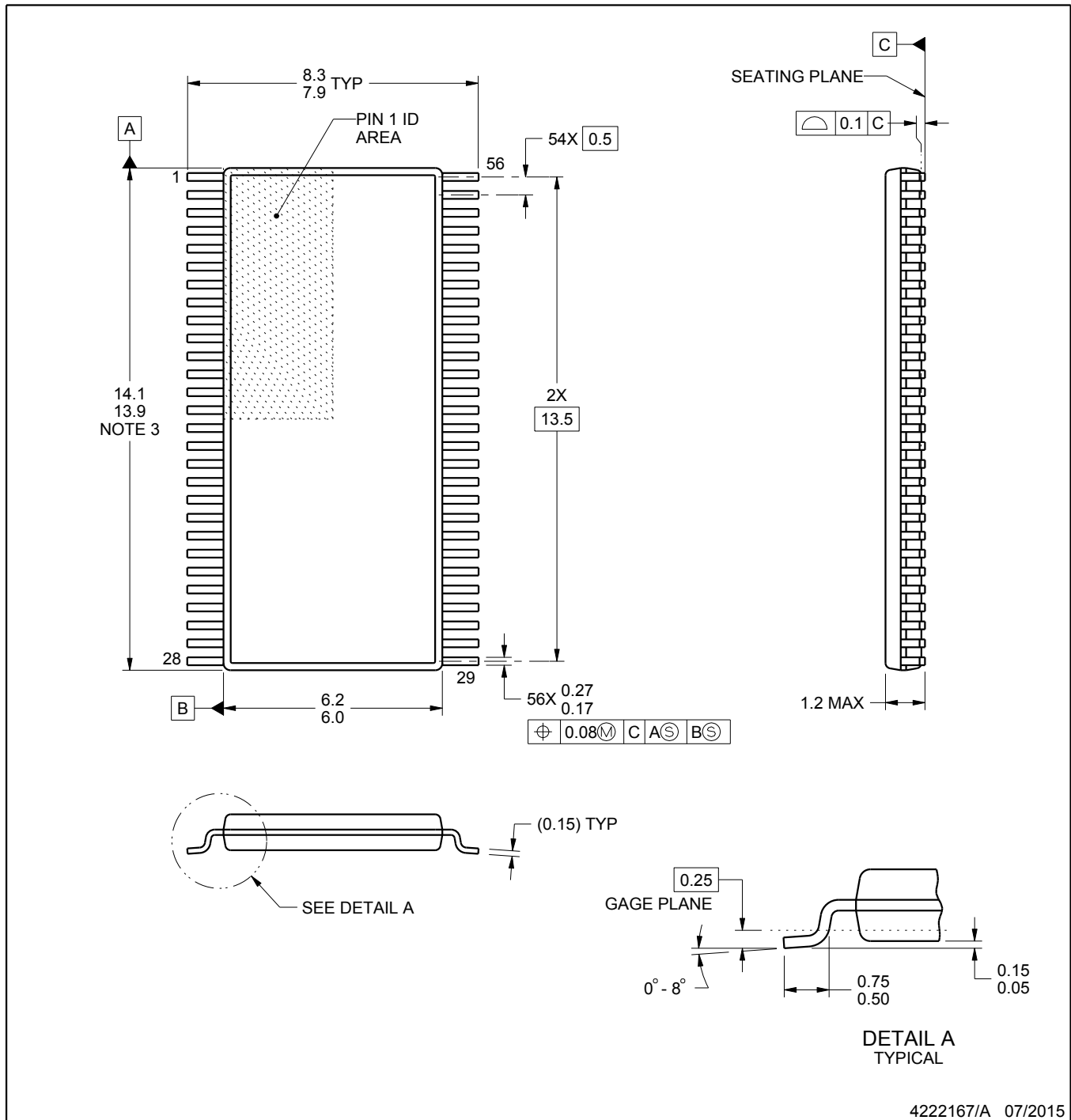
DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118



4222167/A 07/2015

NOTES:

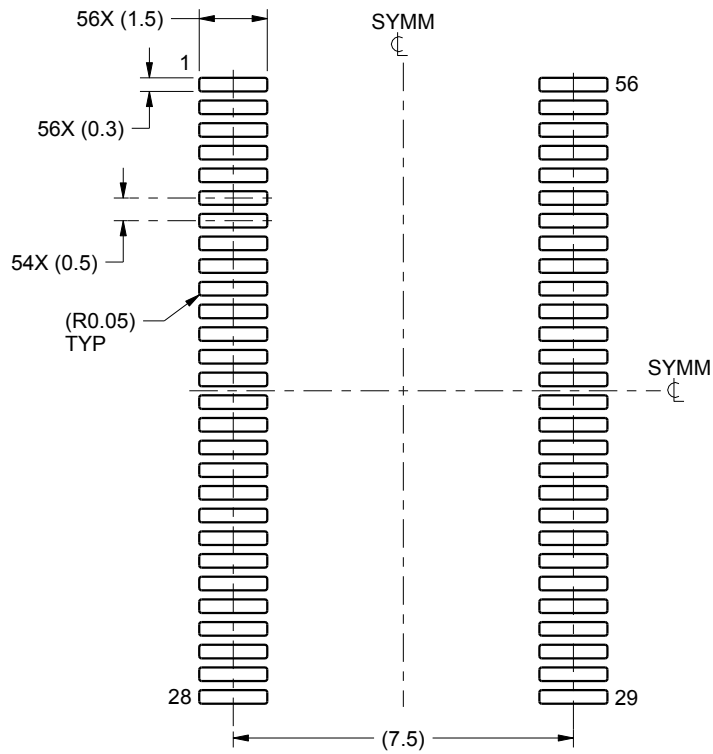
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

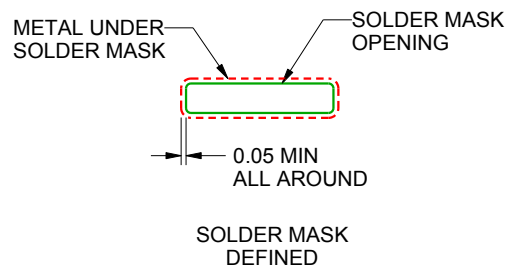
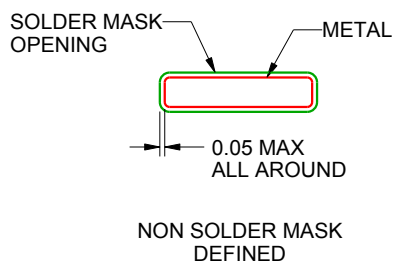
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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