CDC3RL02 低相位噪声双通道时钟扇出缓冲器

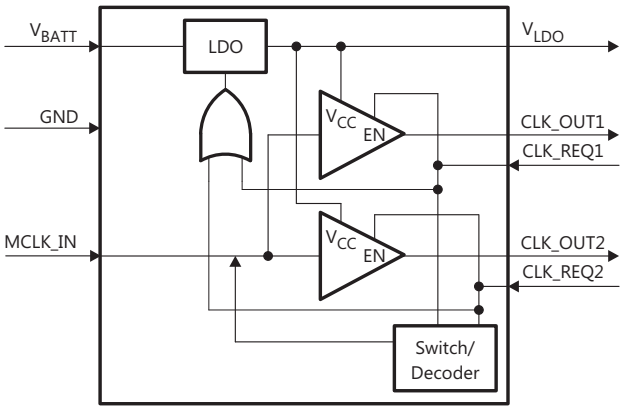
1 特性

- 低附加噪声：
  - 10kHz 偏移相位噪声时为 –149dBc/Hz
  - 0.37ps (RMS) 输出抖动
- 限制输出转换率可降低 EMI（对于 10pF 至 50pF 的负载，上升/下降时间为 1ns 至 5ns）
- 自适应输出级控制反射
- 稳压 1.8V 外部可用 I/O 电源
- 超小型 8 凸点 YFP 0.4mm 间距 WCSP（0.8mm × 1.6mm）
- ESD 性能超过 JESD 22
  - 2000V 人体放电模型 (A114-A)
  - 1000V 带电器件模型（JESD22-C101-A III 级）

2 应用

- 手机
- 全球定位系统 (GPS)
- 无线 LAN
- FM 无线电
- WiMAX
- W-BT

简化框图



3 说明

CDC3RL02 是一款双通道时钟扇出缓冲器，非常适用于需要时钟缓冲且具有最小附加相位噪声和扇出功能的便携式终端设备（如手机）。该器件将温度补偿晶体振荡器 (TCXO) 等单个主时钟缓冲至多个外设。该器件具有两个时钟请求输入（CLK_REQ1 和 CLK_REQ2），其中每个输入均支持单个时钟输出。

CDC3RL02 在主时钟输入 (MCLK_IN) 处接受方波或正弦波，无需交流耦合电容器。可接受的最小正弦波为 0.3V 信号（峰峰值）。CDC3RL02 旨在提供极小的通道间偏差、附加输出抖动和附加相位噪声。自适应时钟输出缓冲器可在宽电容负荷范围内提供受控的转换率，从而更大限度地降低 EMI 辐射、保持信号完整性，并更大限度地减少由时钟分配线上的信号反射造成的振铃效应。

CDC3RL02 具有集成的低压降 (LDO) 稳压器，该稳压器可接受 2.3V 至 5.5V 的输入电压，可输出 1.8 V、50mA。该 1.8V 电源可从外部获得，从而为 TCXO 等外围设备提供稳定电源。

CDC3RL02 采用 0.4mm 间距晶圆级芯片规模 (WCSP) 封装（0.8mm × 1.6mm），并经优化可实现极低的待机电流消耗。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
CDC3RL02	DSBGA (8)	0.80mm × 1.60mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (August 2018) to Revision F — **Page**

- Changed MCLK_IN frequency maximum vale from: 52 MHz to: 54 MHz ... 5

Changes from Revision D (April 2017) to Revision E — **Page**

- Changed V_{LDO} test conditions to V_{IH} conditions in the *Electrical Characteristics* table ... 5
- Added a tablenote to the *Function Table* ... 10
- Added content to the *LDO* section ... 11
- Changed the last sentence in the *Detailed Design Procedure* section ... 12

Changes from Revision C (January 2016) to Revision D — **Page**

- Updated clock request descriptions in the *Pin Functions* table ... 3
- 添加了*接收文档更新通知* 部分 ... 14

Changes from Revision B (December 2015) to Revision C — **Page**

- 添加了*器件比较表* ... 3

Changes from Revision A (September 2015) to Revision B — **Page**

- 已添加 *热性能信息*表、*概述*、*特性* *说明*部分、*电源建议*部分和*布局*部分 ... 1

Changes from Original (November 2009) to Revision A — **Page**

- 已根据新标准设置了文档格式。 ... 1

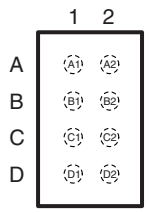
5 器件比较表

T_A	封装 (1)	可订购部件号	内涂层 (2)
-40°C 至 85°C	YFP	CDC3RL02BYFPR	是
-40°C 至 85°C	YFP	CDC3RL02YFPR	否

(1) 封装图样、散热数据和符号可从网站 http://www.ti.com.cn/zh-cn/support-packaging/packaging-information.html 中获取。
(2) 采用内涂层制造的 CSP (DSBGA) 器件由于封装的物理强度增加而具有更强的抗裂性。对于新设计，强烈建议使用带内涂层的器件。

6 Pin Configuration and Functions

YFP Package
8-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{BATT}	A1	I	Input to internal LDO
CLK_OUT1	A2	O	Clock output 1
V_{LDO}	B1	O	1.8 V I/O supply for CDC3RL02 and external TCXO
CLK_REQ1	B2	I	Clock request 1 (from peripheral) for Clock output 1
MCLK_IN	C1	I	Master clock input
CLK_REQ2	C2	I	Clock request 2 (from peripheral) for Clock output 2
GND	D1	–	Ground
CLK_OUT2	D2	O	Clock output 2

YFP Package Pin Assignments

	1	2
A	V_{BATT}	CLK_OUT1
B	V_{LDO}	CLK_REQ1
C	MCLK_LIN	CLK_REQ2
D	GND	CLK_OUT2

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted. (1)

			MIN	MAX	UNIT
V_{BATT}	Voltage range(2)		–0.3	7	V
	Voltage range(3)	CLK_REQ_1/2, MCLK_IN	–0.3	V_{BATT} + 0.3	V
		V_{LDO}, CLK_OUT_1/2(2)	–0.3	V_{BATT} + 0.3	
I_{IK}	Input clamp current at V_{BATT}, CLK_REQ_1/2, and MCLK_IN	V_I < 0		–50	mA
I_O	Continuous output current	CLK_OUT1/2		±20	mA
	Continuous current through GND, V_{BATT}, V_{LDO}			±50	mA
T_J	Operating virtual junction temperature		–40	150	°C
T_A	Operating ambient temperature range		–40	85	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{BATT}	Input voltage to internal LDO		2.3	5.5	V
V_I	Input voltage	MCLK_IN, CLK_REQ1/2	0	1.89	V
V_O	Output voltage	CLK_OUT1/2	0	1.8	V
V_{IH}	High-level input voltage	CLK_REQ1/2	1.3	1.89	V
V_{IL}	Low-level input voltage	CLK_REQ1/2	0	0.5	V
I_{OH}	High-level output current, DC current		–8		mA
I_{OL}	Low-level output current, DC current			8	mA

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

7.4 Thermal Information

THERMAL METRIC(1)		CDC3RL02 YFP (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LDO							
V_{OUT}	LDO output voltage	I_{OUT} = 50 mA		1.71	1.8	1.89	V
C_{LDO}	External load capacitance			1		10	µF
$I_{OUT(SC)}$	Short circuit output current	R_L = 0 Ω			100		mA
$I_{OUT(PK)}$	Peak output current	V_{BATT} = 2.3 V, V_{LDO} = V_{OUT} – 5%				100	mA
PSR	Power supply rejection	V_{BATT} = 2.3 V, I_{OUT} = 2 mA,	f_{IN}= 217 Hz and 1 kHz	60			dB
			f_{IN}= 3.25 MHz	40			
t_{su}	LDO startup time	V_{BATT} = 2.3 V , C_{LDO} = 1 µF, CLK_REQ_n to V_{IH} = 1.71 V			0.2		ms
		V_{BATT} = 5.5 V , C_{LDO} = 10 µF, CLK_REQ_n to V_{IH} = 1.71 V				1	
POWER CONSUMPTION							
I_{SB}	Standby current	Device in standby (all $V_{CLK\_REQ\_n}$ = 0 V)			0.2	1	µA
I_{CCS}	Static current consumption	Device active but not switching			0.4	1	mA
I_{OB}	Output buffer average current	f_{IN} = 26 MHz, C_{LOAD} = 50 pF			4.2		mA
C_{PD}	Output power dissipation capacitance	f_{IN} = 26 MHz				44	pF
MCLK_IN INPUT							
I_I	MCLK_IN, CLK_REQ_1/2 leakage current	V_I = V_{IH} or GND				1	µA
C_I	MCLK_IN capacitance	f_{IN} = 26 MHz			4.75		pF
R_I	MCLK_IN impedance	f_{IN} = 26 MHz			6		kΩ
f_{IN}	MCLK_IN frequency range			10	26	54	MHz
MCLK_IN LVCMOS SOURCE							
	Additive phase noise	f_{IN} = 26 MHz, t_r/t_f ≤ 1 ns	1-kHz offset		–140		dBc/Hz
			10-kHz offset		–149		
			100-kHz offset		–153		
			1-MHz offset		–148		
	Additive jitter	f_{IN} = 26 MHz, V_{PP} = 0.8 V, BW = 10–5 MHz			0.37		ps (rms)
t_{DL}	MCLK_IN to CLK_OUT_n propagation delay				11		ns
DC_L	Output duty cycle	f_{IN} = 26 MHz, DC_{IN} = 50%		45%	50%	55%	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MCLK_IN SINUSOIDAL SOURCE							
V_{MA}	Input amplitude			0.3		1.8	V
	Additive phase noise	f_{IN} = 26 MHz, V_{MA} = 1.8 V_{PP}	1-kHz offset		–141		dBc/Hz
			10-kHz offset		–149		
			100-kHz offset		–152		
			1-MHz offset		–148		
		f_{IN} = 26 MHz, V_{MA} = 0.8 V_{PP}	1-kHz offset		–139		
			10-kHz offset		–146		
			100-kHz offset		–150		
			1-MHz offset		–146		
	Additive jitter	f_{IN} = 26 MHz, V_{MA} = 1.8 V_{PP}, BW = 10–5 MHz			0.41		ps (RMS)
t_{DS}	MCLK_IN to CLK_OUT_1/2 propagation delay				12		ns
DC_S	Output duty cycle	f_{IN} = 26 MHz, V_{MA} > 1.8 V_{PP}		45%	50%	55%	
CLK_OUT_N OUTPUTS							
t_r	20% to 80% rise time	C_L = 10 pF to 50 pF		1		5.2	ns
t_f	20% to 80% fall time	C_L = 10 pF to 50 pF		1		5.2	ns
t_{sk}	Channel-to-channel skew	C_L = 10 pF to 50 pF (C_{L1} = C_{L2})		–0.5		0.5	ns
V_{OH}	High-level output voltage	I_{OH} = –100 μA, reference to V_{LDO}		–0.1			V
		I_{OH} = –8 mA		1.2			
V_{OL}	Low-level output voltage	I_{OL} = 20 μA				0.2	V
		I_{OL} = 8 mA				0.55	

7.6 Typical Characteristics

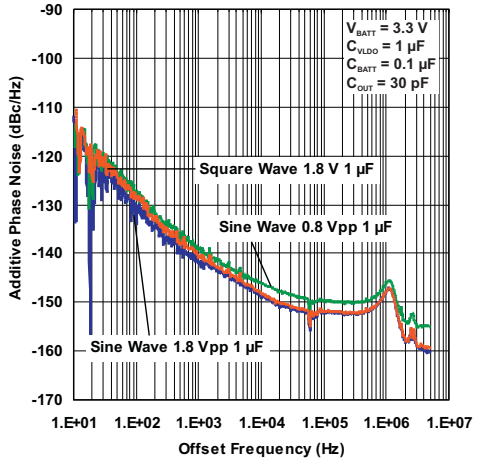


Figure 1. Additive Phase Noise vs Offset Frequency

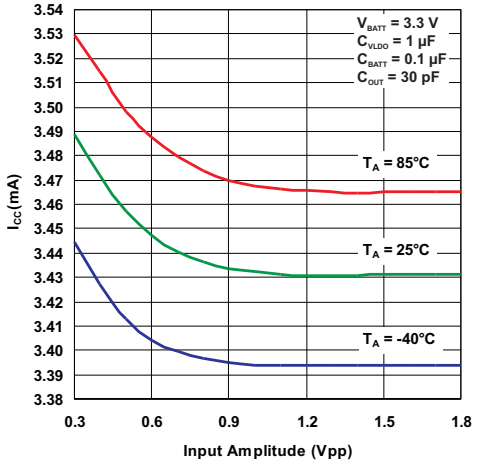


Figure 2. Supply Current vs Input Amplitude

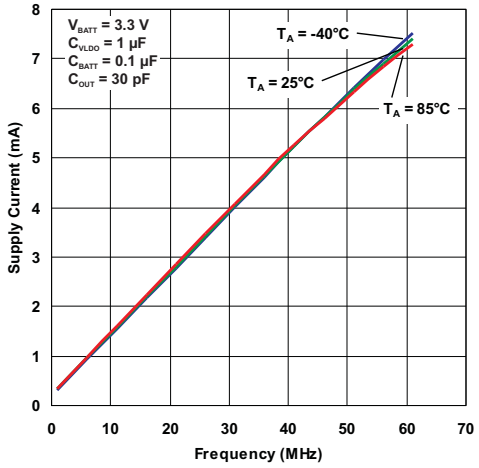


Figure 3. Supply Current vs Input Frequency

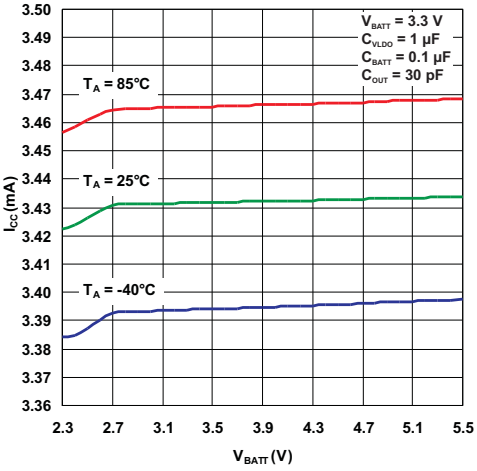


Figure 4. Supply Current vs Supply Voltage

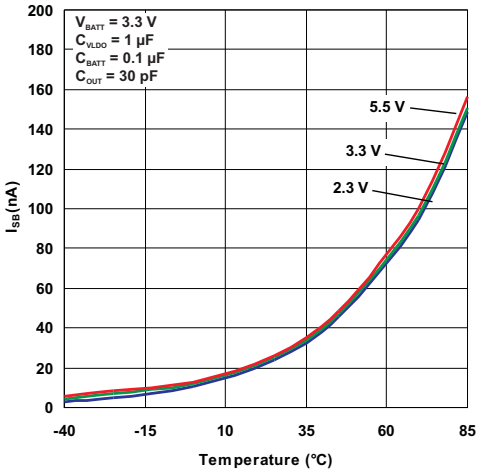


Figure 5. Standby Current vs Temperature

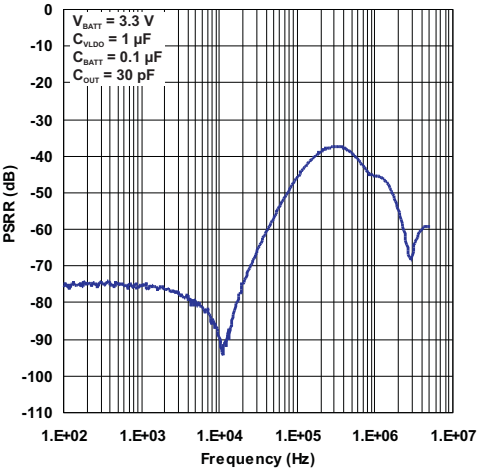


Figure 6. Power Supply Rejection vs Input Frequency

Typical Characteristics (continued)

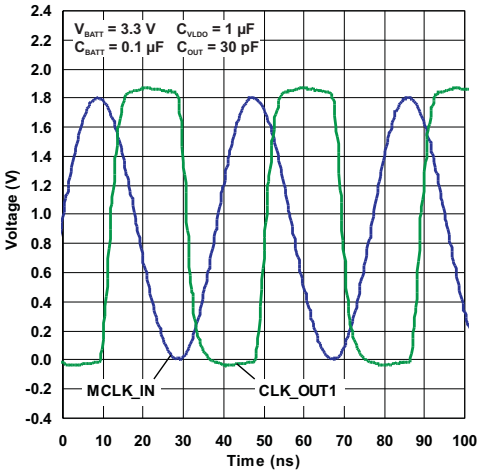


Figure 7. Sine-Wave Input vs Square-Wave Output

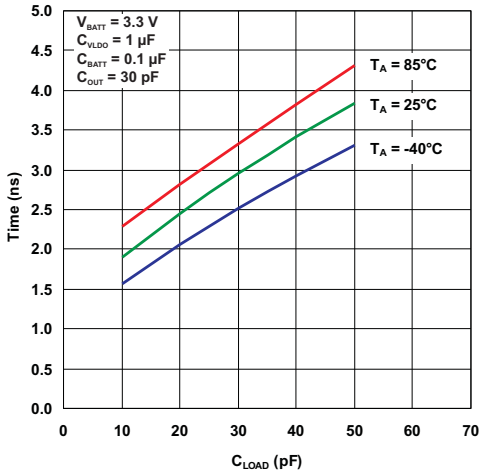


Figure 8. Rise Time vs Load

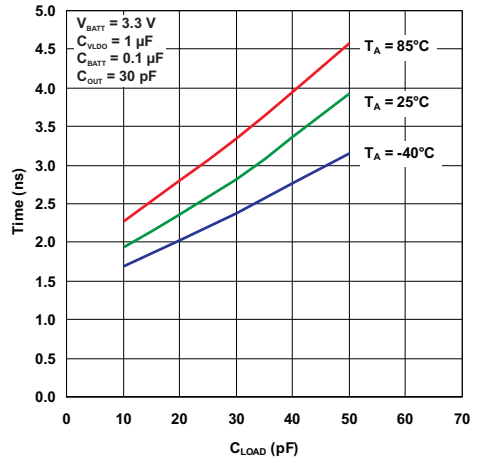


Figure 9. Fall Time vs Load

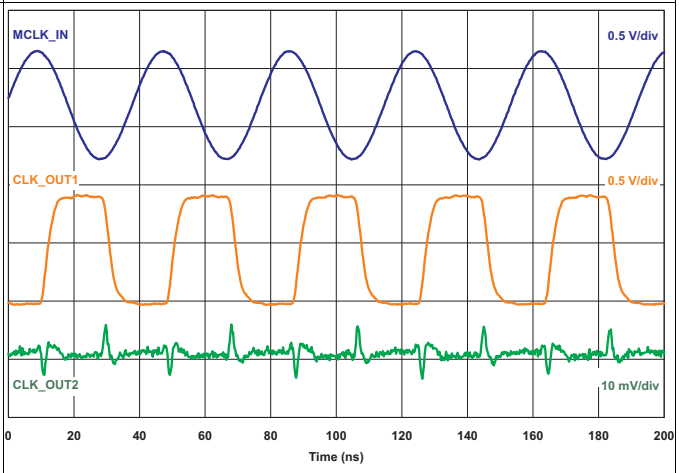


Figure 10. Digital Cross-Talk Scope Shot

8 Detailed Description

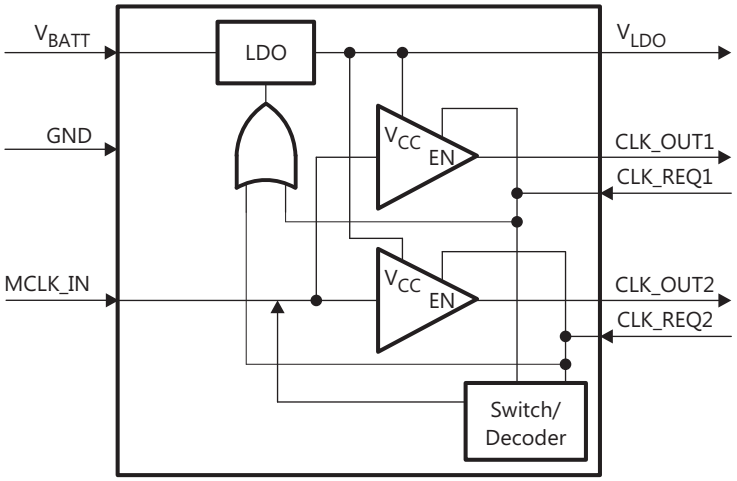
8.1 Overview

The CDC3RL02 is a two-channel clock fan-out buffer and is ideal for use in portable end-equipment, such as mobile phones, that require clock buffering with minimal additive phase noise and fan-out capabilities. It buffers a single master clock, such as a temperature compensated crystal oscillator (TCXO) to multiple peripherals. The device has two clock request inputs (CLK_REQ1 and CLK_REQ2), each of which enable a single clock output.

The CDC3RL02 accepts square or sine waves at the master clock input (MCLK_IN), eliminating the need for an AC coupling capacitor. The smallest acceptable sine wave is a 0.3-V signal (peak-to-peak). CDC3RL02 has been designed to offer minimal channel-to-channel skew, additive output jitter, and additive phase noise. The adaptive clock output buffers offer controlled slew-rate over a wide capacitive loading range which minimizes EMI emissions, maintains signal integrity, and minimizes ringing caused by signal reflections on the clock distribution lines.

The CDC3RL02 has an integrated Low-Drop-Out (LDO) voltage regulator which accepts input voltages from 2.3 V to 5.5 V and outputs 1.8 V, 50 mA. This 1.8-V supply is externally available to provide regulated power to peripheral devices such as a TCXO.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low Additive Noise

The CDC3RL02 features –149 dBc/Hz at 10 kHz offset phase noise and 0.37 ps (RMS) of output jitter, to make sure that the buffered signals are clean.

8.3.2 Regulated 1.8-V Externally Available I/O Supply

The CDC3RL02 allows users to connect to the output of the internal LDO, for providing power to other ICs. For more information, refer to *LDO*.

8.3.3 Ultra-Small 8-bump YFP 0.4-mm Pitch WCSP Package

Using the ultra-small YFP package, the CDC3RL02 is very small and allows it to be placed on a board with minimum work.

8.4 Device Functional Modes

Table 1 is the function table for CDC3RL02.

Table 1. Function Table

INPUTS			OUTPUTS	
CLK_REQ1(1)	CLK_REQ2(1)	MCLK_IN	CLK_OUT1	CLK_OUT2
L	L	X	L	L
L	H	CLK	L	CLK
H	L	CLK	CLK	L
H	H	CLK	CLK	CLK

(1) If a CLK_OUT will always be enabled, it is acceptable to tie its CLK_REQ pin to an external 1.8 V source (not VLDO).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Clock Squarer

Figure 11 shows the input stage of the CDC3RL02. The input signal at MCLK_IN can be a square wave or sine wave. C_{MCLK} is an internal AC coupling capacitor that allows a direct connection from the TCXO to the CDC3RL02 without an external capacitor.

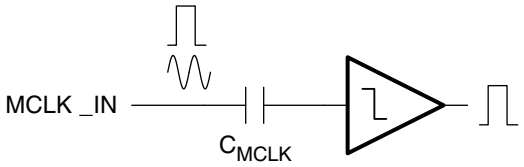


Figure 11. Input Stage with Internal AC Coupling Capacitor

Any external component added in the series path of the clock signal will potentially add phase noise and jitter. The error source associated with the internal decoupling capacitor is included in the specification of the CDC3RL02. The recommended clock frequency band of the CDC3RL02 is 10 MHz to 52 MHz for specified functionality. All performance metrics are specified at 26 MHz. The lowest acceptable sinusoidal signal amplitude is 0.8 V_{PP} for specified performance. Amplitudes as low as 0.3 V_{PP} are acceptable but with reduced phase-noise and jitter performance.

9.1.2 Output Stage

Each output drives 1.8-V LVCMOS levels. Adaptive output buffers limit the rise/fall time of the output to within 1 ns to 5 ns with load capacitance between 10 pF and 50 pF. Fast slew rates introduce EMI into the system. Each output buffer limits EMI by keeping the rise/fall time above 1 ns. Slow rise/fall times can induce additive phase noise and duty cycle errors in the load device. The output buffer limits these errors by keeping the rise/fall time below 5 ns. In addition, the output stage dynamically alters impedance based on the instantaneous voltage level of the output. This dynamic change limits reflections keeping the output signal monotonic during transitions. Each output is active low when not requested to avoid false clocking of the load device.

9.1.3 LDO

A low noise 1.8-V LDO is integrated to provide the I/O supply for the output buffers. The LDO output is externally available to power a clock source such as a TCXO. A clean supply is provided to the clock buffers and the clock source for optimum phase noise performance. The input range of the LDO allows the device to be powered directly from a single cell Li battery. The LDO is enabled by either of the CLK_REQ_N signals. When disabled, the device enters a low power shutdown mode consuming less than 1 μA from the battery. The LDO requires an output decoupling capacitor in the range of 1 μF to 10 μF with an equivalent series resistance (ESR) of at least 0.1 Ω for compensation and high-frequency PSR. This capacitor must stay within the specified range for capacitance and ESR over the entire operating temperature range. A ceramic capacitor can be used if a small external resistance is added in series with it to increase the effective ESR. An input bypass capacitor of 1 μF or larger is recommended.

9.2 Typical Application

The CDC3RL02 is ideal for use in mobile applications as shown in Figure 12. In this example, a single low noise TCXO system clock source is buffered to drive a mobile GPS receiver and WLAN transceiver. Each peripheral independently requests an active clock by asserting a single clock request line (CLK_REQ_1 or CLK_REQ_2). When both clock request lines are inactive, the CDC3RL02 enters a low current shutdown mode. In this mode, the LDO output, CLK_OUT_1, and CLK_OUT_2 are pulled to GND and the TCXO will be unpowered.

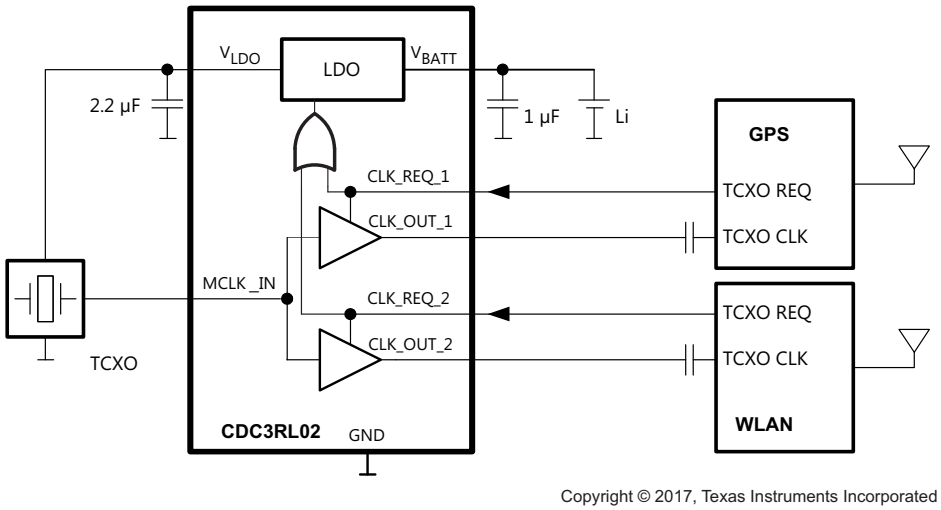


Figure 12. Mobile Application

When either peripheral requests the clock, the CDC3RL02 will enable the LDO and power the TCXO. The TCXO output (square wave, sine wave, or clipped sine wave) is converted to a square wave and buffered to the requested output.

9.2.1 Design Requirements

For the typical application, the user must know the following parameters.

Table 2. Design Parameters

PARAMETER	DESCRIPTION	EXAMPLE VALUE
V_{BATT}	Input voltage from battery or power supply	3.7 V
MCLK_IN	Input frequency from a TCXO	26 MHz

9.2.2 Detailed Design Procedure

The designer must make sure that all parameters are within the ranges specified in *Recommended Operating Conditions*.

Each device which receives a clock output from the CDC3RL02 should have the CLK request pin connected to the appropriate CLK_REQ pin on the CDC3RL02. This will enable the output buffer when a device requests the clock signal.

It is possible to have a control the outputs of the clock by using a GPIO from a controller to control the CLK_REQ pins.

If one of the outputs is unused, then tie the CLK_REQ and CLK_OUT pins to ground. If the user wants a CLK_OUT pin always enabled, it is acceptable to tie the paired CLK_REQ pin to an external 1.8-V source (not V_{LDO} because the LDO output is not enabled until at least one CLK_REQ pin is high).

9.2.3 Application Curve

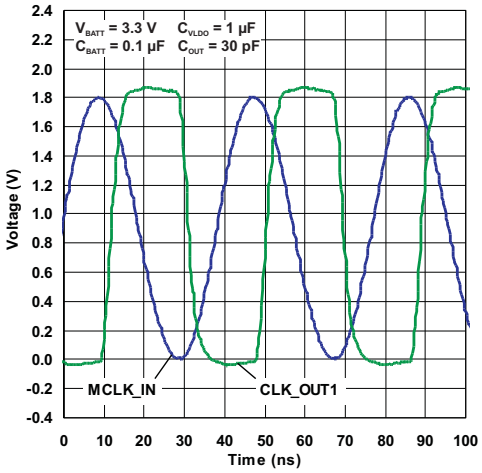


Figure 13. Sine Wave Input vs Output

10 Power Supply Recommendations

General power supply recommendations are to be considered for the CDC3RL02. These include:

- Decoupling capacitors placed close to the V_{BATT} pin of typical values (1 µF)
- V_{BATT} be within the recommended voltage range

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{BATT} pin
- Short trace-lengths should be used to avoid excessive loading
- For improved performance on the clock output lines, use a ground trace on the sides of the clock trace to minimize crosstalk and EMI

11.2 Layout Example

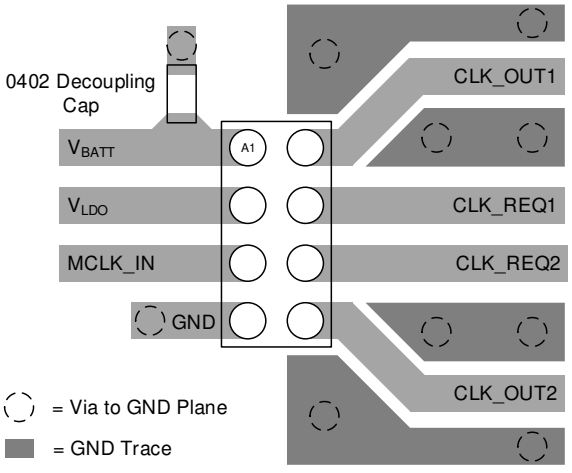


Figure 14. Example Layout for YFP Package

12 器件和文档支持

12.1 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.
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12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC3RL02BYFPR	ACTIVE	DSBGA	YFP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN	Samples
CDC3RL02YFPR	ACTIVE	DSBGA	YFP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

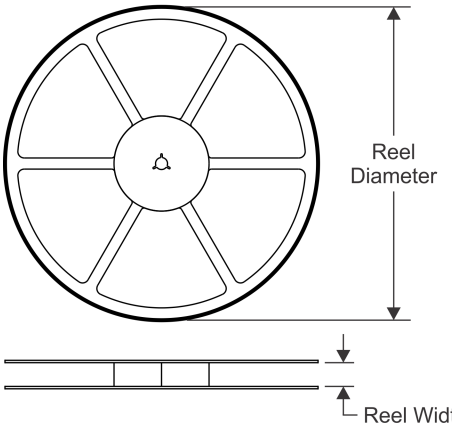
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

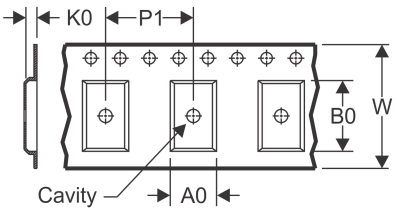
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

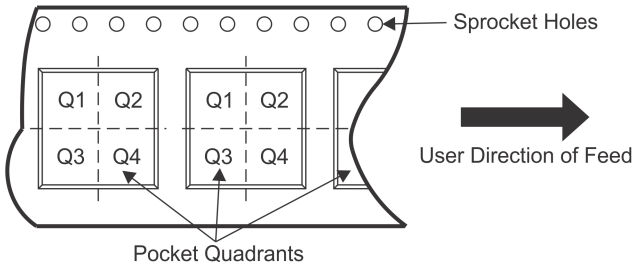


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

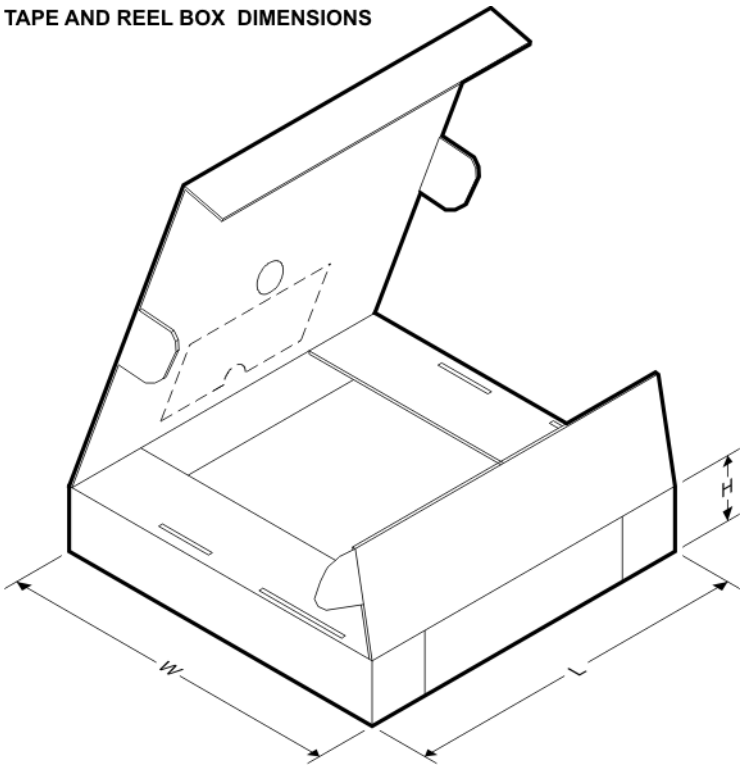
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

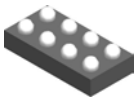
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC3RL02BYFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
CDC3RL02YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC3RL02BYFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
CDC3RL02YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0

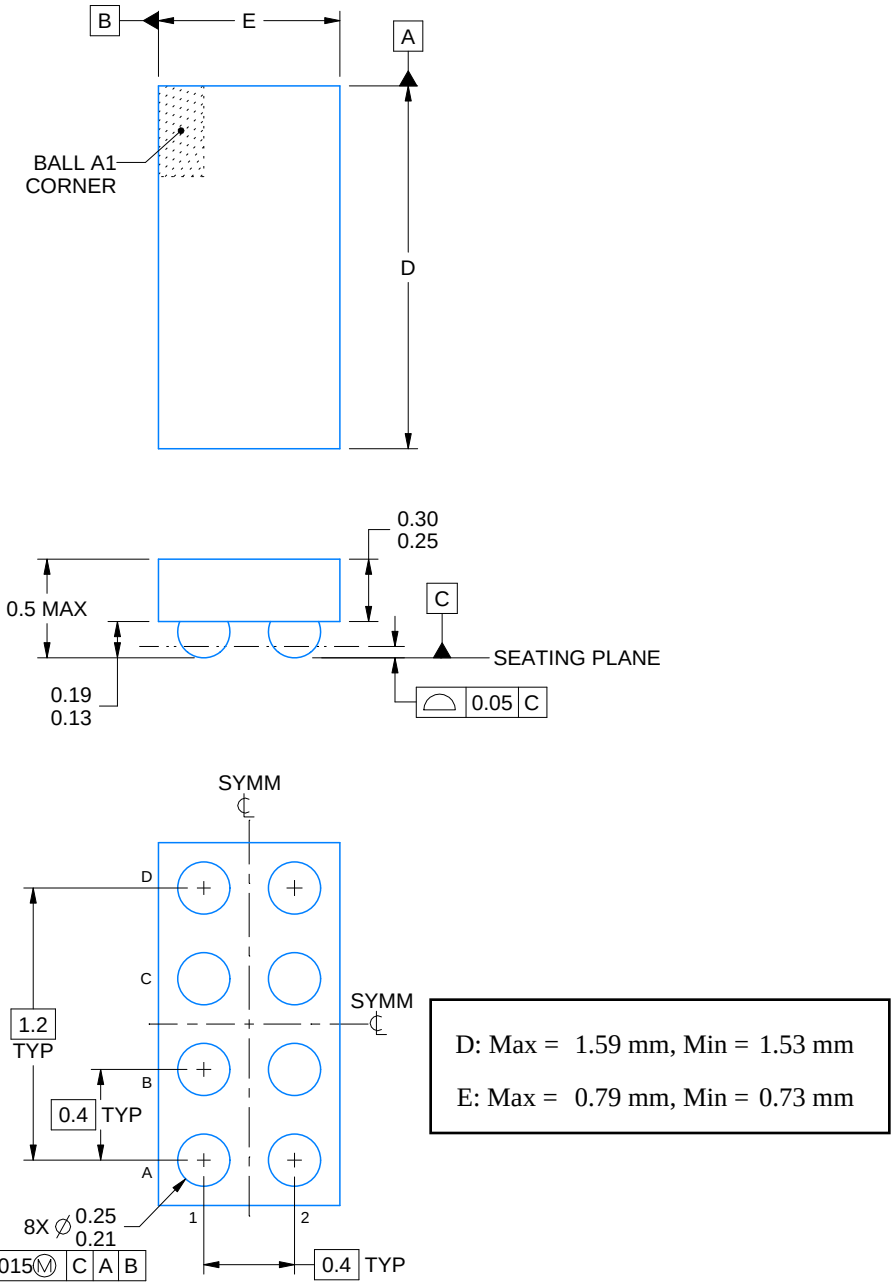


PACKAGE OUTLINE

YFP0008

DSBGA - 0.5 mm max height

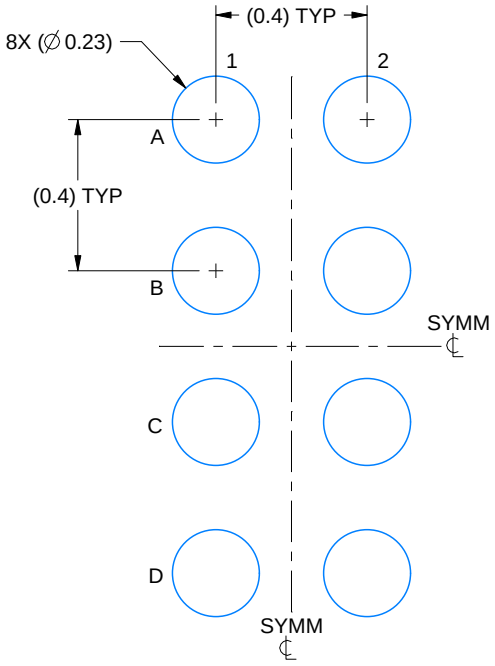
DIE SIZE BALL GRID ARRAY



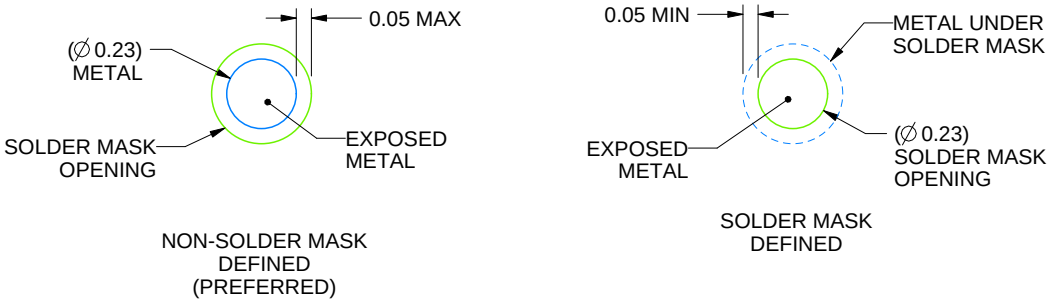
4225242/A 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

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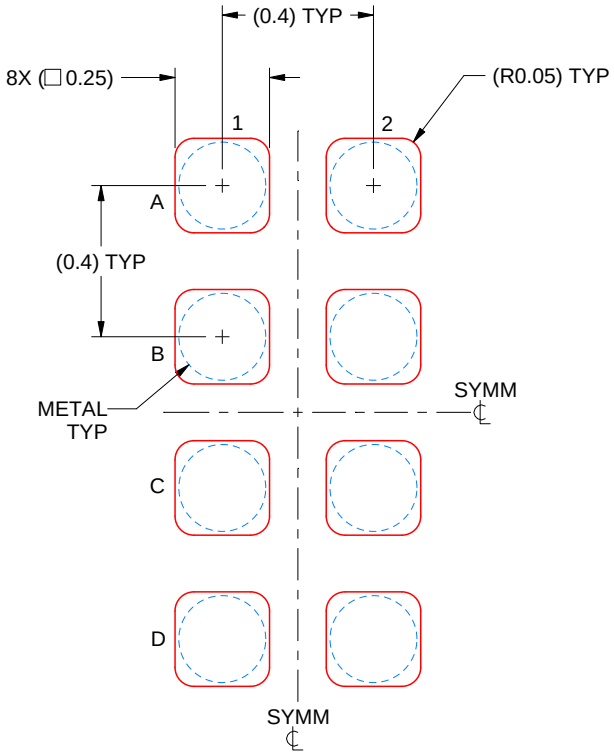
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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