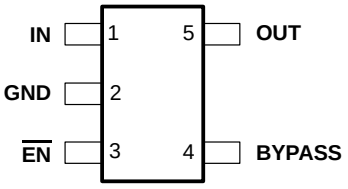
- **100-mA Low-Dropout Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 2.8-V, 3.0-V**
- **Output Noise Typically 56 $\mu V_{RMS}$ (TPS78930)**
- **Only 17 μA Quiescent Current at 100 mA**
- **1 μA Quiescent Current in Standby Mode**
- **Dropout Voltage Typically 115 mV at 100 mA (TPS78930)**
- **Over Current Limitation**
- **–40°C to 125°C Operating Junction Temperature Range**
- **5-Pin SOT-23 (DBV) Package**

**DBV PACKAGE**
**(TOP VIEW)**

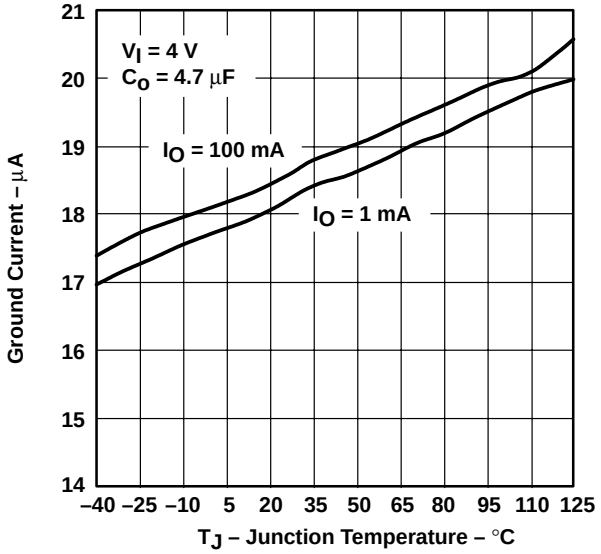



## description

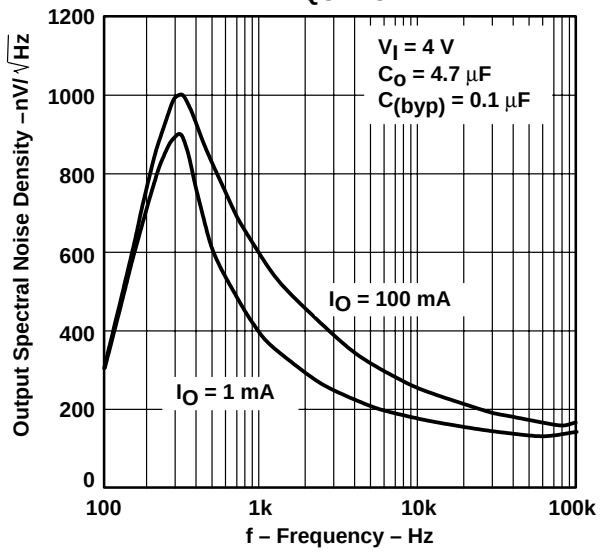
The TPS789xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, ultralow-power operation, low-output noise, and miniaturized packaging. These regulators feature low-dropout voltages and ultralow quiescent current compared to conventional LDO regulators. An internal resistor, in conjunction with an external bypass capacitor, creates a low-pass filter to reduce the noise. The TPS78930 exhibits only 56 $\mu V_{RMS}$ of output voltage noise using 0.01 μF bypass and 10 μF output capacitors. Offered in a 5-terminal small outline integrated-circuit SOT-23 package, the TPS789xx series devices are ideal for micropower operations, low output noise, and where board space is limited.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 115 mV at 100 mA of load current (TPS78930), and is directly proportional to the load current. The quiescent current is ultralow (17 μA typically) and is stable over the entire range of output load current (0 mA to 100 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-dropout voltage feature and ultralow-power operation result in a significant increase in system battery operating life.

**TPS78930**
**GROUND CURRENT**
**vs**
**JUNCTION TEMPERATURE**




**TPS78930**
**OUTPUT SPECTRAL NOISE DENSITY**
**vs**
**FREQUENCY**




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## description (continued)

The TPS789xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA typical at $T_J$ = 25°C. The TPS789xx is offered in 1.5 V, 1.8 V, 2.5 V, 2.8 V, and 3.0 V.

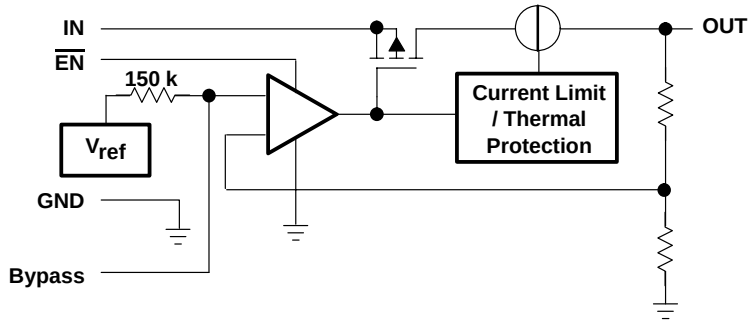
**AVAILABLE OPTIONS**

| $T_J$ | VOLTAGE | PACKAGE | PART NUMBER | | SYMBOL |
|---|---|---|---|---|---|
| –40°C to 125°C | 1.5 V | SOT-23 (DBV) | TPS78915DBVT† | TPS78915DBVR‡ | PDWI |
| | 1.8 V | | TPS78918DBVT† | TPS78918DBVR‡ | PDXI |
| | 2.5 V | | TPS78925DBVT† | TPS78925DBVR‡ | PDYI |
| | 2.8 V | | TPS78928DBVT† | TPS78928DBVR‡ | PDZI |
| | 3.0 V | | TPS78930DBVT† | TPS78930DBVR‡ | PEAI |

† The DBVT indicates tape and reel of 250 parts.
‡ The DBVR indicates tape and reel of 3000 parts.

## functional block diagram

**TPS78915/18/25/28/30**




## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| BYPASS | 4 | I | The external bypass capacitor, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise. |
| $\overline{EN}$ | 3 | I | Active low enable. |
| GND | 2 | | Regulator ground |
| IN | 1 | I | The IN terminal is the input to the device. |
| OUT | 5 | O | The OUT terminal is the regulated output of the device. |

## detail description

The TPS789xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS789xx is essentially constant from no load to maximum load.

The TPS789xx family of low-dropout (LDO) regulators have been optimized for use in battery-operated equipment. They feature extremely low dropout voltages, low output noise, low quiescent current (17 μA typically), and enable inputs to reduce supply currents to 1 μA when the regulators are turned off.

The internal voltage reference is a key source of noise in a LDO regulator. The TPS789xx has a BYPASS pin which is connected to the voltage reference through a 150-kΩ internal resistor. The 150-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. Note that the output will start up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 150-kΩ resistor and external capacitor.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the $\overline{EN}$ input will disable the TPS789xx internal circuitry, reducing the supply current to 1 μA. A voltage of less than 0.9 V on the $\overline{EN}$ input will enable the TPS789xx and will enable normal operation to resume. The $\overline{EN}$ input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1) . . . . . –0.3 V to 13.5 V
Voltage range at $\overline{EN}$ . . . . . –0.3 V to $V_I$ + 0.3 V
Voltage on OUT . . . . . 7 V
Peak output current . . . . . Internally limited
ESD rating, HBM . . . . . 2 kV
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$ . . . . . –40°C to 150°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A \le 25°C$ POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|---|---|
| Low K‡ | DBV | 65.8 °C/W | 259 °C/W | 3.9 mW/°C | 386 mW | 212 mW | 154 mW |
| High K§ | DBV | 65.8 °C/W | 180 °C/W | 5.6 mW/°C | 555 mW | 305 mW | 222 mW |

‡ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.

§ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Input voltage, $V_I$ (see Note 2) | 2.7 | | 10 | V |
| Continuous output current, $I_O$ (see Note 3) | 0 | | 100 | mA |
| Operating junction temperature, $T_J$ | –40 | | 125 | °C |

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_I(min) = V_O(max) + V_{DO}$ (max load)
3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

## electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_o = 4.7$ μF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output voltage (see Note 4) | TPS78915 | $T_J$ = 25°C, | 2.7 V < $V_I$ < 10 V | | 1.5 | | V |
| | | $T_J$ = –40°C to 125°C, | 2.7 V < $V_I$ < 10 V | 1.455 | | 1.545 | |
| | TPS78918 | $T_J$ = 25°C, | 2.8 V < $V_I$ < 10 V | | 1.8 | | |
| | | $T_J$ = –40°C to 125°C, | 2.8 V < $V_I$ < 10 V | 1.746 | | 1.854 | |
| | TPS78925 | $T_J$ = 25°C, | 3.5 V < $V_I$ < 10 V | | 2.5 | | |
| | | $T_J$ = –40°C to 125°C, | 3.5 V < $V_I$ < 10 V | 2.425 | | 2.575 | |
| | TPS78928 | $T_J$ = 25°C, | 3.8 V < $V_I$ < 10 V | | 2.8 | | |
| | | $T_J$ = –40°C to 125°C, | 3.8 V < $V_I$ < 10 V | 2.716 | | 2.884 | |
| | TPS78930 | $T_J$ = 25°C, | 4.0 V < $V_I$ < 10 V | | 3 | | |
| | | $T_J$ = –40°C to 125°C, | 4.0 V < $V_I$ < 10 V | 2.910 | | 3.090 | |
| Quiescent current (GND current) (see Notes 4 and 5) | | $\overline{EN}$ = 0 V, $T_J$ = 25°C | 10 μA < $I_O$ < 100 mA, | | 17 | | μA |
| | | $\overline{EN}$ = 0 V, $T_J$ = –40°C to 125°C | $I_O$ = 100 mA, | | | 28 | |
| Load regulation | | $\overline{EN}$ = 0 V, $T_J$ = 25°C | $I_O$ = See Note 4 | | 12 | | mV |
| Output voltage line regulation ($\Delta V_O/V_O$) (see Note 5) | | $V_O$ + 1 V < $V_I$ ≤ 10 V, See Note 4 | $T_J$ = 25°C, | | 0.04 | | %/V |
| | | $V_O$ + 1 V < $V_I$ ≤ 10 V, $T_J$ = –40°C to 125°C, | See Note 4 | | | 0.1 | |
| Output noise voltage (TPS78930) | | BW = 300 Hz to 50 kHz, $C_{(byp)}$ = 0.01 μF, $C_O$ = 10 μF, | $I_O$ = 100 mA, $T_J$ = 25°C | | 56 | | $\mu V_{RMS}$ |
| Output current limit | | $V_O$ = 0 V, | See Note 4 | | 350 | 750 | mA |
| Standby current | | $\overline{EN}$ = $V_I$, | 2.7 < $V_I$ < 10 V | | 1 | | μA |
| | | $T_J$ = –40°C to 125°C | | | | 2 | μA |

NOTES: 4. The minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. The maximum IN voltage is 10 V. The minimum output current is 10 μA and the maximum output current is 100 mA.
5. If $V_O \le 1.8$ V then $V_{Imin} = 2.7$ V, $V_{Imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O \ge 2.5$ V then $V_{Imin} = V_O + 1$ V, $V_{Imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

**electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_o = 4.7$ μF (unless otherwise noted) (continued)**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| High level enable input voltage | | 2.7 V < $V_I$ < 10 V | | 1.7 | | | V |
| Low level enable input voltage | | 2.7 V < $V_I$ < 10 V | | | | 0.9 | V |
| Power supply ripple rejection (TPS78930) | | f = 1 kHz, $T_J$ = 25°C, | $C_O$ = 10 μF, $C_{(byp)}$ = 0.01 μF | | 85 | | dB |
| Input current (EN) | | $\overline{EN}$ = 0 V | | –1 | 0 | 1 | μA |
| | | $\overline{EN}$ = $V_I$ | | –1 | | 1 | μA |
| Dropout voltage (see Note 6) | TPS78928 | $I_O$ = 50 mA, | $T_J$ = 25°C | | 60 | | mV |
| | | $I_O$ = 50 mA, | $T_J$ = –40°C to 125°C | | | 125 | |
| | | $I_O$ = 100 mA, | $T_J$ = 25°C | | 122 | | |
| | | $I_O$ = 100 mA, | $T_J$ = –40°C to 125°C | | | 245 | |
| | TPS78930 | $I_O$ = 50 mA, | $T_J$ = 25°C | | 57 | | |
| | | $I_O$ = 50 mA, | $T_J$ = –40°C to 125°C | | | 115 | |
| | | $I_O$ = 100 mA, | $T_J$ = 25°C | | 115 | | |
| | | $I_O$ = 100 mA, | $T_J$ = –40°C to 125°C | | | 230 | |

NOTE 6. IN voltage equals $V_O$(typ) – 100 mV; The TPS78930 output voltage is set to 2.9 V. The TPS78915, TPS78918, and TPS78925 dropout voltage is limited by the input voltage range limitations.

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_O$ | Output voltage | vs Output current | 1, 2, 3 |
| | | vs Junction temperature | 4, 5, 6 |
| | Ground current | vs Junction temperature | 7 |
| | Output spectral noise density | vs Frequency | 8 – 10 |
| | Root mean squared output noise | vs Bypass capacitance | 11 |
| $Z_o$ | Output impedance | vs Frequency | 12 |
| $V_{DO}$ | Dropout voltage | vs Junction temperature | 13 |
| | Ripple rejection | vs Frequency | 14 – 16 |
| $V_O$ | Output voltage, enable voltage | vs Time (start-up) | 17 – 19 |
| | Line transient response | | 20, 22 |
| | Load transient response | | 21, 23 |
| | Equivalent series resistance (ESR) | vs Output current | 24, 25 |

## TYPICAL CHARACTERISTICS

**TPS78925**
**OUTPUT VOLTAGE vs OUTPUT CURRENT**

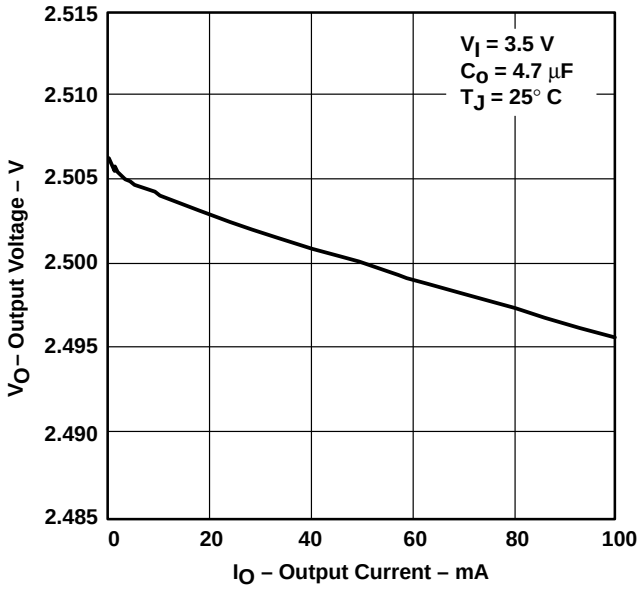



**Figure 1**

**TPS78915**
**OUTPUT VOLTAGE vs OUTPUT CURRENT**

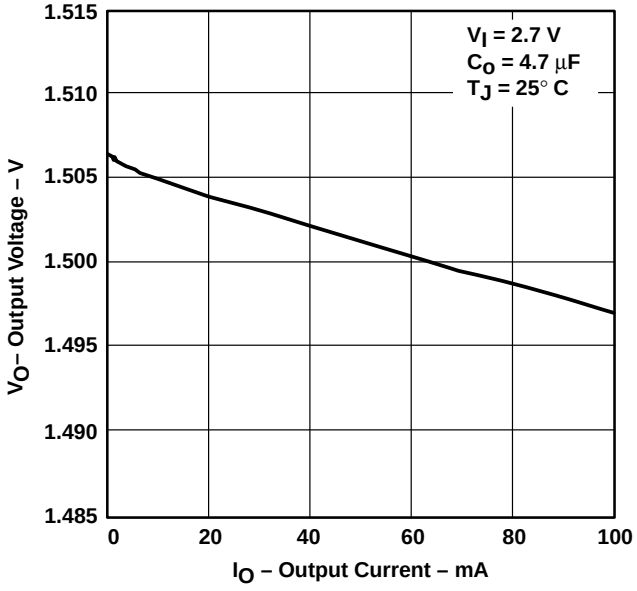



**Figure 2**

**TPS78930**
**OUTPUT VOLTAGE vs OUTPUT CURRENT**

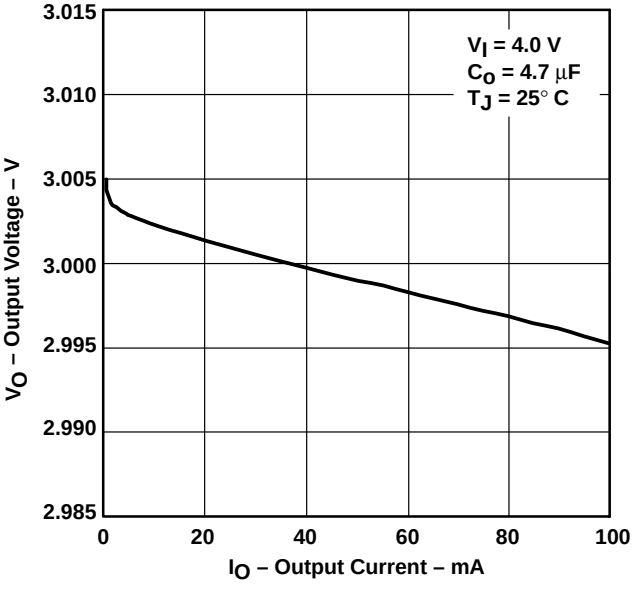



**Figure 3**

**TPS78915**
**OUTPUT VOLTAGE vs JUNCTION TEMPERATURE**

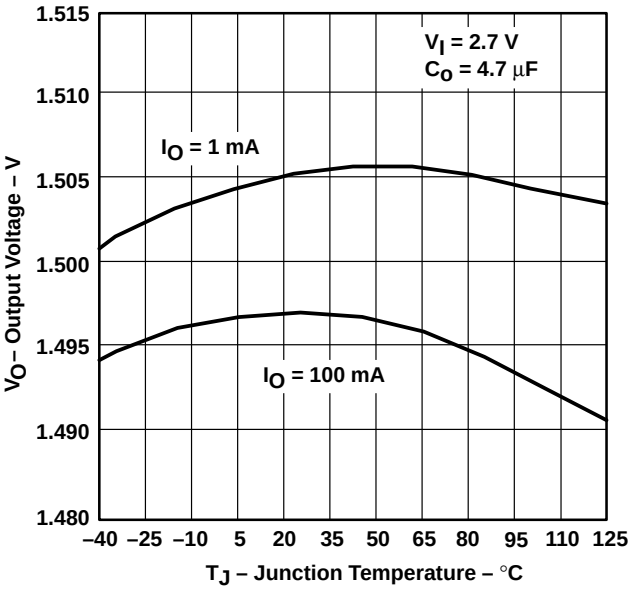



**Figure 4**

## TYPICAL CHARACTERISTICS

**TPS78925**
**OUTPUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

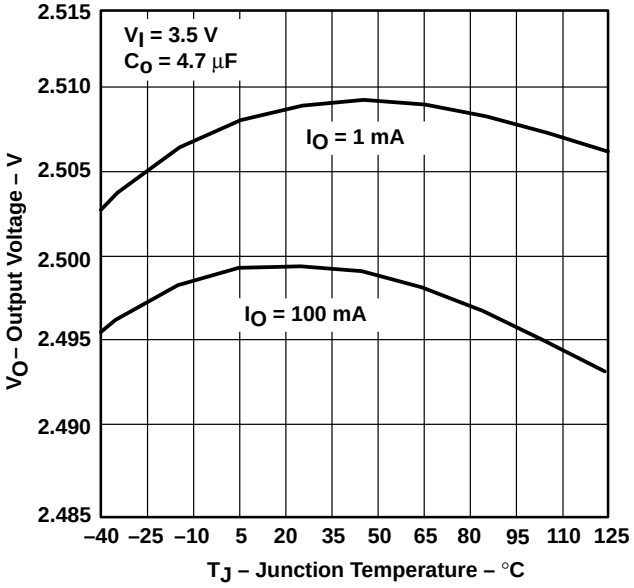



**Figure 5**

**TPS78930**
**OUTPUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

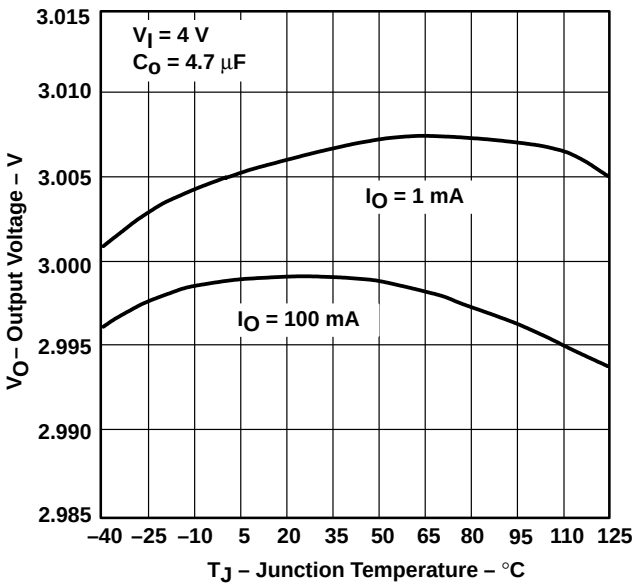



**Figure 6**

**TPS78930**
**GROUND CURRENT**
**vs**
**JUNCTION TEMPERATURE**

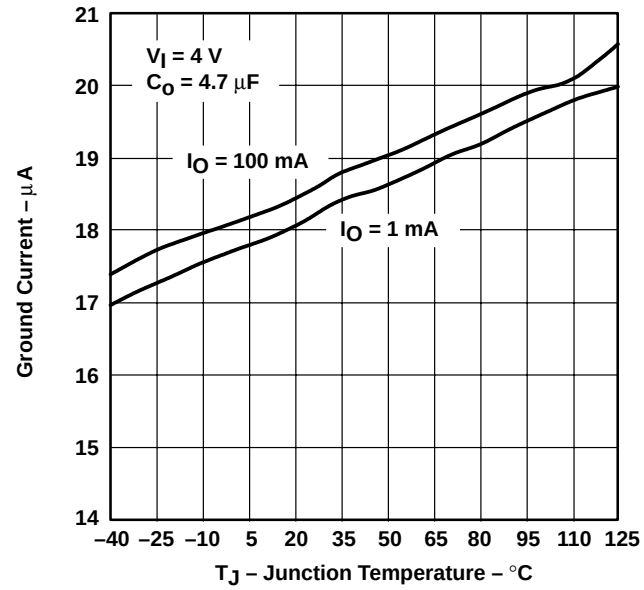



**Figure 7**

**TPS78930**
**OUTPUT SPECTRAL NOISE DENSITY**
**vs**
**FREQUENCY**

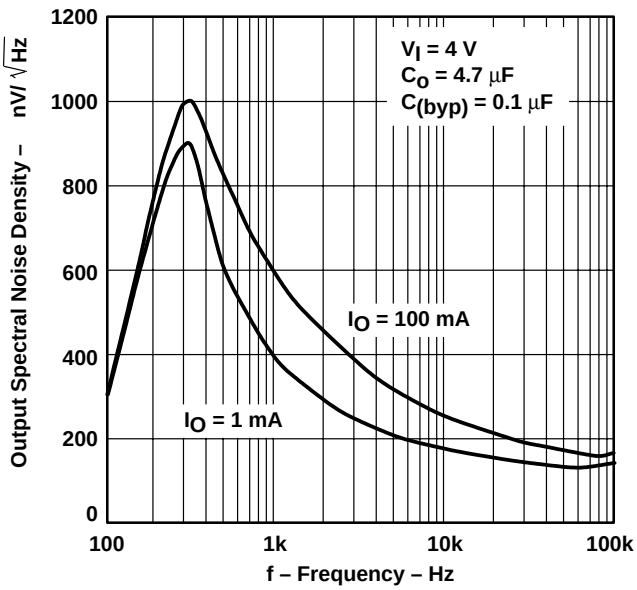



**Figure 8**

## TYPICAL CHARACTERISTICS

TPS78930
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

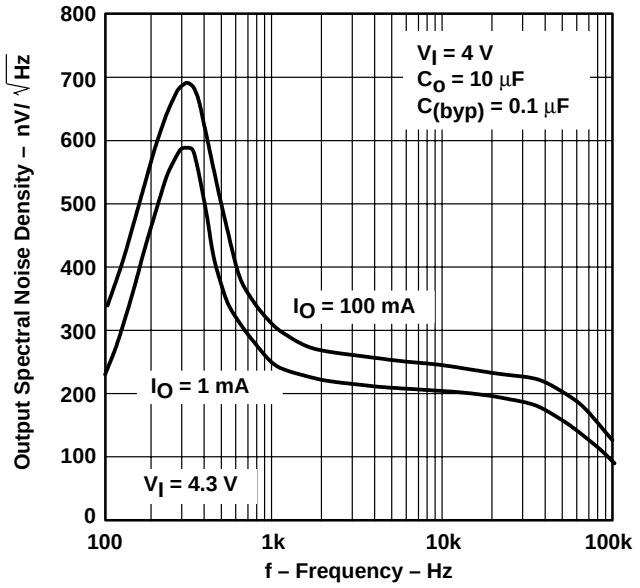



Figure 9

TPS78930
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

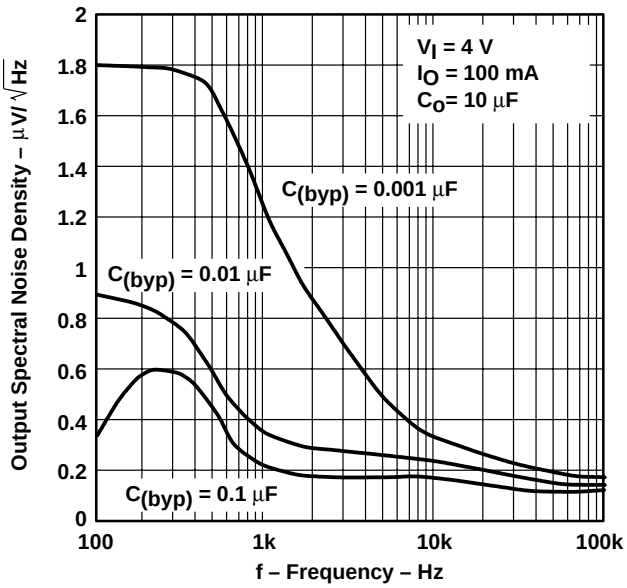



Figure 10

ROOT MEAN SQUARED OUTPUT NOISE
vs
BYPASS CAPACITANCE

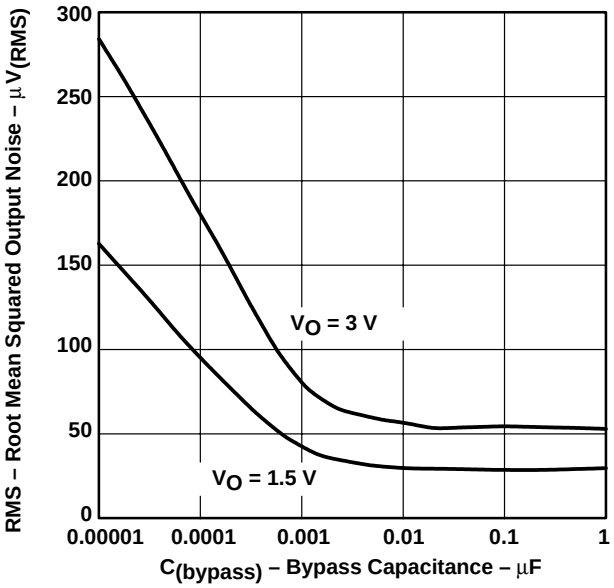



Figure 11

OUTPUT IMPEDANCE
vs
FREQUENCY

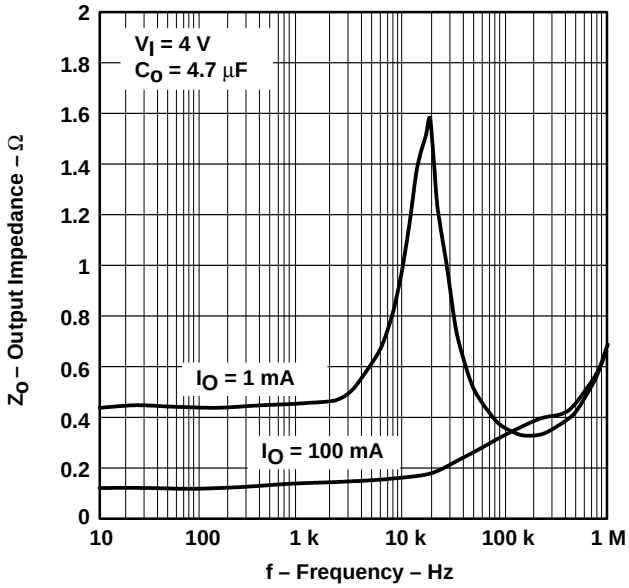



Figure 12

## TYPICAL CHARACTERISTICS

TPS78930
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

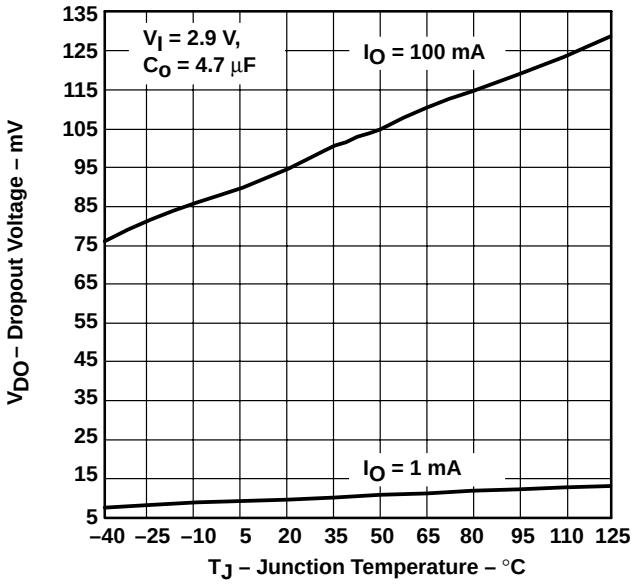



Figure 13

TPS78930
RIPPLE REJECTION
vs
FREQUENCY

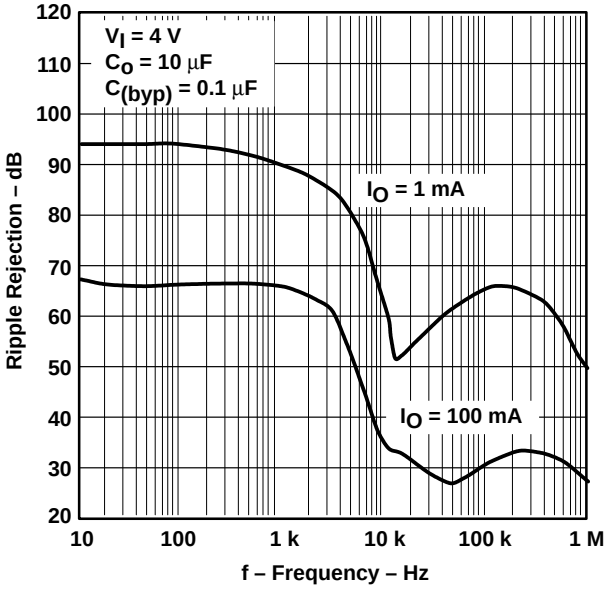



Figure 14

TPS78930
RIPPLE REJECTION
vs
FREQUENCY

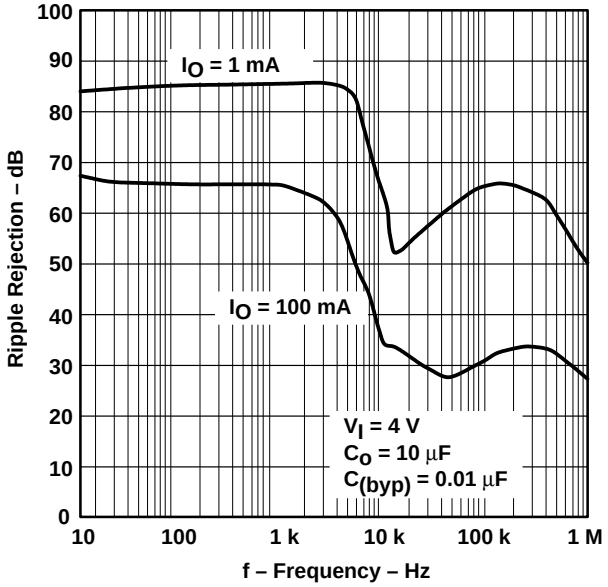



Figure 15

TPS78930
RIPPLE REJECTION
vs
FREQUENCY

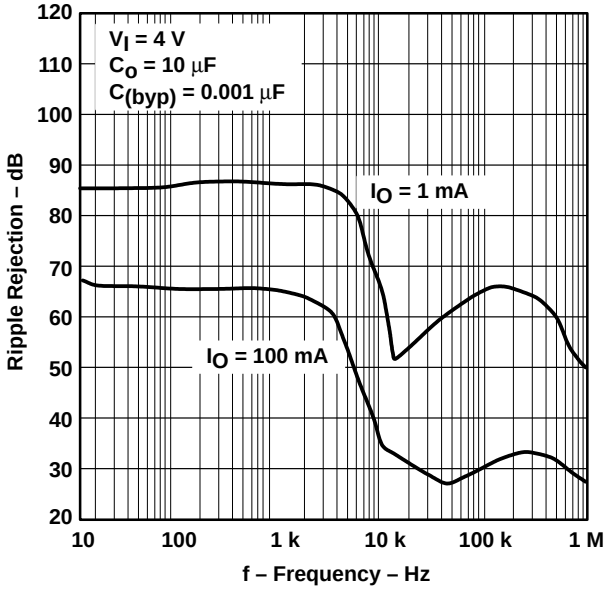



Figure 16

## TYPICAL CHARACTERISTICS

**TPS78930**
**OUTPUT VOLTAGE, ENABLE VOLTAGE**
**vs**
**TIME (START-UP)**

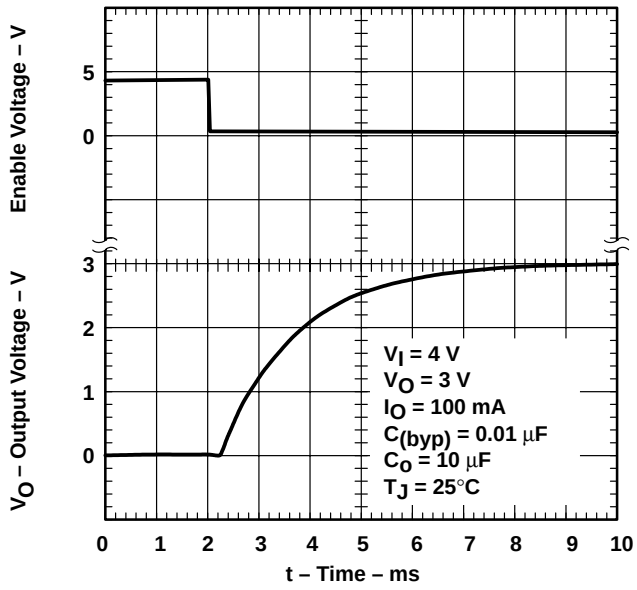



**Figure 17**

**TPS78930**
**OUTPUT VOLTAGE, ENABLE VOLTAGE**
**vs**
**TIME (START-UP)**

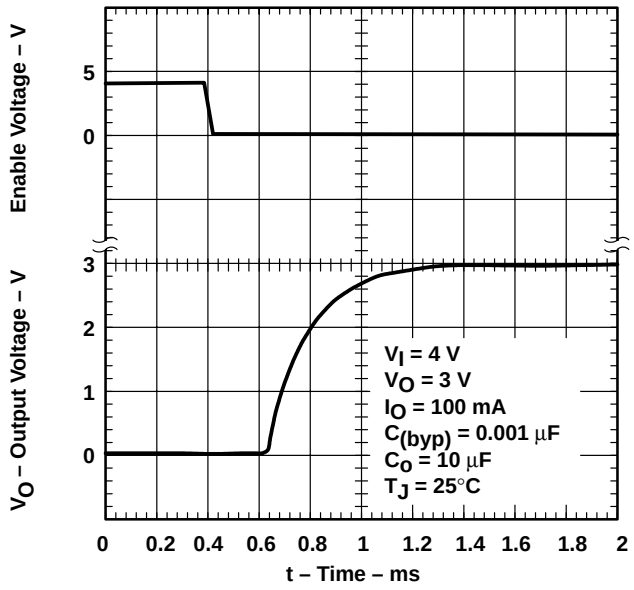



**Figure 18**

**TPS78930**
**OUTPUT VOLTAGE, ENABLE VOLTAGE**
**vs**
**TIME (START-UP)**

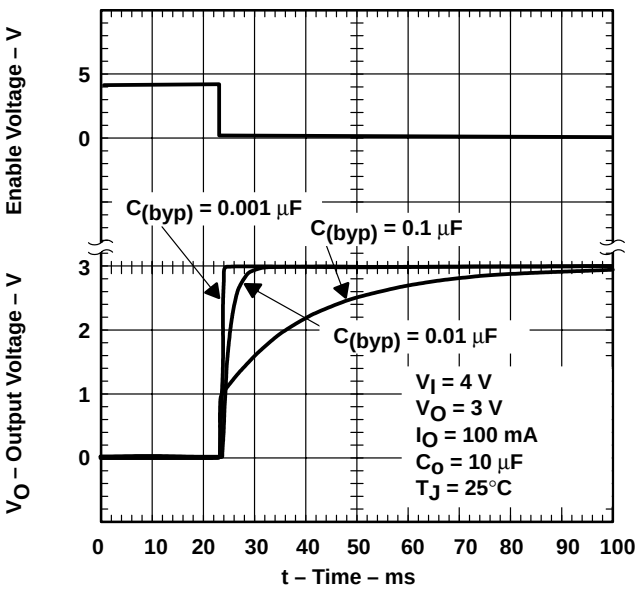



**Figure 19**

## TYPICAL CHARACTERISTICS

TPS78915
LINE TRANSIENT RESPONSE

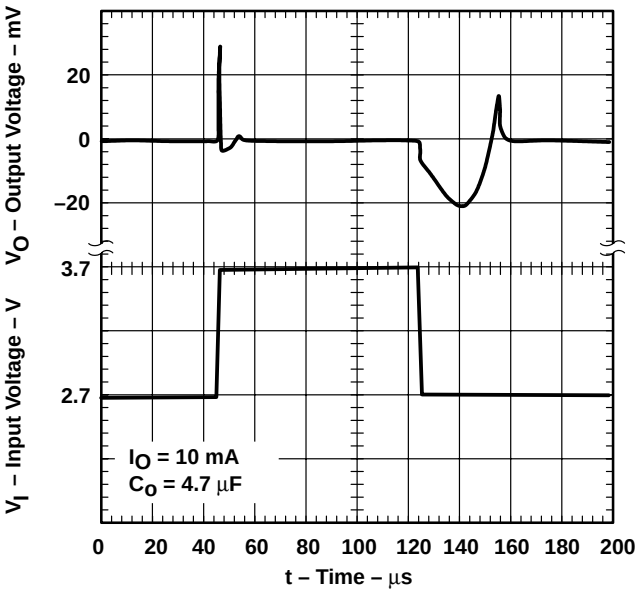



**Figure 20**

TPS78915
LOAD TRANSIENT RESPONSE

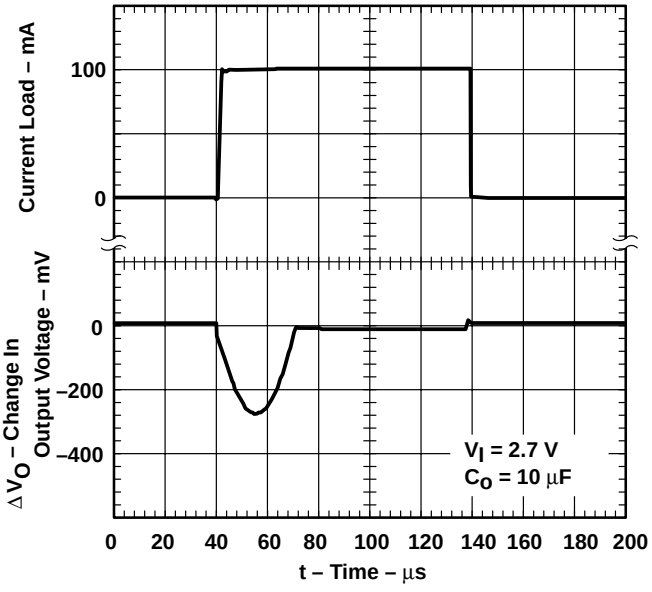



**Figure 21**

TPS78930
LINE TRANSIENT RESPONSE

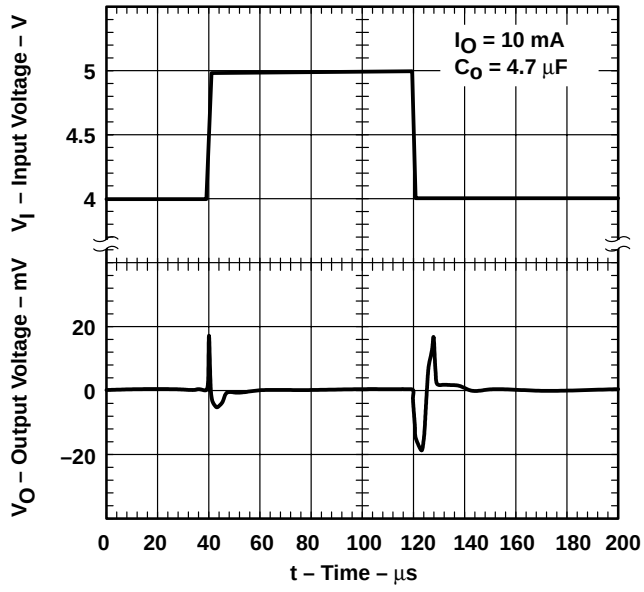



**Figure 22**

TPS78930
LOAD TRANSIENT RESPONSE

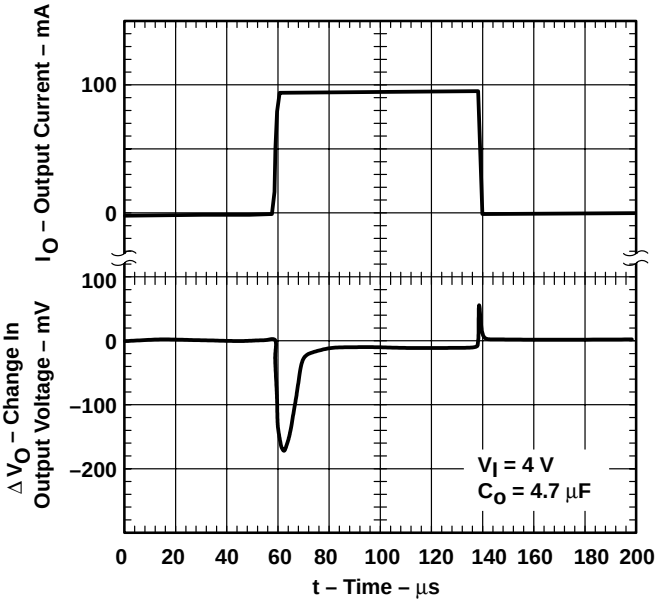



**Figure 23**

## TYPICAL CHARACTERISTICS

**TPS78930**
**TYPICAL REGIONS OF STABILITY**
**EQUIVALENT SERIES RESISTANCE (ESR)**
**vs**
**OUTPUT CURRENT**

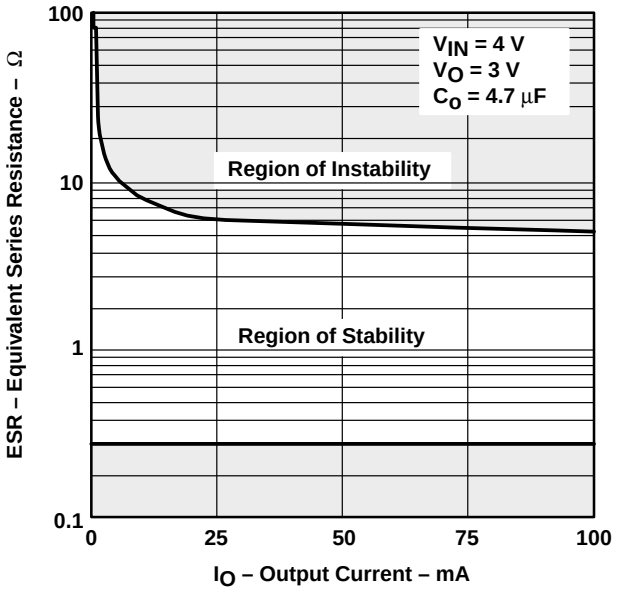



Figure 24

**TPS78930**
**TYPICAL REGIONS OF STABILITY**
**EQUIVALENT SERIES RESISTANCE (ESR)**
**vs**
**OUTPUT CURRENT**

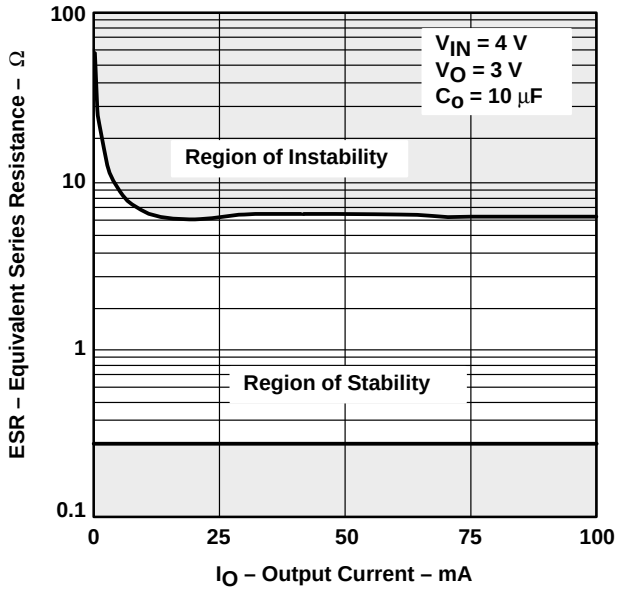



Figure 25

## APPLICATION INFORMATION

The TPS789xx family of low-dropout (LDO) regulators have been optimized for use in battery-operated equipment. They feature extremely low dropout voltages, low output noise, low quiescent current (17 μA typically), and enable inputs to reduce supply currents to 1 μA when the regulators are turned off.

A typical application circuit is shown in Figure 26.

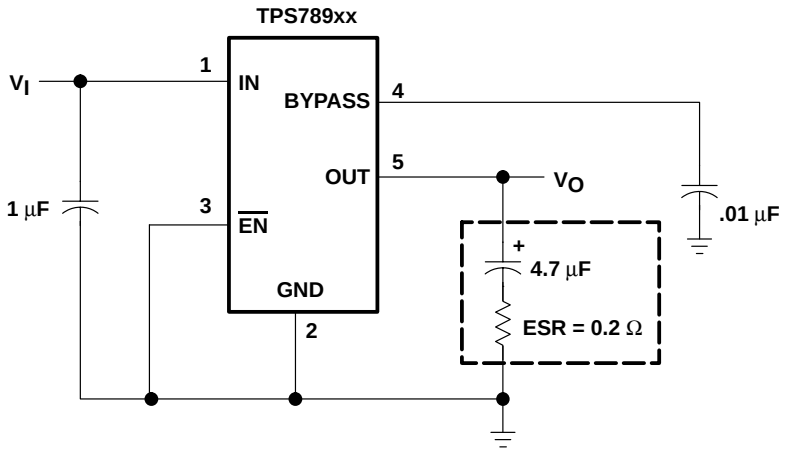



**Figure 26. Typical Application Circuit**

### external capacitor requirements

Although not required, a 0.047-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS789xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS789xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μF. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω. to ensure stability. Capacitor values larger than 4.7 μF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 μF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

**CAPACITOR SELECTION**

| PART NO. | MFR. | VALUE | MAX ESR† | SIZE (H × L × W)† |
|---|---|---|---|---|
| T494B475K016AS | KEMET | 4.7 μF | 1.5 Ω | 1.9 × 3.5 × 2.8 |
| 195D106x0016x2T | SPRAGUE | 10 μF | 1.5 Ω | 1.3 × 7.0 × 2.7 |
| 695D106x003562T | SPRAGUE | 10 μF | 1.3 Ω | 2.5 × 7.6 × 2.5 |
| TPSC475K035R0600 | AVX | 4.7 μF | 0.6 Ω | 2.6 × 6.0 × 3.2 |

† Size is in mm. The ESR maximum resistance is in ohms at 100 kHz and $T_A$ = 25°C. Contact the manufacturer for the minimum ESR values.

## APPLICATION INFORMATION

### external capacitor requirements (continued)

The external bypass capacitor, used in conjunction with an internal resistor to form a low-pass filter, should be a low ESR ceramic capacitor. For example, the TPS78930 exhibits only 56 $\mu V_{RMS}$ of output voltage noise using a 0.01 μF ceramic bypass capacitor and a10 μF ceramic output capacitors. Note that the output will start up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 150 kΩ resistor and external capacitor.

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

$T_A$ is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

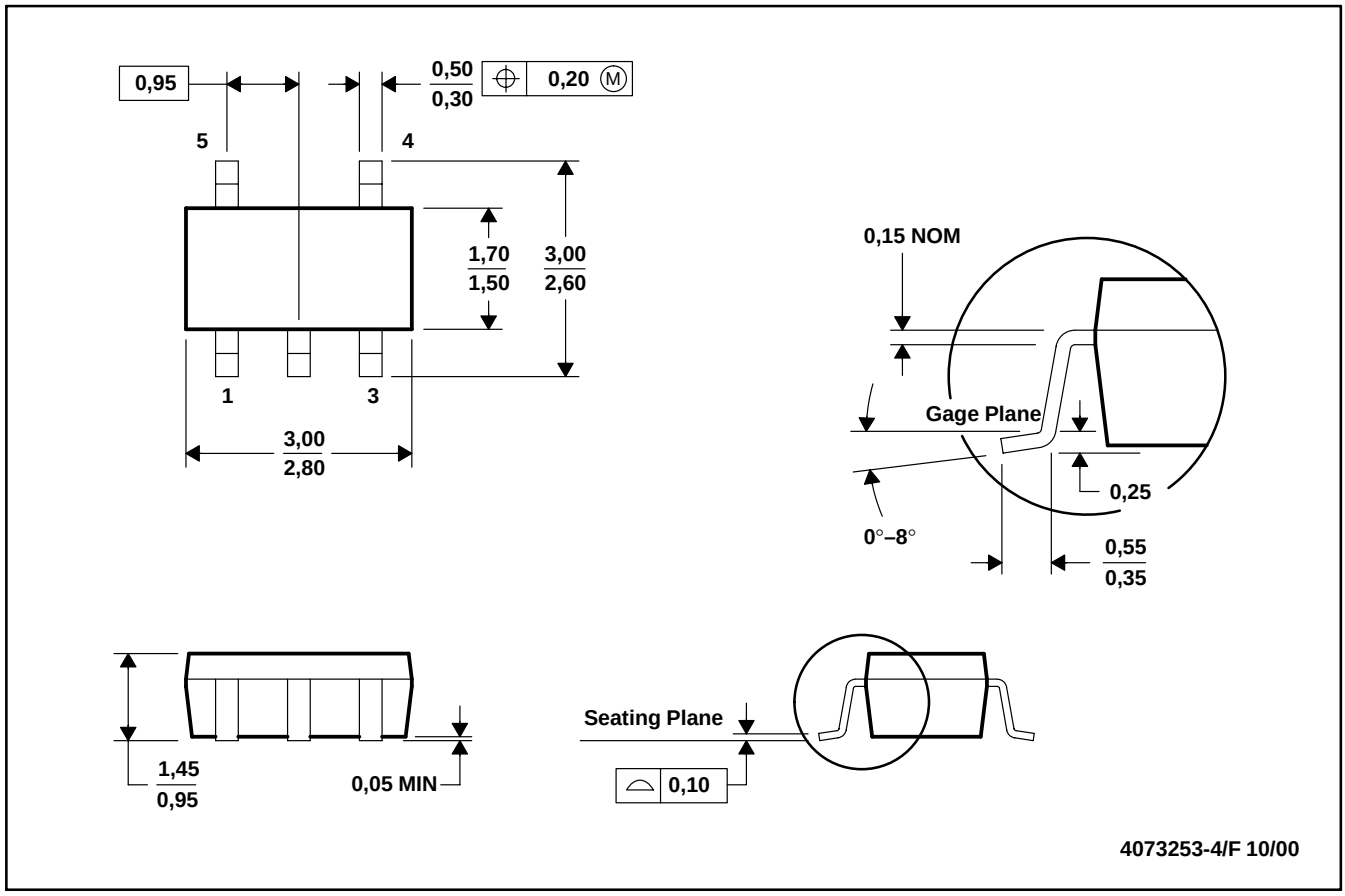
### regulator protection

The TPS789xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS789xx features internal current limiting and thermal protection. During normal operation, the TPS789xx limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

## MECHANICAL DATA

**DBV (R-PDSO-G5)** **PLASTIC SMALL-OUTLINE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS78915DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDWI | Samples |
| TPS78915DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDWI | Samples |
| TPS78918DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDXI | Samples |
| TPS78918DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDXI | Samples |
| TPS78925DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDYI | Samples |
| TPS78925DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDYI | Samples |
| TPS78925DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDYI | Samples |
| TPS78928DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDZI | Samples |
| TPS78928DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PDZI | Samples |
| TPS78930DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PEAI | Samples |
| TPS78930DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PEAI | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

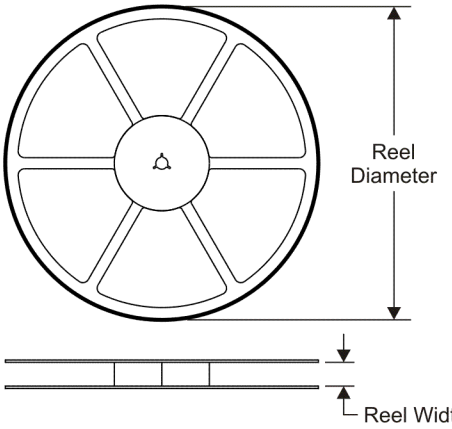
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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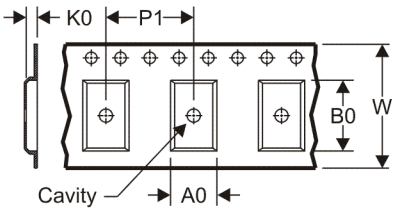
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

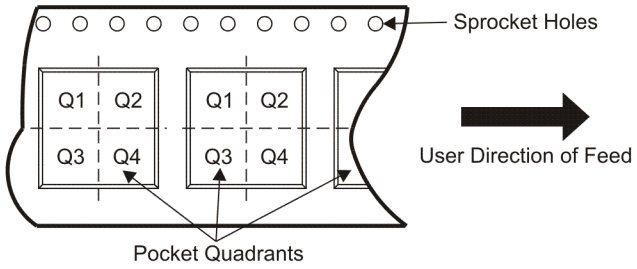



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

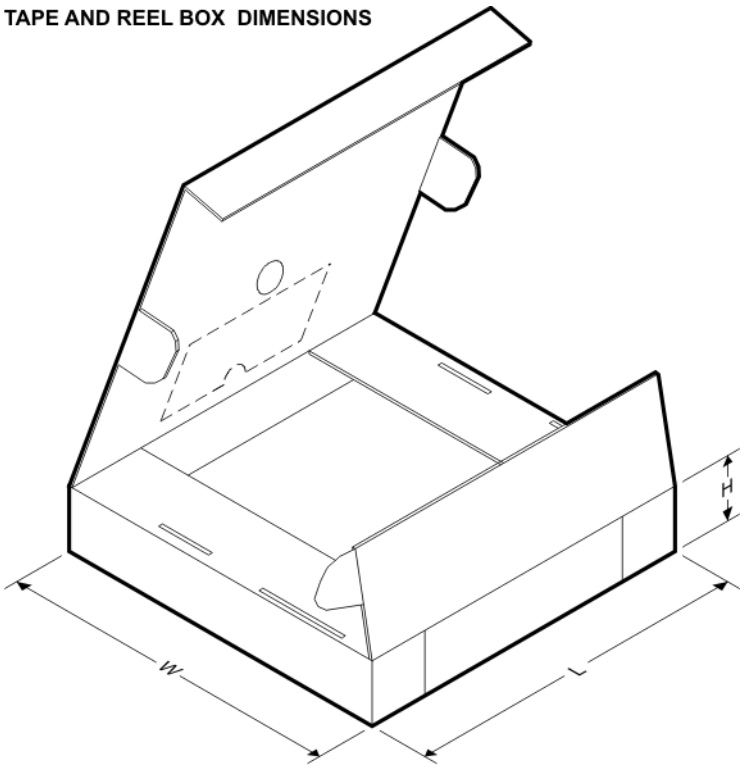
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS78915DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78915DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78918DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78918DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78925DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78925DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78928DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78928DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78930DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78930DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS78915DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS78915DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TPS78918DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS78918DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TPS78925DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS78925DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TPS78928DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS78928DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TPS78930DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS78930DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |

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