DRV8834 Dual-Bridge Stepper or DC Motor Driver

1 Features

- Dual-H-Bridge Current-Control Motor Driver
  - Capable of Driving Two DC Motors or One Stepper Motor
- Two Control Modes:
  - Built-In Indexer Logic With Simple STEP/DIRECTION Control and Up to 1/32-Step Microstepping
  - PHASE/ENABLE Control, With the Ability to Drive External References for > 1/32-Step Microstepping
- Output Current 1.5-A Continuous, 2.2-A Peak per H-Bridge (at V_M = 5 V, 25°C)
- Low $R_{DS(ON)}$: 305-mΩ HS + LS (at V_M = 5 V, 25°C)
- Wide Power Supply Voltage Range: 2.5 V to 10.8 V
- Dynamic t_{BLANK} and Mixed Decay Modes for Smooth Microstepping
- PWM Winding Current Regulation and Limiting
- Thermally Enhanced Surface-Mount Package

2 Applications

- Battery-Powered Toys
- POS Printers
- Video Security Cameras
- Office Automation Machines
- Gaming Machines
- Robotics

3 Description

The DRV8834 provides a flexible motor driver solution for toys, printers, cameras, and other mechatronic applications. The device has two H-bridge drivers, and is intended to drive a bipolar stepper motor or two DC motors.

The output driver block of each H-bridge consists of N-channel power MOSFETs configured as an H-bridge to drive the motor windings. Each H-bridge includes circuitry to regulate or limit the winding current.

With proper PCB design, each H-bridge of the DRV8834 can driving up to 1.5-A RMS (or DC) continuously, at 25°C with a V_M supply of 5 V. The device can support peak currents of up to 2.2 A per bridge. Current capability is reduced slightly at lower V_M voltages.

Internal shutdown functions with a fault output pin are provided for overcurrent protection, short-circuit protection, undervoltage lockout and overtemperature. A low-power sleep mode is also provided.

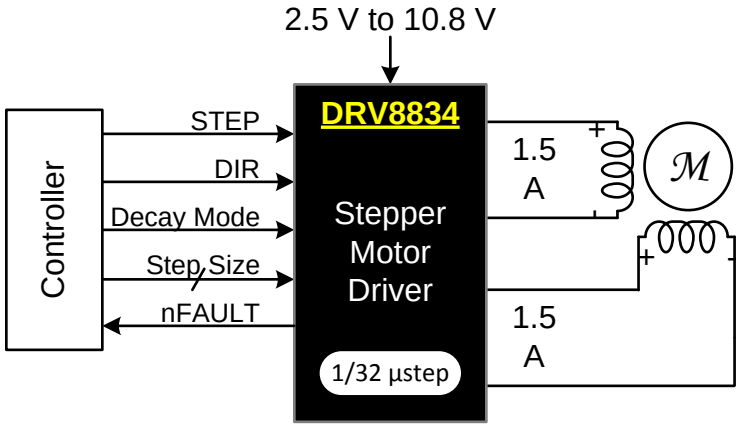
The DRV8834 is packaged in a 24-pin HTSSOP or VQFN package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8834	HTSSOP (24)	7.80 mm × 4.40 mm
	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

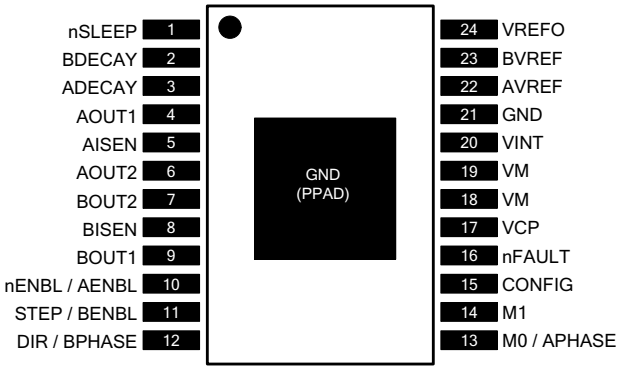
Changes from Revision C (June 2013) to Revision D **Page**

- Added *ESD Ratings table*, *Features Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information table*. ... 3

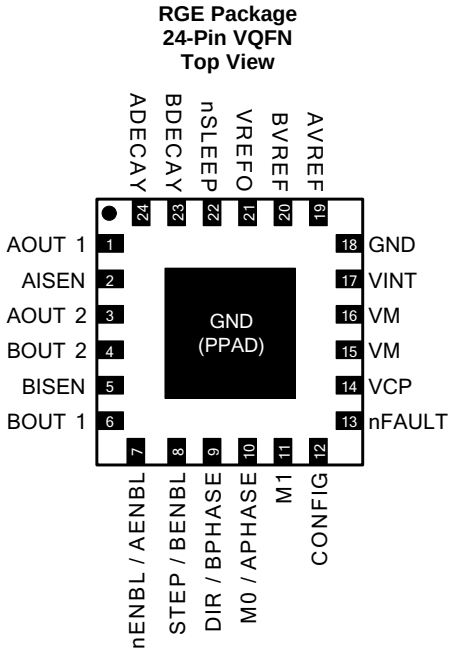
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6 Pin Configuration and Functions

PWP Package
24-Pin HTSSOP
Top View



RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN			I/O	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	HTSSOP	VQFN			
POWER AND GROUND					
GND	21, PPAD	18, PPAD	—	Device ground	Both the GND pin and device PowerPAD must be connected to ground
VM	18, 19	15, 16	—	Bridge A power supply	Connect to motor supply. A 10-µF (minimum) capacitor to GND is recommended.
VINT	20	17	—	Internal supply	Bypass to GND with 2.2-µF (minimum), 6.3-V capacitor. Can be used to provide logic high voltage for configuration pins (except nSLEEP).
VREFO	24	21	O	Reference voltage output	May be connected to AVREF/BVREF inputs. Do not place a bypass capacitor on this pin.
VCP	17	14	O	High-side gate drive voltage	Connect a 0.01-µF, 16-V (minimum) X7R ceramic capacitor to VM.
CONTROL (INDEXER MODE OR PHASE/ENABLE MODE)					
nENBL/AENBL	10	7	I	Step motor enable/Bridge A enable	Indexer mode: Logic low enables all outputs. Phase/enable mode: Logic high enables the AOUTx outputs. Internal pulldown.
STEP/BENBL	11	8	I	Step input/Bridge B enable	Indexer mode: Rising edge moves indexer to next step. Phase/enable mode: Logic high enables the BOUTx outputs. Internal pulldown.
DIR/BPHASE	12	9	I	Direction input/Bridge B Phase	Indexer mode: Level sets direction of step. Phase/enable mode: Logic high sets BOUT1 high, BOUT2 low. Internal pulldown.

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Pin Functions (continued)

PIN			I/O	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	HTSSOP	VQFN			
M0/APHASE	13	10	I	Microstep mode/Bridge A phase	Indexer mode: Controls microstep mode (full, half, up to 1/32-step) along with M1. Phase/enable mode: Logic high sets AOUT1 high, AOUT2 low. Internal pulldown.
M1	14	11	I	Microstep mode/Disable state	Indexer mode: Controls microstep mode (full, half, up to 1/32-step) along with M0. Phase/enable mode: Determines the state of the outputs when xENBL = 0. Internal pulldown.
CONFIG	15	12	I	Device configuration	Logic high to put the device in indexer mode. Logic low to put the device into phase/enable mode. State is latched at power up and sleep exit. Internal pulldown.
nSLEEP	1	22	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode and reset all internal logic.
AVREF	22	19	I	Bridge A current set reference input	Reference voltage for AOUT winding current. In Indexer Mode, it should be tied to a reference voltage for the internal DAC (for example, VREFO). In Phase/Enable Mode, an external DAC can drive it for microstepping.
BVREF	23	20	I	Bridge B current set reference input	Reference voltage for BOUT winding current. In Indexer Mode, it should be tied to a reference voltage for the internal DAC (for example, VREFO). In Phase/Enable Mode, an external DAC can drive it for microstepping.
ADECAY	3	24	I	Decay mode for bridge A	Determines decay mode for H-Bridge A (or A and B in indexer mode) – slow, fast or mixed decay
BDECAY	2	23	I	Decay mode for bridge B	Determines decay mode for H-Bridge B – slow, fast or mixed decay
STATUS					
nFAULT	16	13	OD	Fault output	Logic low when in fault condition (overtemp, overcurrent, undervoltage)
OUTPUT					
AISEN	5	2	IO	Bridge A ground/Isense	Connect to current sense resistor for bridge A, or GND if current control not needed
BISEN	8	5	IO	Bridge B ground/Isense	Connect to current sense resistor for bridge B, or GND if current control not needed
AOUT1	4	1	O	Bridge A output 1	Connect to motor winding A
AOUT2	6	3	O	Bridge A output 2	
BOUT1	9	6	O	Bridge B output 1	Connect to motor winding B
BOUT2	7	4	O	Bridge B output 2	

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
VM	Power supply voltage	–0.3	11.8	V
AVREF, BVREF, VINT, ADECAY, BDECAY	Analog input pin voltage	–0.5	3.6	V
	Digital input pin voltage	–0.5	7	V
	xISEN pin voltage	–0.3	0.5	V
	Peak motor drive output current, t < 1 µs	Internally limited		A
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	2.5		10.8	V
V_{REF}	VREF input voltage range(2)	1		2.1	V
I_{VINT}	VINT external load current			1	mA
I_{VREF}	VREF external load current			400	µA
V_{DIGIN}	Digital input pin voltage range	–0.3		5.75	V
I_{OUT}	Continuous RMS or DC output current per bridge(3)			1.5	A

(1) $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.
(3) Power dissipation and thermal limits must be observed.

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7.4 Thermal Information

THERMAL METRIC(1)		DRV8834		UNIT
		PWP [HTSSOP]	RGE [VQFN]	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.2	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.7	36.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.9	12.2	
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.6	
ψ_{JB}	Junction-to-board characterization parameter	21.7	12.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	V_M = 5 V, excluding winding current		2.4	4	mA
		V_M = 10 V, excluding winding current		2.75		
I_{VMQ}	VM sleep mode supply current	V_M = 5 V		0.6	2	µA
		V_M = 10 V		9.6		
V_{UVLO}	VM undervoltage lockout voltage	V_M falling			2.39	V
INTERNAL REGULATORS						
V_{INT}	VINT voltage	V_M > 3.3 V, I_{OUT} = 0 A to 1 mA	2.85	3	3.15	V
V_{REFO}	VREF voltage	I_{OUT} = 0 A to 400 µA	1.9	2	2.1	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage	nSLEEP			0.5	V
		All other digital input pins			0.7	
V_{IH}	Input high voltage	nSLEEP	2.5			V
		All other digital input pins	2			
V_{HYS}	Input hysteresis	nSLEEP		0.2		V
		All except nSLEEP		0.4		
R_{PD}	Input pulldown resistance	nSLEEP		500		kΩ
		All except nSLEEP, M0		200		
I_{IL}	Input low current	VIN = 0			1	µA
I_{IN}	Input current (M0)		-20		20	µA
I_{IH}	Input high current	VIN = 3.3 V, nSLEEP		6.6	13	µA
		VIN = 3.3 V, all except nSLEEP		16.5	33	
t_{DEG}	Input deglitch time		312		468	ns
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
H-BRIDGE FETs						
$R_{DS(ON)}$	HS FET ON-resistance	V_M = 5 V, I_O = 500 mA, T_J = 25°C		160	250	mΩ
		V_M = 5 V, I_O = 500 mA, T_J = 85°C		190		
		V_M = 2.7 V, I_O = 500 mA, T_J = 25°C		200	295	
		V_M = 2.7 V, I_O = 500 mA, T_J = 85°C		240		
	LS FET ON-resistance	V_M = 5 V, I_O = 500 mA, T_J = 25°C		145	240	
		V_M = 5 V, I_O = 500 mA, T_J = 85°C		180		
		V_M = 2.7 V, I_O = 500 mA, T_J = 25°C		190	285	
		V_M = 2.7 V, I_O = 500 mA, T_J = 85°C		235		
I_{OFF}	Off-state leakage current		–2		2	µA
MOTOR DRIVER						
f_{PWM}	Current control PWM frequency	Internal PWM frequency		42.5		kHz
t_{BLANK}	Current sense blanking time	V_{REF} > 375 mV or DAC codes > 29%		2.4		µs
		V_{REF} < 375 mV or DAC codes < 29%		1.6		
t_R	Rise time	V_M = 5 V, 16 Ω to GND, 10% to 90% V_M		120		ns
t_F	Fall time	V_M = 5 V, 16 Ω to GND, 10% to 90% V_M		100		ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2			A
t_{OCP}	Overcurrent protection period	V_{REF} > 375 mV or DAC codes > 29%		1.6		µs
		V_{REF} < 375 mV or DAC codes < 29%		1.1		

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Electrical Characteristics (continued)

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	VREF input current	VREF = 3.3 V	–1		1	µA
V_{TRIP}	xISEN trip voltage	For 100% current step		xVREF/5		V
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

7.6 Timing Requirements

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
1	f_{STEP}	Step frequency			250	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1.9			µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1.9			µs
4	$t_{SU(STEP)}$	Setup time, command to STEP rising	200			ns
5	$t_{H(STEP)}$	Hold time, command to STEP rising	1			µs
6	t_{WAKE}	Wake-up time, nSLEEP inactive to STEP			1	ms

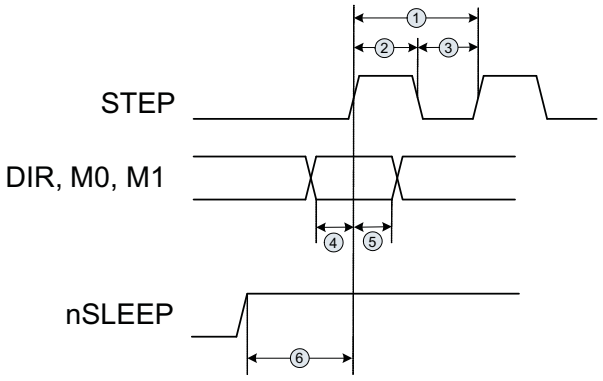


Figure 1. Timing Diagram

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7.7 Typical Characteristics

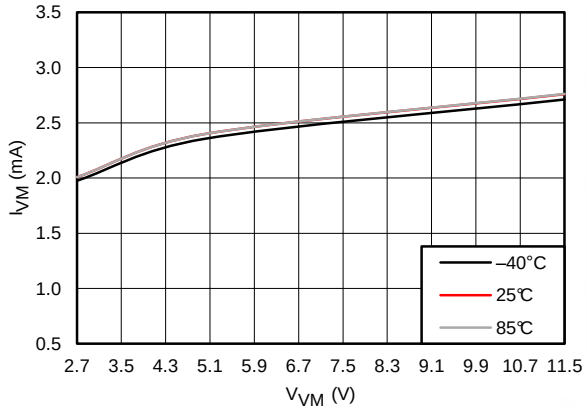


Figure 2. Operating Current

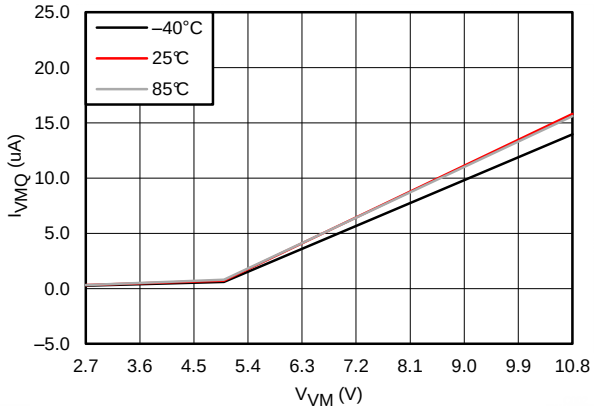


Figure 3. Sleep Current

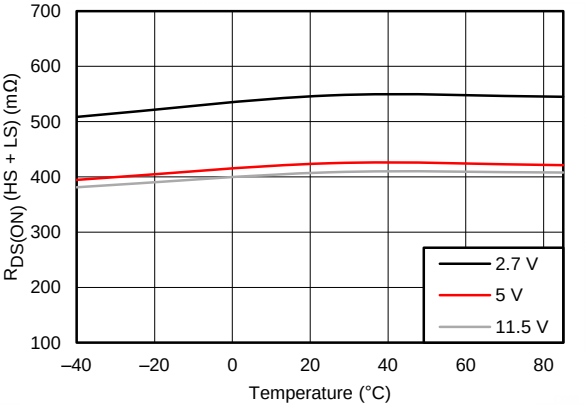


Figure 4. $R_{DS(ON)}$

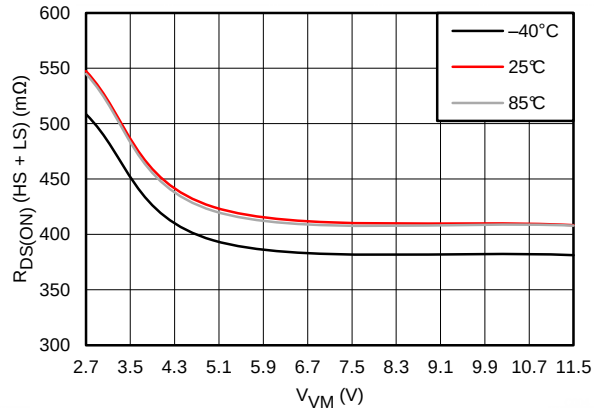


Figure 5. $R_{DS(ON)}$

8 Detailed Description

8.1 Overview

The DRV8834 supports two configurations: phase/enable mode, where the outputs are controlled by phase (direction) and enable signals for each H-bridge, and indexer mode, which allow control of a stepper motor using simple step and direction inputs.

DC motors can only be controlled in phase/enable mode; indexer mode is not applicable to DC motors.

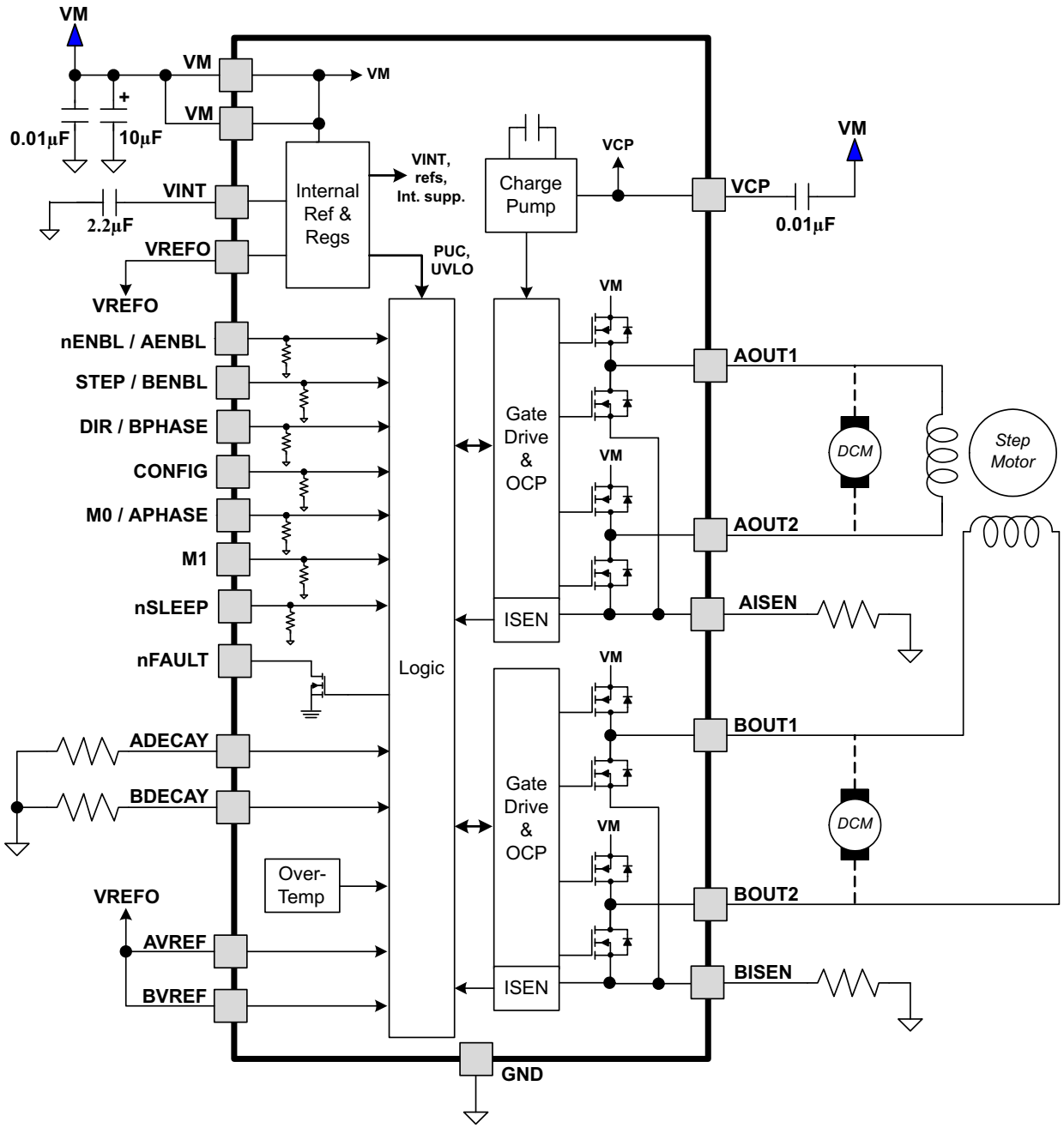
Stepper motors can be controlled using either phase/enable load, or indexer mode.

The device is configured to be controlled either way using CONFIG pin. Logic HIGH on the CONFIG pin puts the device in the STEP/DIR mode; logic LOW lets the motor to be controlled using the xPHASE/xENBL pins.

The state of the CONFIG pin is latched at power up, and also whenever exiting sleep mode. CONFIG has an internal pulldown resistor.

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8.2 Functional Block Diagram



8.3 Feature Description

DRV8834 contains two identical H-bridge motor drivers with current-control PWM circuitry. A block diagram of the circuitry is shown in Figure 6:

Feature Description (continued)

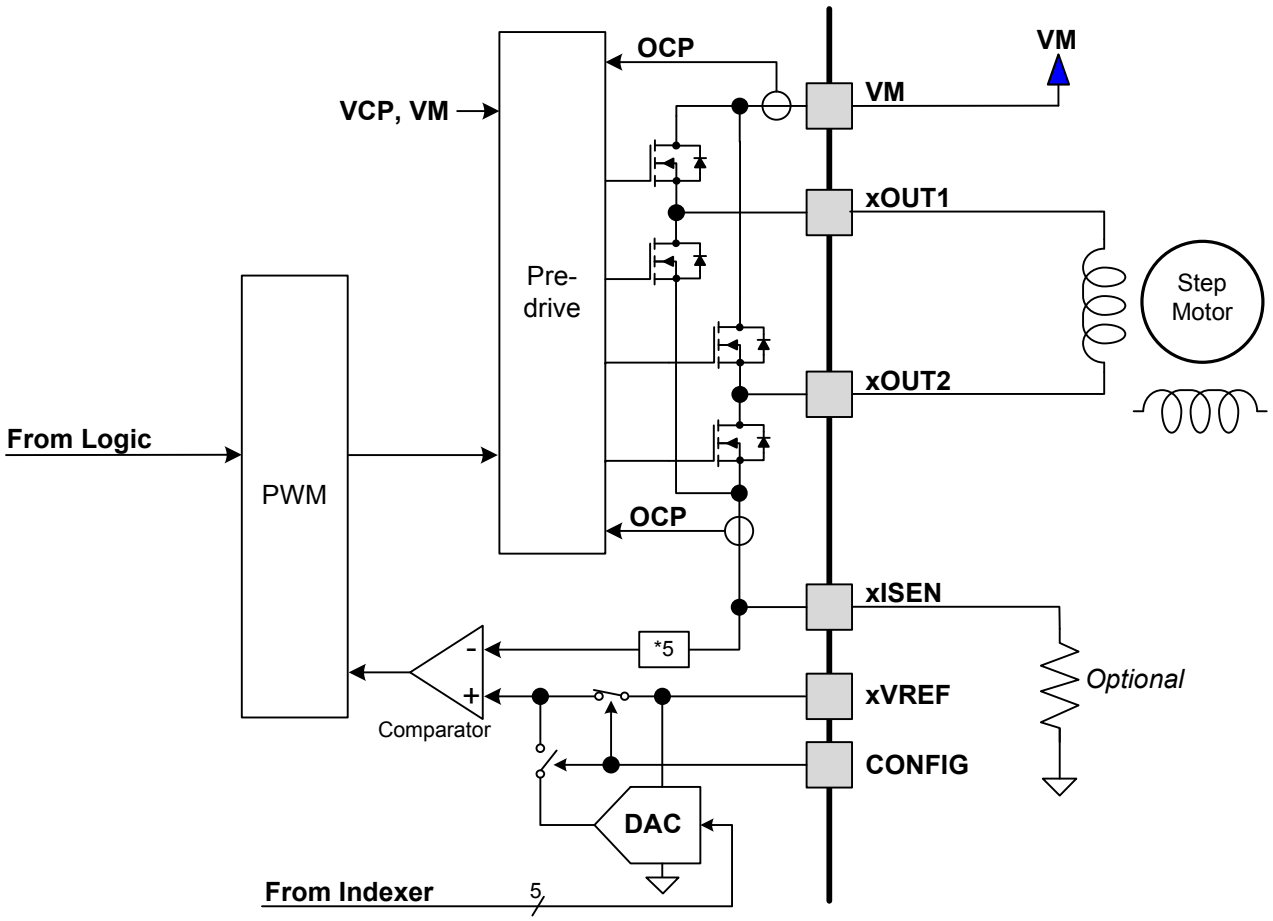


Figure 6. Motor Control Circuitry

8.3.1 Current Control

The current through the motor windings may be regulated by a fixed-frequency PWM current regulation (current chopping).

With stepping motors, current control is normally used at all times. Often it is used to vary the current in the two windings in a sinusoidal fashion to provide smooth motion. This is referred to as microstepping. The DRV8834 can provide up to 1/32 step microstepping, using internal 5-bit DACs. Finer microstepping can be implemented using the xPHASE/xENBL signals to control the stepper motor, and varying the xVREF voltages. The current flowing through the corresponding H-bridge varies according to the equation given below. A very high degree of microstepping can be achieved through this technique.

With DC motors, current control can be used to limit the start-up current of the motor to less than the stall current of the motor.

Current regulation works as follows:

When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Immediately after the current is enabled, the voltage on the xISEN pin is ignored for a period of time before enabling the current sense circuitry. This blanking time also sets the minimum on time of the PWM when operating in current chopping mode.

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Feature Description (continued)

The blanking time also sets the minimum PWM duty cycle. This can cause current control errors near the zero current level when microstepping. To help eliminate this error, the DRV8834 has a *dynamic* t_{BLANK} time. When the commanded current is low, the blanking period is reduced, which in turn lowers the minimum duty cycle. This provides a smoother current transition across the zero crossing region of the current waveform. The end result is smoother and quieter motor operation.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, with a reference voltage supplied to the AVREF and BVREF pins. In indexer mode, the reference voltages are scaled by internal DACs to provide scaled currents used to perform microstepping.

The chopping current is calculated as follows:

$$Full\text{-}Scale\ I_{TRIP} = \frac{xVREF}{5 \bullet R_{ISENSE}} \quad (1)$$

Example: If xVREF is 2 V (as it would be if xVREF is connected directly to VREFO) and a 400-mΩ sense resistor is used, the chopping current will be 2 V / 5 × 400 mΩ = 1 A.

In indexer mode, this current value is scaled by between 5% and 100% by the internal DACs, as shown in the step table in the "Microstepping Indexer" section of the data sheet.

If current control is not needed, the xISEN pins may be connected directly to ground. In this case, TI also recommends connecting AVREF and BVREF directly to VREFO.

8.3.2 Current Recirculation and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7 as case 1. The current flow direction shown indicates positive current flow in the step table below for indexer mode, or the current flow with xPHASE = 1 in phase/enable mode.

Once the chopping current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in through the opposing FETs. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 7 as case 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. Slow decay is shown as case 3 in Figure 7.

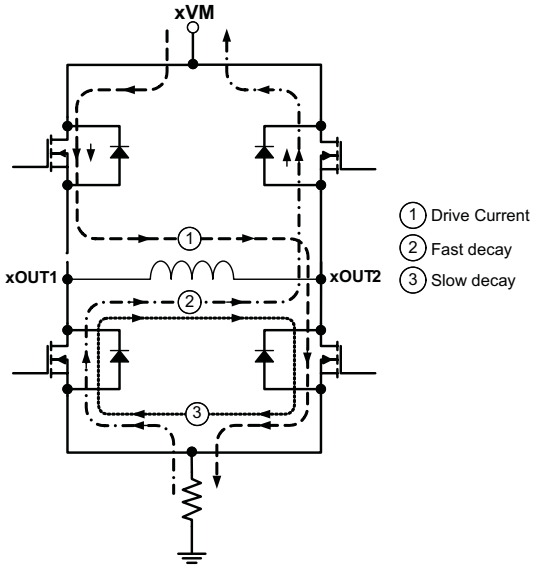


Figure 7. Decay Modes

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Feature Description (continued)

The DRV8834 supports fast, slow, and also mixed decay modes. With DC motors, slow decay is nearly always used to minimize current ripple and optimize speed control; with stepper motors, the decay mode is chosen for a given stepper motor and operating conditions to minimize mechanical noise and vibration.

In mixed decay mode, the current recirculation begins as fast decay, but at a fixed period of time (determined by the state of the xDECAY pins shown in Table 1) switches to slow decay mode for the remainder of the fixed PWM period.

Table 1. Decay Pin Configuration

RESISTANCE ON xDECAY PIN	-OR- VOLTAGE FORCED ON xDECAY PIN	% OF PWM CYCLE IS FAST DECAY
< 1 kΩ	< 0.1 V	0%
20 kΩ ±5%	0.2 V ±5%	25%
50 kΩ ±5%	0.5 V ±5%	50%
100 kΩ ±5%	1 V ±5%	75%
> 200 kΩ	> 2 V	100%

Figure 8 shows the current waveforms in slow, 25% mixed, and fast decay modes.

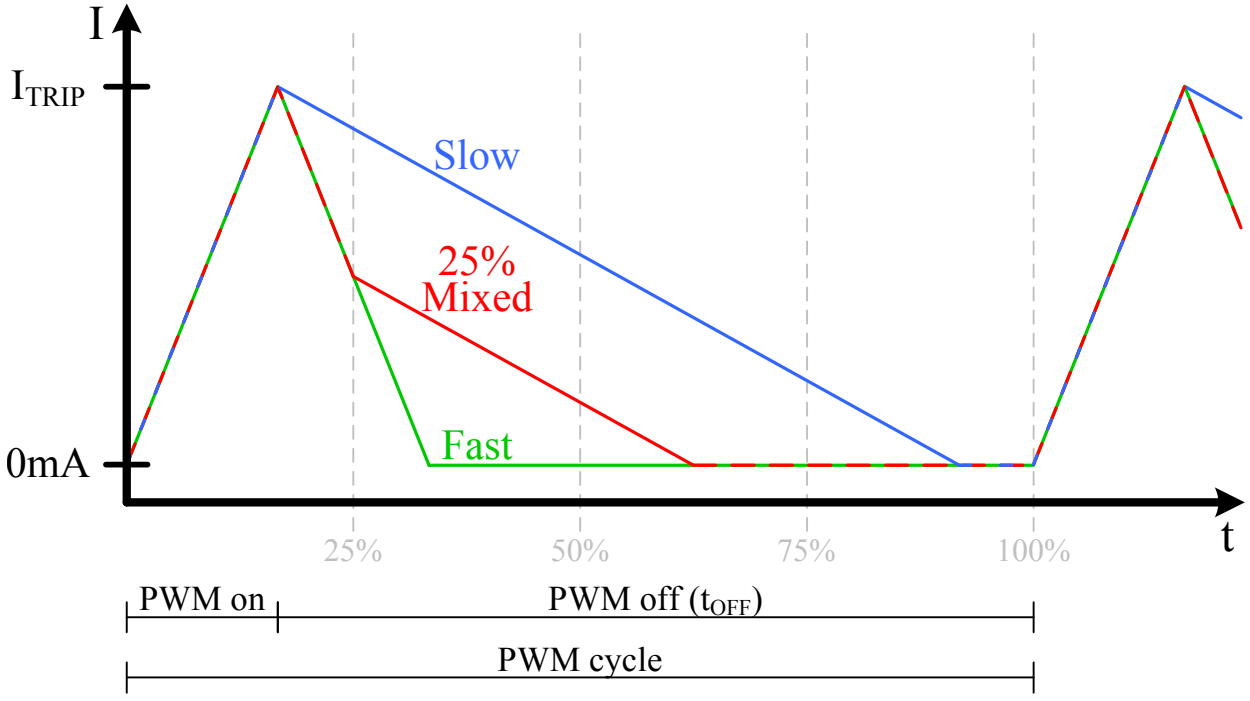


Figure 8. Current Decay Modes

Decay mode is selected by the voltage present on the xDECAY pins. Internal current sources of 10 µA (typical) are connected to the pins, which allows setting of the decay mode by a resistor connected to ground if desired.

It is possible to drive the xDECAY pin with a tristate GPIO pin and also place the resistor to ground. This allows a microcontroller to select fast, slow, or mixed decay modes by driving the pin high, low, or high-impedance. The logic-low voltage must be less than 0.1 V with 10-µA of current sourced from the DRV8834 to attain slow decay.

In indexer mode, only the ADECAY pin is used, and slow decay mode is always used when at any point in the step table where the current is increasing. When current is decreasing or remaining constant, the decay mode used will be fast, slow, or mixed, as commanded by the ADECAY pin.

8.3.3 Protection Circuits

The DRV8834 is fully protected against undervoltage, overcurrent and overtemperature events.

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8.3.3.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge are disabled and the nFAULT pin are driven low. The driver will be re-enabled after the OCP retry period (approximately 1.2 ms) has passed. nFAULT becomes high again at this time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted. Only the H-bridge in which the OCP is detected will be disabled while the other bridge will function normally.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for PWM current control, so functions even without presence of the xISEN resistors.

8.3.3.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. When the die temperature falls to a safe level, operation automatically resumes and nFAULT becomes inactive.

8.3.3.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. The nFAULT pin is driven low during an undervoltage condition, and also at power up or sleep mode, until the internal power supplies have stabilized.

8.4 Device Functional Modes

8.4.1 Phase/Enable Mode

In phase/enable mode, the xPHASE input pins control the direction of current flow through each H-bridge. This sets the direction of rotation of a DC motor, or the direction of the current flow in a stepper motor winding. Driving the xENBL input pins active high enables the H-bridge outputs. This can be used as PWM speed control of a DC motor, or to enable/disable the current in a stepper motor.

In phase/enable mode, the M1 input pin controls the state of the H-bridges when xENBL = 0. If M1 is high, the outputs are disabled (high impedance) when xENBL = 0; this corresponds to asynchronous fast decay mode, and is usually used in stepper motor applications to command a "zero current" state. If M1 is low, then the outputs are both driven low; this corresponds to slow decay or brake mode, and is usually used when controlling the speed of a DC motor by PWMing the xENBL pin.

Table 2. H-Bridge Control Using Phase/Enable Mode

M1	xENBL	xPHASE	xOUT1	xOUT2
1	0	X	Z	Z
0	0	X	0	0
X	1	0	L	H
X	1	1	H	L

8.4.2 Indexer Mode

To allow a simple step and direction interface to control stepper motors, the DRV8834 contains a microstepping indexer. The indexer controls the state of the H-bridges automatically. Whenever there is a rising edge at the STEP input, the indexer moves to the next step, according to the direction set by the DIR pin.

The nENBL pin is used to disable the output stage in indexer mode. When nENBL = 1, the indexer inputs are still active and will respond to the STEP and DIR input pins; only the output stage is disabled.

The indexer logic in the DRV8834 allows a number of different stepping configurations. The M0 and M1 pins are used to configure the stepping format as shown in Table 3.

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Table 3. Stepping Format

M1	M0	STEP MODE
0	0	Full step (2-phase excitation)
0	1	1/2 step (1-2 phase excitation)
0	Z	1/4 step (W1-2 phase excitation)
1	0	8 microsteps/step
1	1	16 microsteps/step
1	Z	32 microsteps/step

The M0 pin is a tri-level input. It can be driven logic low, logic high, or high-impedance (Z).

The M0 and M1 pins can be statically configured by connecting to VINT, GND, or left open, or can be driven with standard tristate microcontroller I/O port pins. Their state is latched at each rising edge of the STEP input.

The step mode may be changed on-the-fly while the motor is moving. The indexer will advance to the next valid state for the new M0/M1 setting at the next rising edge of STEP.

The home state is 45°. This state is entered after power up, after exiting undervoltage lockout, or after exiting sleep mode. This is shown in Table 4 by cells shaded yellow.

Table 4 shows the relative current and step directions for different step mode settings. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

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Table 4. Current and Step Directions

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
1	1	1	1	1		100%	0%	0
2						100%	5%	3
3	2					100%	10%	6
4						99%	15%	8
5	3	2				98%	20%	11
6						97%	24%	14
7	4					96%	29%	17
8						94%	34%	20
9	5	3	2			92%	38%	23
10						90%	43%	25
11	6					88%	47%	28
12						86%	51%	31
13	7	4				83%	56%	34
14						80%	60%	37
15	8					77%	63%	39
16						74%	67%	42
17	9	5	3	2	1	71%	71%	45
18						67%	74%	48
19	10					63%	77%	51
20						60%	80%	53
21	11	6				56%	83%	56
22						51%	86%	59
23	12					47%	88%	62
24						43%	90%	65
25	13	7	4			38%	92%	68
26						34%	94%	70
27	14					29%	96%	73
28						24%	97%	76
29	15	8				20%	98%	79
30						15%	99%	82
31	16					10%	100%	84
32						5%	100%	87
33	17	9	5	3		0%	100%	90
34						–5%	100%	93
35	18					–10%	100%	96
36						–15%	99%	98
37	19	10				–20%	98%	101
38						–24%	97%	104
39	20					–29%	96%	107
40						–34%	94%	110
41	21	11	6			–38%	92%	113
42						–43%	90%	115
43	22					–47%	88%	118
44						–51%	86%	121
45	23	12				–56%	83%	124
46						–60%	80%	127
47	24					–63%	77%	129

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Table 4. Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
48						–67%	74%	132
49	25	13	7	4	2	–71%	71%	135
50						–74%	67%	138
51	26					–77%	63%	141
52						–80%	60%	143
53	27	14				–83%	56%	146
54						–86%	51%	149
55	28					–88%	47%	152
56						–90%	43%	155
57	29	15	8			–92%	38%	158
58						–94%	34%	160
59	30					–96%	29%	163
60						–97%	24%	166
61	31	16				–98%	20%	169
62						–99%	15%	172
63	32					–100%	10%	174
64						–100%	5%	177
65	33	17	9	5		–100%	0%	180
66						–100%	–5%	183
67	34					–100%	–10%	186
68						–99%	–15%	188
69	35	18				–98%	–20%	191
70						–97%	–24%	194
71	36					–96%	–29%	197
72						–94%	–34%	200
73	37	19	10			–92%	–38%	203
74						–90%	–43%	205
75	38					–88%	–47%	208
76						–86%	–51%	211
77	39	20				–83%	–56%	214
78						–80%	–60%	217
79	40					–77%	–63%	219
80						–74%	–67%	222
81	41	21	11	6	3	–71%	–71%	225
82						–67%	–74%	228
83	42					–63%	–77%	231
84						–60%	–80%	233
85	43	22				–56%	–83%	236
86						–51%	–86%	239
87	44					–47%	–88%	242
88						–43%	–90%	245
89	45	23	12			–38%	–92%	248
90						–34%	–94%	250
91	46					–29%	–96%	253
92						–24%	–97%	256
93	47	24				–20%	–98%	259
94						–15%	–99%	262

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Table 4. Current and Step Directions (continued)

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 70%	WINDING CURRENT A	WINDING CURRENT B	ELECTRICAL ANGLE
95	48					–10%	–100%	264
96						–5%	–100%	267
97	49	25	13	7		0%	–100%	270
98						5%	–100%	273
99	50					10%	–100%	276
100						15%	–99%	278
101	51	26				20%	–98%	281
102						24%	–97%	284
103	52					29%	–96%	287
104						34%	–94%	290
105	53	27	14			38%	–92%	293
106						43%	–90%	295
107	54					47%	–88%	298
108						51%	–86%	301
109	55	28				56%	–83%	304
110						60%	–80%	307
111	56					63%	–77%	309
112						67%	–74%	312
113	57	29	15	8	4	71%	–71%	315
114						74%	–67%	318
115	58					77%	–63%	321
116						80%	–60%	323
117	59	30				83%	–56%	326
118						86%	–51%	329
119	60					88%	–47%	332
120						90%	–43%	335
121	61	31	16			92%	–38%	338
122						94%	–34%	340
123	62					96%	–29%	343
124						97%	–24%	346
125	63	32				98%	–20%	349
126						99%	–15%	352
127	64					100%	–10%	354
128						100%	–5%	357

8.4.3 nSLEEP Operation

Driving nSLEEP low will put the device into a low-power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, all internal logic is reset (this returns the indexer to the home state), the VINT supply is disabled, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high.

Because the VINT supply is disabled during sleep mode, it cannot be used to provide a logic high signal to the nSLEEP pin. To simplify board design, the nSLEEP can be pulled up directly to the supply (VM) if it is not actively driven. Unless VM is less than 5.75 V, a pullup resistor is required.

The nSLEEP pin is protected by a Zener diode that will clamp the pin voltage to approximately 6.5 V. The pullup resistor limits the current to the input in case VM is higher than 6.5 V. The recommended pullup resistor is 20 kΩ to 50 kΩ.

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When exiting sleep mode, the nFAULT pin will be briefly driven active low as the internal power supplies turn on. nFAULT will return to inactive high once the internal power supplies (including charge pump) have stabilized. This process takes some time (up to 1 ms), before the motor driver becomes fully operational.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8834 is a very flexible motor driver. It can be used to drive two DC motors or a stepper motor, in a number of different configurations.

The following applications schematics show various configurations and connections for the DRV8834.

Component values, especially for RSENSE and the DECAY pins, may be different depending on your motor and application. Refer to the information above to determine the best values for these components in your application.

9.1.1 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 2 A, and a 0.05-Ω sense resistor is used, the resistor will dissipate $2_A^2 \times 0.05\ \Omega = 0.2$ W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

9.2 Typical Application

9.2.1 Phase/Enable Mode Driving Two DC Motors

In this configuration, the DRV8834 is used to drive two independent DC motors. Current up to 1 A per motor is possible. The M1 pin is pulled low to allow slow decay PWM from the controller (if desired) to control the motor speed by PWMing the xENBL inputs, and ADECAY and BDECAY are connected to ground to set slow decay mode during current limiting. The value of the RSENSE resistors shown is for a 1-A current limit; if current limiting is not needed, the AISEN and BISEN pins may be connected directly to ground. If the sleep function is not needed, nSLEEP can be connected to VM with an approximate 47-kΩ resistor.

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Typical Application (continued)

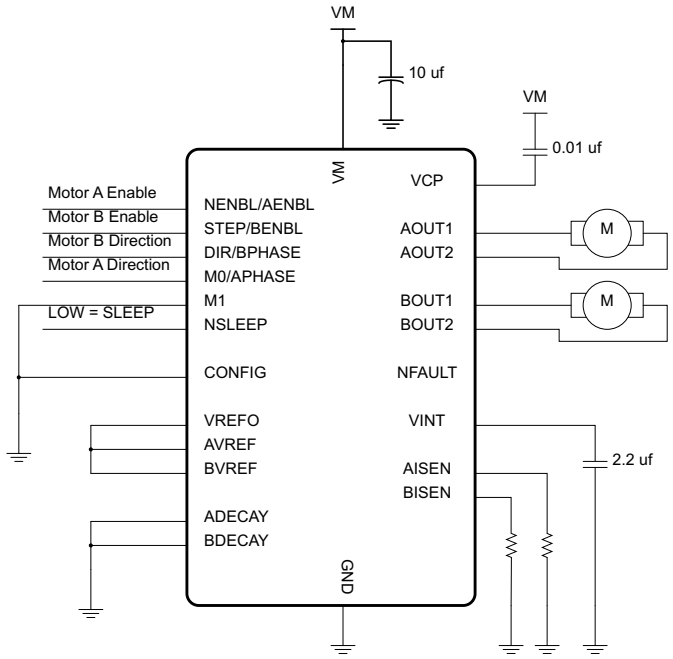


Figure 9. Phase/Enable Mode Driving Two DC Motors

9.2.1.1 Design Requirements

Table 5 lists the design parameters.

Table 5. Design Parameters

PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	VM	10 V
Motor RMS current	I_{RMS}	0.8 A
Motor start-up current	I_{START}	1 A
Motor current trip point	I_{TRIP}	1.5 A

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

9.2.1.2.2 Power Dissipation

The power dissipation of the DRV8834 is a function of RMS motor current and the FET resistance ($_{RDS(ON)}$) of each output.

$$\text{Power} \approx I_{RMS}^2 \times (\text{High-Side } R_{DS(ON)} + \text{Low-Side } R_{DS(ON)}) \quad (2)$$

For this example, the ambient temperature is 35°C, and the junction temperature reaches 65°C. At 65°C, the sum of $R_{DS(ON)}$ is about 1 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat will be $0.8\ A^2 \times 1\ \Omega = 0.64$ W.

The temperature that the DRV8834 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, in order dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8834 had an effective thermal resistance $R_{\theta JA}$ of 47°C/W, and:

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$T_J = T_A + (P_D \times R_{\theta JA}) = 35°C + (0.64\ W \times 47°\ C/W) = 65°C.$ (3)

9.2.1.2.3 Motor Current Trip Point

When the voltage on pin SENSE exceeds V_{TRIP} (0.5 V), overcurrent is detected. The R_{SENSE} resistor should be sized to set the desired I_{TRIP} level.

$R_{SENSE} = 0.5\ V / I_{TRIP}$ (4)

To set I_{TRIP} to 2 A, $R_{SENSE} = 0.5\ V / 2\ A = 0.25\ \Omega$.

To prevent false trips, I_{TRIP} must be higher than regular operating current. Motor current during start-up is typically much higher than steady-state spinning, because the initial load torque is higher, and the absence of back-EMF causes a higher voltage and extra current across the motor windings.

It can be beneficial to limit start-up current by using series inductors on the DRV8834 output, as that allows I_{TRIP} to be lower, and it may decrease the system's required bulk capacitance. Start-up current can also be limited by ramping the forward drive duty cycle.

9.2.1.3 Application Curves

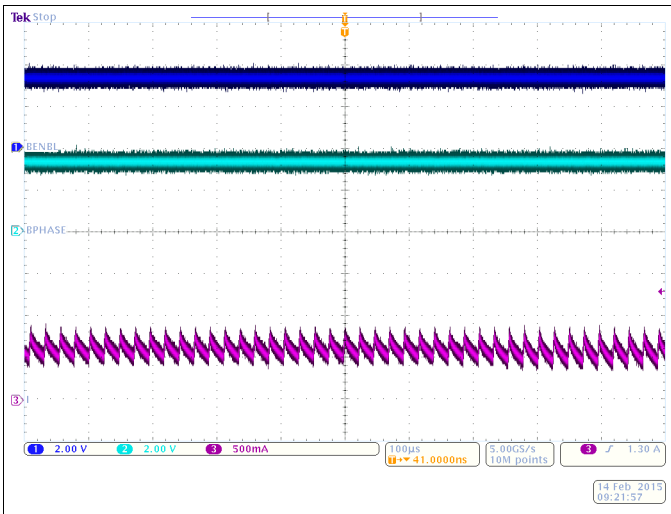


Figure 10. Brushed Motor – VM = 8 V, DRV8834 is Regulating Current

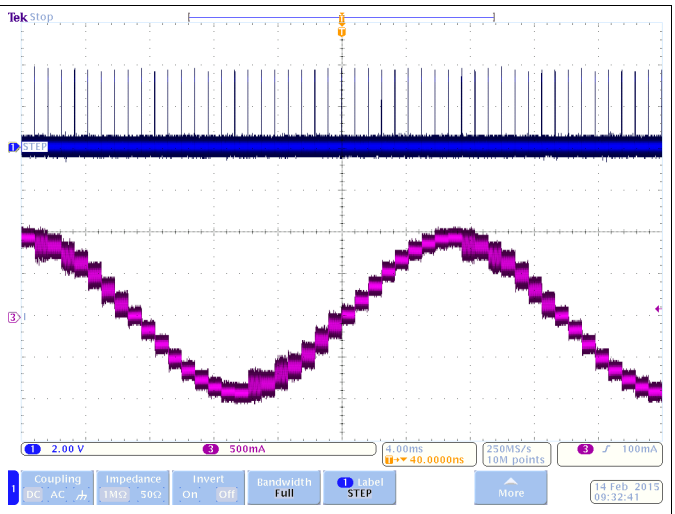


Figure 11. Internal Indexer – VM = 8 V, 1200 Steps per second, 1/8 microstep mode, 1-A Current regulation

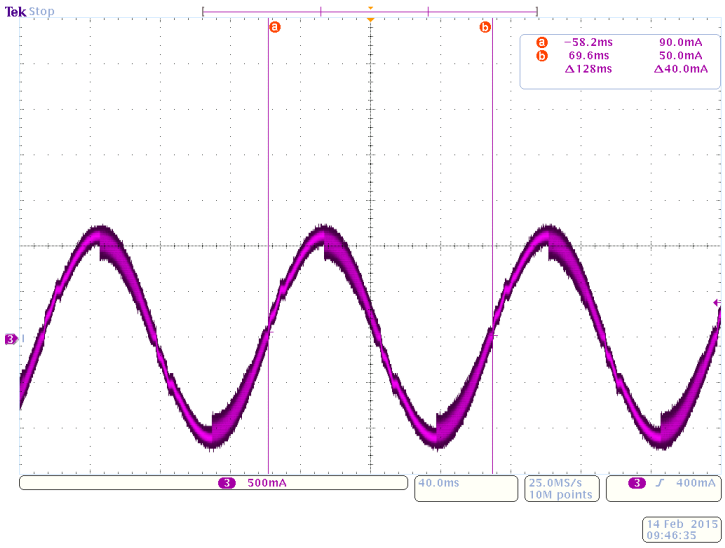


Figure 12. External Microstepping – VM = 8 V, 4000 Steps Per Second, 1/128 microstep mode, 1.2-A Current Regulation

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9.2.2 Phase/Enable Mode Driving a Stepper Motor

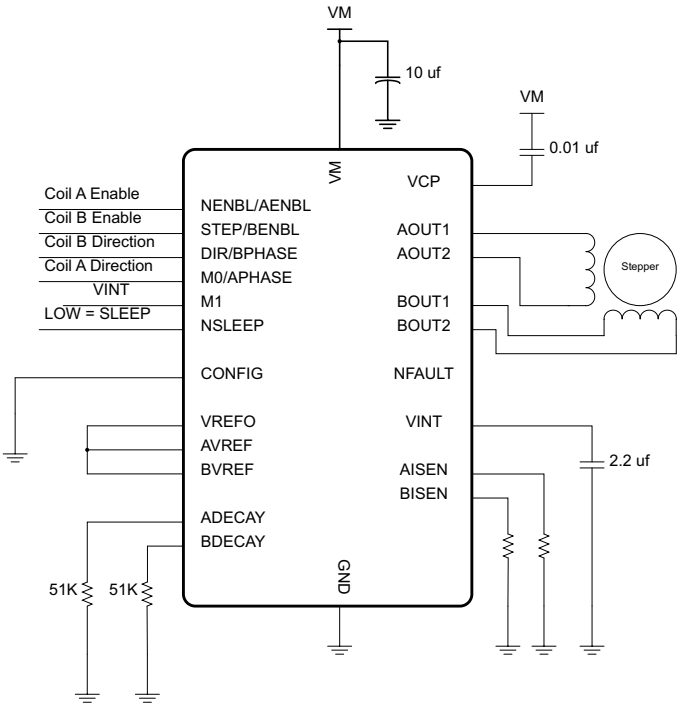


Figure 13. Phase/Enable Mode Driving a Stepper Motor

9.2.2.1 Design Requirements

Table 6 lists the design parameters.

Table 6. Design Parameters

PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_M	6 V
Motor winding resistance	R_L	3.9 Ω
Motor winding inductance	I_L	2.9 mH
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	2 µsteps per step
Target motor speed	V	120 RPM
Target full-scale current	I_{FS}	1.25 A

9.2.2.2 Detailed Design Procedure

Phase/enable mode can be used with a simple interface to a controller to operate a stepper motor in full or half step modes. The decay mode can be set by changing the values of the resistors connected to the ADECAY and BDECAY pins. The M1 pin is driven to logic high (by connecting to the VINT supply), to allow a zero-current (off) state when the xENBL pin is set low. Coil current is set by the R_{SENSE} resistors. If the sleep function is not needed, nSLEEP can be connected to VM with an approximate 47-kΩ resistor.

9.2.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8834 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor start-up speed is too high, the motor will not spin. Make sure that the motor can support the target speed or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (v), microstepping level (nm), and motor full step angle (θ_{step}),

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θstep can be found in the stepper motor data sheet or written on the motor itself.

For the DRV8834, the microstepping level is set by the MODE pins and can be any of the settings in Table 6. Higher microstepping will mean a smoother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

9.2.2.2.2 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the xVREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8834 is set for 5 V/V.

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.2 Ω, xVREF should be 1.25 V.

9.2.2.2.3 Decay Modes

The DRV8834 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8834 will place the winding in one of the three decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time T_{BLANK} defines the minimum drive time for the current chopping. I_{TRIP} is ignored during T_{BLANK}, so the winding current may overshoot the trip level.

9.2.2.3 Application Curves

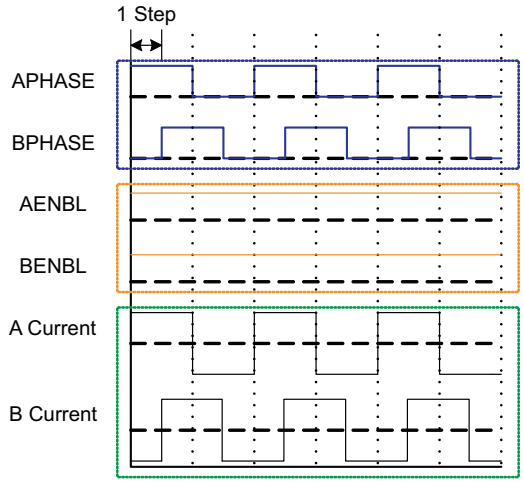


Figure 14. Full Step Sequence (2-Phase)

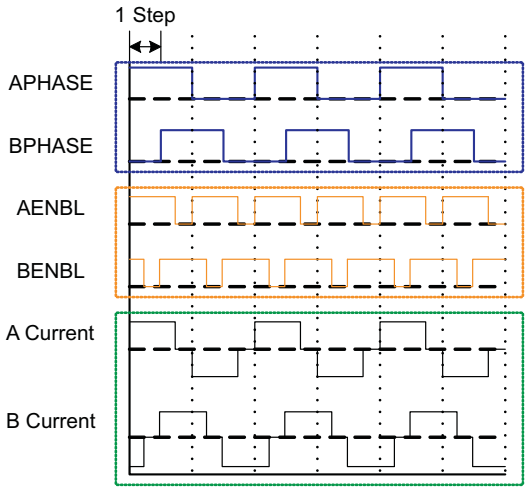


Figure 15. Half Step Sequence (1-2 Phase)

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9.2.3 Indexer Mode Driving a Stepper Motor

In indexer mode, only a rising edge on the STEP pin is needed to move the motor to the next step. The DIR pin sets which direction the motor rotates, by reversing the step sequence. The internal indexer can operate in full-step, half-step, and smaller microsteps up to 1/32-step, depending on the state of the M0 and M1 pins. The M0 and M1 pins can also be connected directly to ground or to VINT to program the step modes, if desired. If the sleep function is not needed, nSLEEP can be connected to VM with an approximate 47-kΩ resistor. Step sequences for full and half step are shown below.

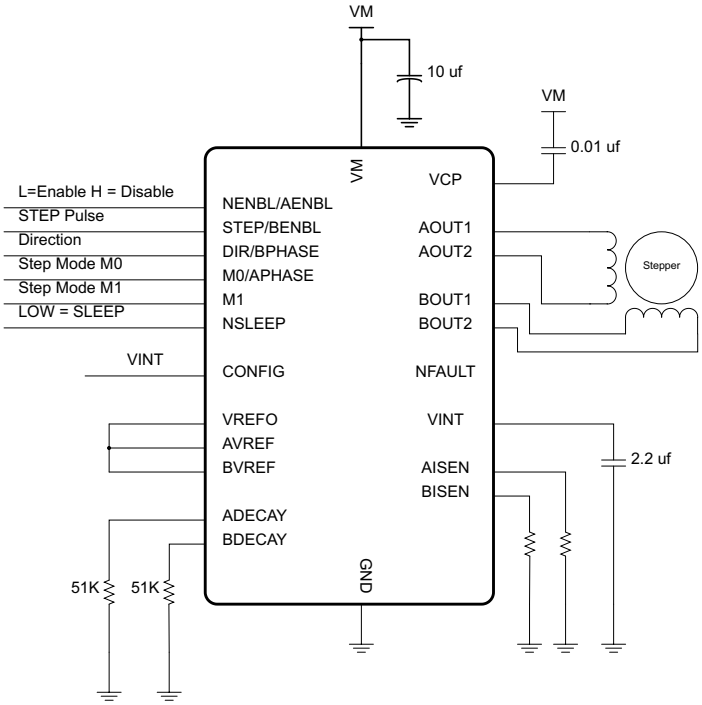


Figure 16. Indexer Mode Driving a Stepper Motor

9.2.3.1 Design Requirements

Table 7 lists the design parameters.

Table 7. Design Parameters

PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M	6 V
Motor Winding Resistance	R_L	3.9 Ω
Motor Winding Inductance	I_L	2.9 mH
Motor Full Step Angle	θ_{step}	1.8°/step
Target Microstepping Level	n_m	8 µsteps per step
Target Motor Speed	V	120 RPM
Target Full-Scale Current	I_{FS}	1.25 A

9.2.3.2 Detailed Design Procedures

Phase/enable mode can be used with a simple interface to a controller to operate a stepper motor in full or half step modes. The decay mode can be set by changing the values of the resistors connected to the ADECAY and BDECAY pins. The M1 pin is driven to logic high (by connecting to the VINT supply), to allow a zero-current (off) state when the xENBL pin is set low. Coil current is set by the R_{SENSE} resistors. If the sleep function is not needed, nSLEEP can be connected to VM with an approximate 47-kΩ resistor.

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9.2.3.2.1 Stepper Motor Speed

The first step in configuring the DRV8834 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor start-up speed is too high, the motor will not spin. Make sure that the motor can support the target speed or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (v), microstepping level (nm), and motor full step angle (θ_{step}),

θstep can be found in the stepper motor data sheet or written on the motor itself.

For the DRV8834, the microstepping level is set by the MODE pins and can be any of the settings in Table 6. Higher microstepping will mean a smoother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

9.2.3.2.2 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the xVREF analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8834 is set for 5 V/V.

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.2 Ω, xVREF should be 1.25 V.

9.2.3.2.3 Decay Modes

The DRV8834 supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8834 will place the winding in one of the three decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time T_{BLANK} defines the minimum drive time for the current chopping. I_{TRIP} is ignored during T_{BLANK}, so the winding current may overshoot the trip level.

9.2.3.3 Application Curves

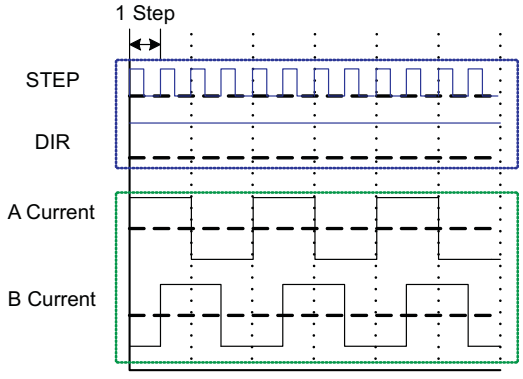


Figure 17. Full Step Sequence (2-Phase)

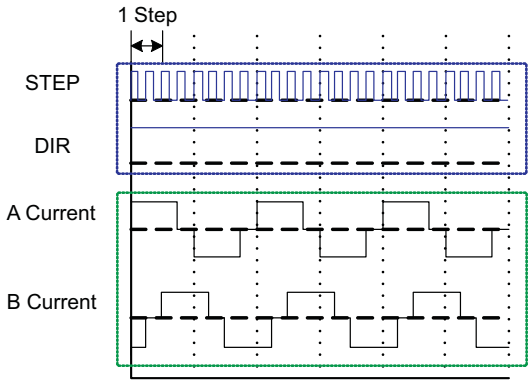


Figure 18. Half Step Sequence (1-2 Phase)

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9.2.4 High-Resolution Microstepping Using a Microcontroller to Modulate VREF Signals

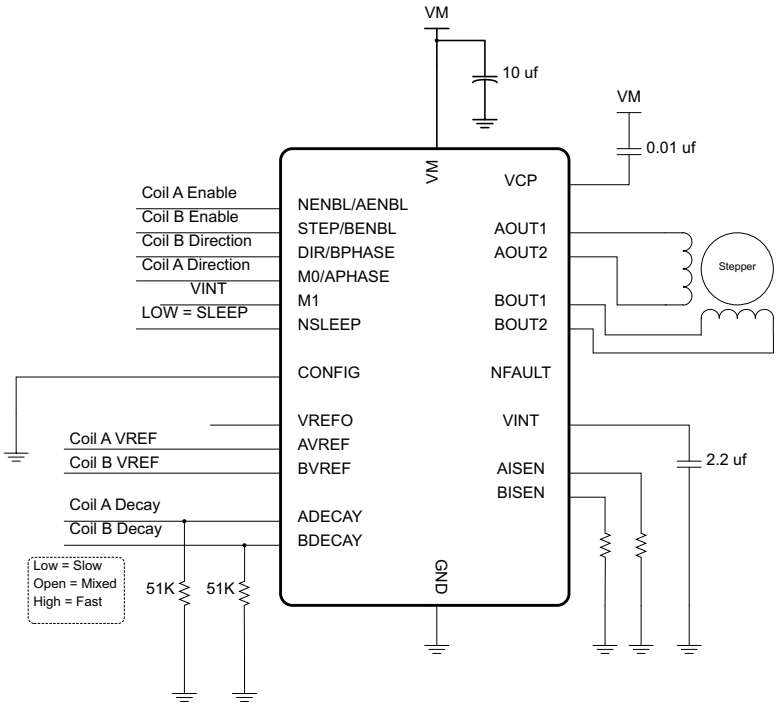


Figure 19. High-Resolution Microstepping

9.2.4.1 Design Requirements

Table 8 lists the design parameters.

Table 8. Design Parameters

PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_M	6 V
Motor winding resistance	R_L	3.9 Ω
Motor winding inductance	I_L	2.9 mH
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	128 µsteps per step
Target motor speed	V	120 RPM
Target full-scale current	I_{FS}	1.25 A

9.2.4.2 Detailed Design Procedure

Using a microcontroller with two DAC outputs, very high resolution microstepping can be performed with the DRV8834. In this mode, the coil current direction is controlled by the PHASE pins, and the current in each coil is independently set using the two VREF input pins, which are connected to DACs. In addition, the microcontroller can set the decay mode for each coil dynamically, by driving the xDECAY pin low for slow decay, high for fast decay, or high-impedance which sets mixed decay (based on the value of a resistor connected to ground). If the sleep function is not needed, nSLEEP can be connected to VM with an approximate 47-kΩ resistor.

For more details on this technique, refer to TI Application Report, *High Resolution Microstepping Driver With the DRV88xx Series* (SLVA416).

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9.2.4.3 Application Curves

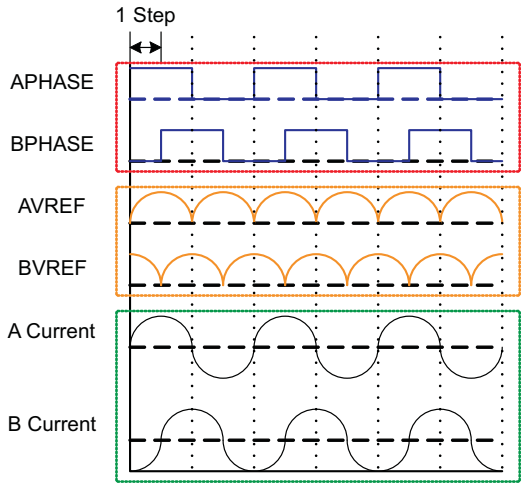


Figure 20. Microstepping Sequence

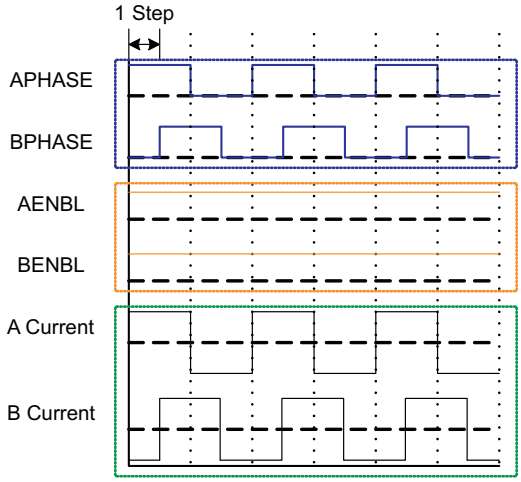


Figure 21. Full Step Sequence (2-Phase)

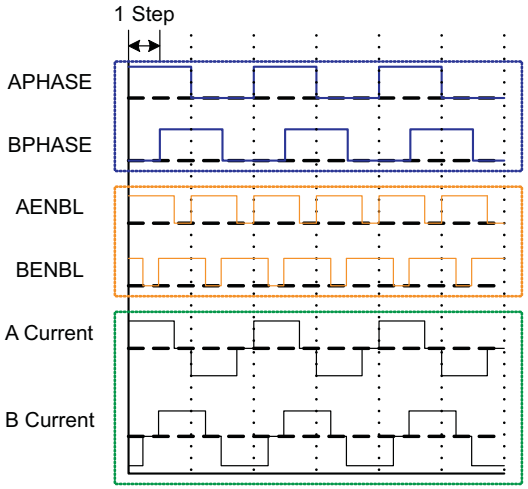


Figure 22. Half Step Sequence (1-2 Phase)

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10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and its ability to source or sink current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

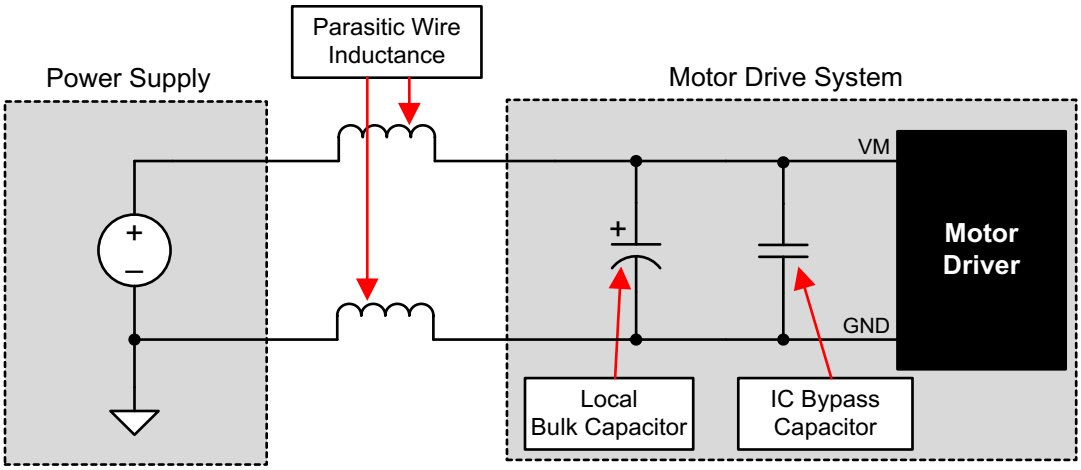


Figure 23. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

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11 Layout

11.1 Layout Guidelines

The VM pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.01-µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin. The VM pin must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8834. A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.01- µF rated for 16 V. Place this component as close to the pins as possible.

Bypass VINT to ground with a 2.2-µF ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible.

11.2 Layout Example

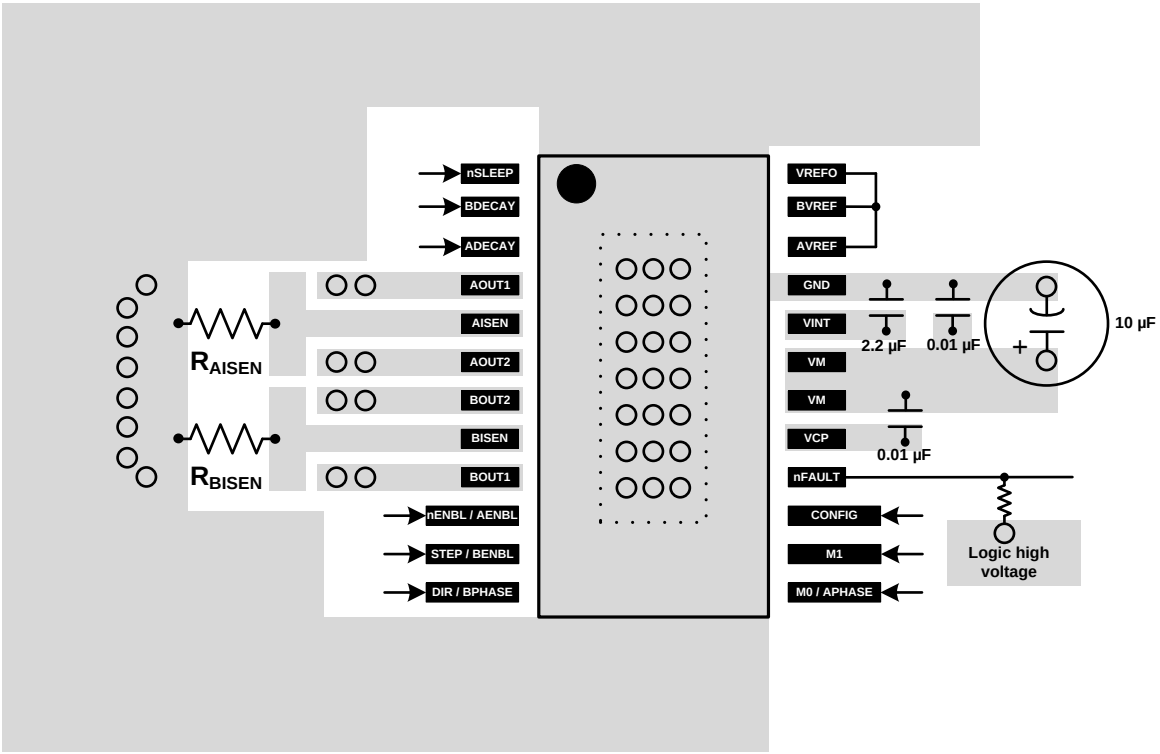


Figure 24. Recommended Layout

11.3 Thermal Considerations

11.3.1 Maximum Output Current

In actual operation, the maximum output current achievable with a motor driver is a function of die temperature. This in turn is greatly affected by ambient temperature and PCB design. Basically, the maximum motor current will be the amount of current that results in a power dissipation level that, along with the thermal resistance of the package and PCB, keeps the die at a low enough temperature to stay out of thermal shutdown.

The thermal data given in the data sheet can be used as a guide to calculate the approximate maximum power dissipation that can be expected to be possible without entering thermal shutdown for several different PCB constructions. However, for accurate data, the actual PCB design must be analyzed via measurement or thermal simulation.

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Thermal Considerations (continued)

11.3.2 Thermal Protection

The DRV8834 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 160°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11.3.3 Power Dissipation

Power dissipation in the DRV8834 is dominated by the DC power dissipated in the output FET resistance, or $R_{DS(ON)}$. There is additional power dissipated due to PWM switching losses, which are dependent on PWM frequency, rise and fall times, and VM supply voltages. These switching losses are typically on the order of 10% to 20% of the DC power dissipation.

The DC power dissipation of one H-bridge can be roughly estimated by Equation 5.

$$P_{TOT} = (HS - R_{DS(ON)} \bullet I_{OUT(RMS)}^{2}) + (LS - R_{DS(ON)} \bullet I_{OUT(RMS)}^{2}) \quad (5)$$

where P_{TOT} is the total power dissipation, HS - $R_{DS(ON)}$ is the resistance of the high side FET, LS - $R_{DS(ON)}$ is the resistance of the low side FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to the motor.

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

11.3.4 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report, *PowerPAD™ Thermally Enhanced Package*(SLMA002), and TI application brief, *PowerPAD™ Made Easy* (SLMA004), available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *High Resolution Microstepping Driver With the DRV88xx Series*, SLVA416
- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004

12.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8834PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8834	Samples
DRV8834PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8834	Samples
DRV8834RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8834	Samples
DRV8834RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8834	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

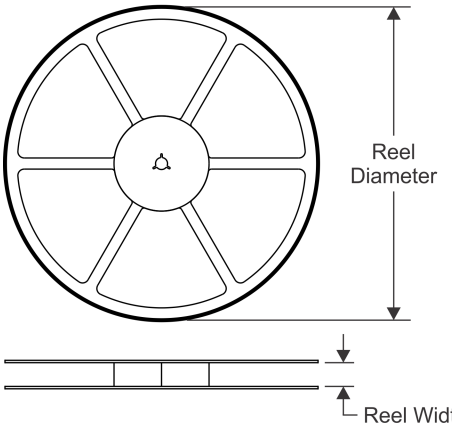
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

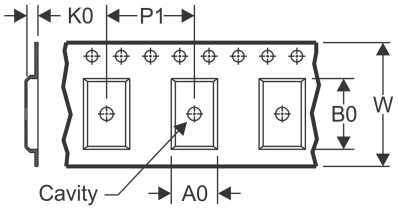
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

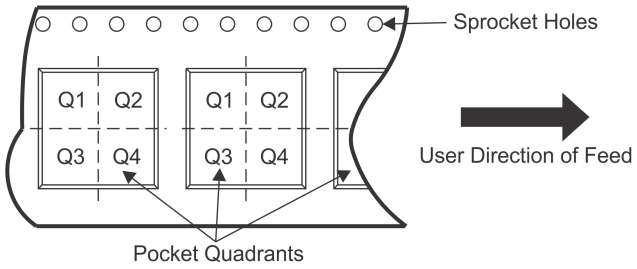


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

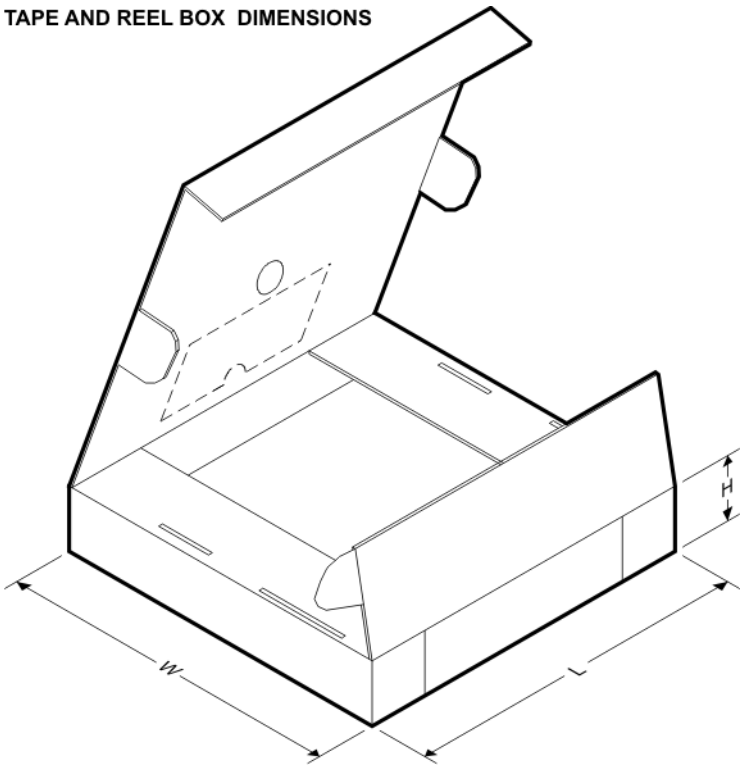
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8834PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8834RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8834RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

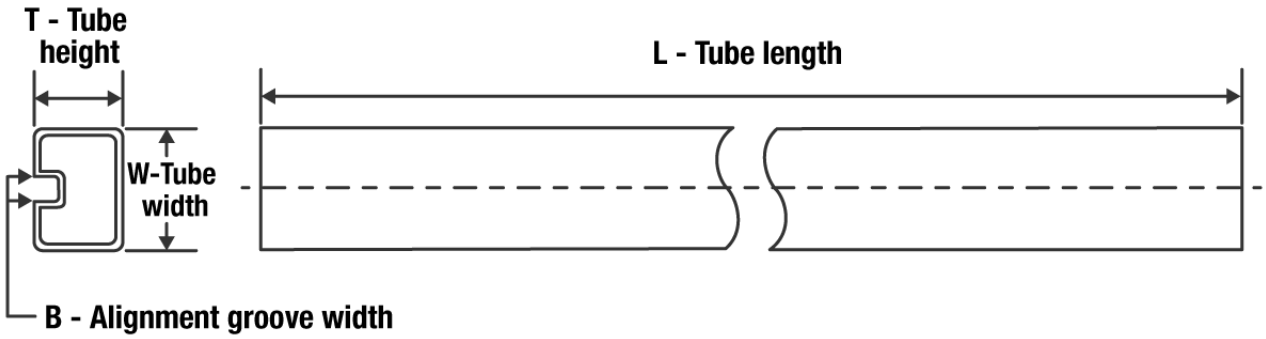
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8834PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DRV8834RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DRV8834RGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8834PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

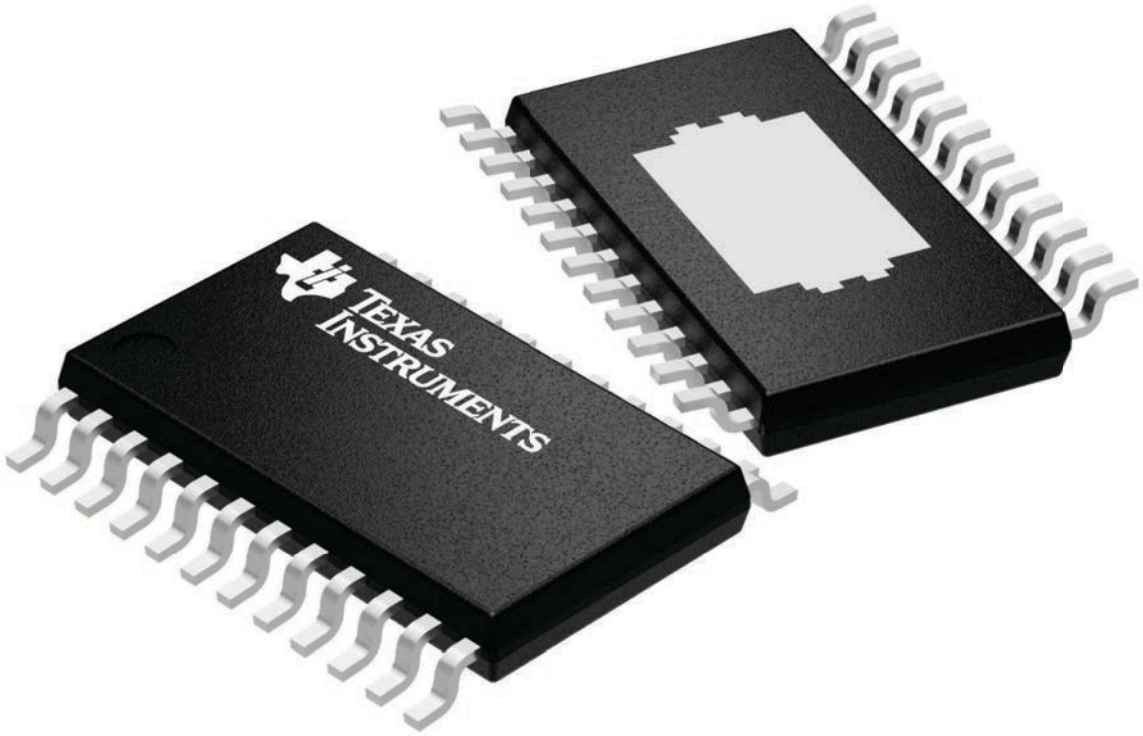
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

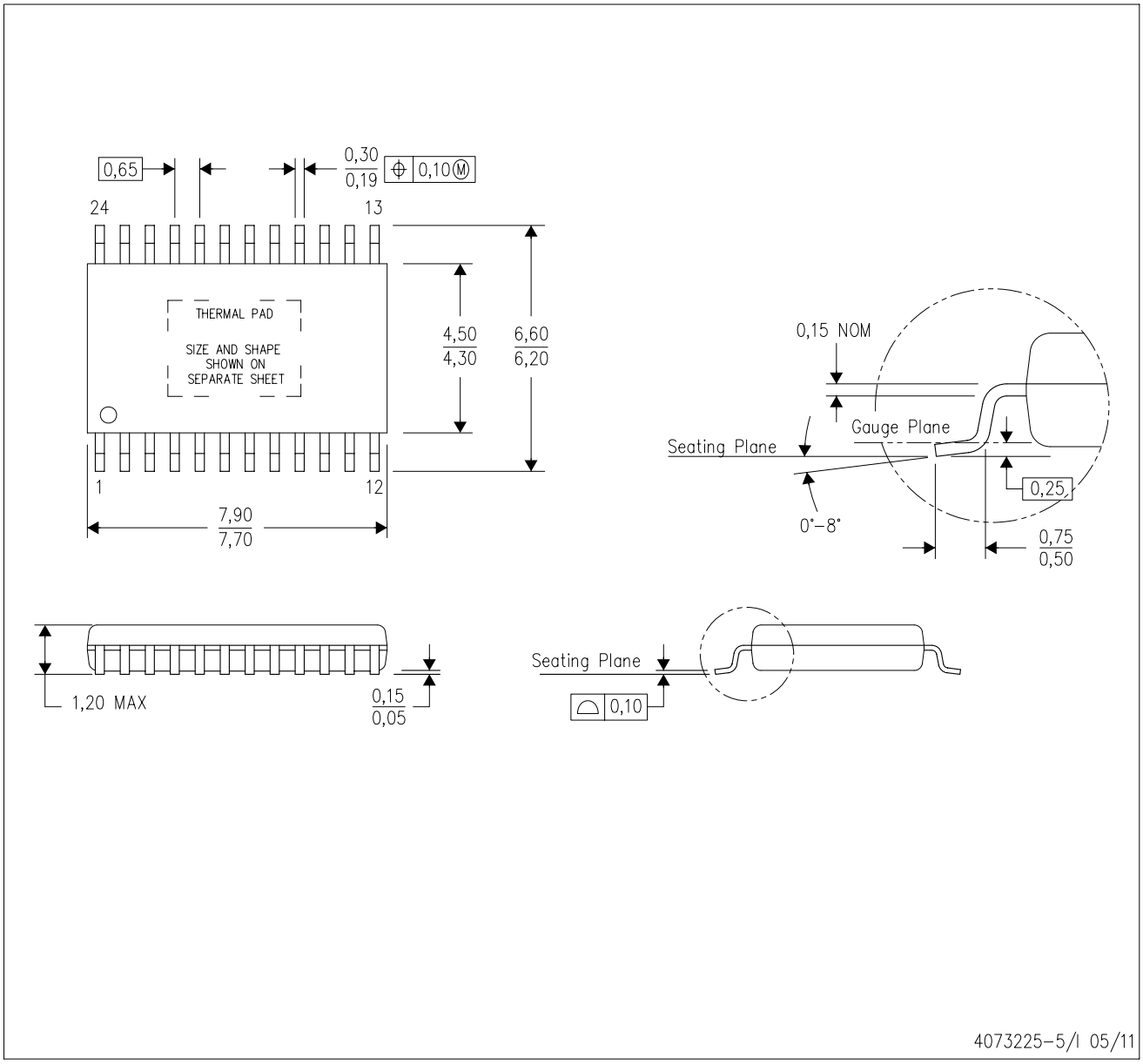
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

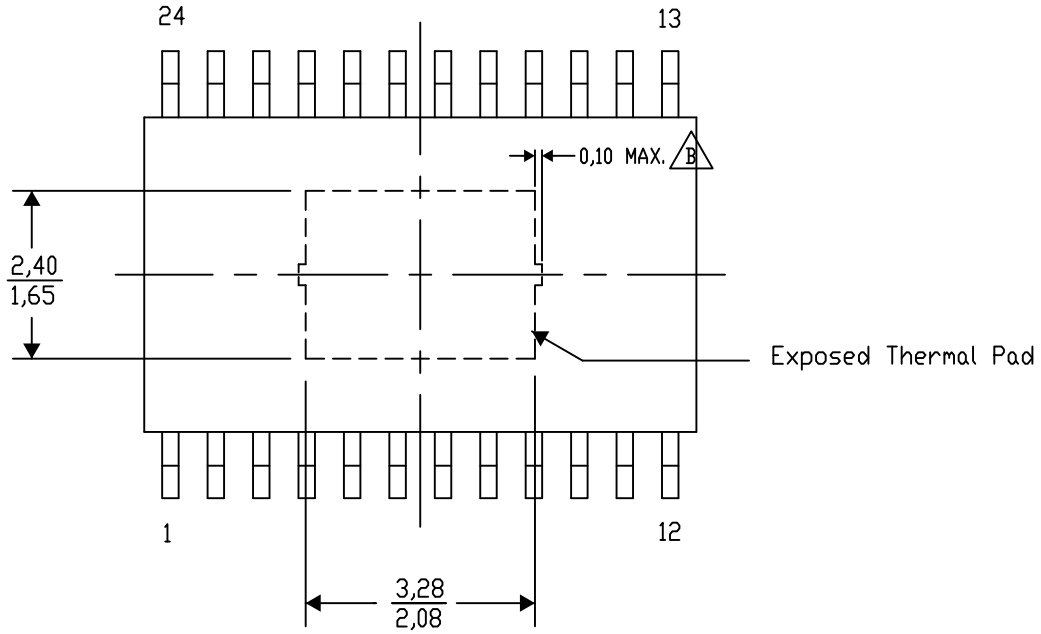
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

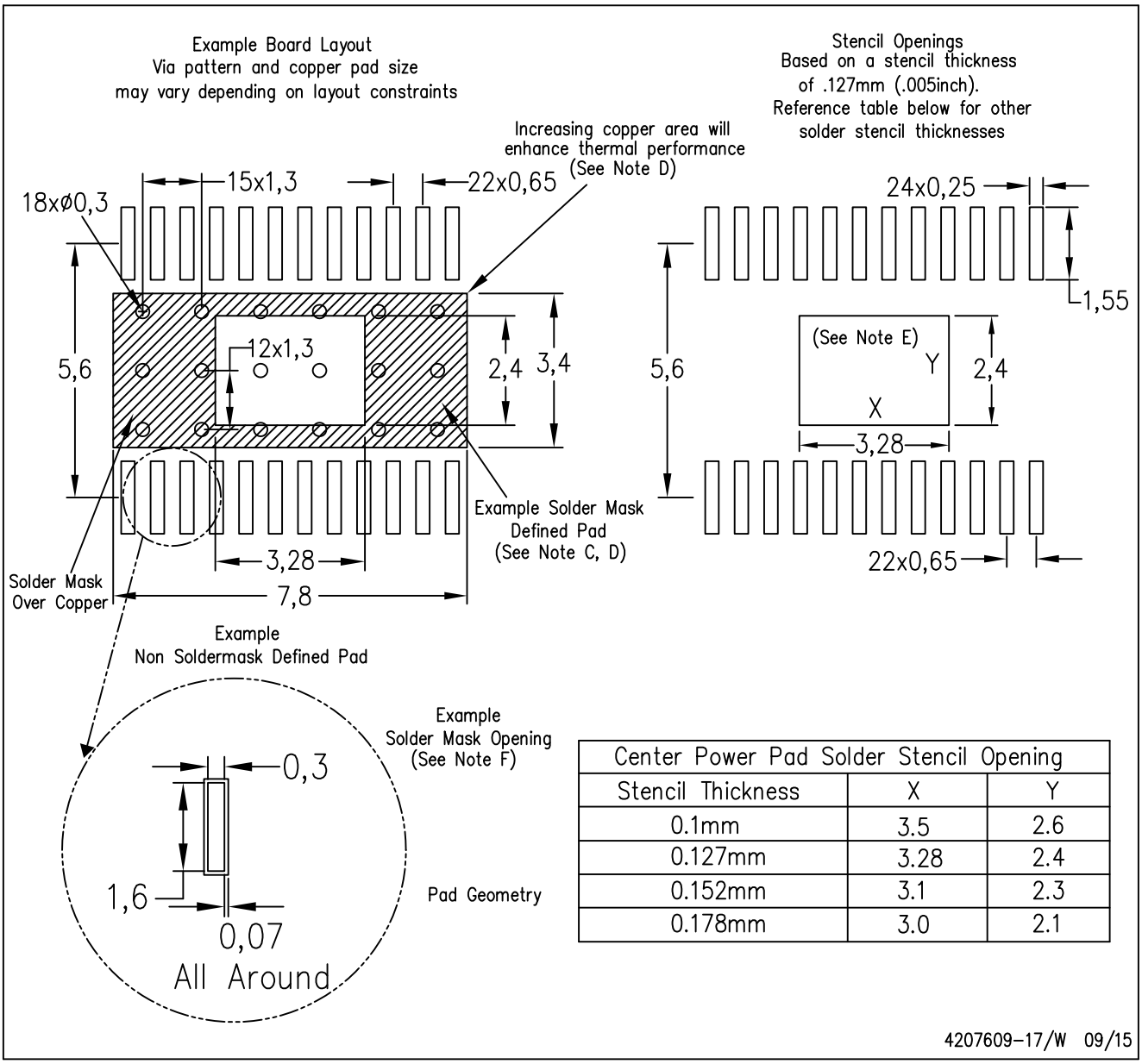
4206332–31/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.5	2.6
0.127mm	3.28	2.4
0.152mm	3.1	2.3
0.178mm	3.0	2.1

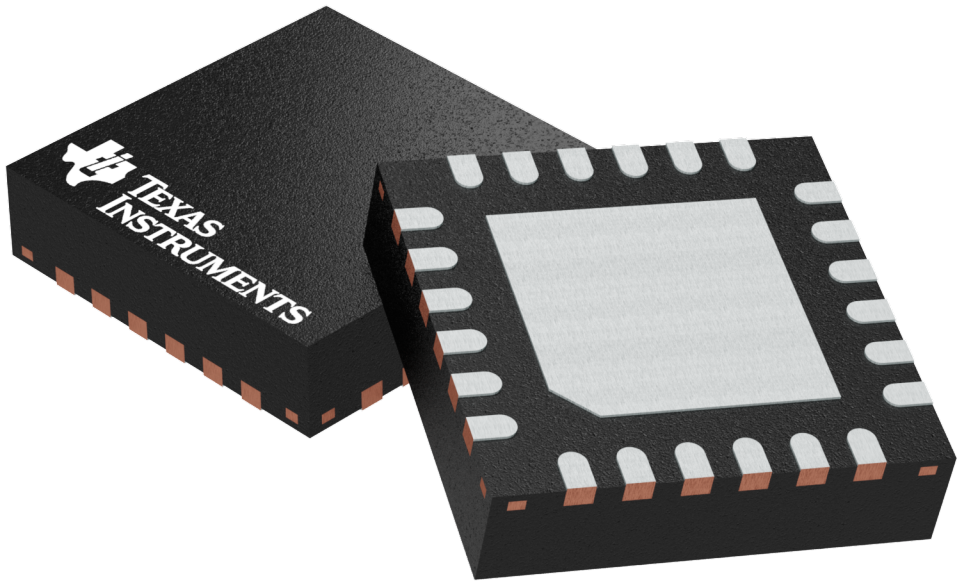
4207609–17/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

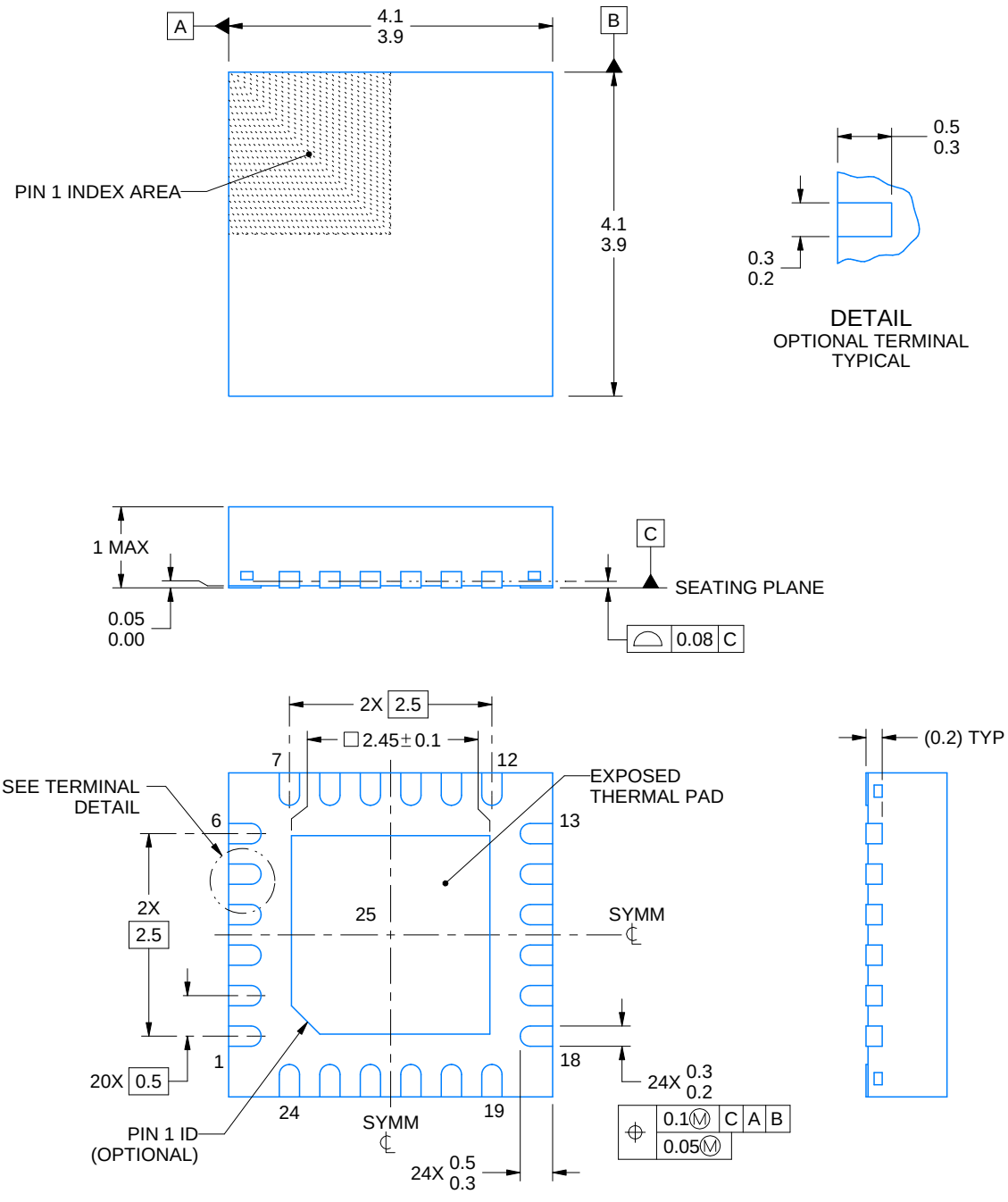
4204104/H

PACKAGE OUTLINE

RGE0024B

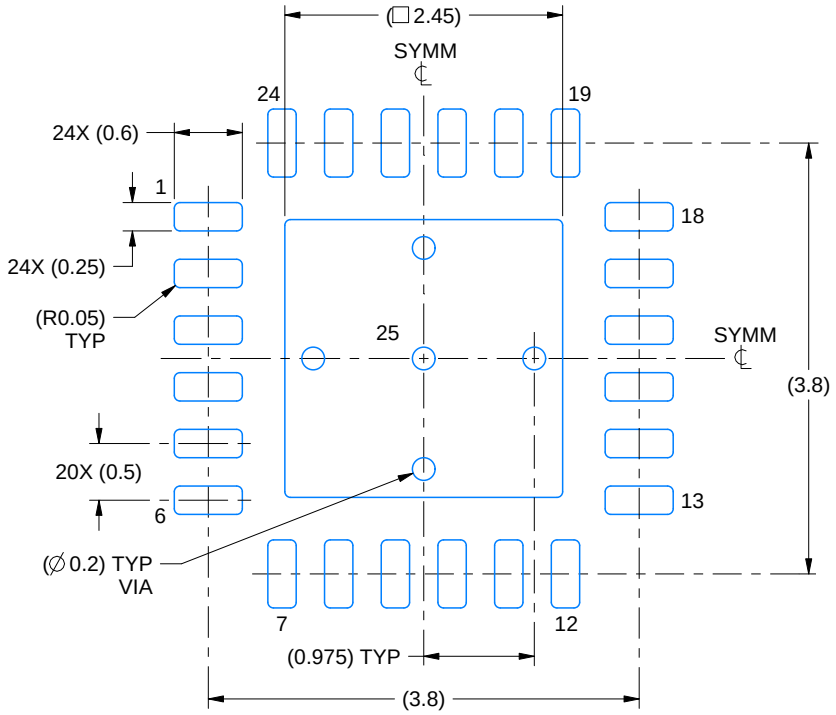
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

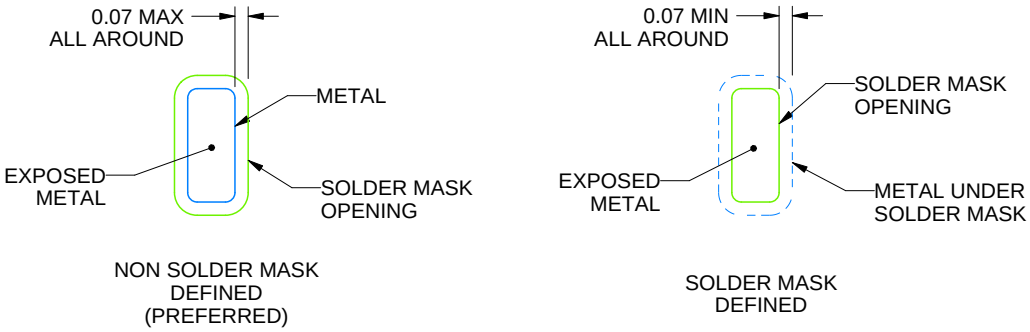


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

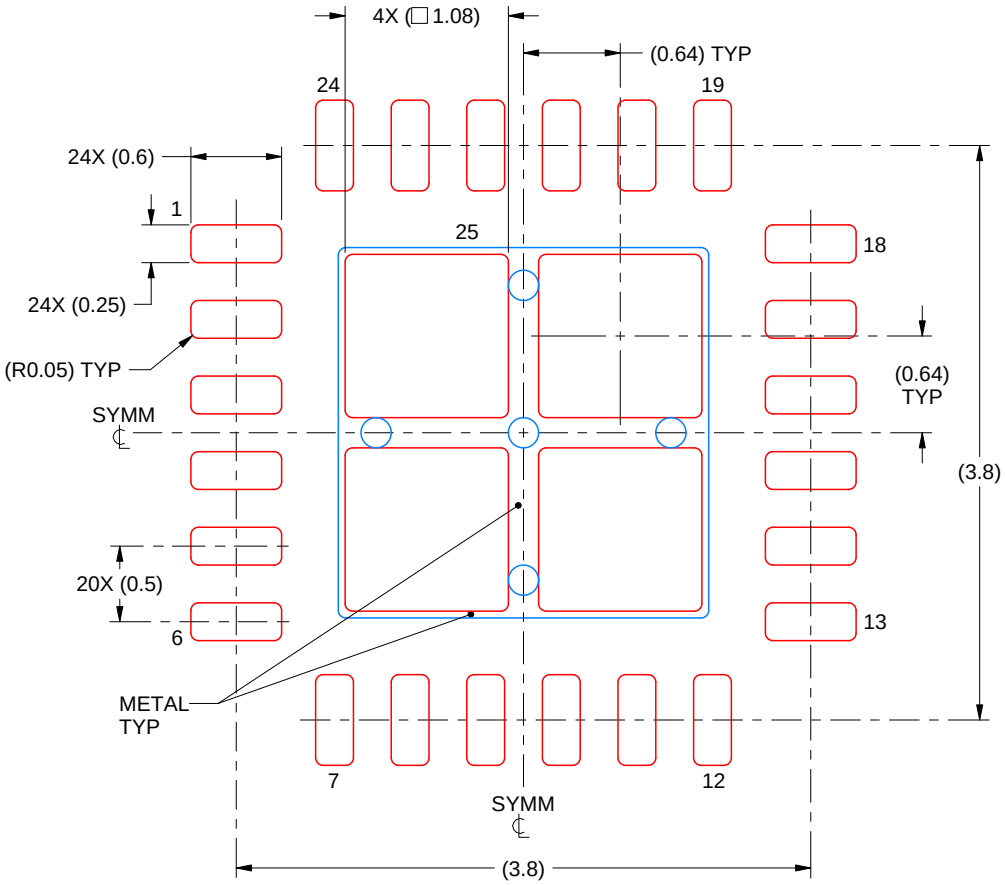


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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