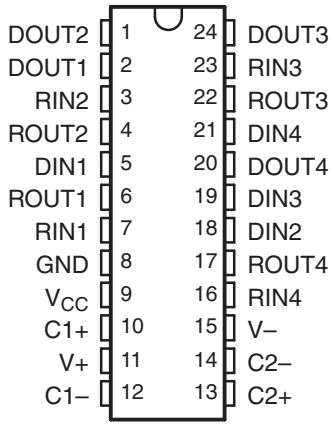
5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD PROTECTION

FEATURES

- **ESD Protection for RS-232 I/O Pins**
  - **±15-kV Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V V_{CC} Supply**
- **Four Drivers and Four Receivers**
- **Operates up to 120 kbit/s**
- **External Capacitors: 4 × 0.1 μF**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DB OR DW PACKAGE
(TOP VIEW)



APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DESCRIPTION

The MAX208 device consists of four line drivers, four line receivers, and a dual charge-pump circuit with ±15-kV HBM ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The devices operate at data signaling rates up to 120 kbit/s and a maximum of 30-V/μs driver output slew rate.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	MAX208CDW	MAX208C
		Reel of 2000	MAX208CDWR	
	SSOP – DB	Tube of 60	MAX208CDB	MA208C
		Reel of 2000	MAX208CDBR	
–40°C to 85°C	SOIC – DW	Tube of 25	MAX208IDW	MAX208I
		Reel of 2000	MAX208IDWR	
	SSOP – DB	Tube of 60	MAX208IDB	MB208I
		Reel of 2000	MAX208IDBR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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FUNCTION TABLE EACH DRIVER(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

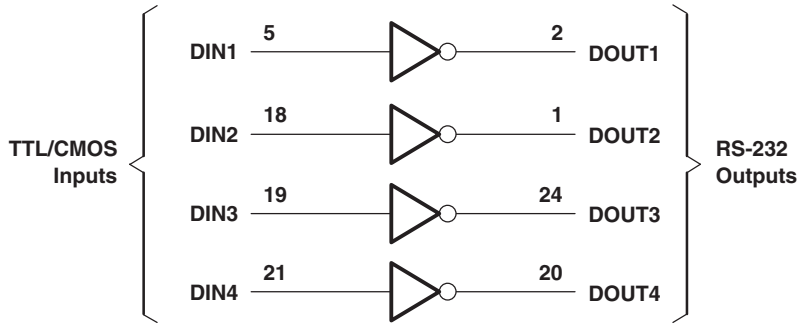
(1) H = high level, L = low level

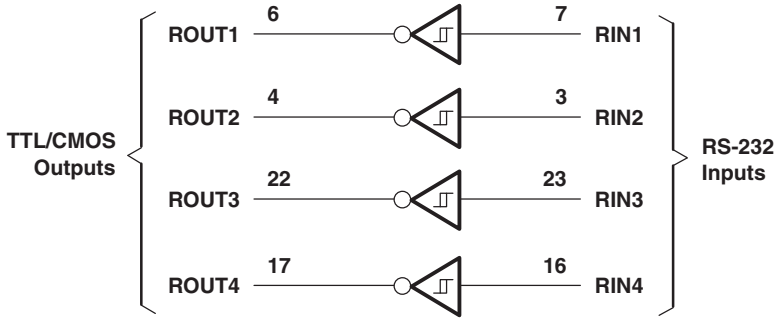
FUNCTION TABLE EACH RECEIVER(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or
connected driver off

logic diagram (positive logic)





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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range(2)		–0.3 V to 6 V
V+	Positive charge pump voltage range(2)		V_{CC} – 0.3 V to 14 V
V–	Negative charge pump voltage range(2)		–14 V to 0.3 V
V+ – V–	Supply voltage difference(2)		13 V
V_I	Input voltage range	Drivers	–0.3 V to V+ + 0.3 V
		Receivers	±30 V
V_O	Output voltage range	Drivers	V– – 0.3 V to V+ + 0.3 V
		Receivers	–0.3 V to V_{CC} + 0.3 V
	Short-circuit duration on DOUT		Continuous
θ_{JA}	Package thermal impedance(3)(4)	DB package	63°C/W
		DW package	46°C/W
T_J	Operating virtual-junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

C1 to C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V (see Figure 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
V_{IL}	Driver low-level input voltage	DIN			0.8	V
V_I	Driver input voltage	DIN	0		5.5	V
	Receiver input voltage		–30		30	
T_A	Operating free-air temperature	MAX208C	0		70	°C
		MAX208I	–40		85	

ELECTRICAL CHARACTERISTICS

C1 to C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V (see Figure 4), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 5 V, T_A = 25°C		11	20	mA

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DRIVER SECTION

ELECTRICAL CHARACTERISTICS

C1 to C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V (see Figure 4), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND, DIN = GND	5	9		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND, DIN = V_{CC}	–5	–9		V
I_{IH}	High-level input current	V_I = V_{CC}		15	200	µA
I_{IL}	Low-level input current	V_I = 0 V		–15	–200	µA
I_{OS}	Short-circuit output current(1)	V_{CC} = 5.5 V, V_O = 0 V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, and V– = 0 V, V_O = ±2 V	300			Ω

(1) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS

C1 to C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V (see Figure 4), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
	Maximum data rate	C_L = 50 to 1000 pF, One DOUT switching, R_L = 3 kΩ to 7 kΩ, See Figure 1	120			kbit/s
$t_{PLH\ (D)}$	Propagation delay time, low- to high-level output	C_L = 2500 pF, All drivers loaded, R_L = 3 kΩ, See Figure 1		2		µs
$t_{PHL\ (D)}$	Propagation delay time, high- to low-level output	C_L = 2500 pF, All drivers loaded, R_L = 3 kΩ, See Figure 1		2		µs
$t_{sk(p)}$	Pulse skew(2)	C_L = 150 pF to 2500 pF, See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	C_L = 50 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ, V_{CC} = 5 V	3	6	30	V/µs

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

ESD PROTECTION

PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	Human-Body Model	±15	kV

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RECEIVER SECTION

ELECTRICAL CHARACTERISTICS

C1 to C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V (see Figure 4), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	3.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)	V_{CC} = 5 V	0.2	0.5	1	V
r_i	Input resistance	V_I = ±3 V to ±25 V, V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ

SWITCHING CHARACTERISTICS

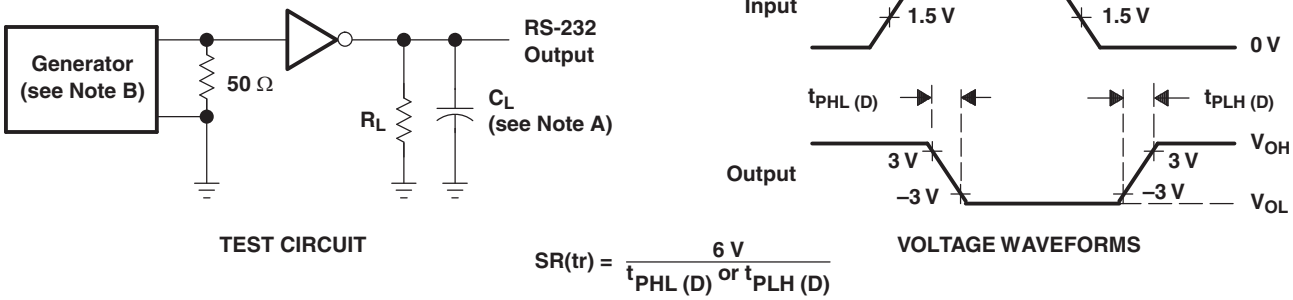
C1 to C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V (see Figure 4), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{PLH\ (R)}$	Propagation delay time, low- to high-level output	C_L = 150 pF		0.5	10	µs
$t_{PHL\ (R)}$	Propagation delay time, high- to low-level output	C_L = 150 pF		0.5	10	µs
$t_{sk(p)}$	Pulse skew(2)			300		ns

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

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PARAMETER MEASUREMENT INFORMATION

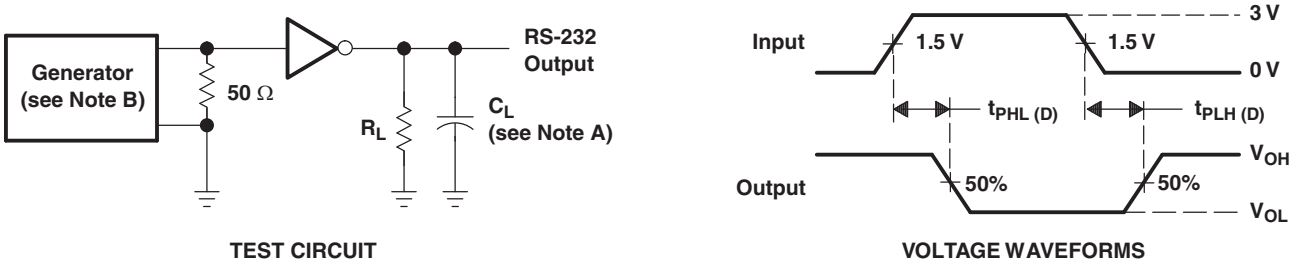


$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)} \text{ or } t_{PLH\ (D)}}$$

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics:
PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

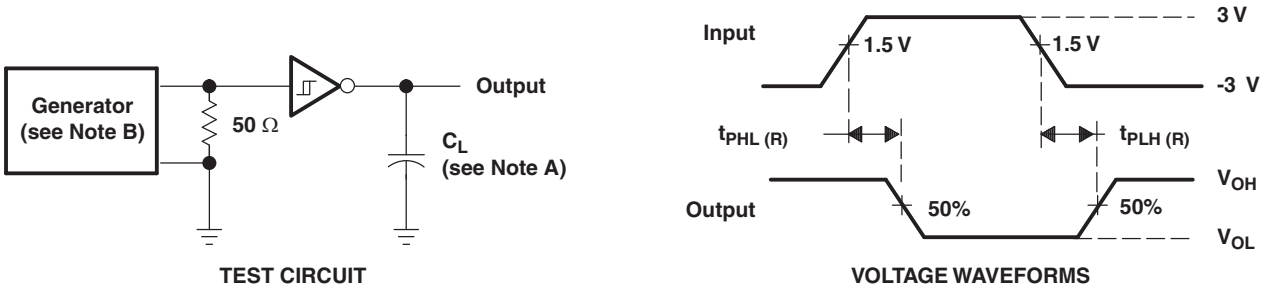
Figure 1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics:
PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 2. Driver Pulse Skew



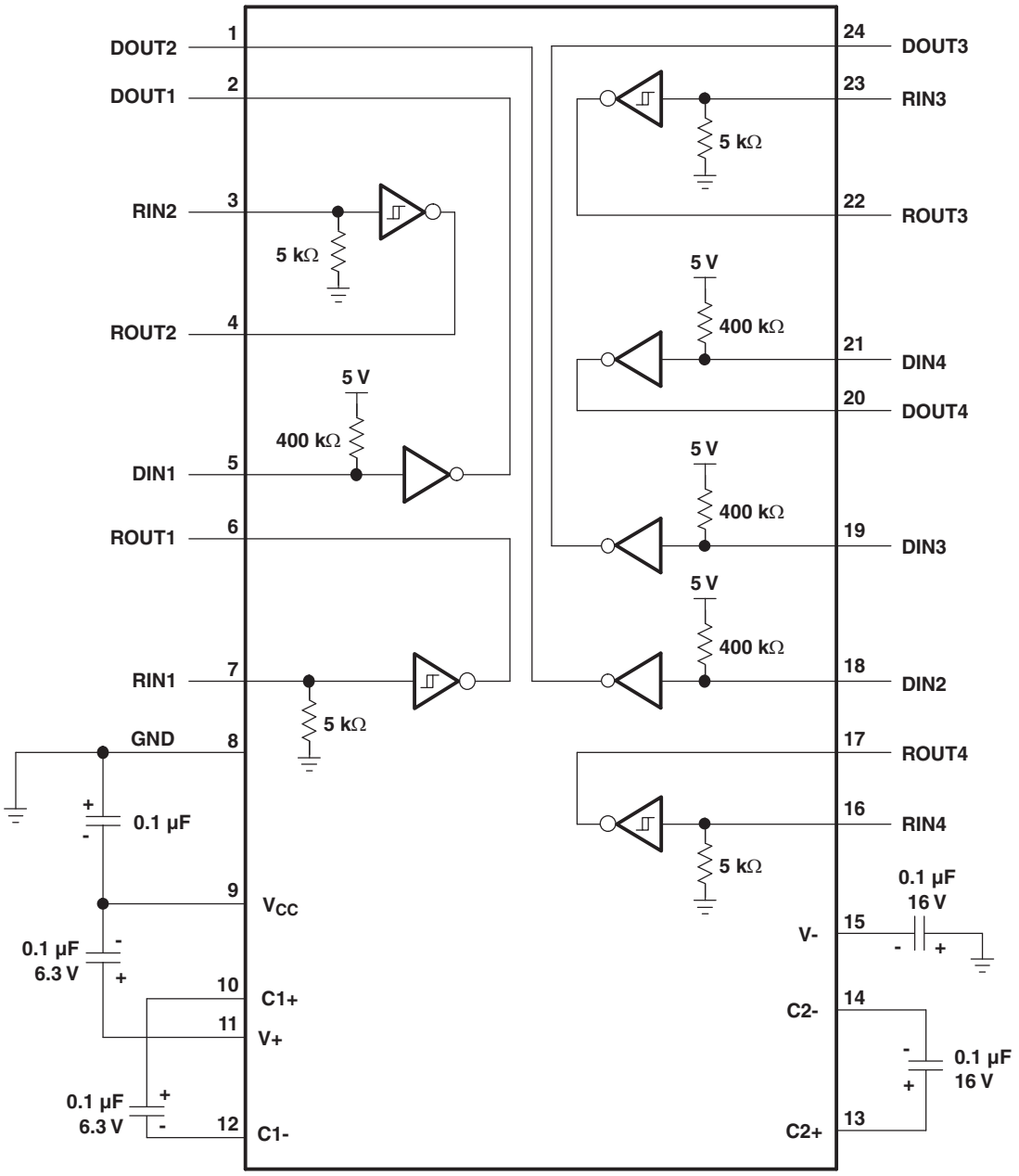
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 3. Receiver Propagation Delay Times

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APPLICATION INFORMATION



A. Resistor values shown are nominal.

B. Non-polarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX208 requires 0.1-µF capacitors, although capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for the 0.1-µF capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10 µF) to reduce the output impedance at V+ and V–.

Bypass V_{CC} to ground with at least 0.1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

ESD Protection

TI MAX208 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15 kV when powered down.

ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern and subsequently discharged into the DUT through a 1.5-kΩ resistor.

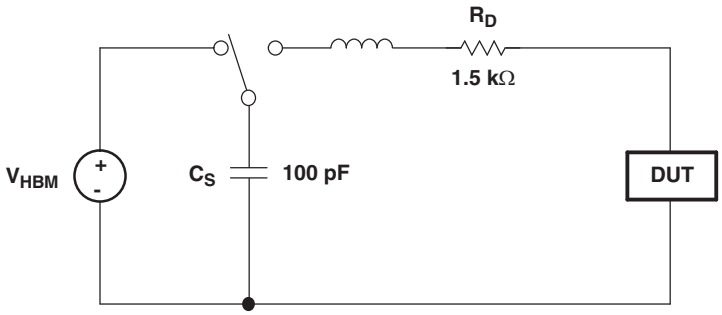


Figure 5. HBM ESD Test Circuit

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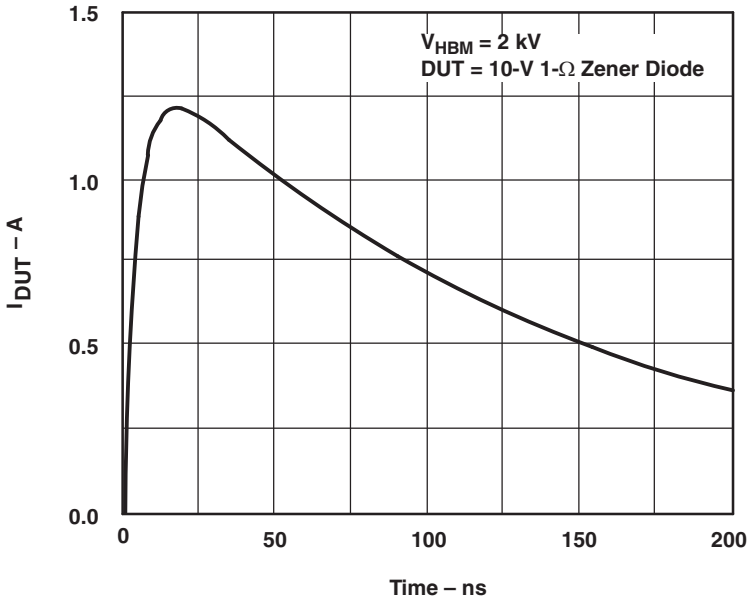


Figure 6. Typical HBM Current Waveform

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX208CDB	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA208C	Samples
MAX208CDBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA208C	Samples
MAX208CDBRG4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA208C	Samples
MAX208CDW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX208C	Samples
MAX208CDWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX208C	Samples
MAX208IDB	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB208I	Samples
MAX208IDBE4	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB208I	Samples
MAX208IDBG4	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB208I	Samples
MAX208IDBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB208I	Samples
MAX208IDW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX208I	Samples
MAX208IDWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX208I	Samples
MAX208IDWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX208I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

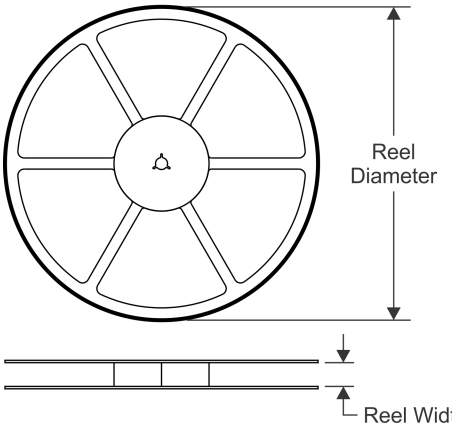
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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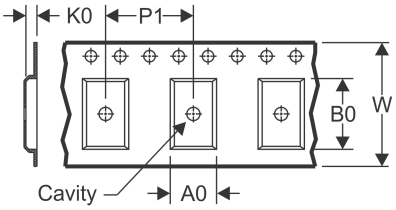
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

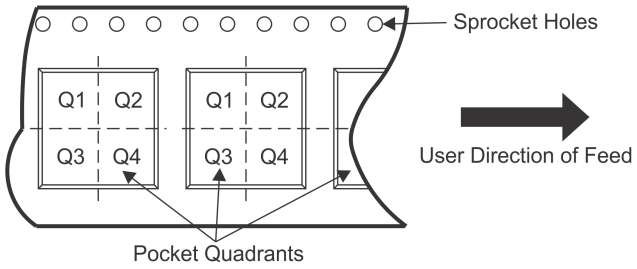


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

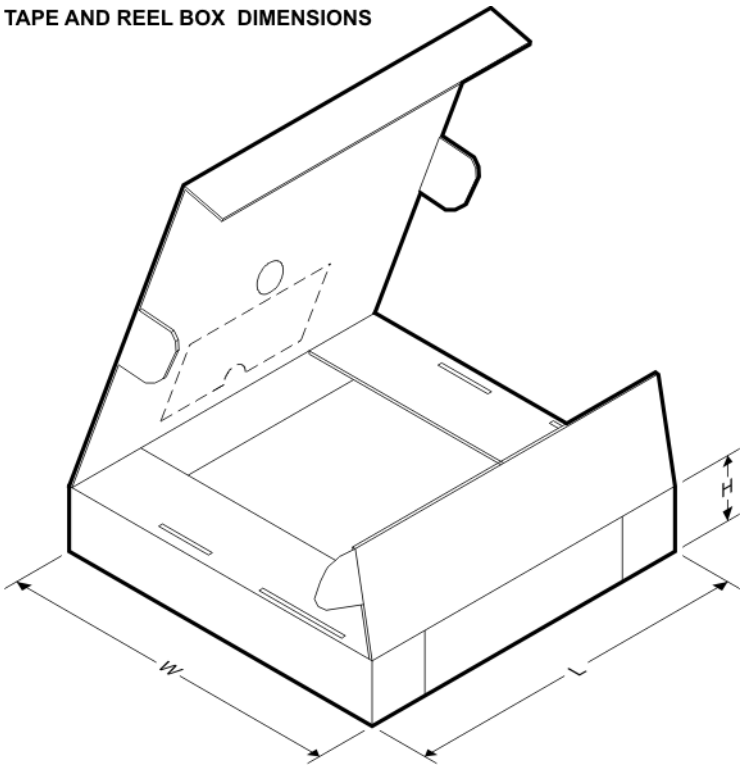
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX208CDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
MAX208CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
MAX208IDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
MAX208IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

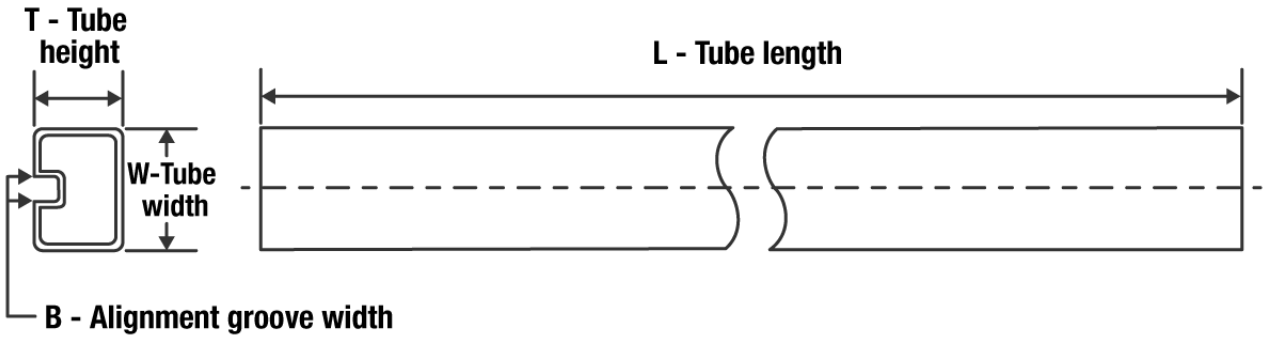
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX208CDBR	SSOP	DB	24	2000	853.0	449.0	35.0
MAX208CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
MAX208IDBR	SSOP	DB	24	2000	853.0	449.0	35.0
MAX208IDWR	SOIC	DW	24	2000	350.0	350.0	43.0

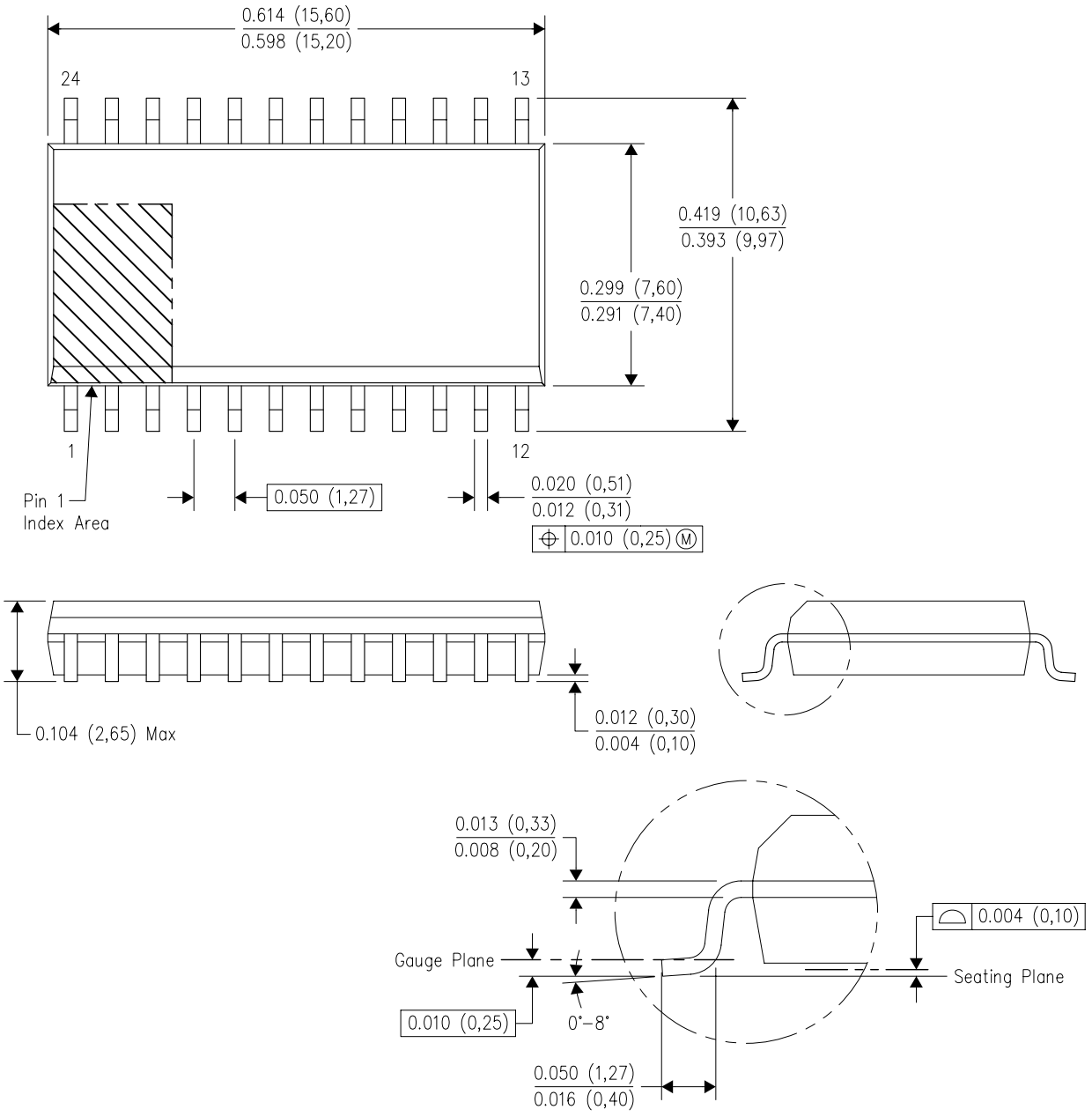
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX208CDB	DB	SSOP	24	60	530	10.5	4000	4.1
MAX208CDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
MAX208IDB	DB	SSOP	24	60	530	10.5	4000	4.1
MAX208IDBE4	DB	SSOP	24	60	530	10.5	4000	4.1
MAX208IDBG4	DB	SSOP	24	60	530	10.5	4000	4.1
MAX208IDW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

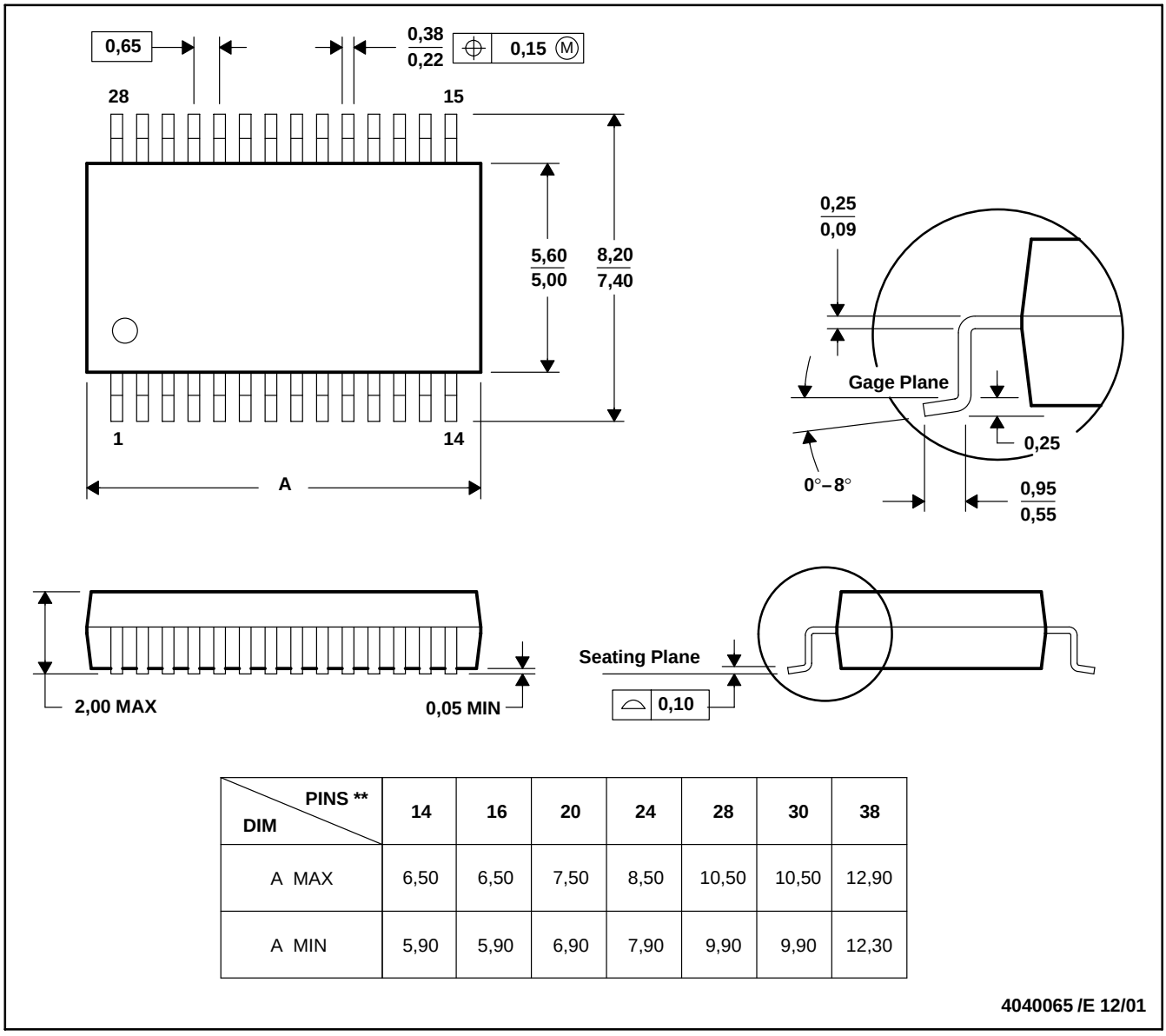


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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