LM1771 Low-Voltage Synchronous Buck Controller With Precision Enable and No External Compensation

1 Features

- Input Voltage Range of 2.8 V to 5.5 V
- 0.8-V Reference Voltage
- Precision Enable
- No Compensation Required
- Constant Frequency Across Input Range
- Low Quiescent Current of 400 µA
- Internal Soft-Start
- Short Circuit Protection
- 6-Pin WSON Package and 8-Pin VSSOP Package

2 Applications

- Simple-to-Design, High-Efficiency, Step-Down Switching Regulators
- FPGAs, DSPs, and ASIC Power Supplies
- Set-Top Boxes
- Cable Modems
- Printers
- Digital Video Recorders
- Servers
- Graphic Cards

3 Description

The LM1771 device is an efficient synchronous buck switching controller with a precision enable requiring no external compensation. The constant ON-time control scheme provides a simple design free of compensation components, allowing minimal component count and board space. The precision enable pin allows flexibility in sequencing multiple rails and setting UVLO. The LM1771 also incorporates a unique input feedforward to maintain a constant frequency independent of the input voltage. The LM1771 is optimized for a low-voltage input range of 2.8 V to 5.5 V and can provide an adjustable output as low as 0.8 V. Driving an external high-side PFET and low-side NFET, it can provide efficiencies as high as 95%.

Three versions of the LM1771 are available depending on the switching frequency desired for the application. Nominal switching frequencies are in the range of 100 kHz to 1000 kHz.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM1771	WSON (6)	3.00 mm × 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

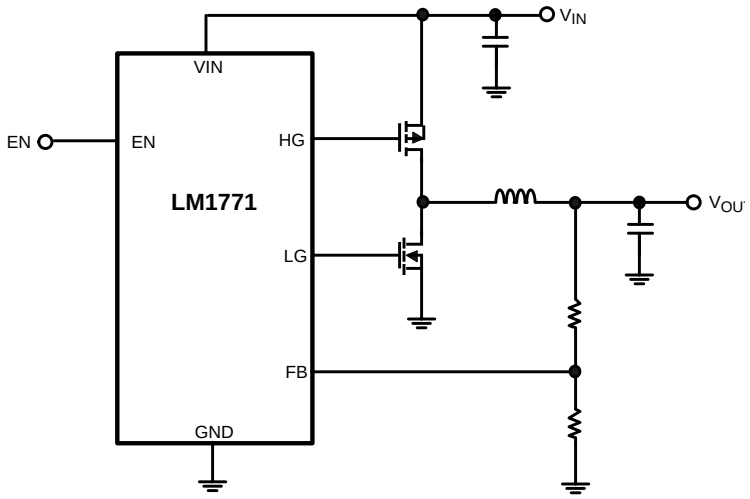


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 Detailed Description ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 12
8 Application and Implementation ... 13
8.1 Application Information ... 13
8.2 Typical Applications ... 13
9 Power Supply Recommendations ... 20
10 Layout ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Examples ... 21
10.3 Thermal Considerations ... 22
11 Device and Documentation Support ... 23
11.1 Device Support ... 23
11.2 Documentation Support ... 23
11.3 Community Resources ... 23
11.4 Trademarks ... 23
11.5 Electrostatic Discharge Caution ... 23
11.6 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D **Page**

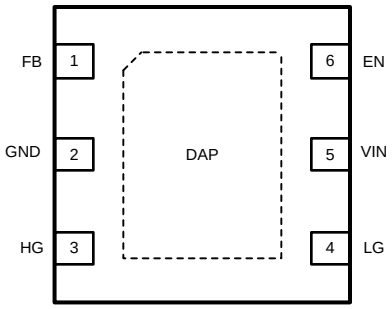
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision B (April 2013) to Revision C **Page**

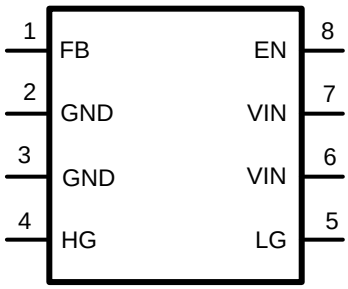
- Changed layout of National Data Sheet to TI format ... 22

5 Pin Configuration and Functions

NGG Package
6-Pin WSON
Top View



DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	WSON	VSSOP		
DAP	—	—	GND	Die Attach Pad is internally connected to GND, but it cannot be used as the primary GND connection
EN	6	8	I	Enable Pin
FB	1	1	A	Feedback Pin
GND	2	2, 3	GND	Ground
HG	3	4	AO	PFET Gate Drive
LG	4	5	AO	NFET Gate Drive
VIN	5	6, 7	PWR	Input Supply

(1) I = Input, A = Analog, GND = Ground, AO = Analog output, PWR = Power

6 Specifications

6.1 Absolute Maximum Ratings

See (1) (2)

		MIN	MAX	UNIT
V_{IN}		–0.3	6	V
EN, FB, HG, LG		–0.3	V_{IN}	V
Junction temperature			150	°C
Lead temperature	Soldering, 10 sec		260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{IN} to GND	2.8	5.5	V
Junction temperature, T_J	−40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LM1771		UNIT
		NGG (WSON)	DGK (VSSOP)	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.8	169.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	59.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.2	89.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	7.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	87.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specifications are for T_J = 25°C. All maximum and minimum limits apply over the full junction temperature range (−40°C to +125°C), unless otherwise specified. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. Unless otherwise specified, V_{IN} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback pin voltage		0.782	0.8	0.818	V
I_Q	Quiescent current	V_{FB} = 0.9 V		400	700	µA
T_{ON}	Switch ON-time	LM1771S - (500 ns)	0.4	0.5	0.6	µs
		LM1771T - (1000 ns)	0.8	1	1.2	
		LM1771U - (2000 ns)	1.6	2	2.4	
T_{OFF_MIN}	Minimum OFF-time	LM1771S - (500 ns)		150	250	ns
		LM1771T - (1000 ns)		135	225	
		LM1771U - (2000 ns)		120	220	
T_D	Gate drive dead-time			70		ns
V_{IH_EN}	EN pin rising threshold		1.15	1.2	1.25	V
V_{EN_HYS}	EN pin hysteresis			50	200	mV
I_{FB}	Feedback pin bias current	V_{FB} = 0.9 V		50		nA
V_{UVLO}	Undervoltage lockout	V_{IN} Rising Edge		2.65	2.8	V
V_{UVLO_HYS}	Undervoltage lockout hysteresis			50		mV
V_{SC_TH}	Feedback pin short circuit latch threshold		0.42	0.55	0.65	V
$R_{DS(ON)\ 1}$	HG FET driver pullup ON-resistance	I_{HG} = 20 mA		4		Ω
$R_{DS(ON)\ 2}$	HG FET driver pulldown ON-resistance	I_{HG} = 20 mA		6		Ω
$R_{DS(ON)\ 3}$	LG FET driver pullup ON-resistance	I_{LG} = 20 mA		4		Ω
$R_{DS(ON)\ 4}$	LG FET driver pulldown ON-resistance	I_{LG} = 20 mA		6		Ω

6.6 Typical Characteristics

All curves taken at VIN = 3.3 V with configuration in typical application circuit shown in *Typical Applications*. T_J = 25°C, unless otherwise specified.

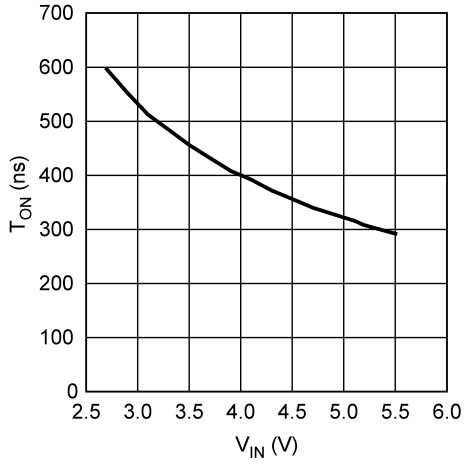


Figure 1. T_{ON} vs V_{IN} (LM1771S)

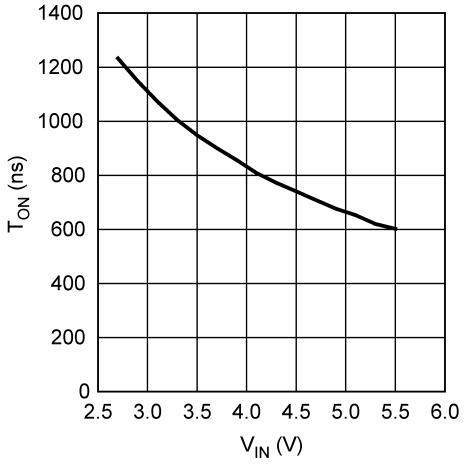


Figure 2. T_{ON} vs V_{IN} (LM1771T)

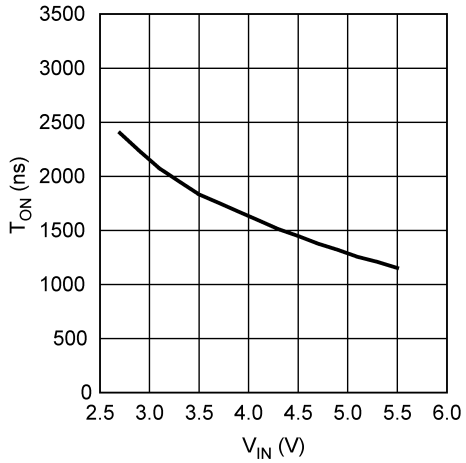


Figure 3. T_{ON} vs V_{IN} (LM1771U)

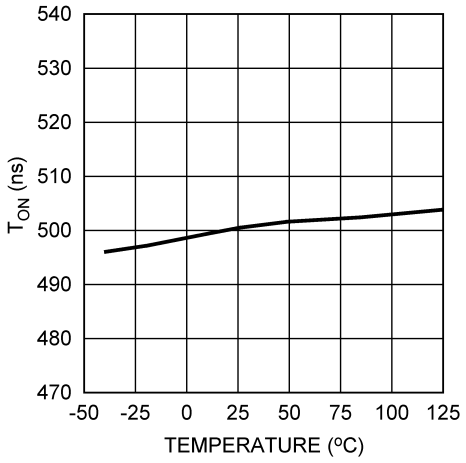


Figure 4. T_{ON} vs Temperature (LM1771S)

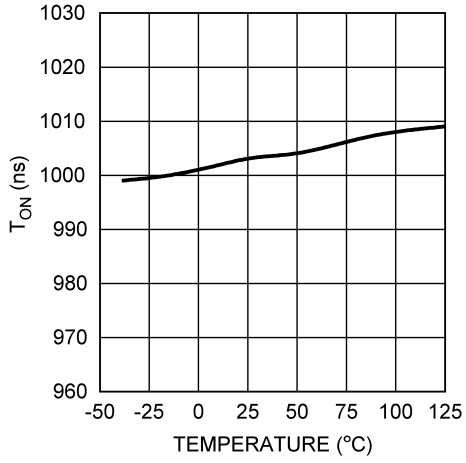


Figure 5. T_{ON} vs Temperature (LM1771T)

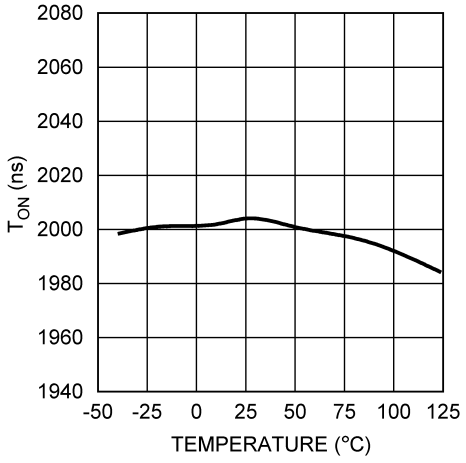


Figure 6. T_{ON} vs Temperature (LM1771U)

Typical Characteristics (continued)

All curves taken at VIN = 3.3 V with configuration in typical application circuit shown in *Typical Applications*. T_J = 25°C, unless otherwise specified.

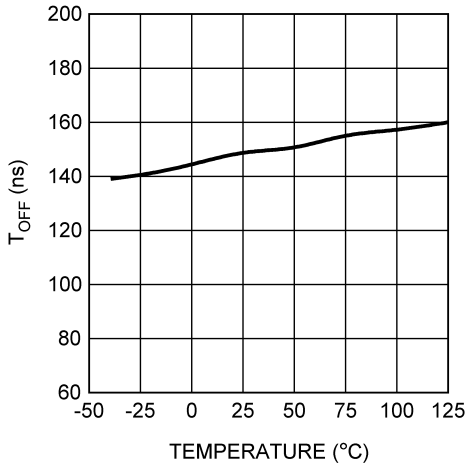


Figure 7. T_{OFF} vs Temperature (LM1771S)

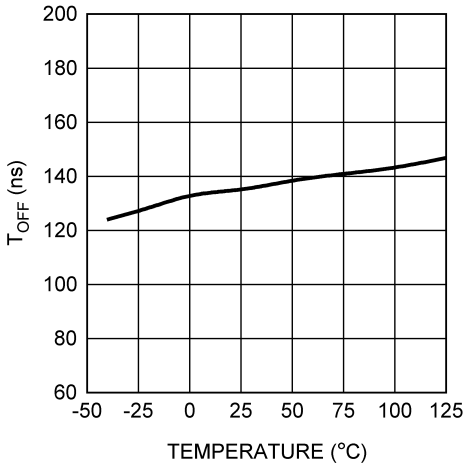


Figure 8. T_{OFF} vs Temperature (LM1771T)

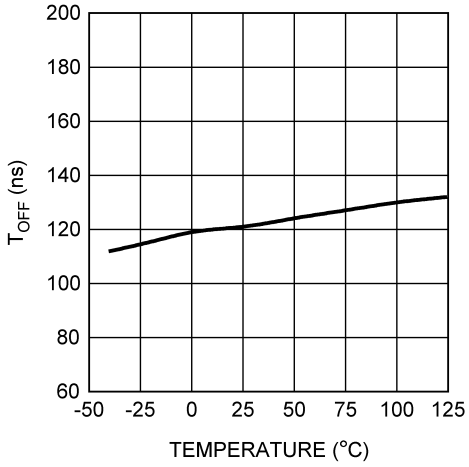


Figure 9. T_{OFF} vs Temperature (LM1771U)

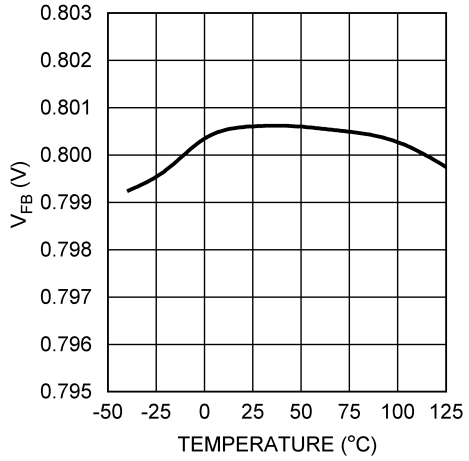


Figure 10. Feedback Voltage vs Temperature

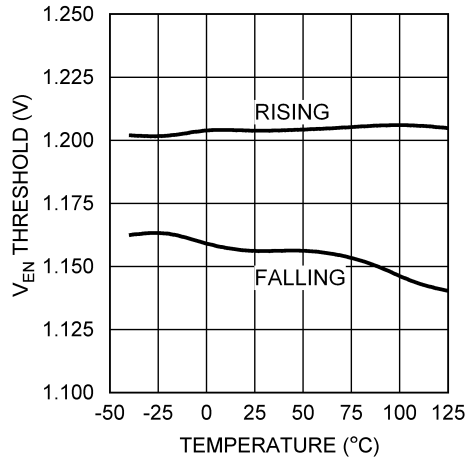


Figure 11. V_{EN} Threshold vs Temperature

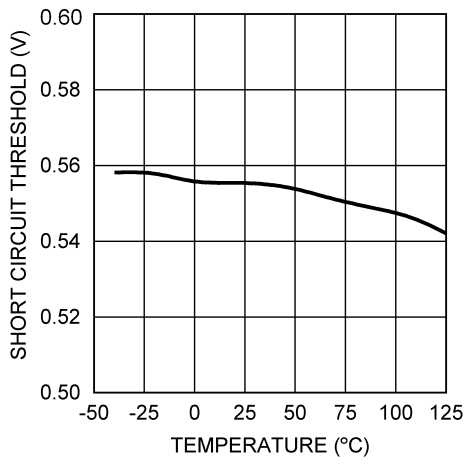


Figure 12. Short-Circuit Threshold vs Temperature

Typical Characteristics (continued)

All curves taken at VIN = 3.3 V with configuration in typical application circuit shown in *Typical Applications*. T_J = 25°C, unless otherwise specified.

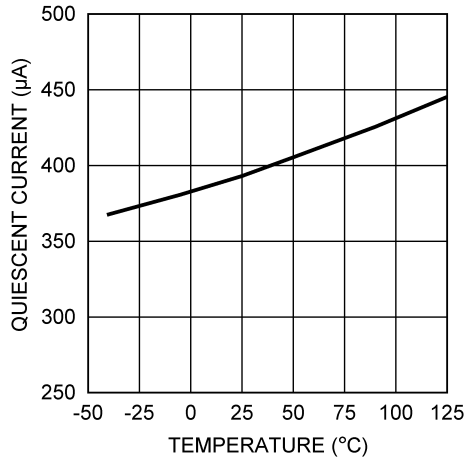


Figure 13. Quiescent Current vs Temperature

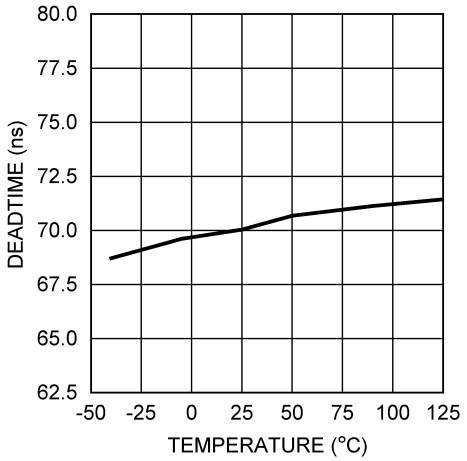
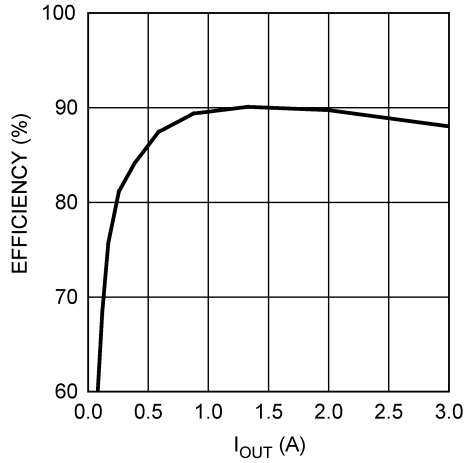
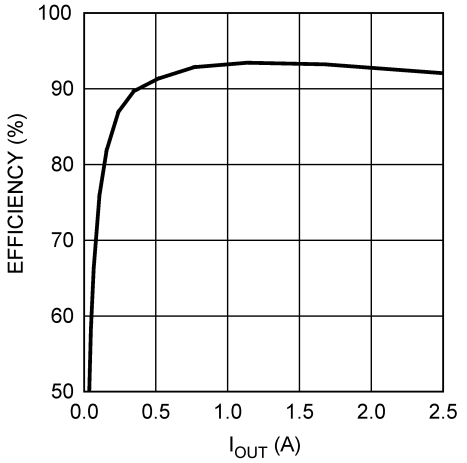


Figure 14. Dead-Time vs Temperature



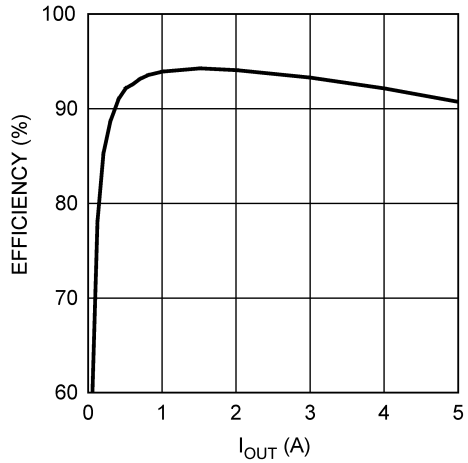
V_{IN} = 5 V V_{OUT} = 1.8 V F_{SW} = 545 kHz

Figure 15. Efficiency vs I_{OUT} (LM1771T)



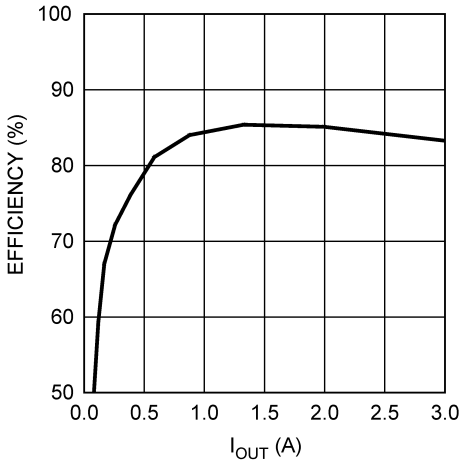
V_{IN} = 5 V V_{OUT} = 2.5 V F_{SW} = 379 kHz

Figure 16. Efficiency vs I_{OUT} (LM1771U)



V_{IN} = 5 V V_{OUT} = 3.3 V F_{SW} = 500 kHz

Figure 17. Efficiency vs I_{OUT} (LM1771U)



V_{IN} = 5 V V_{OUT} = 1.2 V F_{SW} = 727 kHz

Figure 18. Efficiency vs I_{OUT} (LM1771S)

7 Detailed Description

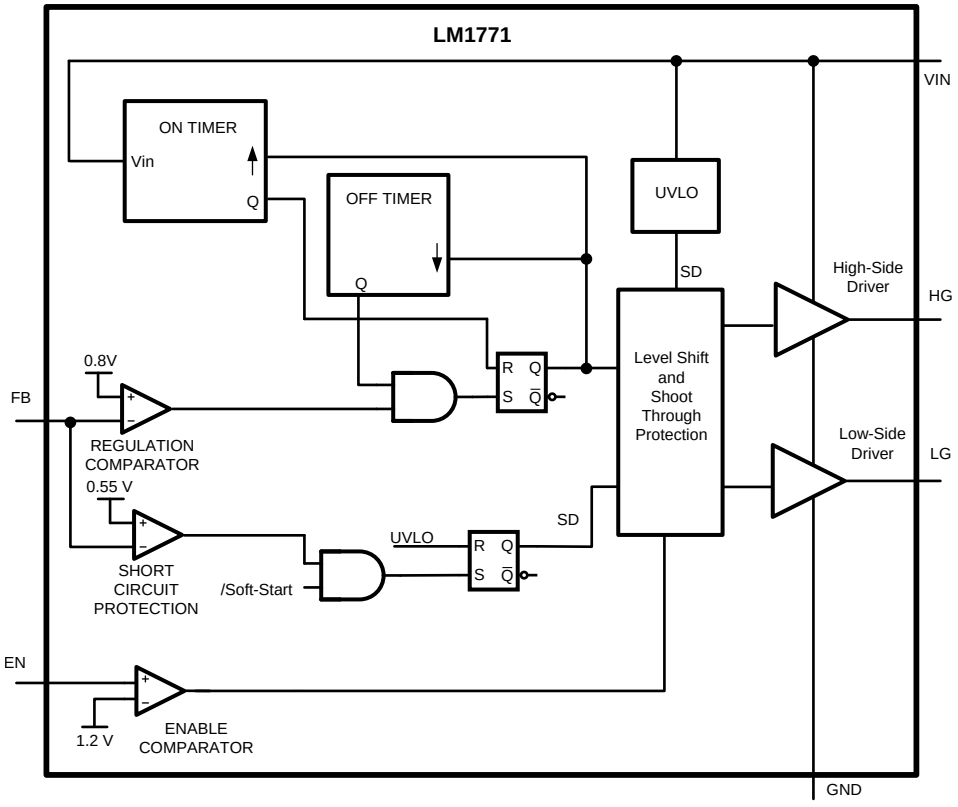
7.1 Overview

The LM1771 synchronous buck controller has a control scheme that is referred to as adaptive ON-time control. This topology relies on a fixed switch ON-time to regulate the output voltage. This ON-time is internally set by EEPROM and is available with three different set-points to allow for different frequency options. The LM1771 automatically adjusts the ON-time during operation inversely with the input voltage (VIN) to maintain a constant frequency. Therefore the switching frequency during continuous conduction mode is independent of the inductor and capacitor size unlike hysteretic switchers.

At the beginning of the cycle, the LM1771 turns on the high-side PFET for a fixed duration. This ON-time is predetermined (internally set by EEPROM and adjusted by V_{IN}) and the switch does not turn off until the timer has completed its period. The PFET then turns off for a minimum predetermined time period. This minimum T_{OFF} of 150 ns is internally set and cannot be adjusted. This is to prevent false triggering from occurring on the comparator due to noise from the SW node transition. After the minimum T_{OFF} period has expired, the PFET remains off until the comparator trip-point has been reached. Upon passing this trip-point (set at 0.8 V at the feedback pin), the PFET turns back on and the process repeats, thus regulating the output.

The NFET control is complementary to the PFET control with the exception of a short dead-time to prevent shoot-through from occurring.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Timing Opinion

Three versions of the LM1771 are available each with a predetermined T_{ON} set internally by EEPROM. This T_{ON} setting determines the switching frequency for the application. Derivation and calculation of the dependence of the switching frequency on V_{IN} and T_{ON} is shown in Equation 1 through Equation 6.

In a PWM buck switcher, Equation 1, Equation 2, and Equation 3 can be manipulated to obtain the switching frequency. Equation 1 shows the standard duty-cycle equation given by the volts-seconds balance on the inductor with Equation 2 and Equation 3 defining standard relationships:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$T_{ON} = D \times T_P \quad (2)$$

$$T_P = \frac{1}{f_{SW}} \quad (3)$$

Using these equations and solving for duty-cycle for Equation 4:

$$D = f_{SW} \times T_{ON} \quad (4)$$

Frequency can now be expressed in Equation 5:

$$F = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad (5)$$

Or simply written as Equation 6:

$$f_{SW} = \frac{V_{OUT}}{\alpha}$$

where

- $\alpha = V_{IN} \times T_{ON}$ (6)

To maintain a set frequency in an application, α is always held constant by varying T_{ON} inversely with V_{IN}. The three versions of the LM1771 are identified by the ON-times at a V_{IN} of 3.3 V for consistency. For clarification, see Table 1.

Table 1. Timing for All Variants

Product ID	T_{ON} at 3.3 V	α (V µs)
LM1771S	0.5 µs	1.65
LM1771T	1.0 µs	3.3
LM1771U	2.0 µs	6.6

The variation of T_{ON} versus V_{IN} can also be expressed graphically. These graphs can be found in the *Typical Characteristics* of the data sheet.

With α being a constant regardless of the version of the LM1771 used, Equation 6 shows that the only dependent variable remaining is V_{OUT}. Because V_{OUT} is a constant in any application, the frequency also remains constant. The switching frequency at which the application runs depends upon the V_{OUT} desired and the LM1771 version chosen. For any V_{OUT}, three frequency options (LM1771 versions) can be selected. This can be seen Table 2. The recommended frequency range of operation is 100 kHz to 1000 kHz.

Table 2. Frequency vs V_{OUT} for Variants

V_{OUT}	TIMING OPTIONS (1)		
	500 ns	1000 ns	2000 ns
0.8	485	242	121
1	606	303	152
1.2	727	364	182
1.5	909	455	227
1.8	1091	545	273
2.5	1515	758	379
3.3	2000	1000	500

(1) Switching Frequency (kHz) of LM1771 based on output voltage and timing option.

7.3.2 Short-Circuit Protection

The LM1771 has an internal short-circuit comparator that constantly monitors the feedback node (except during soft-start). If the feedback voltage drops below 0.55 V (equivalent to the output voltage dropping below 68% of nominal), the comparator trips causing the part to latch off. The LM1771 does not resume switching until the input voltage is taken below the UVLO threshold and then brought back into its normal operating range, or the part is disabled then re-enabled through the enable pin. The purpose of this function is to prevent a severe short circuit from causing damage to the application. Due to the fast transient response of the LM1771 a severe short on the output causing the feedback to drop would only occur if the load applied had an effective resistance that approaches the PMOS $R_{DS(ON)}$.

7.3.3 Precision Enable

The LM1771 features a precision enable circuit. If the voltage on the EN pin is 1.2 V or greater, the part is enabled and switching occurs. If the enable voltage falls below 1.2 V, the part is placed into a shutdown state and the drivers is tri-stated. This allows the LM1771 to be easily sequenced using a resistive divider from the output of another regulator, or the working input voltage range of the LM1771 to be set using a resistive divider on V_{IN}. There is no internal pullup connected to the EN pin, so an external signal is required to initiate switching.

NOTE

When power is first applied to the LM1771, there is a slight delay before the enable comparator is functional. During this delay, typically on the order of 400 µs, the part is disabled regardless of the voltage on the EN pin. The falling enable threshold features 50 mV of hysteresis

7.3.4 Soft-Start

To limit in-rush current and allow for a controlled start-up the LM1771 incorporates an internal soft-start scheme. Every time the enable voltage rises above 1.2 V while V_{IN} is greater than the UVLO threshold, the LM1771 goes through an adaptive soft-start that limits the ON-time and expands the minimum OFF-time. In addition the part only activates the PMOS allowing a discontinuous mode of operation enabling a prebiased start-up. The time spent in soft-start depends on the load applied to the output, but is usually close to a set time that is dependent on the timing option. The approximate soft-start time can be seen in Table 3 for each timing option.

Table 3. Soft-Start Timing for All Variants

PRODUCT ID	TIMING	T_{SS}
LM1771S	0.5 µs	1 ms
LM1771T	1.0 µs	1.2 ms
LM1771U	2.0 µs	1.8 ms

Therefore, if the input supply is extremely slow rising such that at the end of soft-start the input voltage is still near the UVLO threshold, a timing option must be chosen to ensure that maximum duty-cycle permits the output to meet the minimum condition. TI recommends using the 2000-ns option (LM1771U) in conditions where the output voltage is 2.5 V or greater to avoid false latch-offs when there is concern regarding the input supply slew rate.

NOTE

As soon as soft-start terminates the short-circuit protection is enabled. This means that if the output voltage does not reach at least 68% of its final value the part latches off.

In some situations, the internal soft-start routine can create a slight overshoot on the output voltage. If this must be avoided, the use of a feedforward capacitor as detailed in the *Feedforward Capacitor* section.

7.3.5 Jitter

The LM1771 uses an adaptive ON-time control scheme that relies on the output voltage ripple to provide a consistent switching frequency. Under certain conditions, excessive noise can couple onto the feedback pin causing the switch node to appear to have a slight amount of jitter. This is not indicative of an unstable design. The output voltage still regulates to the exact same value. Careful component selection and layout must minimize any external influence.

In addition to any external noise that can add to the jitter seen on the switch node, the LM1771 always has a slight amount of switch jitter. This is because the LM1771 makes a small alteration in the reference voltage every 128 cycles to improve its accuracy and long-term performance. This has the effect of causing a change in the switching frequency at that instant. When viewed on an oscilloscope this can be seen as a jitter in the switch node. The change in feedback voltage or output voltage, however, is almost indistinguishable.

7.4 Device Functional Modes

The LM1771 has essentially one normal operational mode: in normal operation, the part operates in full synchronous mode to regulate the FB input to 0.8 V (typical) after soft-start period is over. The EN pin allows the user to shut down the part. When the part is enabled, the IC enters soft-start for 1 ms to 1.8 ms depending on the variant of the IC. See *Soft-Start* for more detail on the soft-start pattern.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

Design Guide details the design procedure to follow for the typical application. Because of the nature of constant ON-time controller, a certain degree of iteration might be necessary on the sizing of some key components to achieve optimal response, such as the inductor L1.

8.2 Typical Applications

8.2.1 LM1771 Typical Application

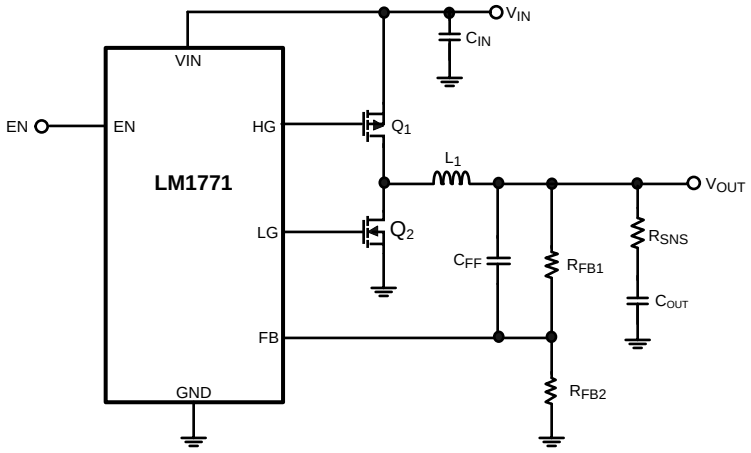


Figure 19. Example Circuit Schematic

8.2.1.1 Design Requirements

The main parameters needed to successfully design an application based on the LM1171 are typical of buck DC–DC converters. The input and output voltage must be known as well as the worst-case input voltage operating conditions. The maximum output current helps the designer size the inductor appropriately. In addition, the designer needs to be aware of the requirement on the output capacitor to achieve stable operation. See *Output Capacitor* for details on the output capacitor requirements.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Design Guide

As with any DC–DC converter, numerous trade-offs are possible to optimize the design for efficiency, size, or performance. These are taken into account and highlighted throughout this discussion.

Equation 7 calculates for any buck converter is duty-cycle. Ignoring conduction losses associated with the FETs and parasitic resistances it can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (7)$$

A more accurate calculation for duty-cycle can be used that takes into account the voltage drops across the FETs. Equation 8 determines the slight load dependency on switch frequency if needed. Otherwise the simplified equation works well for component calculation.

Typical Applications (continued)

$$D = \frac{V_{OUT} + V_{DS\_NMOS}}{V_{IN} + V_{DS\ NMOS} + V_{DS\ PMOS}} \quad (8)$$

8.2.1.2.1.1 Frequency Selection

The LM1771 is available with three preset timing options that select the ON-time and hence determine the switching frequency of the application. Increasing the switching frequency has the effect of reducing the inductor size needed for the application while requiring a slight trade-off in efficiency. Table 4 shows the same frequency table as shown earlier (Table 2) with the exception that the recommended timing option for each V_{OUT} is highlighted. TI does not recommend using a high switching frequency with V_{OUT} equal to or greater than 2.5 V due to the maximum duty-cycle limitations of the device coupled with the internal start-up.

Table 4. Recommended Switching Frequency vs V_{OUT}

V_{OUT}	TIMING OPTIONS (1)		
	500 ns	1000 ns	2000 ns
0.8	485	242	-
1	606	303	-
1.2	727	364	-
1.5	909	455	2237
1.8	-	545	273
2.5	-	-	379
3.3	-	-	500

(1) Recommended switching frequency (kHz) based on output voltage and timing option.

8.2.1.2.1.2 Inductor Selection

The inductor selection is an iterative process likely requiring several passes before settling on a final value. The reason for this is because it influences the amount of ripple seen at the output, a critical component to ensure general stability of an adaptive ON-time circuit. For the first pass at inductor selection the value can be obtained by targeting a maximum peak-to-peak ripple current equal to 30% of the maximum load current. The inductor current ripple (ΔI_L) can be calculated by Equation 9:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}} \quad (9)$$

Therefore, L can be initially set by applying the 30% rule in Equation 10:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{0.3 \times f_{SW} \times I_{OUT}} \quad (10)$$

The other features of the inductor that can be selected besides inductance value are saturation current and core material. Because the LM1771 does not have a current limit, TI recommends having a saturation current higher than the maximum output current to handle any ripple or momentary overcurrent events. The core material also influences the saturation characteristics as ferrite materials have a hard saturation curve and take care that they never saturate during normal use. A shielded inductor or low-profile unshielded inductor is recommended to reduce EMI. This also helps prevent any spurious noise from picking up on the feedback node resulting in unexpected tripping of the feedback comparator.

8.2.1.2.1.3 Output Capacitor

One of the most important components to select with the LM1771 is the output capacitor. This is because its size and ESR have a direct effect on the stability of the loop. A constant ON-time control scheme works by sensing the output voltage ripple and switching the FETs appropriately. The output voltage ripple on a buck converter can be approximated by stating that the AC inductor ripple flows entirely into the output capacitor and is created by the ESR of the capacitor. This can be expressed in Equation 11:

$$\Delta V_{OUT} = \Delta I_L \times R_{ESR} \quad (11)$$

To ensure stability, two constraints need to be met. The first is that there is sufficient ESR to create enough voltage ripple at the feedback pin. TI recommends having at least 10 mV of ripple seen at the feedback pin. This can be calculated by multiplying the output voltage ripple by the gain seen through the feedback resistors. This gain, H, can be calculated in Equation 12:

$$H = \frac{V_{FB}}{V_{OUT}} = \frac{0.8V}{V_{OUT}} \quad (12)$$

If the output voltage is fairly high, causing significant attenuation through the feedback resistors, a feedforward capacitor can be used. This is actually recommended for most circuits as it improves performance. See the *Feedforward Capacitor* section for more details.

The second criteria is to ensure that there is sufficient ripple at the output that is in-phase with the switch. The problem exists that there is actually ripple caused by the capacitor charging and discharging, not only the ESR ripple. Because these are effectively out of phase, problems can exist. To avoid this issue, TI recommends that the ratio of the two ripples (β) is always greater than 5. To calculate the minimum ESR value needed, Equation 13 can be used:

$$I_{CIN\_RMS} = I_{OUT} \sqrt{D\left(1 - D + \frac{\Delta I_L^2}{12 \times I_{OUT}^2}\right)} \quad (13)$$

In general, the best capacitors to use are chemistries that have a known and consistent ESR across the entire operating temperature range. Tantalum capacitors or similar chemistries such as Niobium Oxide perform well along with certain families of Aluminum Electrolytics. Small value POSCAPs and SP CAPs also work as they have sufficient ESR. When used in conjunction with a low-value inductor it is possible to have an extremely stable design. The only capacitors that require modification to the circuit are ceramic capacitors. Ceramic capacitors cause problems meeting both criteria because they have low ESR and low capacitance. Therefore, if they are to be used, an external ESR resistor (R_{SNS}) must be added. This can be seen in Figure 20.

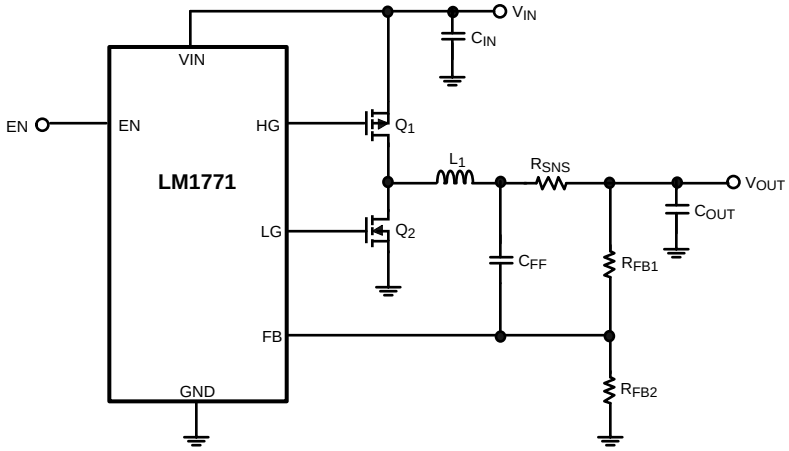


Figure 20. LM1771 With an External ESR Resistor (R_{SNS})

This circuit uses an additional resistor in series with the inductor to add ripple at the output. It is placed in this location and used in combination with the feedforward capacitor (C_{FF}) to provide ripple to the feedback pin, without adding ripple or a DC offset to the output. The benefit of using a ceramic capacitor is still obtained with this technique. Because the addition of the resistor results in power loss, this circuit implementation is only recommended for low currents (2 A and below). The power loss and rating of the resistor must be taken into account when selecting this component.

This circuit implementation using the feedforward capacitor begins to experience limitations when the output voltage is small. Previously the circuit relied on the C_{FF} for all the ripple at the feedback node by assuming that the resistor divider was negligible. As V_{OUT} decreases this can not be assumed. The resistor divider contributes a larger amount of ripple which is problematic as it is also out of phase. Therefore the resistor location must be changed to be in series with the output capacitor. This can be viewed as adding an effective ESR to the output capacitor. This can be seen in Figure 21.

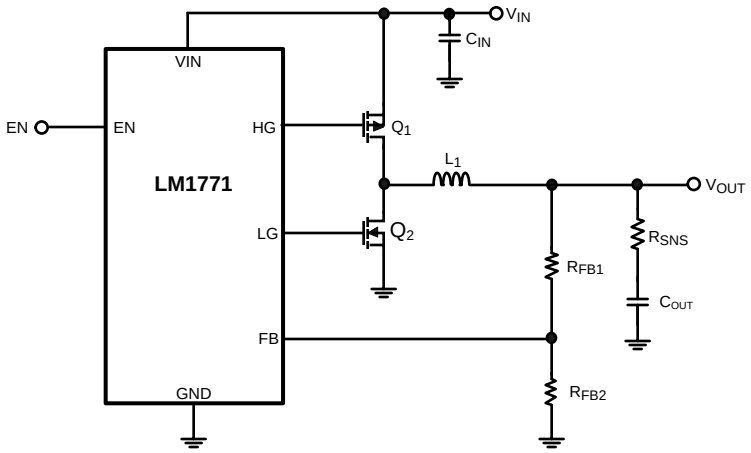


Figure 21. LM1771 With ESR Resistor (R_{SNS}) in Series With Output Capacitor

8.2.1.2.1.4 Feedforward Capacitor

The feedforward capacitor is used across the top feedback resistor to provide a lower impedance path for the high-frequency ripple without degrading the DC accuracy. Typically the value for this capacitor must be small enough to prevent load transient errors because of the discharging time, but large enough to prevent attenuation of the ripple voltage. In general a small ceramic capacitor in the range of 1 nF to 10 nF is sufficient.

If C_{FF} is used then it can be assumed that the ripple voltage seen at the feedback pin is the same as the ripple voltage at the output. The attenuation factor H no longer needs to be used. However, in these conditions, TI recommends having a minimum of 20-mV ripple at the feedback pin. The use of a C_{FF} capacitor is recommended as it improves the regulation and stability of the design. However, its benefit is diminished as V_{OUT} starts approaching V_{REF} , therefore it is not needed in this situation.

8.2.1.2.1.5 Input Capacitor

The dominating factor that usually sets the size of an input capacitor is the current handling ability. This is usually determined by the package size and ESR of the capacitor. If these two criteria are met then there usually must be enough capacitance to prevent impedance interactions with the source. In general, TI recommends using a ceramic capacitor for the input as they provide a low impedance and small footprint.

NOTE

Use a good dielectric for the ceramic capacitor such as X5R or X7R. These provide better over temperature performance and also minimize the DC voltage derating that occurs on Y5V capacitors.

To calculate the input capacitor RMS current, Equation 14 can be used:

$$I_{CIN\_RMS} = I_{OUT} \sqrt{D\left(1 - D + \frac{\Delta I_L^2}{12 \times I_{OUT}^2}\right)} \quad (14)$$

which can be approximated by, Equation 15

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1 - D)} \quad (15)$$

8.2.1.2.2 MOSFET Selection

The two FETs used in the LM1771 requires attention to selection of parameters to ensure optimal performance of the power supply. The high-side FET must be a PFET and the low-side an NFET. These can be integrated in one package or as two separate packages.

8.2.1.2.2.1 VDS Voltage Rating

The first selection criteria is to select FETs that have sufficient V_{DS} voltage ratings to handle the maximum voltage seen at the input plus any transient spikes that can occur from parasitic ringing. In general most FETs available for this application have ratings from 8 V to 20 V. If a larger voltage rating is used then the performance is most likely be degraded because of higher gate capacitance.

8.2.1.2.2.2 RDSON

The $R_{DS(ON)}$ specification is important as it determines several attributes of the FET and the overall power supply. The first is that it sets the maximum current of the FET for a given package. A lower $R_{DS(ON)}$ permits a higher allowable current and reduce conduction losses, however, it increases the gate capacitance and the switching losses.

8.2.1.2.2.3 Gate Drive

The next step is to ensure that the FETs are capable of switching at the low V_{in} supplies used by the LM1771. The FET must have the Rdson specified at either 1.8 V or 2.5 V to ensure that it can switch effectively as soon as the LM1771 starts up.

8.2.1.2.2.4 Gate Charge

Because the LM1771 uses a fixed dead-time scheme to prevent cross conduction, the FET transitions must occur in this time. The rise and fall time of the FETs gate can be influenced by several factors including the gate capacitance. Therefore the total gate charge of both FETs must be limited to less than 20 nC at 4.5 V V_{GS}. The lower the number the faster the FETs must switch and the better the efficiency.

8.2.1.2.2.5 Rise and Fall Times

A better indication of the actual switching times of the FETs can be found in their *Electrical Characteristics* table. The rise and fall time must be specified and selected to be at a minimum. This helps improve efficiency and ensuring that shoot-through does not occur.

8.2.1.2.2.6 Gate Charge Ratio

Another consideration in selecting the FETs is to pay attention to the Qgd / Qgs ratio. The reason for this is that proper selection can prevent spurious turnon. If we look at the NFET for example, when the FET is turning off, the gate signal pulls to ground. Conversely the PFET is turning on, causing the SW node to rise towards V_{IN}. The gate-to-drain capacitance of the NFET couples the SW node to the gate and causes it to rise. If this voltage is excessive, then it could weakly turn on the low-side FET causing an efficiency loss. However, this coupling is mitigated by having a large gate to source capacitance of the FET, which helps to hold the gate voltage down. Ideally, a very low Qgd / Qgs would be ideal, but in practice it is common to find the number around 1. As a general rule, the lower the ratio, the better.

If the above selection criteria have been met it is useful to generate a figure of merit to allow comparison between the FETs. One such method is to multiply the $R_{DS(ON)}$ of the FET by the total gate charge. This allows an easy comparison of the different FETs available. Once again, the lower the product, the better.

8.2.1.2.2.7 Feedback Resistors

The feedback resistors are used to scale the output voltage to the internal reference value such that the loop can be regulated. The feedback resistors must not be made arbitrarily large as this creates a high impedance node at the feedback pin that is more susceptible to noise. A combined value of 50 kΩ for the two resistors is adequate. To calculate the resistor values use Equation 16. Typically, the low-side resistor is initially set to a predetermined value such as 10 kΩ.

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (16)$$

where

- V_{FB} is the internal reference voltage that can be found in the *Electrical Characteristics* table or approximated by 0.8 V

The output voltage value can be set in a precise manner by taking into account the fact that the reference voltage is regulating the bottom of the output ripple as opposed to the average value. This relationship is shown in Figure 22.

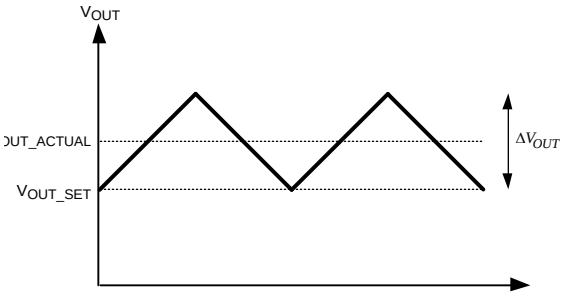


Figure 22. Output Voltage Waveform

The average output voltage (V_{OUT_ACTUAL}) is higher than the output voltage (V_{OUT_SET}) that was calculated by the earlier equation by exactly half the output voltage ripple. The output voltage that is targeted for regulation may then be appended according to the voltage ripple. This can be seen in Equation 17:

$$V_{OUT\_ACTUAL} = V_{OUT\_SET} + ½\Delta V_{OUT} = V_{OUT\_SET} + ½\Delta I_L \times R_{ESR} \quad (17)$$

8.2.1.2.3 Efficiency Calculations

One of the most important parameters to calculate during the design stage is the expected efficiency of the system. This can help determine optimal FET selection and can be used to calculate expected temperature rise of the individual components.

8.2.1.2.3.1 Quiescent Current

The quiescent current consumed by the LM1771 is one of the major sources of loss within the controller. However, from a system standpoint this is usually less than 0.5% of the overall efficiency. Therefore, it could easily be omitted but is shown for completeness:

$$P_{IQ} = V_{IN} \times I_Q \quad (18)$$

8.2.1.2.3.2 Conduction Loss

There are three losses associated with the external FETs. From the DC standpoint there is the I-squared R loss, caused by the ON-resistance of the FET. This can be modeled for the PMOS by:

$$P_{P\_COND} = D \times R_{DSON\_PMOS} \times I_{OUT}^2 \quad (19)$$

and the NMOS by:

$$P_{N\_COND} = (1 - D) \times R_{DSON\_NMOS} \times I_{OUT}^2 \quad (20)$$

8.2.1.2.3.3 Switching Loss

The next loss is the switching loss that is caused by the need to charge and discharge the gate capacitance of the FETs every cycle. This can be approximated by:

$$P_{P\_SWITCH} = V_{IN} \times Q_{g\_PMOS} \times f_{SW} \quad (21)$$

for the PMOS, and the same approach can be adapted for the NMOS:

$$P_{N\_SWITCH} = V_{IN} \times Q_{g\_NMOS} \times f_{SW} \quad (22)$$

8.2.1.2.3.4 Transitional Loss

The last FET power loss is the transitional loss. This is caused by switching the PMOS while it is conducting current. This approach only models the PMOS transition, the NMOS loss is considered negligible because it has minimal drain to source voltage when it switches due to the conduction of the body diode. Therefore the transitional loss of the PMOS can be modeled by:

$$P_{P\_TRANSITIONAL} = 0.5 \times V_{IN} \times I_{OUT} \times f_{SW} \times (t_r + t_f) \quad (23)$$

t_r and t_f are the rise and fall times of the FET and can be found in their corresponding datasheet. Typically these numbers are simulated using a 6-Ω drive, which corresponds well to the LM1771. Given this, no adjustment is needed.

8.2.1.2.3.5 DCR Loss

The last source of power loss in the system that needs to be calculated is the loss associated with the inductor resistance (DCR) which can be calculated by Equation 24:

$$P_{DCR} = R_{DCR} \times I_{OUT}^2 \quad (24)$$

8.2.1.2.3.6 Efficiency

The efficiency, η, can then be calculated by summing all the power losses and then using Equation 25:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSSES}} \quad (25)$$

8.2.1.3 Application Curve

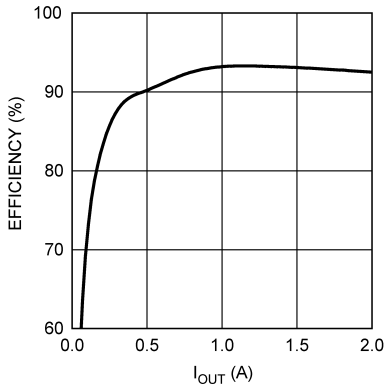


Figure 23. Typical Efficiency 5 V_{IN} to 2.5 V_{OUT}

8.2.2 Example Application 5 V_{IN} to 1.8 V_{OUT}

Figure 24 and Table 5 show an application with conversion from 5-V input to 1.8-V output with a switching frequency of 1.1 MHz and a 2-A maximum output current.

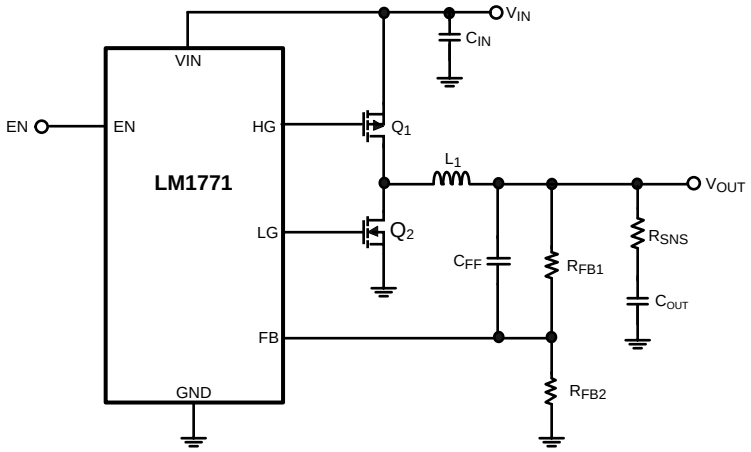


Figure 24. Example Circuit Schematic, 5 V_{IN} to 1.8 V_{OUT}

Table 5. Bill of Materials (5-V to 1.8-V Conversion, f_{SW} = 1090 kHz, I_{OUT} = 2 A)

DESIGNATOR	DESCRIPTION	PART NUMBER	QUANTITY	VENDOR
U_1	LM1771, 500 ns	LM1771S	1	Texas Instruments
Q_1	PMOS	Si3867DV	1	Siliconix
Q_2	NMOS	Si3460DV	1	Siliconix
C_{IN}	22-µF Capacitor, 0805	GRM21BR60J226ME39	1	Murata
C_{OUT}	100-µF Capacitor, 6.3 V, 100 mΩ	TPSY107M006R0100	1	AVX
R_{FB1}	12.4-kΩ Resistor, 0603	CRCW06031242F	1	Vishay
R_{FB2}	10-kΩ Resistor, 0603	CRCW06031002F	1	Vishay
C_{FF}	1-nF Capacitor, 0603	VJ0603102KXXA	1	Vishay
L	3.3-µH Inductor	MSS7341-332NLB	1	Coilcraft

8.2.3 Example Application 5 V_{IN} to 3.3 V_{OUT}

Figure 25 and Table 6 show an application with conversion from 5-V input to 3.3-V output with a switching frequency of 500 kHz and a 5-A maximum output current.

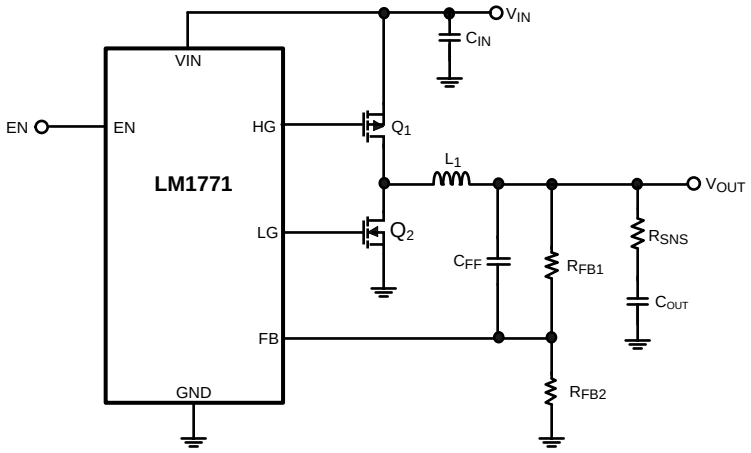


Figure 25. Example Circuit Schematic, 5 V_{IN} to 3.3 V_{OUT}

Table 6. Bill of Materials (5-V to 3.3-V Conversion, f_{SW} = 500 kHz, I_{OUT} = 5 A)

DESIGNATOR	DESCRIPTION	PART NUMBER	QUANTITY	VENDOR
U_1	LM1771, 200 ns	LM1771U	1	Texas Instruments
Q_1	PMOS	Si9433BDY	1	Siliconix
Q_2	NMOS	Si4894DY	1	Siliconix
C_{IN}	100-µF Capacitor, 1812	GRM43SR60J107ME20B	1	Murata
C_{OUT}	150-µF Capacitor, 6.3 V, 70 mΩ	NOSD157M006R0070	1	AVX
R_{FB1}	29.4-kΩ Resistor, 0805	CRCW08052942F	1	Vishay
R_{FB2}	10-kΩ Resistor, 0805	CRCW08051002F	1	Vishay
C_{FF}	1-nF Capacitor, 0805	VJ0805102KXXA	1	Vishay
L	2.2-µH Inductor	DO3316P-222	1	Coilcraft

9 Power Supply Recommendations

The power line feeding the LM1771 must have low impedance. The input capacitor of the system must be placed as close to VIN as possible. If the power supply is very noisy, an additional bulk capacitor might be necessary in the system to ensure that clean power is delivered to the IC.

10 Layout

10.1 Layout Guidelines

The LM1771, like all switching regulators, requires careful attention to layout to ensure optimal performance. The following steps must be taken to aid in the layout. For more information refer to Application Note AN-1299 (SNVA074).

1. Ensure that the ground connections of the input capacitor, output capacitor and NMOS are as close as possible. Ideally these must all be grounded together in close proximity on the component side of the board.
2. Keep the switch node small to minimize EMI without degrading thermal cooling of the FETs.
3. Locate the feedback resistors close to the IC and keep the feedback trace as short as possible. Do not run any feedback traces near the switch node.
4. Keep the gate traces short and keep them away from the switch node as much as possible.
5. If a small bypass capacitor is used on V_{IN} (0.1 µF) place it as close to the pin, with the ground connection as close to the chip ground, as possible.

10.2 Layout Examples

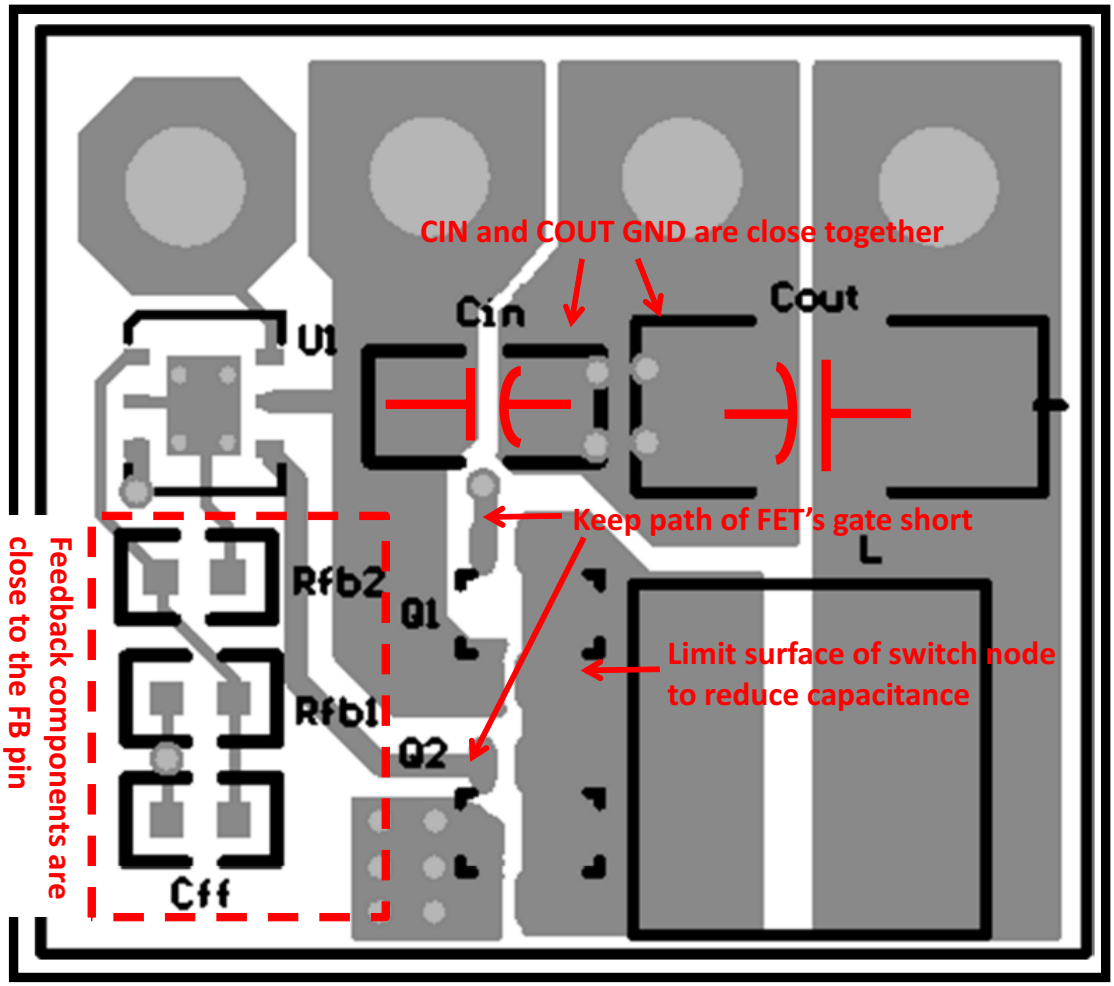


Figure 26. LM1771 Layout Example (Top)

Layout Examples (continued)

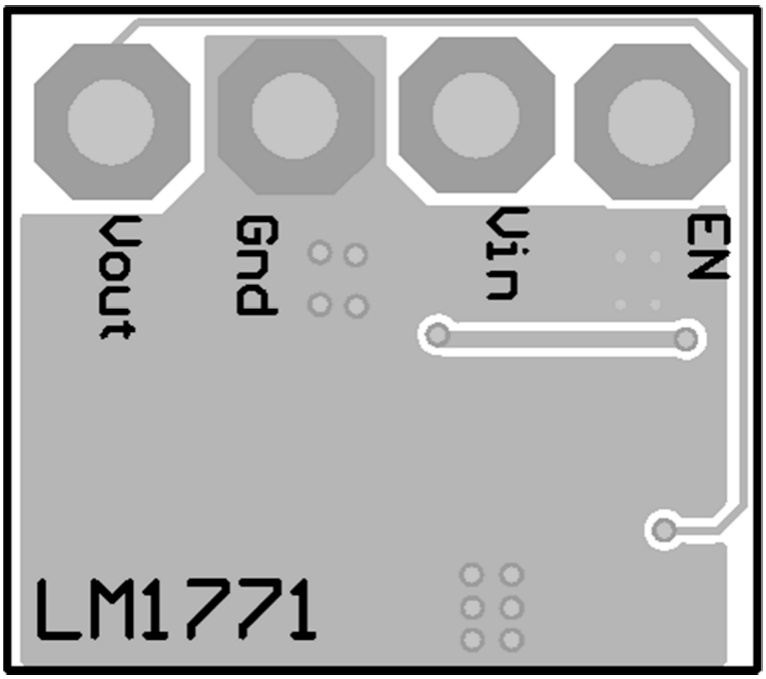


Figure 27. LM1771 Layout Example (Bottom)

10.3 Thermal Considerations

By breaking down the individual power loss in each component it makes it easy to determine the temperature rise of each component. Generally the expected temperature rise of the LM1771 is extremely low as it is not in the power path. Therefore the only two items of concern are the PMOS and the NMOS. The power loss in the PMOS is the sum of the conduction loss and transitional loss, while the NMOS only has conduction loss. It is assumed that any loss associated with the body diode conduction during the dead-time is negligible.

For completeness of design it is important to watch out for the temperature rise of the inductor. Assuming the inductor is kept out of saturation the predominant loss is the DC copper resistance. At higher frequencies, depending on the core material, the core loss could approach or exceed the DCR losses. Consult with the inductor manufacturer for appropriate temp curves based on current.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

User's Guide, *AN-1299 LM5041 Evaluation Board,* SNVA074

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1771SMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		SNRB	Samples
LM1771SSD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1771S	Samples
LM1771TMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		SNSB	Samples
LM1771UMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		SNTB	Samples
LM1771USD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1771U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

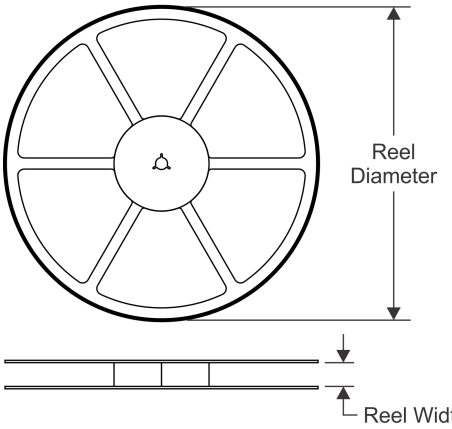
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

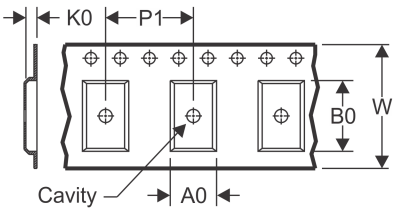
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

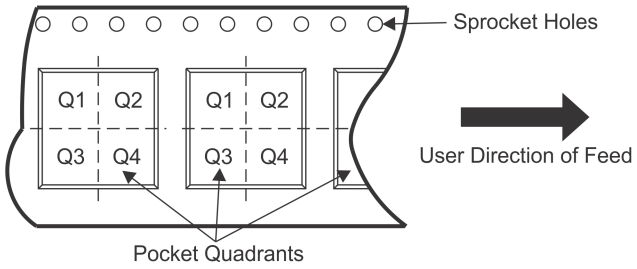


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

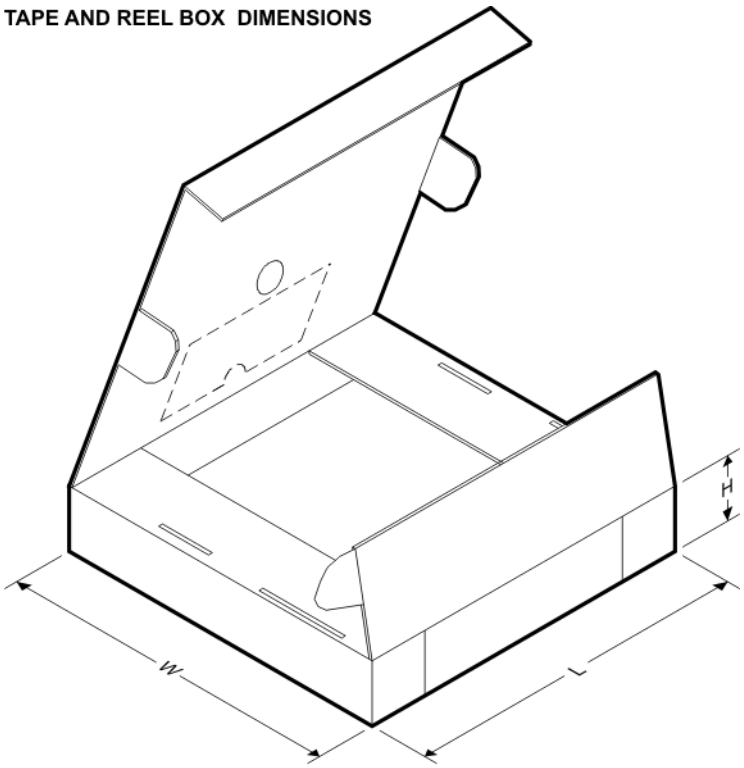
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM1771SMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM1771SSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM1771TMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM1771UMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM1771USD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

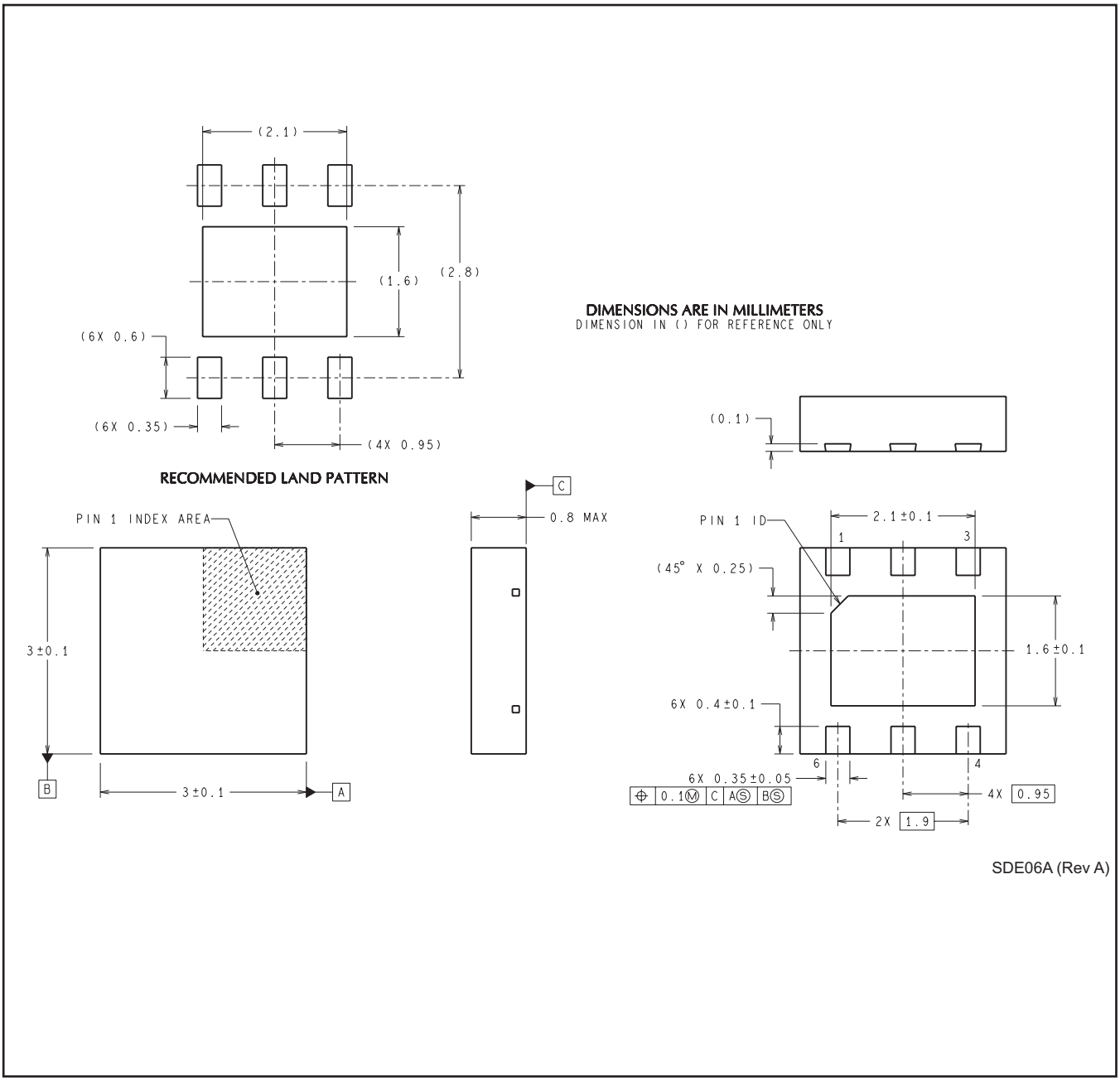
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

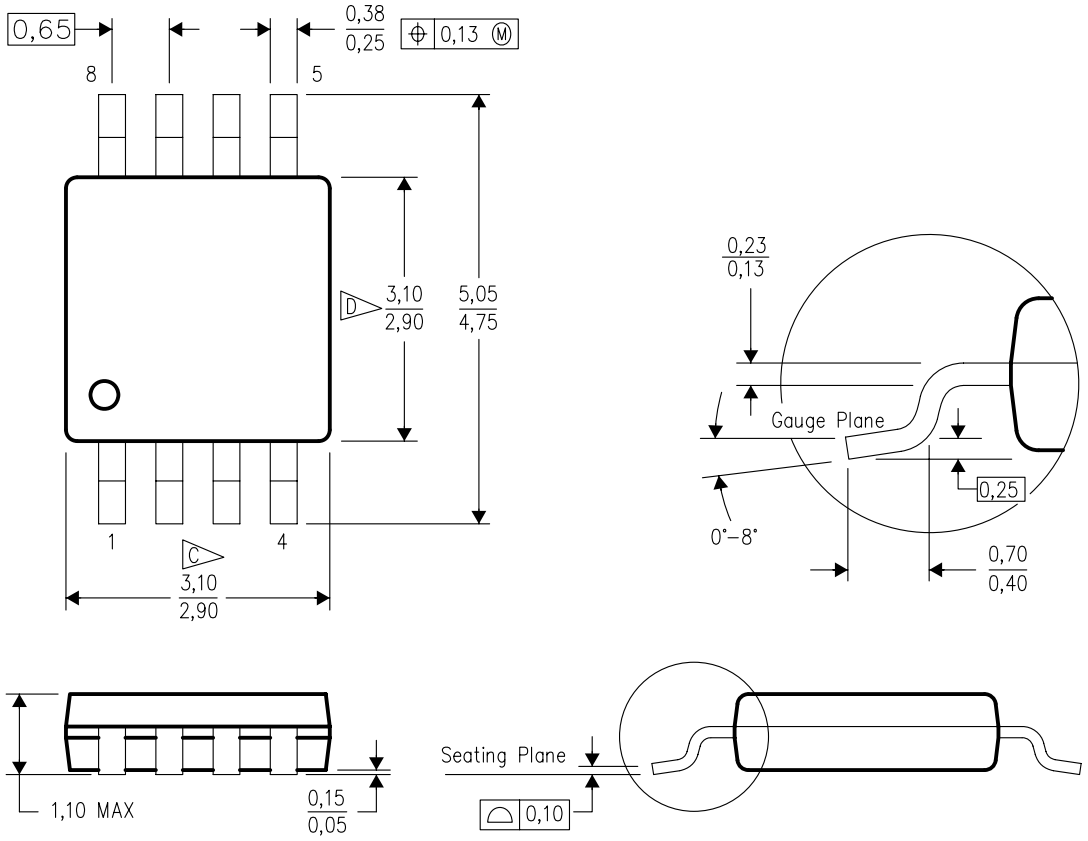
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM1771SMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM1771SSD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM1771TMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM1771UMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM1771USD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0

NGG0006A



SDE06A (Rev A)

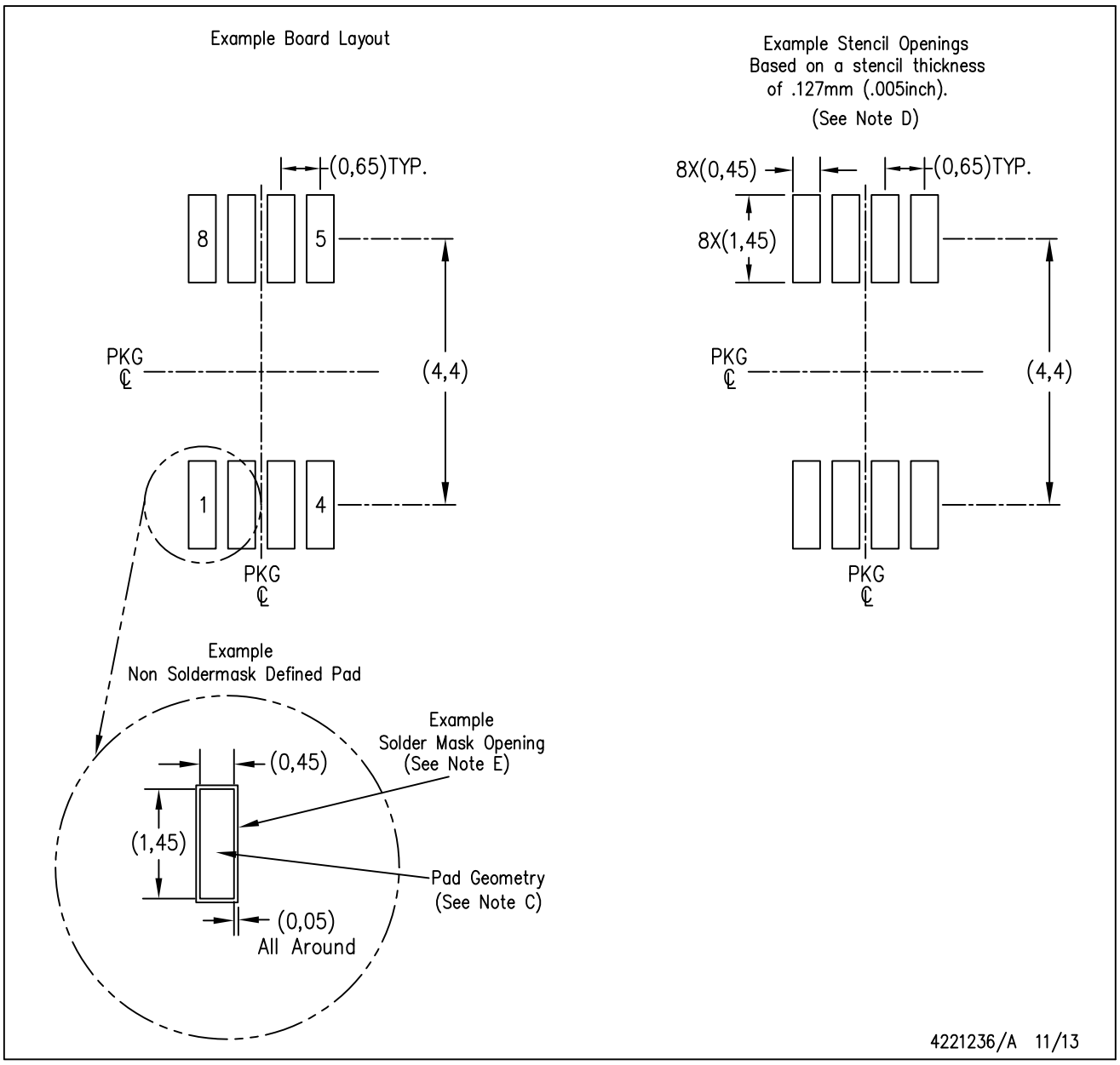
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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