INA199 26V、双向、零漂移、低侧或高侧、电压输出、电流分流监控器

1 特性

- 宽共模范围：–0.3V 至 26V
- 偏移电压：±150µV（最大值）（支持 10mV 满量程分流压降）
- 精度：
  - 增益误差（最大过热误差）：
    - ±1%（C 版本）
    - ±1.5%（A 和 B 版本）
  - 0.5µV/°C 偏移漂移（最大值）
  - 10ppm/°C 增益漂移（最大值）
- 增益选择：
  - INA199x1：50V/V
  - INA199x2：100V/V
  - INA199x3：200V/V
- 静态电流：100µA（最大值）
- 封装：6 引脚 SC70、10 引脚 UQFN

2 应用

- 笔记本电脑
- 手机
- 符合 Qi 标准的无线充电发送器
- 电信设备
- 电源管理
- 电池充电器

3 说明

INA199 系列电压输出、电流分流监控器（也称为电流传感放大器）常用于过流保护、针对系统优化的精密电流测量或闭环反馈电路。该系列器件可在独立于电源电压的 –0.3V 至 26V 共模电压下感应分流电阻器上的电压降。共有三种固定增益可供选择：50V/V、100V/V 和 200V/V。该系列器件采用零漂移架构，偏移较低，因此在进行电流感测时能够将分流电阻器两端的最大压降保持在最低 10mV 的满量程。

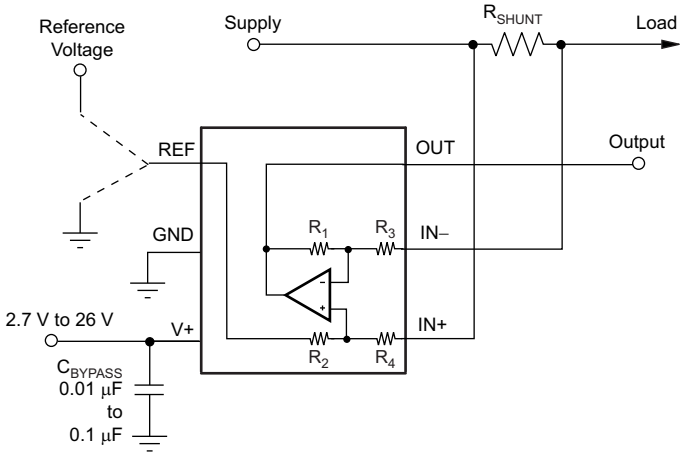
这些器件由 2.7V 至 26V 的单个电源供电，消耗的最大电源电流为 100µA。所有版本的额定温度均为 –40°C 至 125°C，并且提供了 SC70-6 和薄型 UQFN-10 两种封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA199	SC70 (6)	2.00mm × 1.25mm
	UQFN (10)	1.80mm x 1.40mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (June 2016) to Revision G — **Page**

- 已更改 *精度* 特性 项目的第一个子项目：从子项目中删除了 ±1.5% 并增加了版本差异 ... 1
- 已更改 *105°C* 至 *125°C*（在*说明*部分的最后一段） ... 1
- Added *INA199Cx* to last row of *Analog inputs* in *Absolute Maximum Ratings* table ... 5
- Changed INA199Ax HBM value from ±4000 to ±2000 and changed *INA199B1, INA199B2, and INA199B3* to *INA199Bx and INA199Cx* in second $V_{(ESD)}$ section of *ESD Ratings* table ... 5
- Changed maximum specification from *105* to *125* in T_A row of *Recommended Operating Conditions* table ... 6
- Changed all T_A = *–40°C to 105°C* to T_A = *–40°C to 125°C* in *Electrical Characteristics* table ... 7
- Added version C to last row of V_{CM} parameter in *Electrical Characteristics* table ... 7
- Added versions A and B to first *Gain error* parameter row, added second row ... 7
- Changed devices listed in test conditions of GBW parameter in *Electrical Characteristics* table to *INA199x1*, *INA199x2*, and *INA199x3*, respectively for the three rows ... 7
- Changed maximum specification from *105* to *125* in *Specified range* parameter of *Electrical Characteristics* table ... 7
- Changed *105°C* to *125°C* in last paragraph of *Overview* section ... 12
- Changed *INA199A2 and INA199B2* to *INA199x2* and changed *INA199A2 and INA199B2* to *INA199x2* in last paragraph of *Input Filtering* section ... 15
- Changed listed products in table of Figure 22 ... 15
- Changed *version B* to *version B and C* in second paragraph of *Improving Transient Robustness* section ... 18

Changes from Revision E (December 2015) to Revision F — **Page**

- 在*封装* 特性 项目中添加了两种封装的引脚数量 ... 1
- 已删除最后一项*应用*要点 ... 1
- 已更改*说明*部分中的第二句） ... 1
- Changed *Analog inputs* parameter in *Absolute Maximum Ratings* table ... 5
- Changed *ESD Ratings* table: deleted both *Machine model* rows, changed INA199B HBM specification ... 5
- Changed *Electrical Characteristics* table: recombined the two *Electrical Characteristics* tables into one ... 7

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- Added minimum specification to second row of Power Supply, V_S parameter in *Electrical Characteristics* table 7
- Added θ_{JA} parameter back to *Electrical Characteristics* table 7

Changes from Revision D (November 2012) to Revision E **Page**

- 已添加 *ESD 额定值表、热性能信息表、特性 说明* 部分、*器件功能模式、应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

Changes from Revision C (August 2012) to Revision D **Page**

- Changed Frequency Response, *Bandwidth* parameter in Electrical Characteristics table 7
- Updated Figure 21 14
- Updated Figure 22 15

Changes from Revision B (February 2010) to Revision C **Page**

- 已添加 INA199Bx 增益至第四个 特性 项目 1
- Added INA199Bx data to Product Family Table 4
- Added INA199Bx data to Package Information table 4
- Added silicon version B data to Input, *Common-Mode Input Range* parameter of Electrical Characteristics table 7
- Added QFN package information to *Temperature Range* section of *Electrical Characteristics* table 7
- Updated Figure 3 8
- Updated Figure 9 9
- Updated Figure 12 9
- Changed last paragraph of the *Selecting* R_S section to cover both INA199Ax and INA199Bx versions 13
- Changed *Input Filtering* section 14
- Added *Improving Transient Robustness* section 18

Changes from Revision A (June 2009) to Revision B **Page**

- Deleted ordering information content from Package/Ordering table 4
- Updated DCK pinout drawing 4

Changes from Original (April 2009) to Revision A **Page**

- Added *ordering number* and *transport media, quantity* columns to *Package/Ordering Information* table 4

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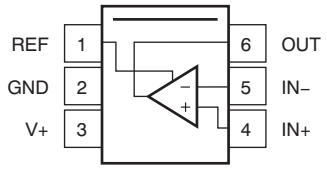
5 Device Comparison Table

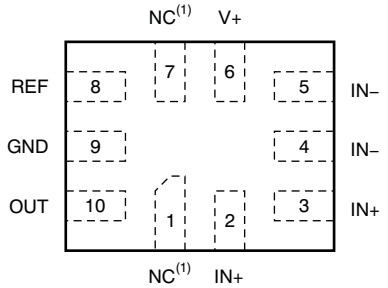
PRODUCT	GAIN	R_3 AND R_4	R_1 AND R_2
INA199x1	50	20 kΩ	1 MΩ
INA199x2	100	10 kΩ	1 MΩ
INA199x3	200	5 kΩ	1 MΩ

6 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



RSW Package
10-Pin UQFN
Top View



(1) NC denotes no internal connection. These pins can be left floating or connected to any voltage between GND and V+.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SC70	UQFN		
GND	2	9	Analog	Ground
IN–	5	4, 5	Analog input	Connect to load side of shunt resistor.
IN+	4	2, 3	Analog input	Connect to supply side of shunt resistor.
NC	—	1, 7	—	Not internally connected. Leave floating or connect to ground.
OUT	6	10	Analog output	Output voltage
REF	1	8	Analog input	Reference voltage, 0 V to V+
V+	3	6	Analog	Power supply, 2.7 V to 26 V

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage			26	V
Analog inputs, V_{IN+}, V_{IN-}[2]	Differential (V_{IN+}) – (V_{IN-})	–26	26	V
	Common-mode[3], INA199Ax	GND – 0.3	26	
	Common-mode[3], INA199Bx and INA199Cx	GND – 0.1	26	
REF input		GND – 0.3	(V+) + 0.3	V
Output[3]		GND – 0.3	(V+) + 0.3	V
Input current Into all pins[3]			5	mA
Operating temperature		–40	125	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin c an exceed the voltage shown if the current at that pin is limited to 5 mA.

7.2 ESD Ratings

			VALUE	UNIT
INA199A1, INA199A2, and INA199A3 in DCK and RSW Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
INA199Bx and INA199Cx in DCK and RSW Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage (applied to V+)		5		V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		INA199		UNIT
		DCK (SC70)	RSW (UQFN)	
		6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	107.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	18.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.4	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, V_{SENSE} = V_{IN+} – $V_{IN–}$, and V_{REF} = V_S / 2 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{CM}	Common-mode input range		Version A, T_A = –40°C to 125°C	–0.3		26	V
			Version B and C, T_A = –40°C to 125°C	–0.1		26	
CMR	Common-mode rejection		V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV, T_A = –40°C to 125°C	100	120		dB
V_{OS}	Offset voltage, RTI(1)		V_{SENSE} = 0 mV		±5	±150	µV
dV_{OS}/dT	V_{OS} vs temperature		T_A = –40°C to 125°C		0.1	0.5	µV/°C
PSR	Power supply rejection		V_S = 2.7 V to 18 V, V_{IN+} = 18 V, V_{SENSE} = 0 mV		±0.1		µV/V
I_B	Input bias current		V_{SENSE} = 0 mV		28		µA
I_{OS}	Input offset current		V_{SENSE} = 0 mV		±0.02		µA
OUTPUT							
G	Gain	INA199x1			50		V/V
		INA199x2			100		
		INA199x3			200		
	Gain error		Version A and B, V_{SENSE} = –5 mV to 5 mV, T_A = –40°C to 125°C		±0.03%	±1.5%	
			Version C, V_{SENSE} = –5 mV to 5 mV, T_A = –40°C to 125°C		±0.03%	±1%	
	Gain error vs temperature		T_A = –40°C to 125°C		3	10	ppm/°C
	Nonlinearity error		V_{SENSE} = –5 mV to 5 mV		±0.01%		
	Maximum capacitive load		No sustained oscillation		1		nF
VOLTAGE OUTPUT(2)							
	Swing to V+ power-supply rail		R_L = 10 kΩ to GND, T_A = –40°C to 125°C		(V+) – 0.05	(V+) – 0.2	V
	Swing to GND		R_L = 10 kΩ to GND, T_A = –40°C to 125°C		(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
GBW	Bandwidth		C_{LOAD} = 10 pF, INA199x1		80		kHz
			C_{LOAD} = 10 pF, INA199x2		30		
			C_{LOAD} = 10 pF, INA199x3		14		
SR	Slew rate				0.4		V/µs
NOISE, RTI(1)							
	Voltage noise density				25		nV/√Hz
POWER SUPPLY							
V_S	Operating voltage range		T_A = –40°C to 125°C	2.7		26	V
			–20°C to 85°C	2.5		26	
I_Q	Quiescent current		V_{SENSE} = 0 mV		65	100	µA
	I_Q over temperature		T_A = –40°C to 125°C			115	µA
TEMPERATURE RANGE							
	Specified range			–40		125	°C
	Operating range			–40		125	°C
θ_{JA}	Thermal resistance	SC70			250		°C/W
		UQFN			80		

(1) RTI = Referred-to-input.
(2) See Typical Characteristic curve, *Output Voltage Swing vs Output Current* (Figure 6).

7.6 Typical Characteristics

performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

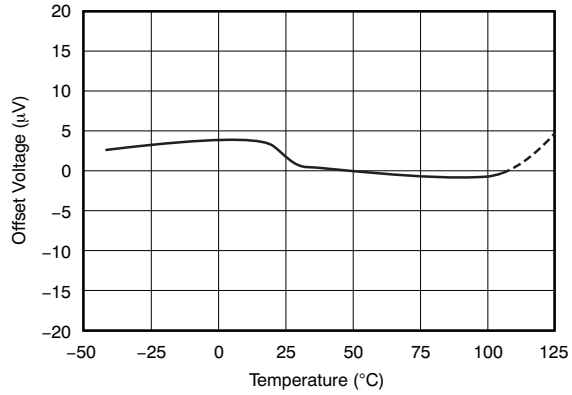

Figure 1. Offset Voltage vs Temperature

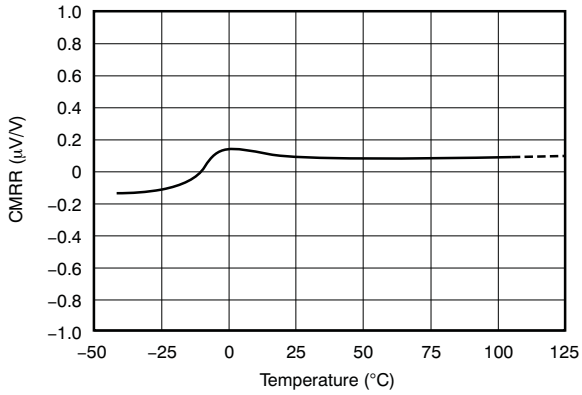

Figure 2. Common-Mode Rejection Ratio vs Temperature

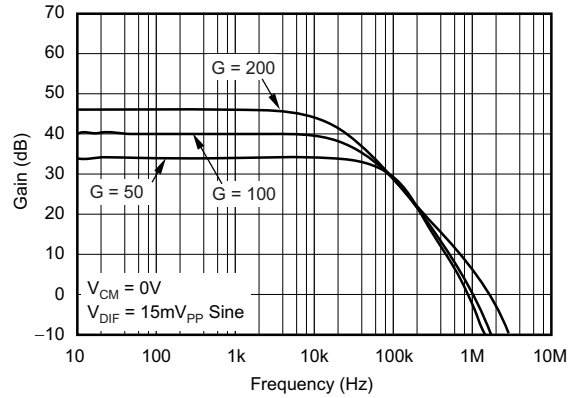

Figure 3. Gain vs Frequency

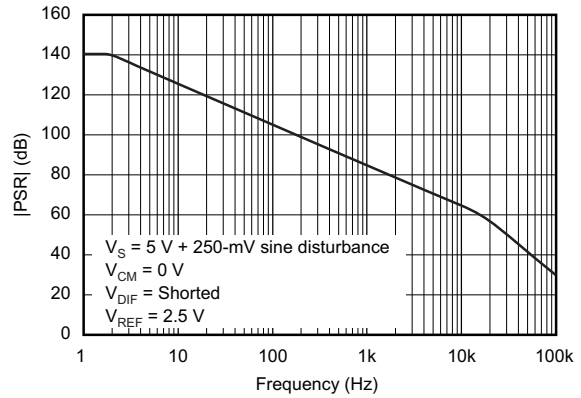

Figure 4. Power-Supply Rejection Ratio vs Frequency

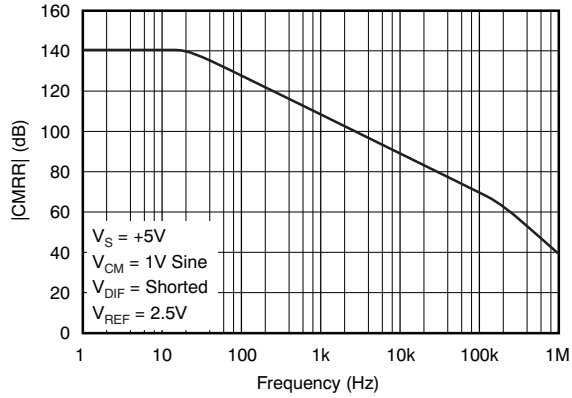

Figure 5. Common-Mode Rejection Ratio vs Frequency

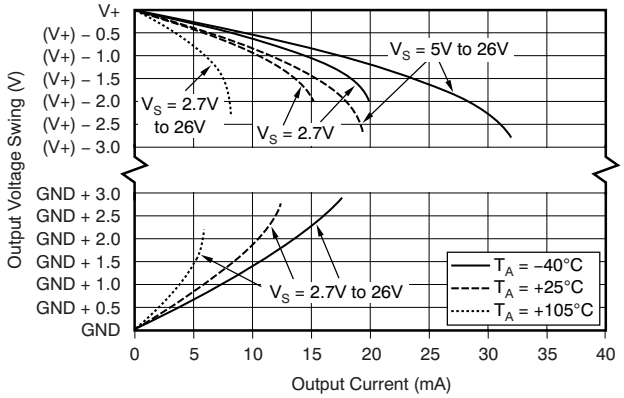

Figure 6. Output Voltage Swing vs Output Current

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Typical Characteristics (continued)

performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

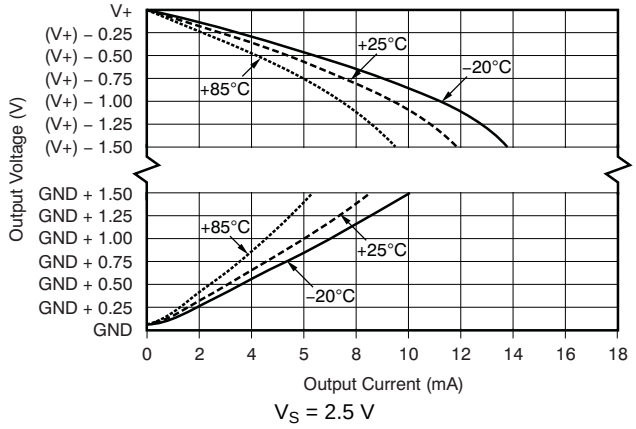

Figure 7. Output Voltage Swing vs Output Current

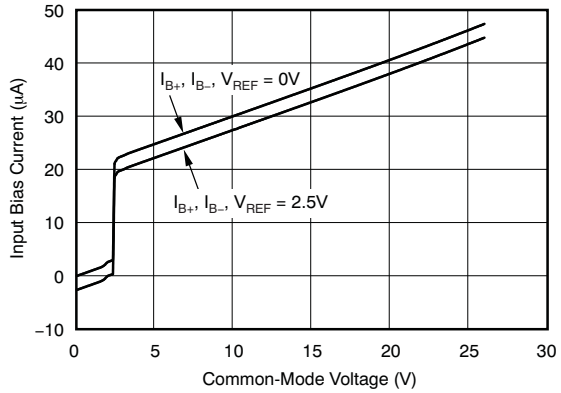

Figure 8. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 5 V

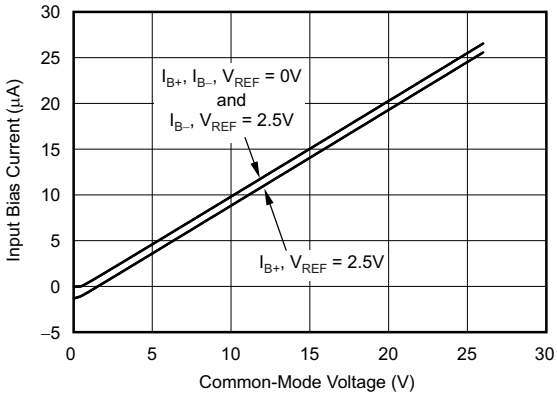

Figure 9. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 0 V (Shutdown)

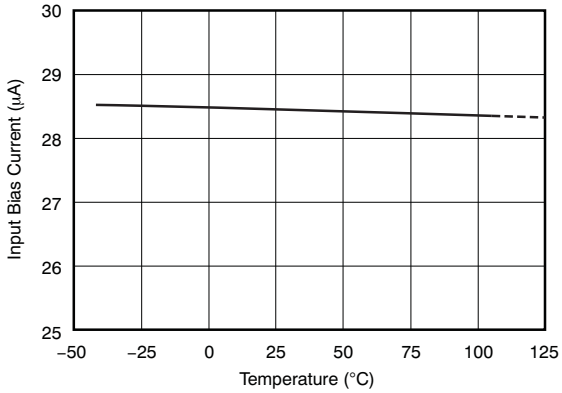

Figure 10. Input Bias Current vs Temperature

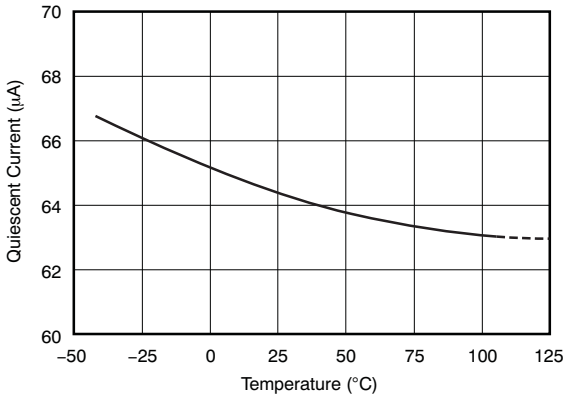

Figure 11. Quiescent Current vs Temperature

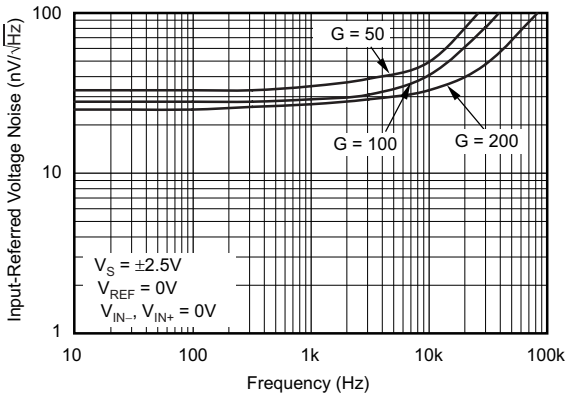

Figure 12. Input-Referred Voltage Noise vs Frequency

Typical Characteristics (continued)

performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

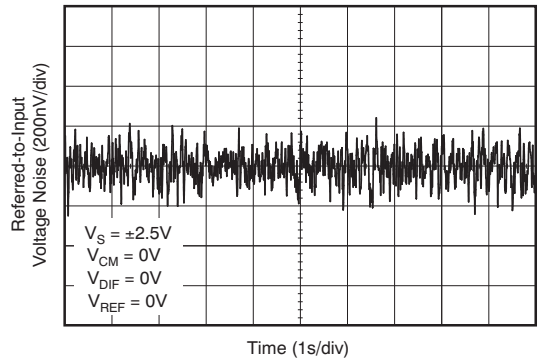

Figure 13. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

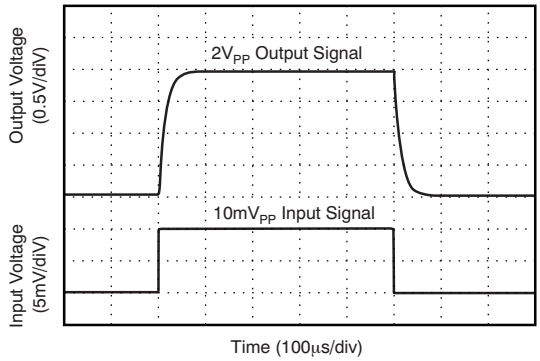

Figure 14. Step Response (10-mV$_{PP}$ Input Step)

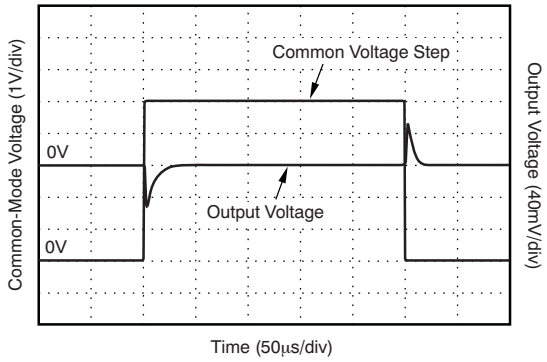

Figure 15. Common-Mode Voltage Transient Response

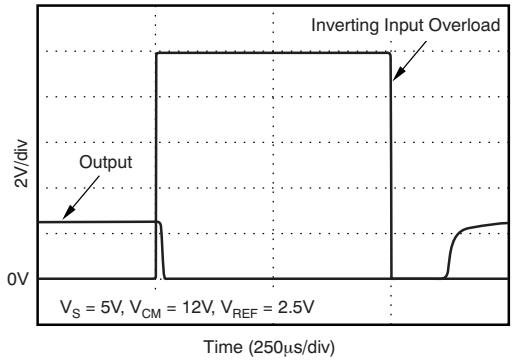

Figure 16. Inverting Differential Input Overload

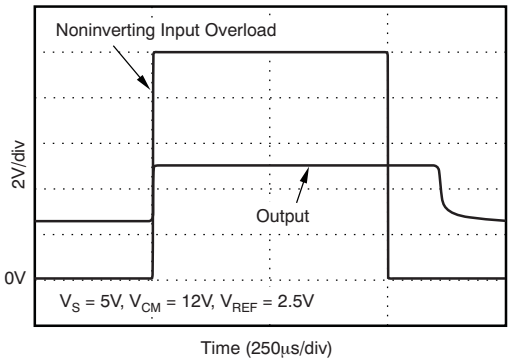

Figure 17. Noninverting Differential Input Overload

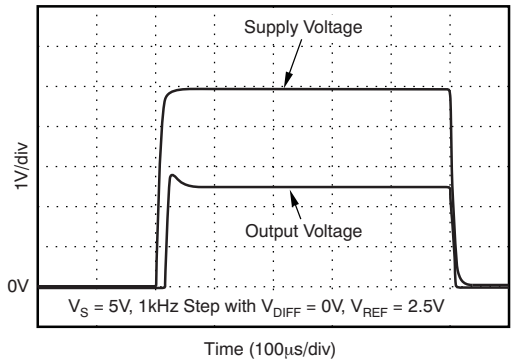

Figure 18. Start-Up Response

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Typical Characteristics (continued)

performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

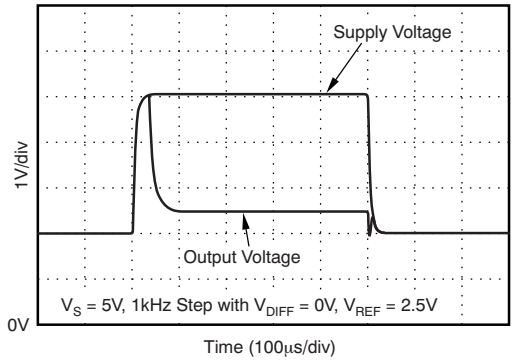


Figure 19. Brownout Recovery

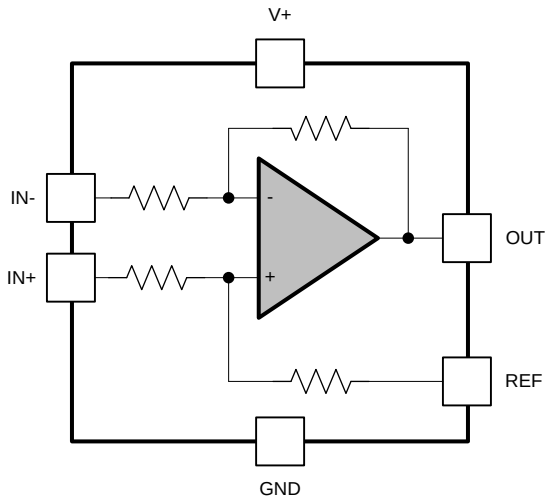
8 Detailed Description

8.1 Overview

The INA199 is a 26-V common mode, zero-drift topology, current-sensing amplifier that can be used in both low-side and high-side configurations. The device is a specially-designed, current-sensing amplifier that is able to accurately measure voltages developed across a current-sensing resistor on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V and the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 150 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40°C to +125°C.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Basic Connections

Figure 20 shows the basic connections for the INA199. The input pins, IN+ and IN–, must be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

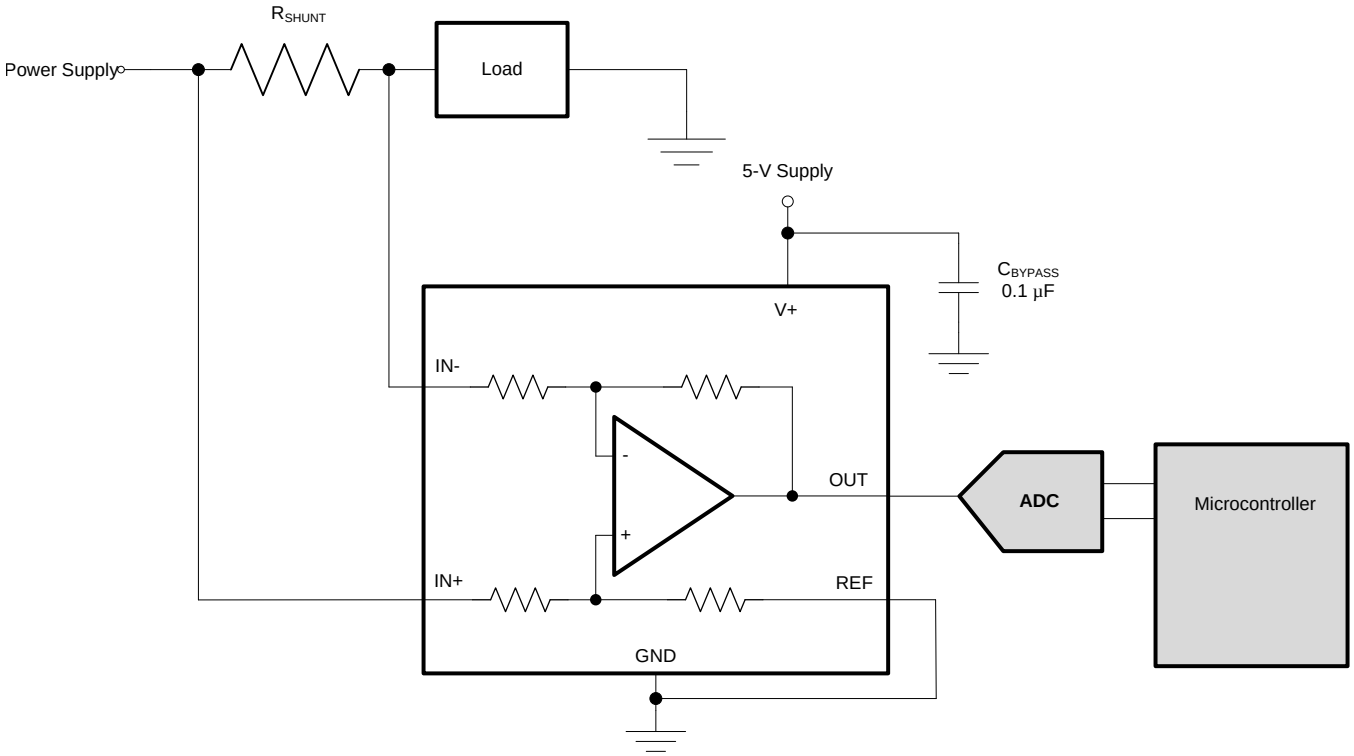

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Figure 20. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

On the RSW package, two pins are provided for each input. These pins must be tied together (that is, tie IN+ to IN+ and tie IN– to IN–).

8.3.2 Selecting R_S

The zero-drift offset performance of the INA199 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100 mV.

The INA199 series gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gain of 50 or 100 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA199A1 operating on a 3.3-V supply can easily handle a full-scale shunt drop of 60 mV, with only 150 µV of offset.

8.4 Device Functional Modes

8.4.1 Input Filtering

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. Figure 21 shows a filter placed at the inputs pins.

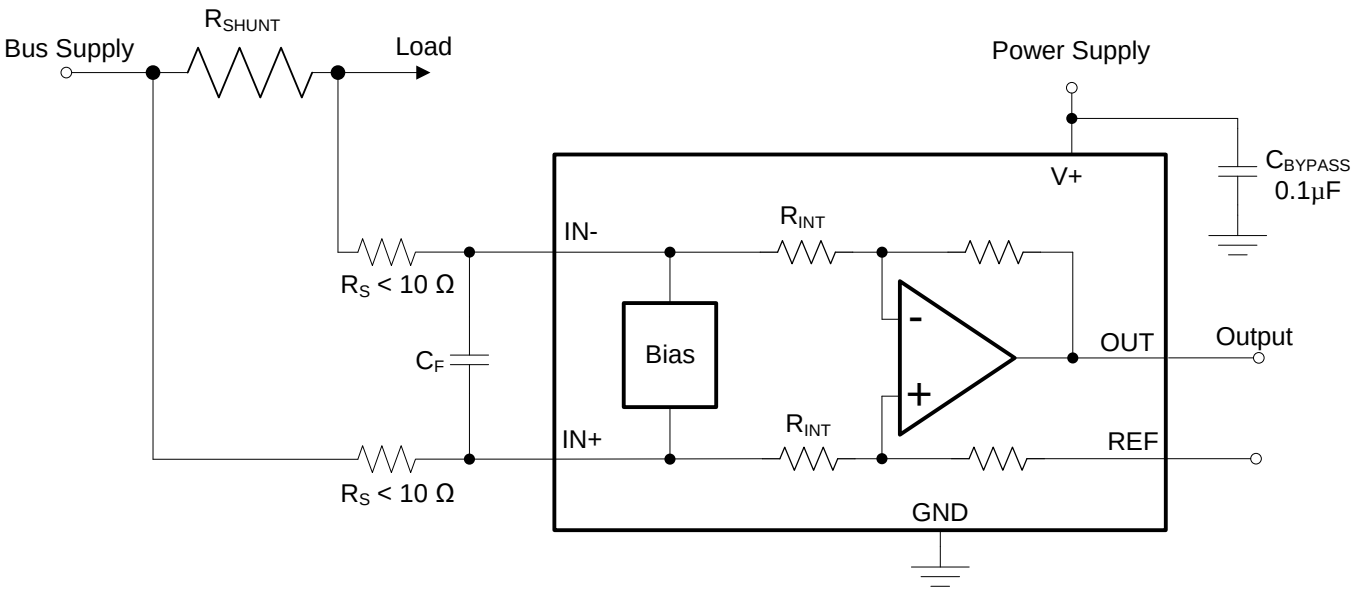

Figure 21. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors must be kept to 10 Ω (or less if possible) to reduce any affect to accuracy. The internal bias network shown in Figure 21 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as shown in Figure 21). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 1:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (1)$$

where:

- R_{INT} is the internal input resistor (R3 and R4).
- R_S is the external series resistance.

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Device Functional Modes (continued)

With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as listed in Table 1. Each individual device gain error factor is listed in Table 2.

Table 1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA199x1	50	20
INA199x2	100	10
INA199x3	200	5

Table 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA199x1	$\frac{20{,}000}{(17 \times R_S) + 20{,}000}$
INA199x2	$\frac{10{,}000}{(9 \times R_S) + 10{,}000}$
INA199x3	$\frac{1000}{R_S + 1000}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

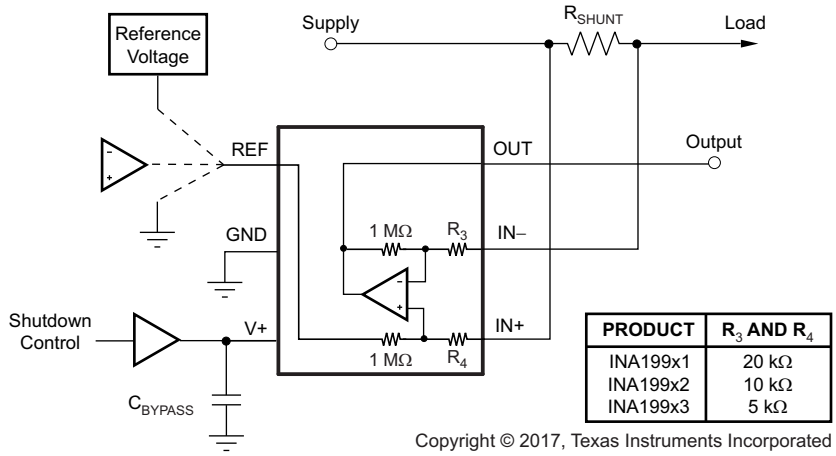
$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (2)$$

For example, using an INA199x2 and the corresponding gain error equation from Table 2, a series resistance of 10-Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 0.89% solely because of the external 10-Ω series resistors. Using an INA199x1 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

8.4.2 Shutting Down the INA199 Series

Although the INA199 series does not have a shutdown pin, the low power consumption of the device allows the output of a logic gate or transistor switch to power the INA199. This gate or switch turns on and turns off the INA199 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INA199 in shutdown mode shown in Figure 22.



NOTE: 1-MΩ paths from shunt inputs to reference and the INA199 outputs.

Figure 22. Basic Circuit for Shutting Down the INA199 With a Grounded Reference

There is typically slightly more than 1-MΩ impedance (from the combination of 1-MΩ feedback and 5-kΩ input resistors) from each input of the INA199 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or operational amplifier is powered when the INA199 is shut down, the calculation is direct; instead of assuming 1-MΩ to ground, however, assume 1-MΩ to the reference voltage. If the reference or operational amplifier is also shut down, some knowledge of the reference or operational amplifier output impedance under shutdown conditions is required. For instance, if the reference source functions as an open circuit when not powered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled INA199 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage impressed across a 1-MΩ resistor.

NOTE

When the device is powered up, there is an additional, nearly constant, and well-matched 25 μA that flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the only current effects are the result of the 1-MΩ resistors.

8.4.3 REF Input Impedance Effects

As with any difference amplifier, the INA199 series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin must be buffered by an operational amplifier.

In systems where the INA199 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 23 depicts a method of taking the output from the INA199 by using the REF pin as a reference.

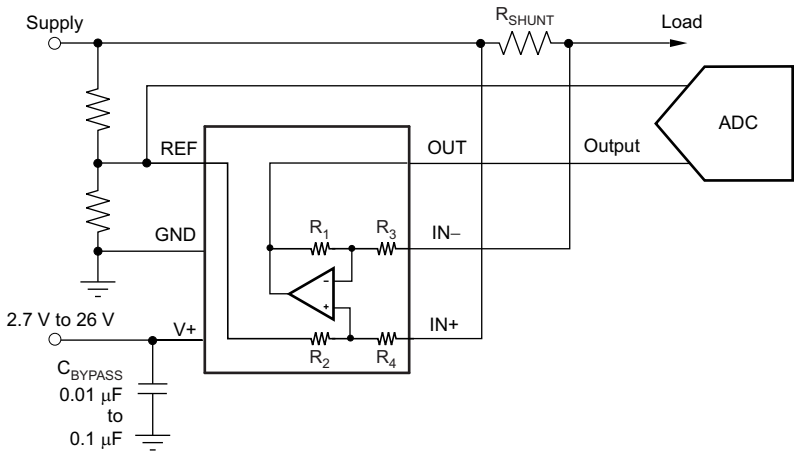


Figure 23. Sensing the INA199 to Cancel Effects of Impedance on the REF Input

8.4.4 Using the INA199 With Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA199 series can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diode or Zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors (see Figure 24) as a working impedance for the Zener. Keeping these resistors as small as possible is preferable, most often approximately 10 Ω. Larger values can be used with an effect on gain as

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discussed in the *Input Filtering* section. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523. See *TIDA-00302 Transient Robustness for Current Shunt Monitor Design Guide*, TIDU473 for more information on transient robustness and current-shunt monitor input protection.

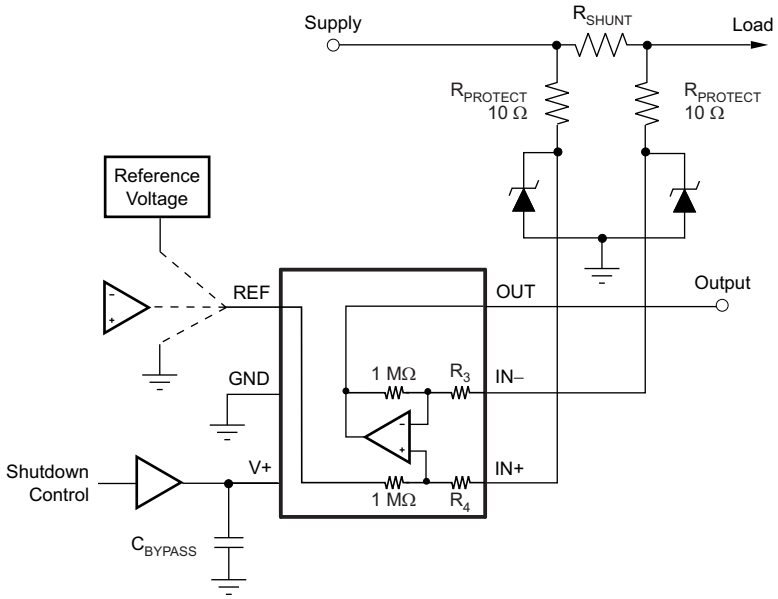

Figure 24. INA199 Transient Protection Using Dual Zener Diodes

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. This method is shown in Figure 25. In either of these examples, the total board area required by the INA199 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

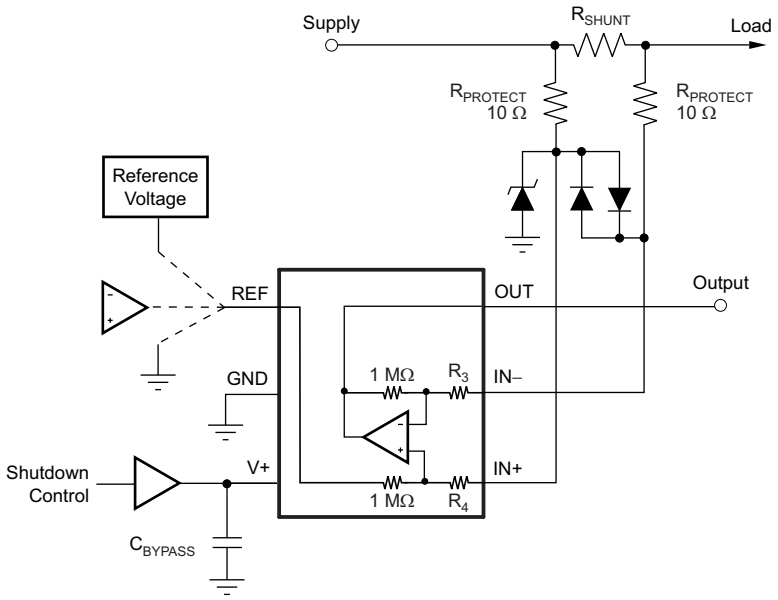

Figure 25. INA199 Transient Protection Using a Single Transzorb and Input Clamps

8.4.5 Improving Transient Robustness

Applications involving large input transients with excessive dV/dt above 2 kV per microsecond present at the device input pins can cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Take care to ensure that external series input resistance does not significantly affect gain error accuracy. For accuracy purposes, keep the resistance under 10 Ω if possible. Ferrite beads are recommended for this filter because of their inherently low dc ohmic value. Ferrite beads with less than 10 Ω of resistance at dc and over 600 Ω of resistance at 100 MHz to 200 MHz are recommended. The recommended capacitor values for this filter are between 0.01 µF and 0.1 µF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 26. Again, see *TIDA-00302 Transient Robustness for Current Shunt Monitor Design Guide*, TIDU473 for more information on transient robustness and current-shunt monitor input protection.

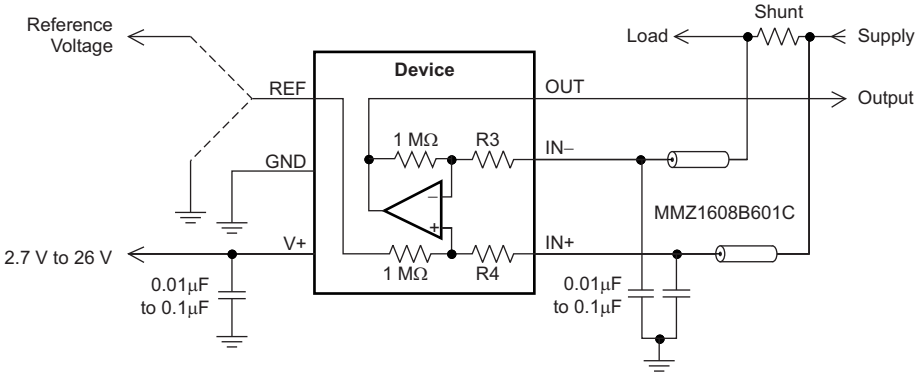

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Figure 26. Transient Protection

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B and C devices are now available with new ESD structures that are not susceptible to this latching condition. Version B and C devices are incapable of sustaining these damage-causing latched conditions so these devices do not have the same sensitivity to the transients that the version A devices have, thus making the version B and C devices a better fit for these applications.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA199 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

9.2 Typical Applications

9.2.1 Unidirectional Operation

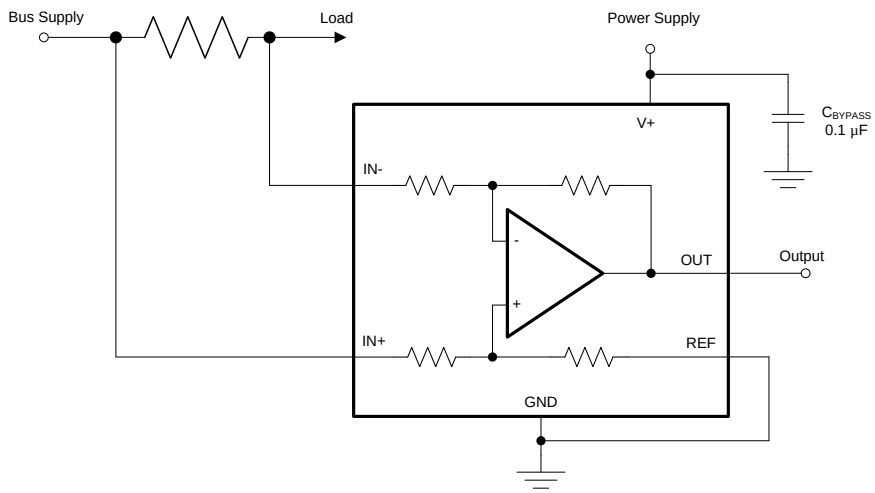

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Figure 27. Unidirectional Application Schematic

9.2.1.1 Design Requirements

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 27. When the input signal increases, the output voltage at the OUT pin increases.

9.2.1.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, TI recommends buffering the reference voltage connected to the REF pin.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

Typical Applications (continued)

9.2.1.3 Application Curve

An example output response of a unidirectional configuration is shown in Figure 28. With the REF pin connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

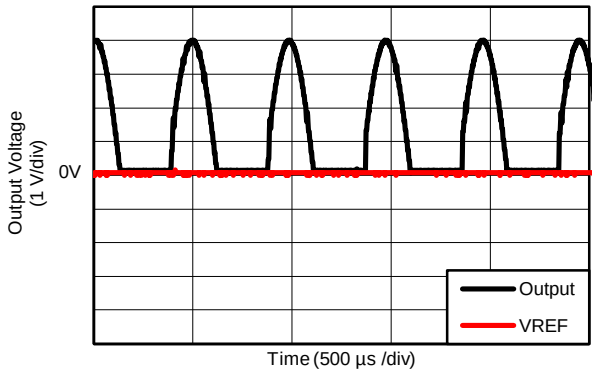

Figure 28. Unidirectional Application Output Response

9.2.2 Bidirectional Operation

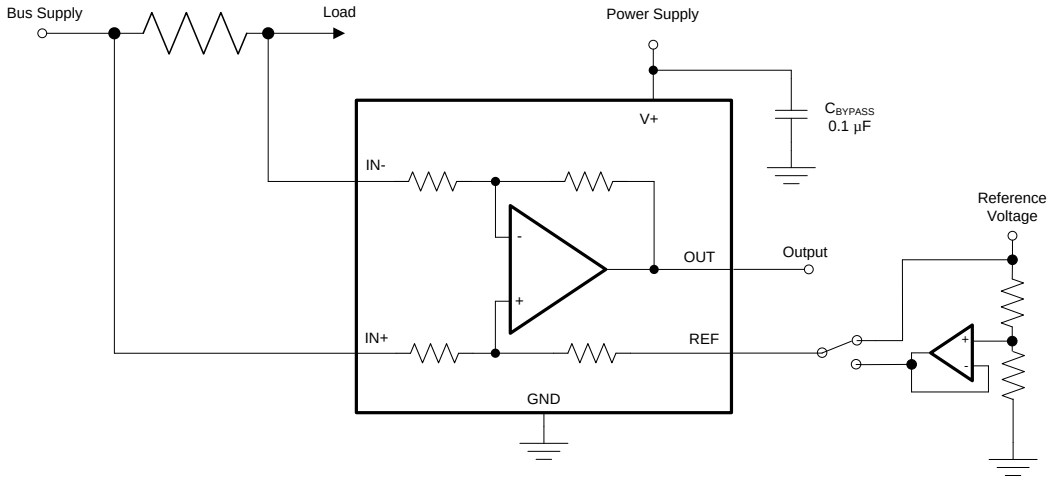

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Figure 29. Bidirectional Application Schematic

9.2.2.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

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Typical Applications (continued)

9.2.2.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin; see Figure 29. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, V_{REF} is typically set at mid-scale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

9.2.2.3 Application Curve

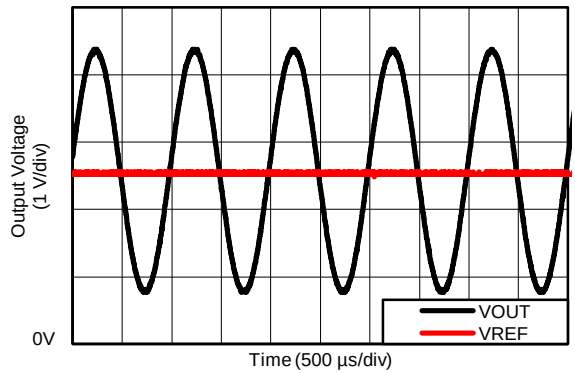

Figure 30. Bidirectional Application Output Response

10 Power Supply Recommendations

The input circuitry of the INA199 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Also, the INA199 can withstand the full input signal range up to 26-V range in the input pins, regardless of whether the device has power applied or not.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends using a bypass capacitor with a value of 0.1 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

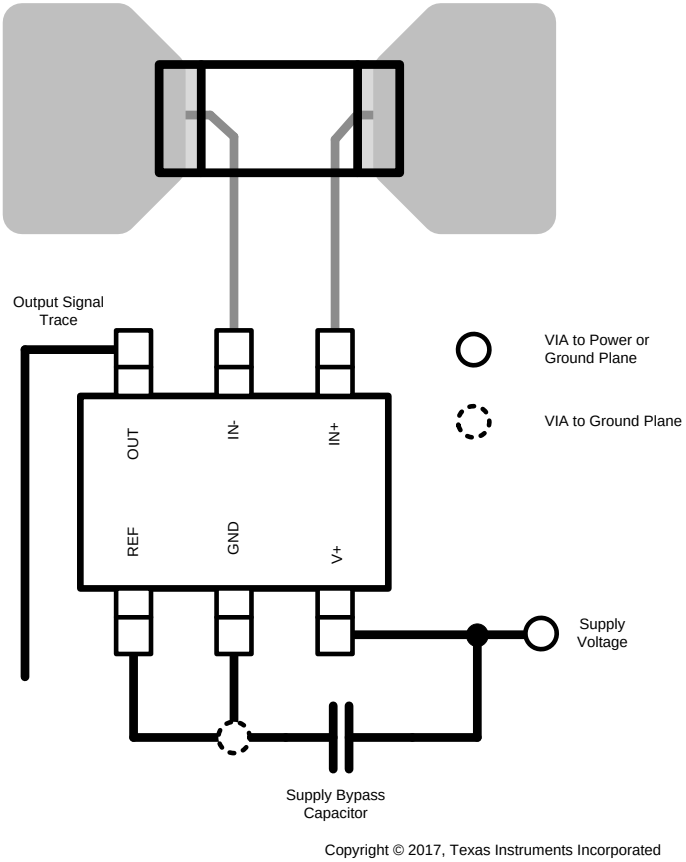

Figure 31. Recommended Layout

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档请参阅以下部分：

- *《INA199A1-A3EVM 用户指南》*
- *《TIDA-00302 电流分流监控器的瞬态稳定性》*

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA199A1DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBG	Samples
INA199A1DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBG	Samples
INA199A1RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NSJ	Samples
INA199A1RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NSJ	Samples
INA199A2DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBH	Samples
INA199A2DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBH	Samples
INA199A2RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NTJ	Samples
INA199A2RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NTJ	Samples
INA199A3DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBI	Samples
INA199A3DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBI	Samples
INA199A3RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NUJ	Samples
INA199A3RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NUJ	Samples
INA199B1DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEB	Samples
INA199B1DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEB	Samples
INA199B1RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHV	Samples
INA199B1RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHV	Samples
INA199B2DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEG	Samples
INA199B2DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEG	Samples
INA199B2RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHW	Samples
INA199B2RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHW	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA199B3DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHE	Samples
INA199B3DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHE	Samples
INA199B3RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHX	Samples
INA199B3RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHX	Samples
INA199C1DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16L	Samples
INA199C1DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16L	Samples
INA199C1RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16O	Samples
INA199C1RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16O	Samples
INA199C2DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16M	Samples
INA199C2DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16M	Samples
INA199C2RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16P	Samples
INA199C2RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16P	Samples
INA199C3DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16N	Samples
INA199C3DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16N	Samples
INA199C3RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16Q	Samples
INA199C3RSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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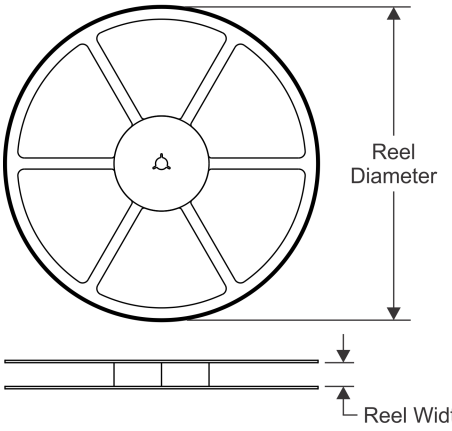
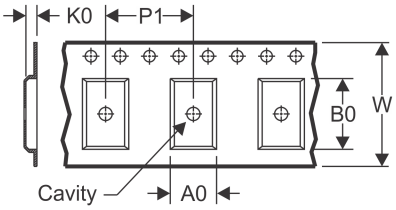
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

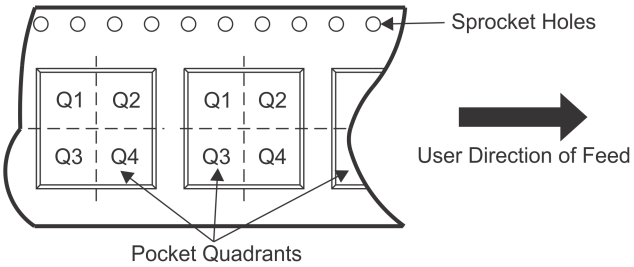


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

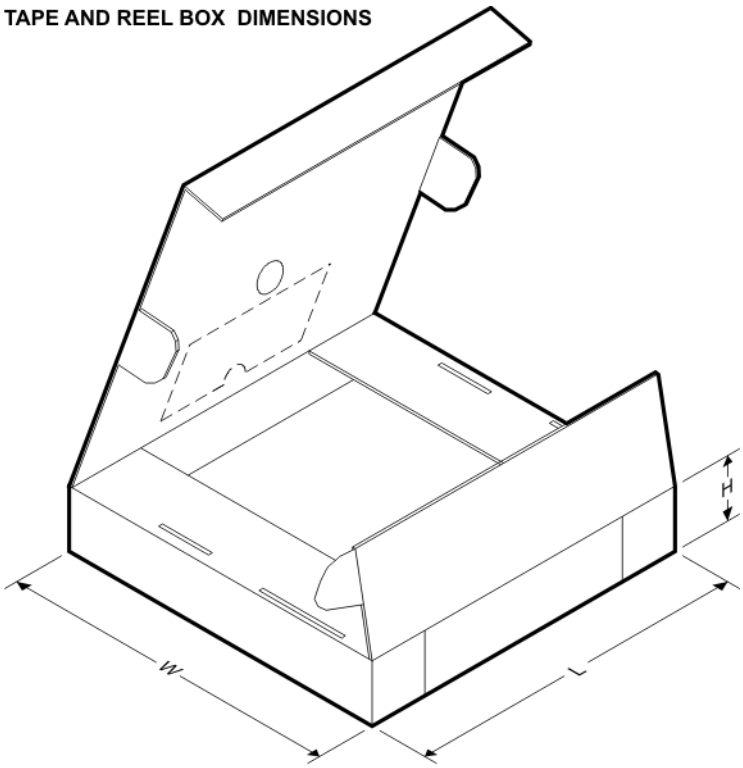


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA199A1DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A1DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A1DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A1DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A1RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A1RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A2DCKR	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA199A2DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A2DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A2DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A2DCKT	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA199A2DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A2RSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA199A2RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A2RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A2RSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA199A3DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A3DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA199A3DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A3DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A3RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A3RSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA199A3RSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA199B1DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B1DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B1RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B1RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B2DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B2DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B2RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B2RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B3DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B3RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B3RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199C1DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199C1DCKT	SC70	DCK	6	250	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA199C1RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199C1RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199C2DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199C2DCKT	SC70	DCK	6	250	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA199C2RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199C2RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199C3DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199C3DCKT	SC70	DCK	6	250	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA199C3RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199C3RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1

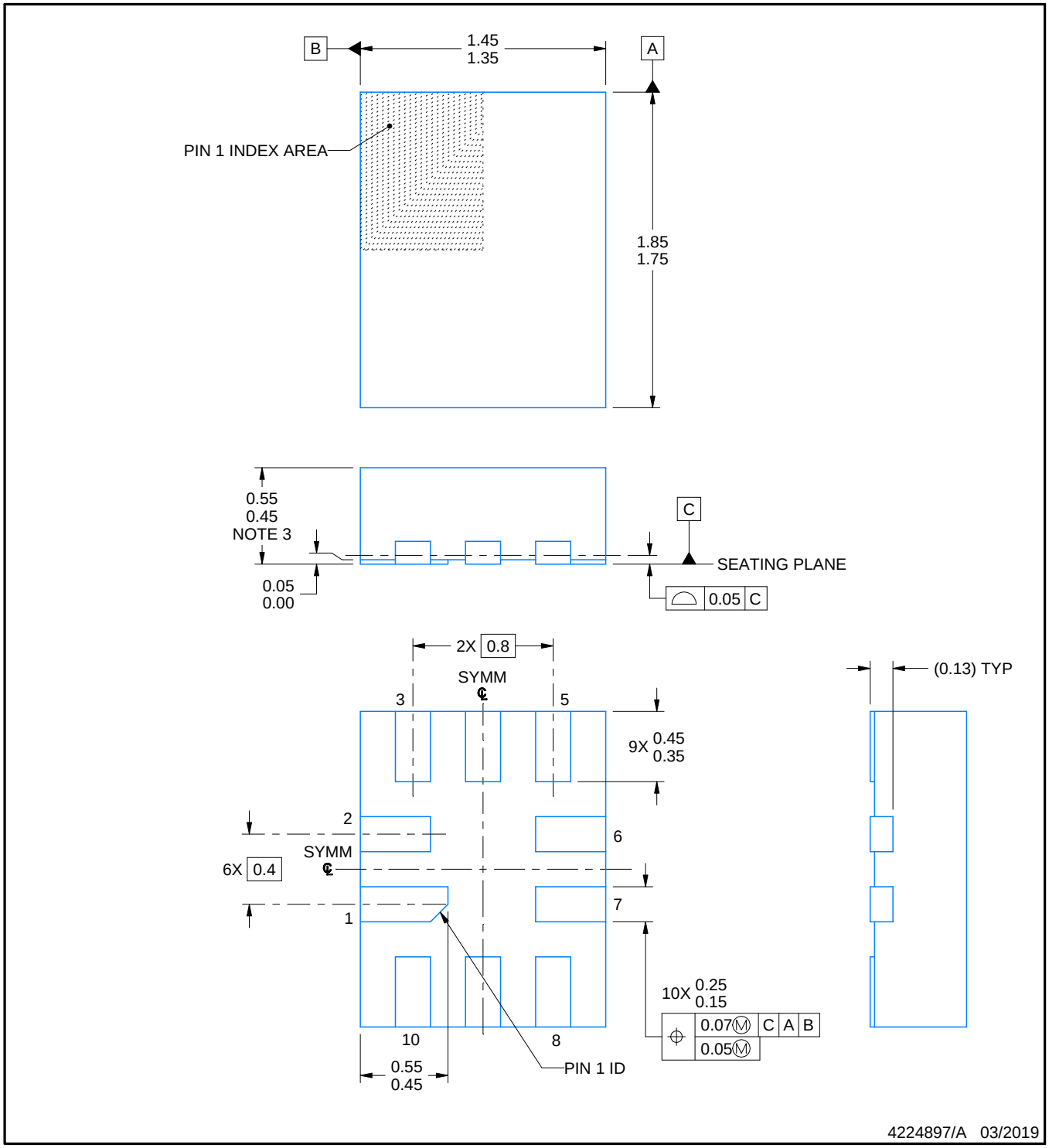
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

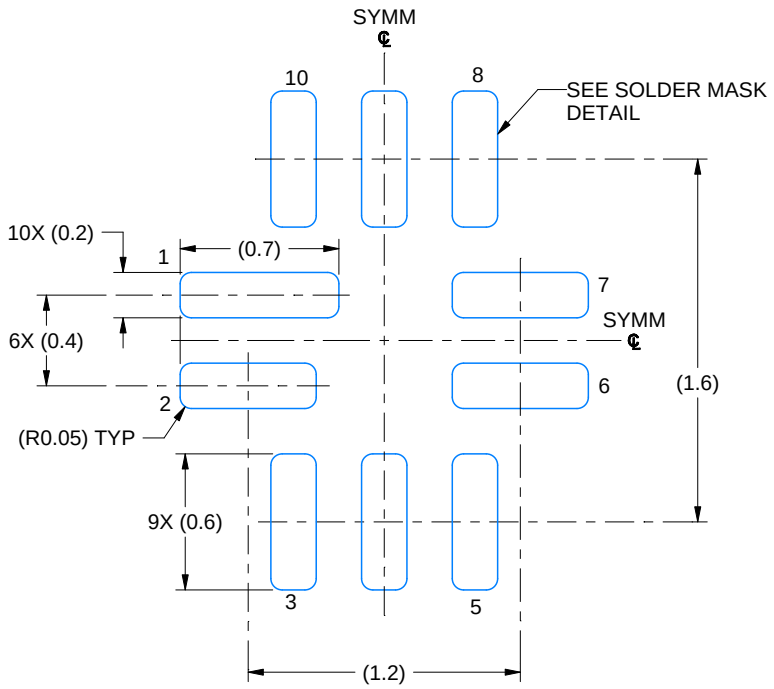
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA199A1DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199A1DCKR	SC70	DCK	6	3000	213.0	191.0	35.0
INA199A1DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199A1DCKT	SC70	DCK	6	250	213.0	191.0	35.0
INA199A1RSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA199A1RSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA199A2DCKR	SC70	DCK	6	3000	223.0	270.0	35.0
INA199A2DCKR	SC70	DCK	6	3000	213.0	191.0	35.0
INA199A2DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199A2DCKT	SC70	DCK	6	250	213.0	191.0	35.0
INA199A2DCKT	SC70	DCK	6	250	223.0	270.0	35.0
INA199A2DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199A2RSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA199A2RSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA199A2RSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA199A2RSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA199A3DCKR	SC70	DCK	6	3000	213.0	191.0	35.0
INA199A3DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199A3DCKT	SC70	DCK	6	250	213.0	191.0	35.0
INA199A3DCKT	SC70	DCK	6	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA199A3RSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA199A3RSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA199A3RSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA199B1DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199B1DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199B1RSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA199B1RSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA199B2DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199B2DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199B2RSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA199B2RSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA199B3DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199B3RSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA199B3RSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA199C1DCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA199C1DCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA199C1RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199C1RSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA199C2DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199C2DCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA199C2RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199C2RSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA199C3DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199C3DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199C3RSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA199C3RSWT	UQFN	RSW	10	250	203.0	203.0	35.0

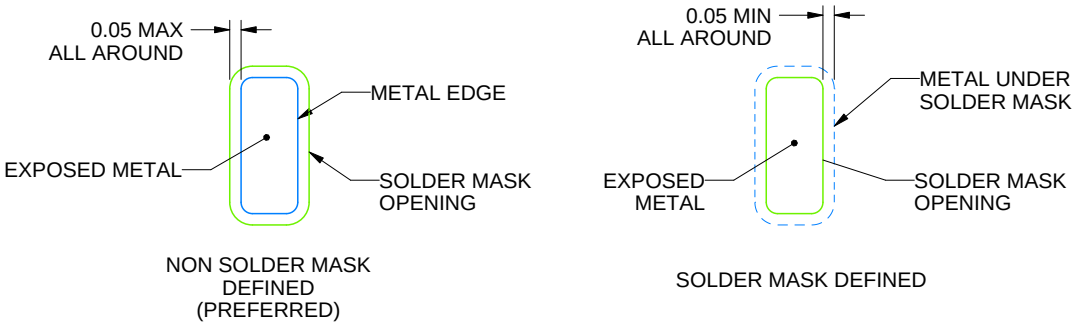


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

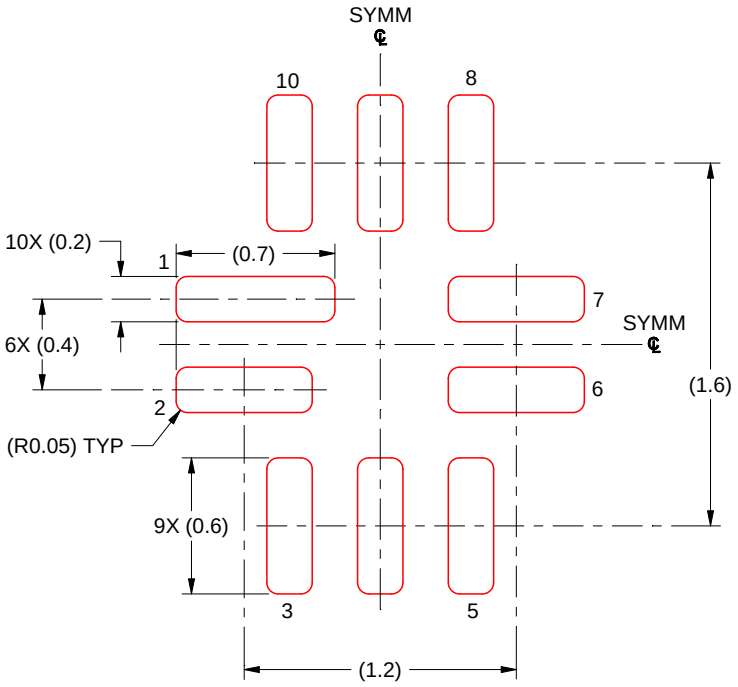


SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



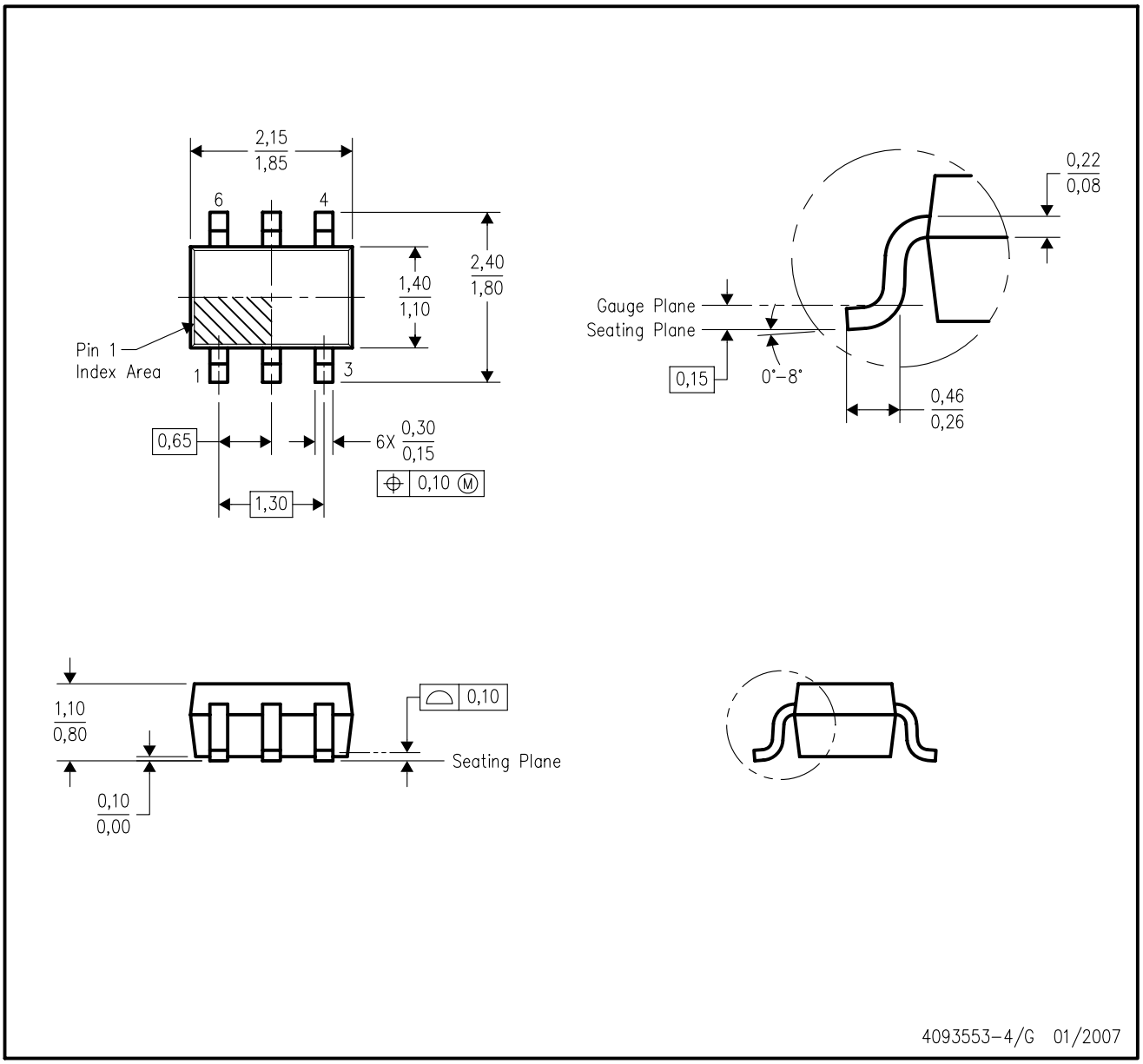
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

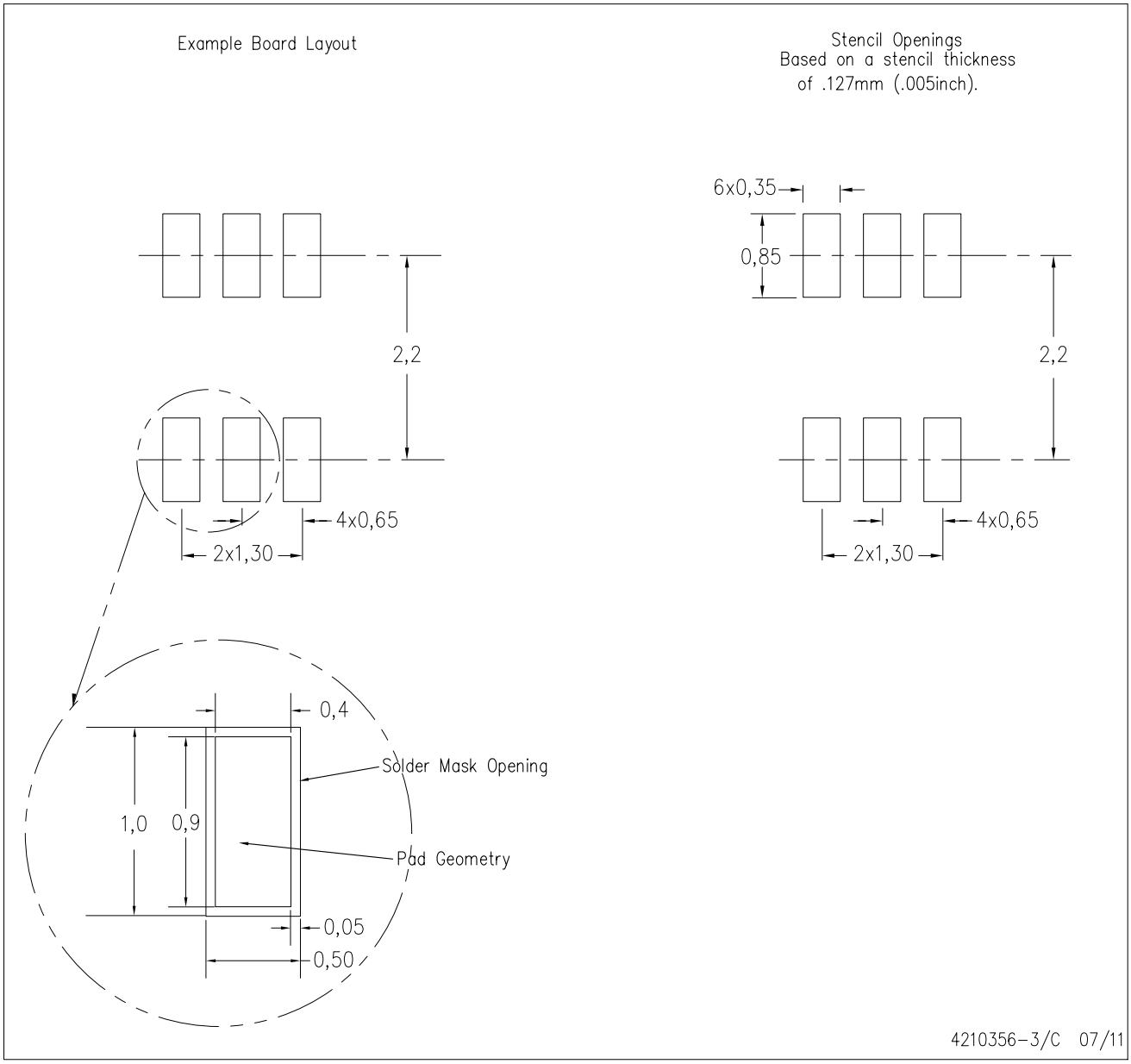
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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