DRV5013 数字锁存霍尔效应传感器

1 特性

- 数字双极锁存霍尔传感器
- 出色的温度稳定性
  - 工作温度范围内 B_{OP} 为 ±10%
- 多个灵敏度选项 (B_{OP}/B_{RP})
  - ±1.3mT（FA，请参阅*器件命名规则*）
  - ±2.7mT（AD，请参阅*器件命名规则*）
  - ±6mT（AG，请参阅*器件命名规则*）
  - ±12mT（BC，请参阅*器件命名规则*）
- 支持宽电压范围
  - 2.5V 至 38V
  - 无需外部稳压器
- 宽工作温度范围
  - T_A = –40 至 +125°C（Q，请参阅*器件命名规则*）
  - T_A = –40 至 +150°C（E，请参阅*器件命名规则*）
- 开漏输出（30mA 灌电流）
- 快速开通时间 35µs
- 小型封装和外形尺寸
  - 表面贴装 3 引脚 SOT-23 (DBZ)
    - 2.92mm × 2.37mm
  - 穿孔式 3 引脚 TO-92（LPG、LPE）
    - 4.00mm × 3.15mm
- 保护 功能
  - 反向电源保护（高达 -22V）
  - 支持高达 40V 的负载突降
  - 输出短路保护
  - 输出电流限制

2 应用

- 电动工具
- 流量计
- 阀和电磁阀状态
- 无刷直流电机
- 接近传感
- 转速计

3 说明

DRV5013 器件是一款斩波稳定霍尔效应传感器，可提供磁检测解决方案（在工作温度范围内具有出色的灵敏度稳定性和集成保护 特性）。

磁场由数字双极锁存输出表示。该集成电路 (IC) 配有一个灌电流能力达 30mA 的漏极开路输出级。该器件具有 2.5V 至 38V 的宽工作电压范围，反极性保护高达 –22V，因此适用于各种工业 应用。

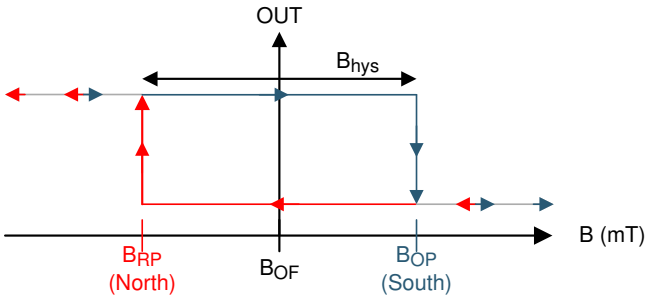
针对反向电源条件、负载突降和输出短路或过流，提供了内部保护功能。

器件信息(1)

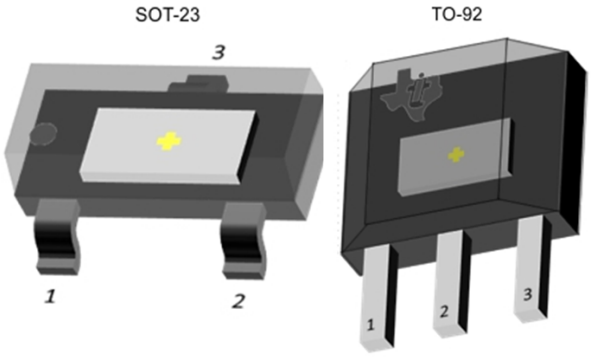
器件型号	封装	封装尺寸（标称值）
DRV5013	SOT-23 (3)	2.92mm × 1.30mm
	TO-92 (3)	4.00mm × 3.15mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

输出状态



器件封装



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 Pin Configuration and Functions ... 4
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 6
6.7 Magnetic Characteristics ... 7
6.8 Typical Characteristics ... 8
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 15
8 Application and Implementation ... 16
8.1 Application Information ... 16
8.2 Typical Applications ... 16
9 Power Supply Recommendations ... 19
10 Layout ... 19
10.1 Layout Guidelines ... 19
10.2 Layout Example ... 19
11 器件和文档支持 ... 20
11.1 器件支持 ... 20
11.2 接收文档更新通知 ... 21
11.3 社区资源 ... 21
11.4 商标 ... 21
11.5 静电放电警告 ... 21
11.6 Glossary ... 21
12 机械、封装和可订购信息 ... 21

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision J (June 2019) to Revision K — **Page**

- Changed T_J to show existing range is for Q version device in the *Absolute Maximum Ratings* table ... 5
- Added E version for T_J to the *Absolute Maximum Ratings* table ... 5
- Changed T_A to show existing range is for Q version device in the *Recommended Operating Conditions* table ... 5
- Added E version for T_A to the *Recommended Operating Conditions* table ... 5
- Changed I_{CC} test condition for T_A from 125 to $T_{A,MAX}$ to highlight the differences between the E and Q version devices ... 6
- Changed $r_{DS(on)}$ test condition for T_A from 125 to $T_{A,MAX}$ to highlight the difference between the E and Q version devices ... 6
- Changed all test conditions for T_A max from 125 to $T_{A,MAX}$ to highlight difference between the E and Q devices ... 7
- Added new condition statement to *Typical Characteristics* section ... 8
- Added data up to 150°C to Figure 1, Figure 2, Figure 4, Figure 6, Figure 8, and Figure 10 ... 8

Changes from Revision I (August 2018) to Revision J — **Page**

- 已添加 向数据表中添加了 TO-92 (LPE) 封装 ... 1

Changes from Revision H (September 2016) to Revision I — **Page**

- Changed *Power Supply Recommendations* section ... 19

Changes from Revision G (August 2016) to Revision H — **Page**

- Changed the power-on time for the FA version in the *Electrical Characteristics* table ... 6

Changes from Revision F (May 2016) to Revision G — **Page**

- Changed the maximum B_{OP} and the minimum B_{RP} for the FA version in the *Magnetic Characteristics* table ... 7
- Added the *Layout* section ... 19

Changes from Revision E (February 2016) to Revision F **Page**

- Revised preliminary limits for the FA version 7

Changes from Revision D (December 2015) to Revision E **Page**

- 已添加 添加了 FA 器件选项 1
- Added the typical bandwidth value to *Magnetic Characteristics* table 7

Changes from Revision C (September 2014) to Revision D **Page**

- 已更正 SOT-23 封装体尺寸并将 SIP 封装名称更正为 TO-92 1
- Added B_{MAX} to *Absolute Maximum Ratings* 5
- Removed table note from junction temperature 5
- 已更新封装卷带选项 M 和空白 20
- 已添加 *社区资源* 21

Changes from Revision B (July 2014) to Revision C **Page**

- 更新了高灵敏度选项 1
- Changed the max operating junction temperature to 150°C 5
- Updated the output rise and fall time typical values and removed max values in *Switching Characteristics* 6
- Updated the values in *Magnetic Characteristics* 7
- Updated all *Typical Characteristics* graphs 8
- Updated Equation 4 17
- 已更新 图 24 20

Changes from Revision A (March 2014) to Revision B **Page**

- Changed I_{OCP} MIN and MAX values from 20 and 40 to 15 and 45, respectively, in the *Electrical Characteristics* 6
- Updated the hysteresis values for each device option in the *Magnetic Characteristics* table 7
- Changed the MIN value for the ±2.3 mt B_{RP} parameter from –4 to –5 in the *Magnetic Characteristics* table 7

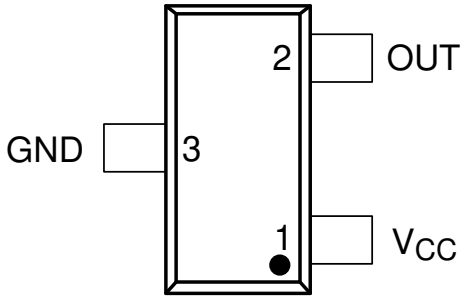
Changes from Original (March 2014) to Revision A **Page**

- 已更改 将所有霍尔 IC 参考更改为“霍尔效应传感器” 1
- 已更改 将 *RPM 表* 更改为*转速计*（在*应用* 列表中） 1
- 已更改 将加电值从 50µs 更改为 35µs（在*特性* 列表中） 1
- Changed the type of the OUT terminal from OD to Output in the *Pin Functions* table 4
- Deleted Output pin current and changed V_{CC}max to V_{CC} after the voltage ramp rate for the supply voltage 5
- Changed R_O to R1 in the test conditions for t_r and t_f in the *Switching Characteristics* table 6
- Added the bandwidth parameter to *Magnetic Characteristics* table 7
- Changed the MIN value for the ±2.3 mt B_{RP} parameter from +2.3 to –2.3 in the *Magnetic Characteristics* table 7
- Deleted condition statement from the *Typical Characteristics* and changed all T_J to T_A in the graph conditions 8
- Deleted *Number* from the Power-On Time case names; added conditions to captions of case timing diagrams 12
- Added the R1 tradeoff and lower current text after the equation in the *Output Stage* section 14
- Added the C2 not required for most applications text after the second equation in the *Output Stage* section 14
- Changed I_O to I_{SINK} in condition statement of FET overload fault condition in *Reverse Supply Protection* section 15

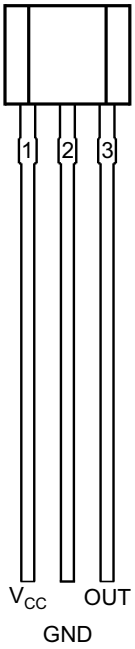
5 Pin Configuration and Functions

For additional configuration information, see *器件标记* and *机械、封装和可订购信息*.

DBZ Package
3-Pin SOT-23
Top View



LPG and LPE Packages
3-Pin TO-92
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG, LPE		
GND	3	2	Ground	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V_{CC}	1	1	Power	2.5 V to 38 V power supply. Bypass this pin to the GND pin with a 0.01-µF (minimum) ceramic capacitor rated for V_{CC}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–22 (2)	40	V
	Voltage ramp rate (V_{CC}), V_{CC} < 5 V	Unlimited		V/µs
	Voltage ramp rate (V_{CC}), V_{CC} > 5 V	0	2	
Output pin voltage		–0.5	40	V
Output pin reverse current during reverse supply condition		0	100	mA
Magnetic flux density, B_{MAX}		Unlimited		
Operating junction temperature, T_J	Q, see 图 24	–40	150	°C
	E, see 图 24	–40	175	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Specified by design. Only tested to –20 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Power supply voltage		2.5	38	V
V_O	Output pin voltage (OUT)		0	38	V
I_{SINK}	Output pin current sink (OUT) (1)		0	30	mA
T_A	Operating ambient temperature	Q, see 图 24	–40	125	°C
		E, see 图 24	–40	150	

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC (1)		DRV5013		UNIT
		DBZ (SOT-23)	LPG, LPE (TO-92)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V_{CC}	V_{CC} operating voltage		2.5		38	V
I_{CC}	Operating supply current	V_{CC} = 2.5 V to 38 V, T_A = 25°C		2.7		mA
		V_{CC} = 2.5 V to 38 V, T_A = $T_{A, MAX}$ (1)		3	3.5	
t_{on}	Power-on time	AD, AG, BC versions		35	50	µs
		FA version		35	70	
OPEN DRAIN OUTPUT (OUT)						
$r_{DS(on)}$	FET on-resistance	V_{CC} = 3.3 V, I_O = 10 mA, T_A = 25°C		22		Ω
		V_{CC} = 3.3 V, I_O = 10 mA, T_A = $T_{A, MAX}$ (1)		36	50	
$I_{lkg(off)}$	Off-state leakage current	Output Hi-Z			1	µA
PROTECTION CIRCUITS						
V_{CCR}	Reverse supply voltage		–22			V
I_{OCP}	Overcurrent protection level	OUT shorted V_{CC}	15	30	45	mA

(1) $T_{A, MAX}$ is 125°C for Q devices and 150°C for E devices (see 图 24).

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t_d	Output delay time	B = B_{RP} – 10 mT to B_{OP} + 10 mT in 1 µs		13	25	µs
t_r	Output rise time (10% to 90%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		200		ns
t_f	Output fall time (90% to 10%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		31		ns

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
f_{BW}	Bandwidth(2)		20	30		kHz
DRV5013FA: ±1.3 mT						
B_{OP}	Operate point; see Figure 12	T_A = –40°C to $T_{A,MAX}$(3)	–0.6	1.3	3.4	mT
B_{RP}	Release point; see Figure 12		–3.4	–1.3	0.6	mT
B_{hys}	Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$		1.2	2.6		mT
B_O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		–1.5	0	1.5	mT
DRV5013AD: ±2.7 mT						
B_{OP}	Operate point; see Figure 12	T_A = –40°C to $T_{A,MAX}$(3)	1	2.7	5	mT
B_{RP}	Release point; see Figure 12		–5	–2.7	–1	mT
B_{hys}	Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$			5.4		mT
B_O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		–1.5	0	1.5	mT
DRV5013AG: ±6 mT						
B_{OP}	Operate point; see Figure 12	T_A = –40°C to $T_{A,MAX}$(3)	3	6	9	mT
B_{RP}	Release point; see Figure 12		–9	–6	–3	mT
B_{hys}	Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$			12		mT
B_O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		–1.5	0	1.5	mT
DRV5013BC: ±12 mT						
B_{OP}	Operate point; see Figure 12	T_A = –40°C to $T_{A,MAX}$(3)	6	12	18	mT
B_{RP}	Release point; see Figure 12		–18	–12	–6	mT
B_{hys}	Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$			24		mT
B_O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		–1.5	0	1.5	mT

(1) 1 mT = 10 Gauss.
(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
(3) $T_{A,\ MAX}$ is 125°C for Q devices and 150°C for E devices (see 图 24).

6.8 Typical Characteristics

T_A > 125°C data are valid for *E* temperature range devices only, see 图 24

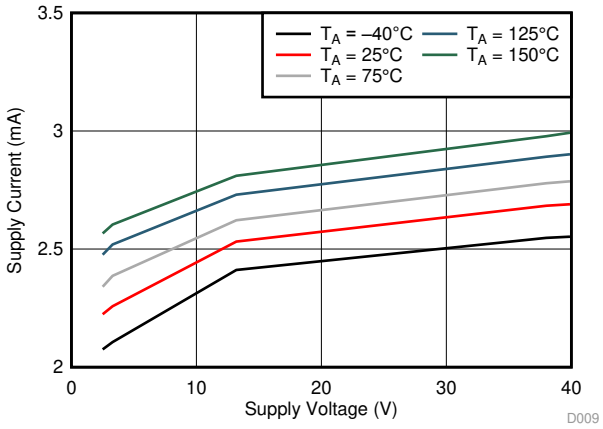


Figure 1. I_{CC} vs V_{CC}

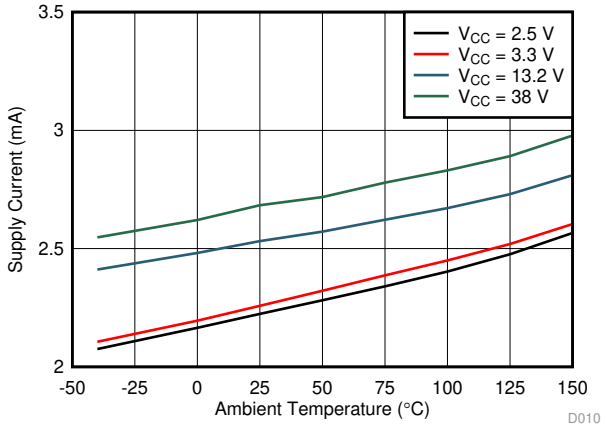


Figure 2. I_{CC} vs Temperature

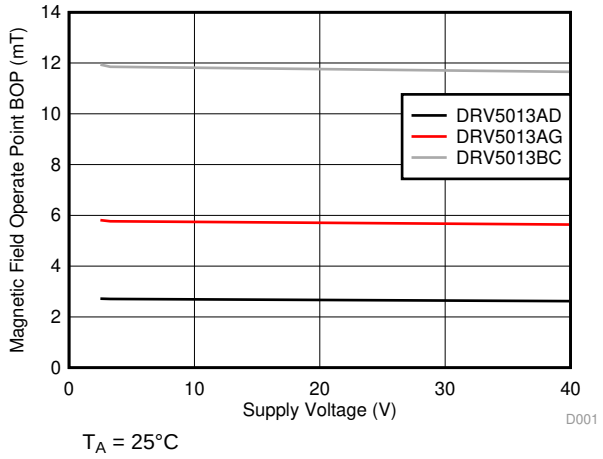


Figure 3. B_{OP} vs V_{CC}

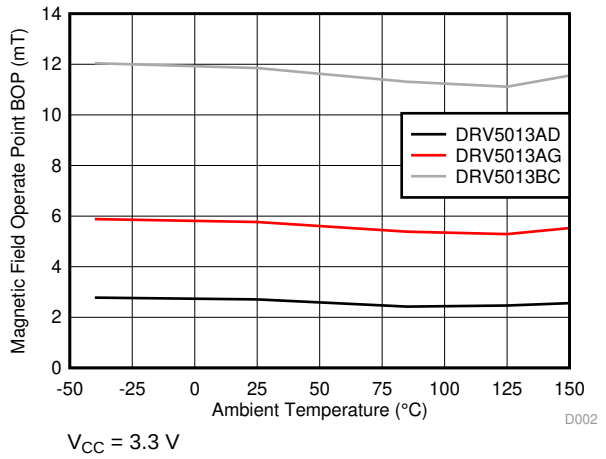


Figure 4. B_{OP} vs Temperature

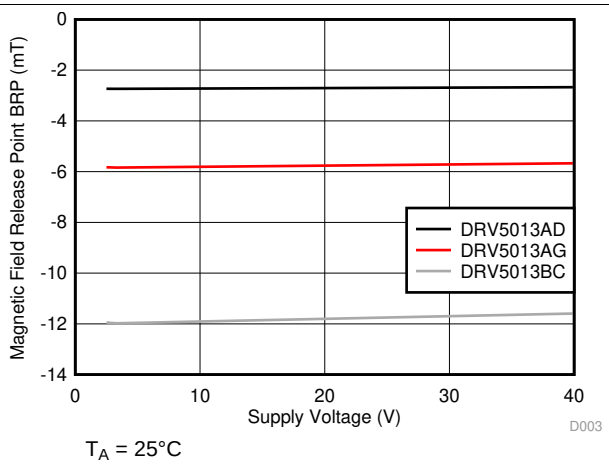


Figure 5. B_{RP} vs V_{CC}

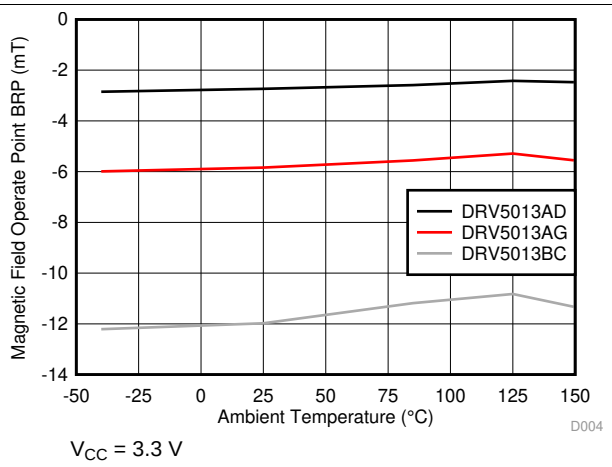
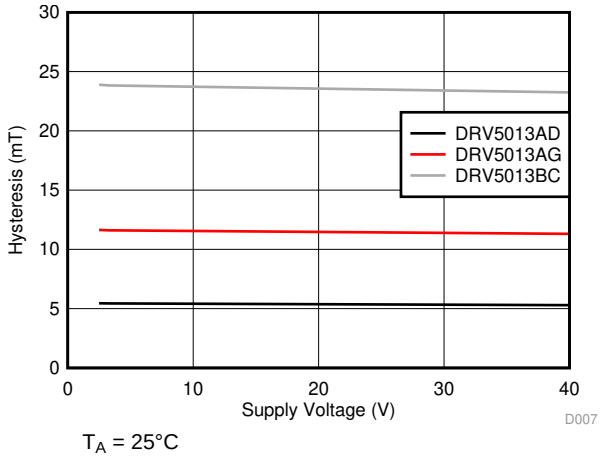


Figure 6. B_{RP} vs Temperature

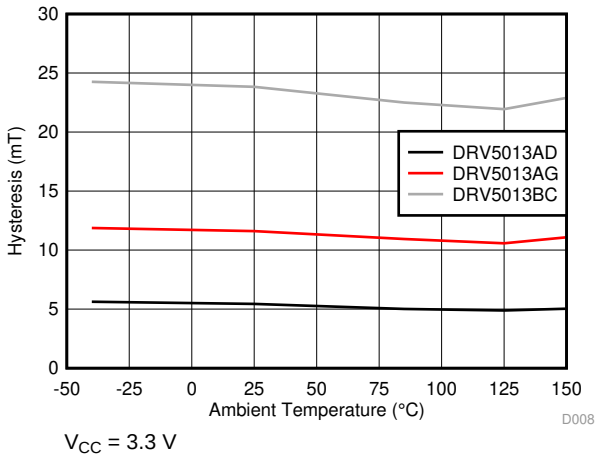
Typical Characteristics (continued)

T_A > 125°C data are valid for *E* temperature range devices only, see 图 24



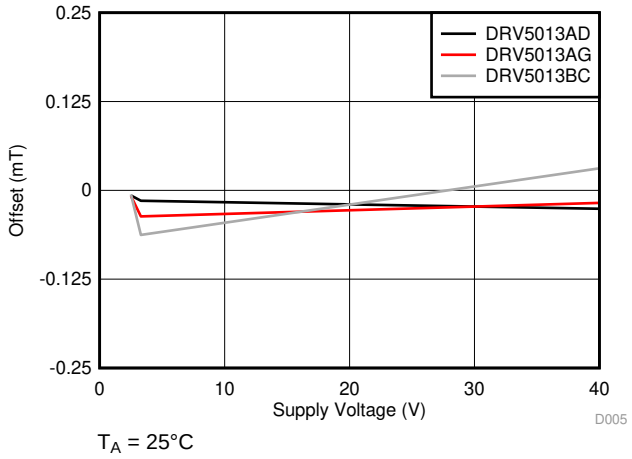
T_A = 25°C

Figure 7. Hysteresis vs V_{CC}



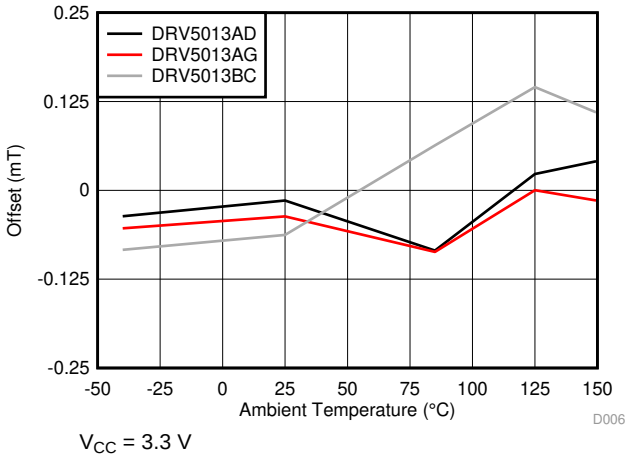
V_{CC} = 3.3 V

Figure 8. Hysteresis vs Temperature



T_A = 25°C

Figure 9. Offset vs V_{CC}



V_{CC} = 3.3 V

Figure 10. Offset vs Temperature

7 Detailed Description

7.1 Overview

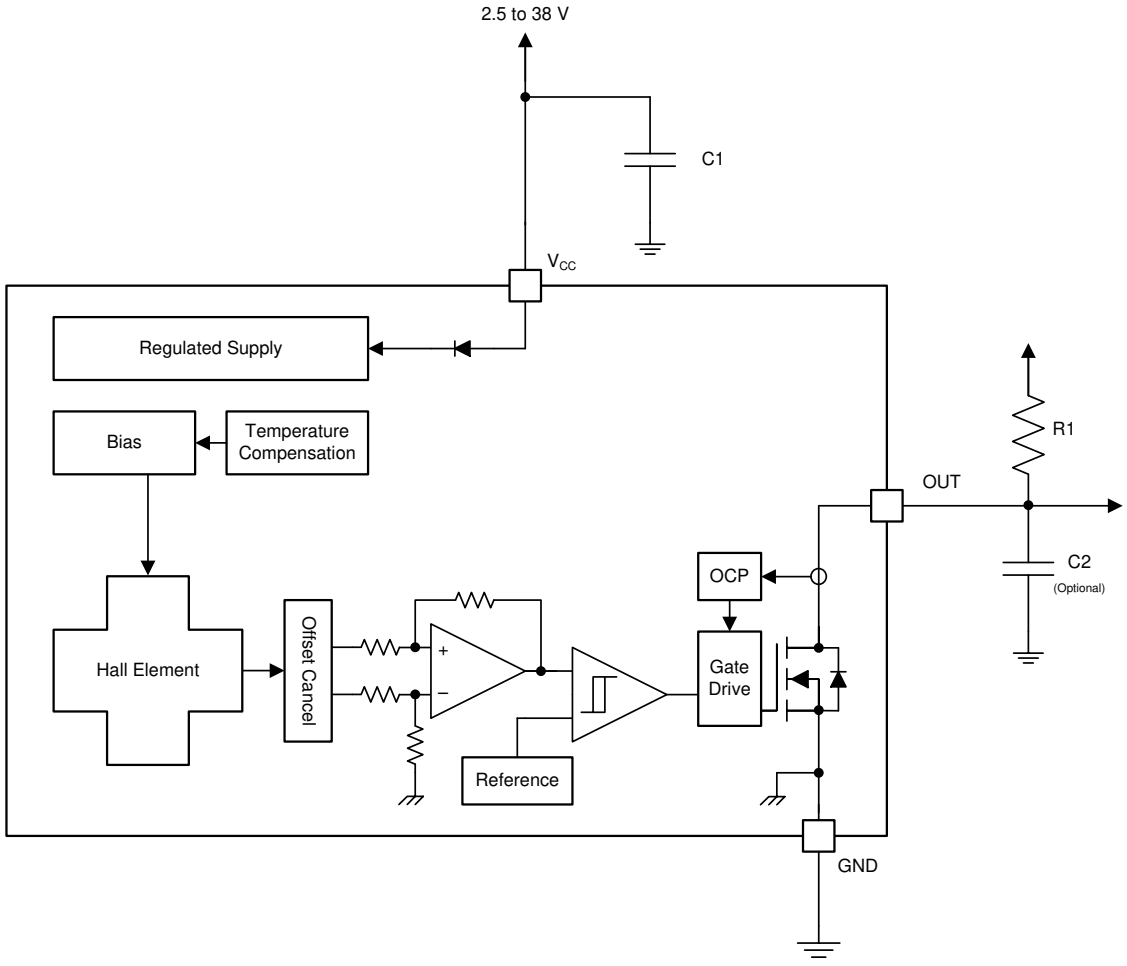
The DRV5013 device is a chopper-stabilized Hall sensor with a digital latched output for magnetic sensing applications. The DRV5013 device can be powered with a supply voltage between 2.5 and 38 V, and continuously survives continuous –22-V reverse-battery conditions. The DRV5013 device does not operate when –22 to 2.4 V is applied to the V_{CC} pin (with respect to the GND pin). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

The output state is dependent on the magnetic field perpendicular to the package. A south pole near the marked side of the package causes the output to pull low (operate point, B_{OP}), and a north pole near the marked side of the package causes the output to release (release point, B_{RP}). Hysteresis is included in between the operate point and the release point therefore magnetic-field noise does not accidentally trip the output.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC}, or to a different voltage supply. This allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 11.

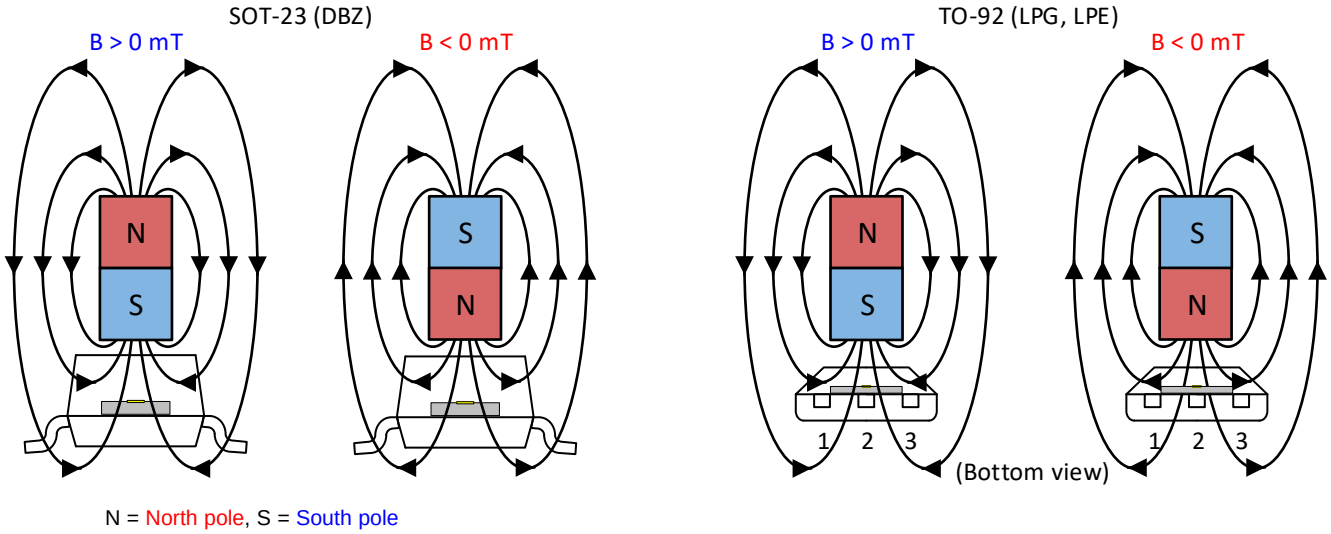


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP}, then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP}, then the output is pulled low. If the field strength is less than B_{RP}, then the output is released.

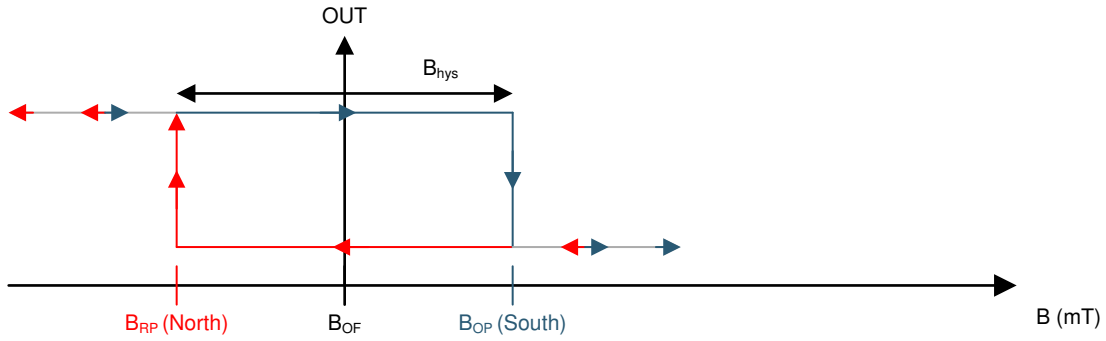


Figure 12. DRV5013—B_{OP} > 0

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5013 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on}. This pulse can allow the host processor to determine when the DRV5013 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field B > B_{OP} and B < B_{RP}.

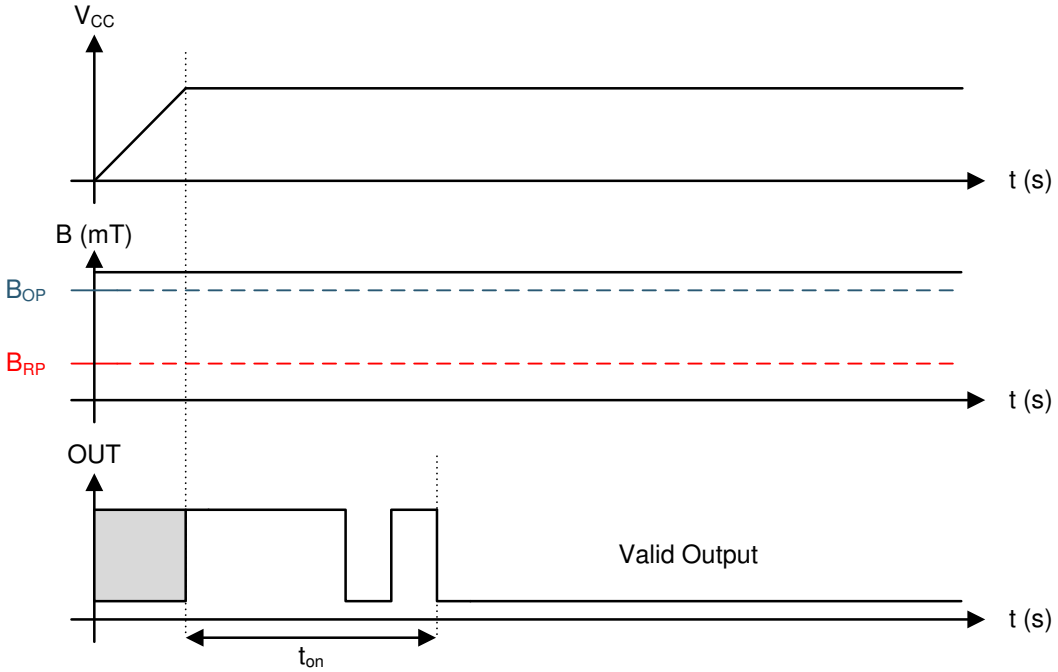


Figure 13. Case 1: Power On When B > B_{OP}

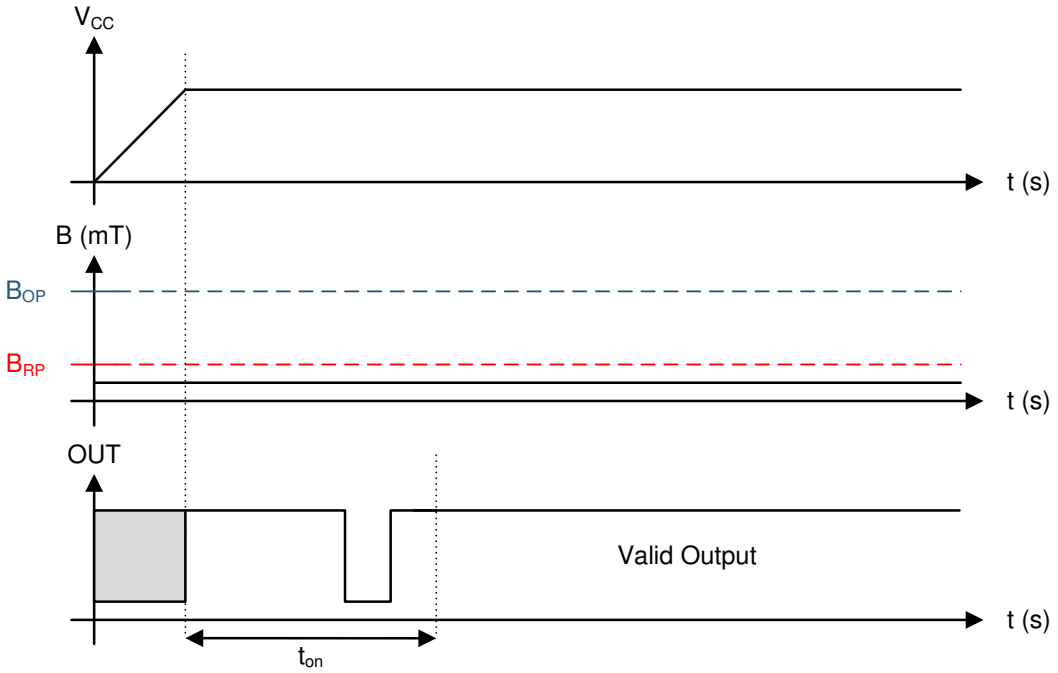


Figure 14. Case 2: Power On When B < B_{RP}

Feature Description (continued)

If the device is powered on with the magnetic field strength B_{RP} < B < B_{OP}, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on}, a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on}, if the magnetic field changes such that B_{OP} < B, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

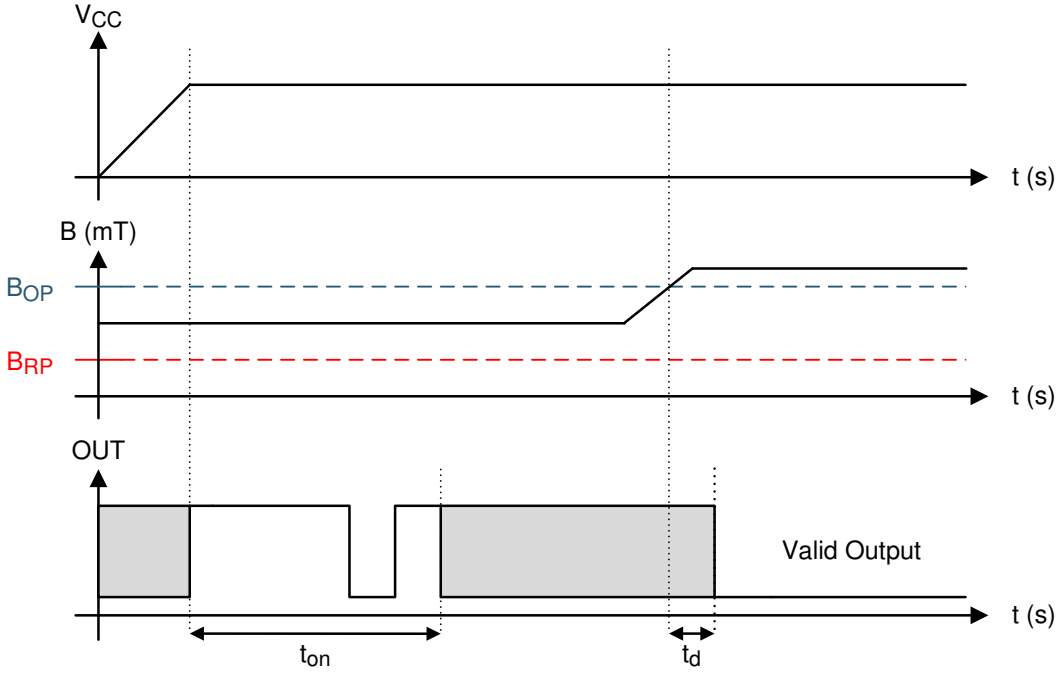


Figure 15. Case 3: Power On When B_{RP} < B < B_{OP}, Followed by B > B_{OP}

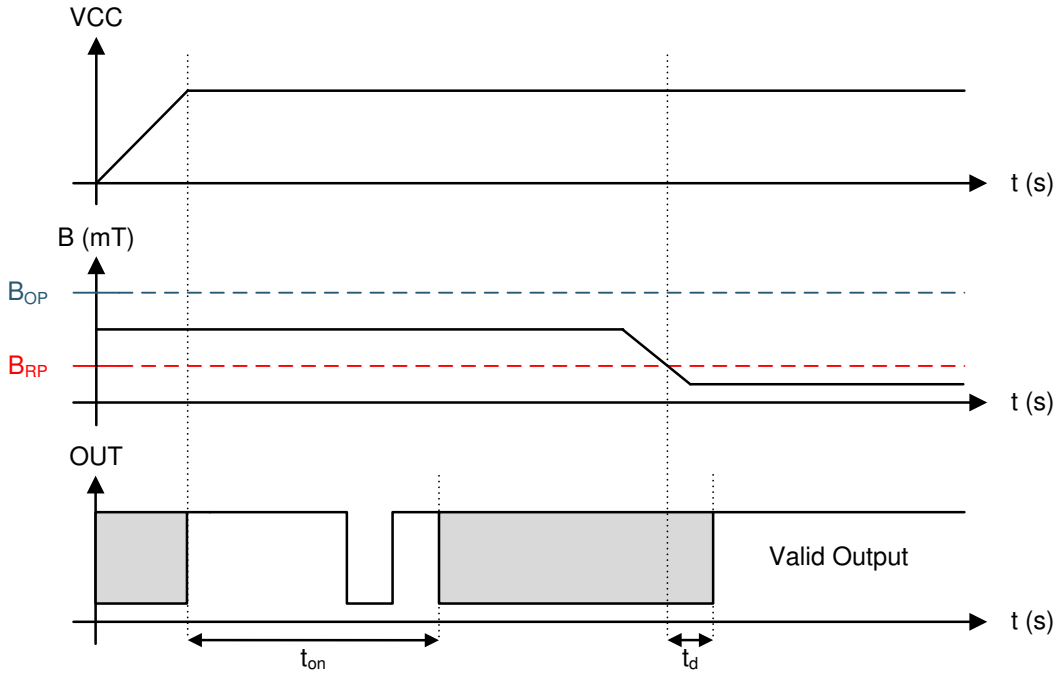


Figure 16. Case 4: Power On When B_{RP} < B < B_{OP}, Followed by B < B_{RP}

Feature Description (continued)

7.3.4 Output Stage

Figure 17 shows the DRV5013 open-drain NMOS output structure, rated to sink up to 30 mA of current. For proper operation, calculate the value of pullup resistor R1 using Equation 1.

$$\frac{V_{ref}\,max}{30\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, make sure that the value of R1 > 500 Ω so that the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC}. The allowable voltage range of this pin is specified in the *Absolute Maximum Ratings*.

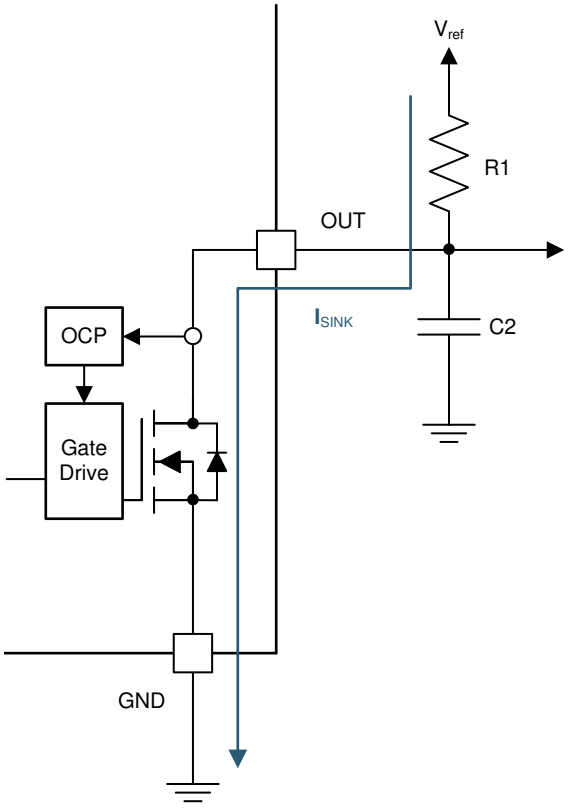


Figure 17. NMOS Open-Drain Output

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.

Feature Description (continued)

7.3.5 Protection Circuits

The DRV5013 device is fully protected against overcurrent and reverse-supply conditions. Table 1 lists a summary of the protection circuits.

Table 1. Protection Circuit Summary

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load dump	$38\ V < V_{CC} < 40\ V$	Operating	Device will operate for a transient duration	$V_{CC} \leq 38\ V$
Reverse supply	$-22\ V < V_{CC} < 0\ V$	Disabled	Device will survive this condition	$V_{CC} \geq 2.5\ V$

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP}. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5013 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5013 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to –22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

7.4 Device Functional Modes

The DRV5013 device is active only when V_{CC} is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5013 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Standard Circuit

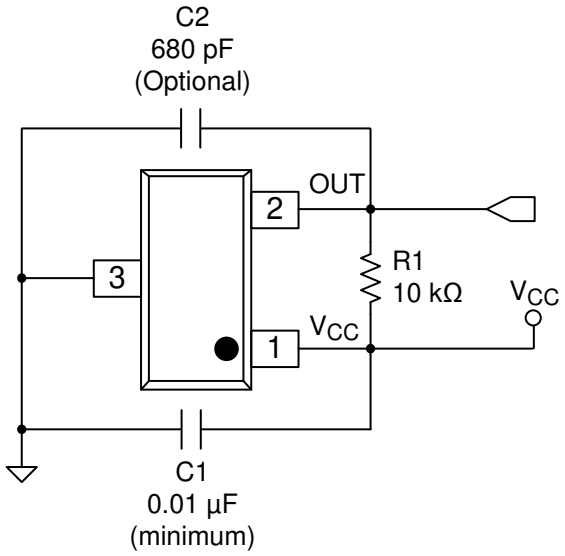


Figure 18. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

8.2.1.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	**Optional**: Place a ceramic capacitor to GND
R1	OUT	REF(1)	Requires a resistor pullup

(1) REF is not a pin on the DRV5013 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC}.

8.2.1.2.1 Configuration Example

In a 3.3-V system, 3.2 V ≤ V_{ref} ≤ 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref}\,max}{30\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \tag{3}$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\ V}{30\ mA} \le R1 \le \frac{3.2\ V}{100\ \mu A} \tag{4}$$

Therefore:

$$113\ \Omega \le R1 \le 32\ k\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

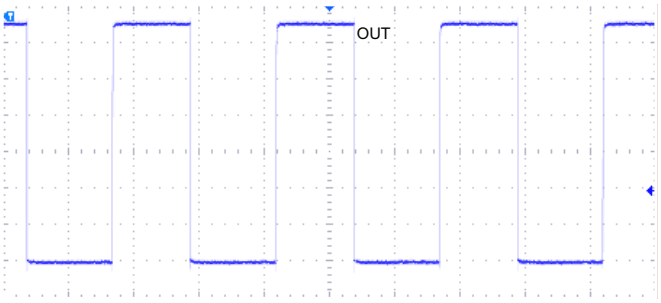
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\ kHz < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

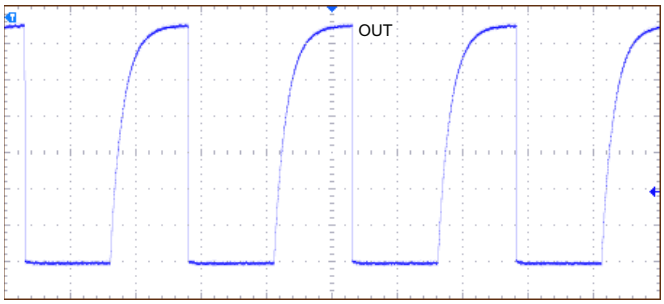
A selection of R1 = 10 kΩ and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

8.2.1.3 Application Curves



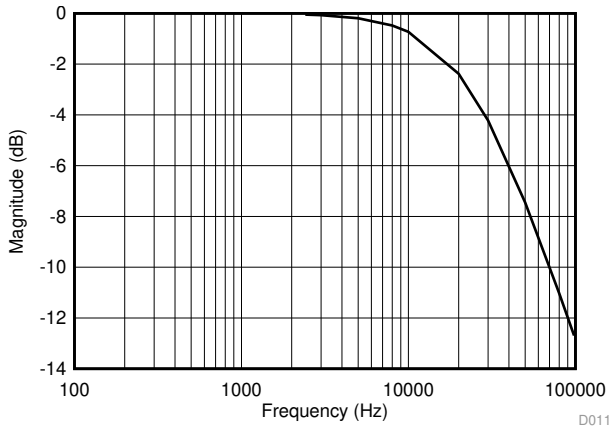
R1 = 10 kΩ pull-up No C2

Figure 19. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pull-up C2 = 680 pF

Figure 20. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pull-up C2 = 680 pF

Figure 21. Low-Pass Filtering

8.2.2 Alternative Two-Wire Application

For systems that require minimal wire count, the device output can be connected to V_{CC} through a resistor, and the total supplied current can be sensed near the controller.

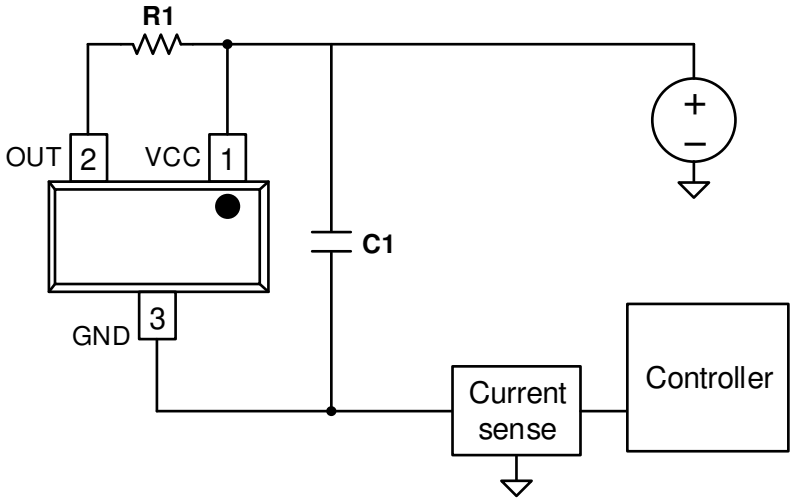


Figure 22. 2-Wire Application

Current can be sensed using a shunt resistor or other circuitry.

8.2.2.1 Design Requirements

Table 4 lists the related design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	12 V
OUT resistor	R1	1 kΩ
Bypass capacitor	C1	0.1 µF
Current when B < B_{RP}	$I_{RELEASE}$	About 3 mA
Current when B > B_{OP}	$I_{OPERATE}$	About 15 mA

8.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to V_{CC} / (R1 + $r_{DS(on)}$). Using 12 V and 1 kΩ, the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 µF, and a larger value if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5013 device is designed to operate from an input voltage supply (VM) range between 2.5 V and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5013 device as possible. Larger values of the bypass capacitor may be needed to attenuate any significant high-frequency ripple and noise components generated by the power source. TI recommends limiting the supply voltage variation to less than 50 mV_{PP}.

10 Layout

10.1 Layout Guidelines

The bypass capacitor should be placed near the DRV5013 device for efficient power delivery with minimal inductance. The external pullup resistor should be placed near the microcontroller input to provide the most stable voltage at the input; alternatively, an integrated pullup resistor within the GPIO of the microcontroller can be used.

Generally, using PCB copper planes underneath the DRV5013 device has no effect on magnetic flux, and does not interfere with device performance. This is because copper is not a ferromagnetic material. However, If nearby system components contain iron or nickel, they may redirect magnetic flux in unpredictable ways.

10.2 Layout Example

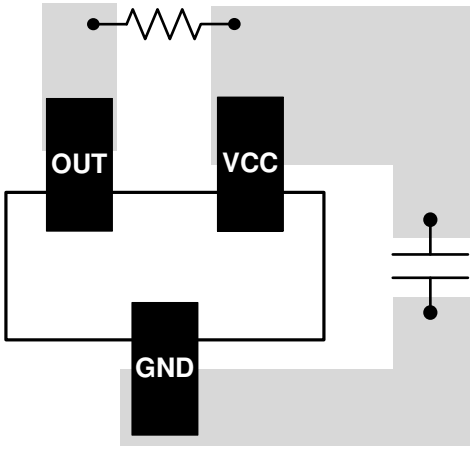


Figure 23. DRV5013 Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

图 24 显示了读取 DRV5013 器件完整器件名称的图例。

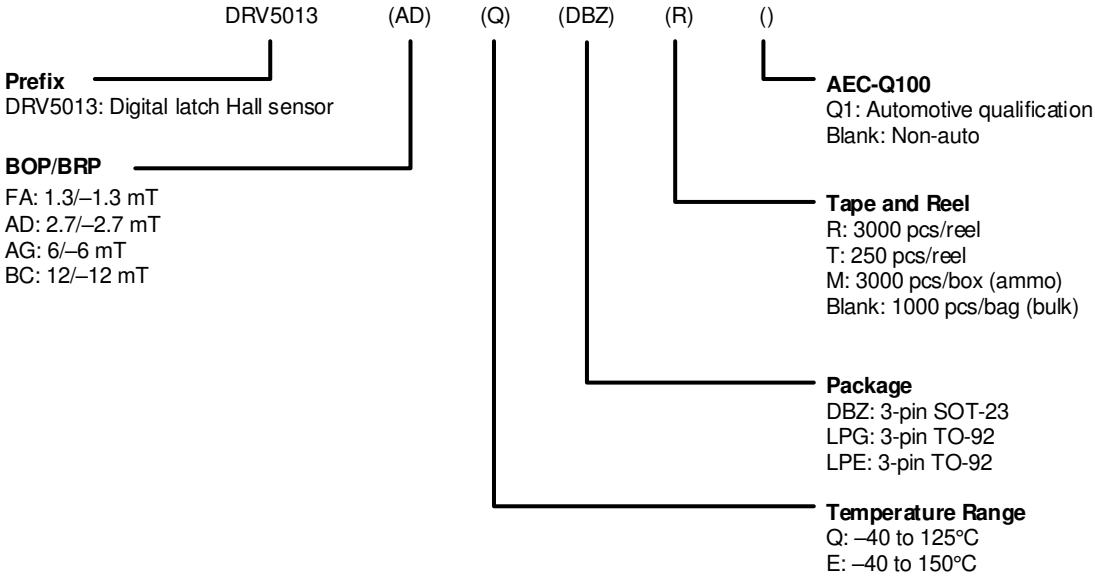


图 **24.** 器件命名规则

11.1.2 器件标记

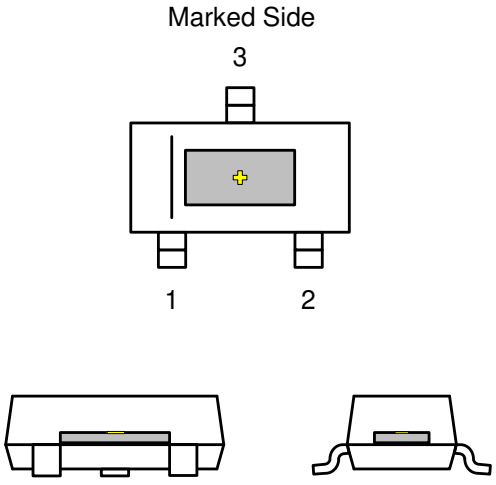


图 **25. SOT-23 (DBZ)** 封装

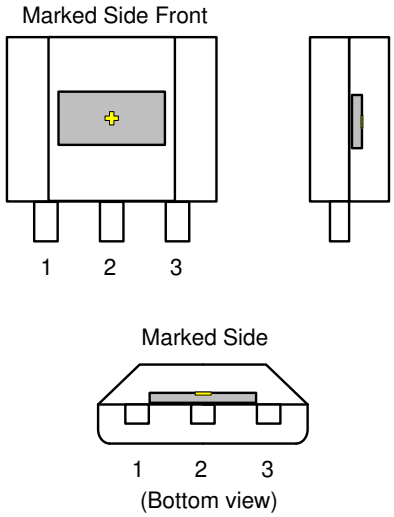


图 **26. TO-92**（**LPG**、**LPE**）封装

✚ 表示霍尔效应传感器（未按比例显示）。霍尔元件置于封装中央位置，容差为 ±100µm。采用 DBZ 封装时，霍尔元件与封装底部的距离是 0.7mm ±50µm；而采用 LPG 和 LPE 封装时，该距离为 0.987mm ±50µm。

11.2 接收文档更新通知

要接收文档更新通知，请转至 TI.com.cn 上您的器件的产品文件夹。请在右上角单击*通知我* 按钮进行注册，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查看任意已修订文档的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5013ADQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+NLAD, 1J52)	Samples
DRV5013ADQDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+NLAD	Samples
DRV5013ADQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+NLAD	Samples
DRV5013ADQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+NLAD	Samples
DRV5013AGQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+NLAG, 1IW2)	Samples
DRV5013AGQDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+NLAG, 1IW2)	Samples
DRV5013AGQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+NLAG	Samples
DRV5013AGQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+NLAG	Samples
DRV5013BCELPE	ACTIVE	TO-92	LPE	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	1UVJ	Samples
DRV5013BCELPEM	ACTIVE	TO-92	LPE	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	1UVJ	Samples
DRV5013BCQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+NLBC, 1IX2)	Samples
DRV5013BCQDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+NLBC, 1IX2)	Samples
DRV5013BCQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+NLBC	Samples
DRV5013BCQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+NLBC	Samples
DRV5013FAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(+NLFA, 1IZ2)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

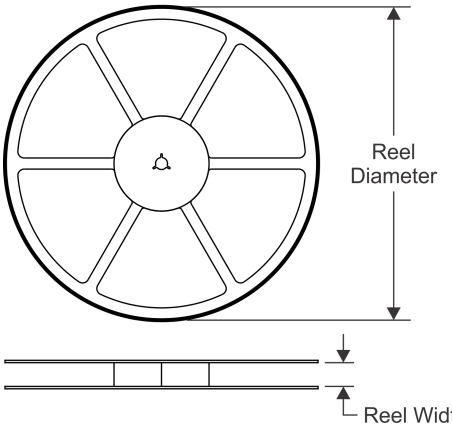
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

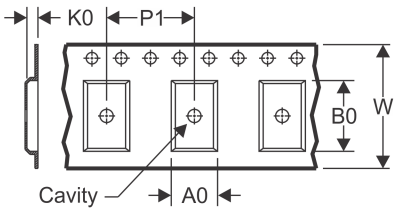
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

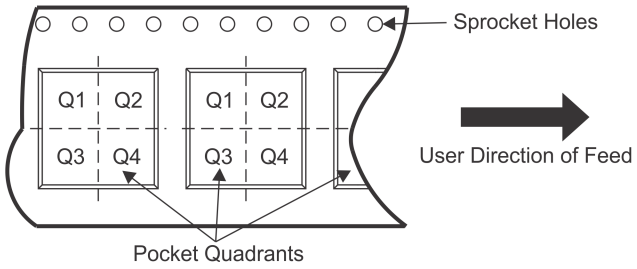


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

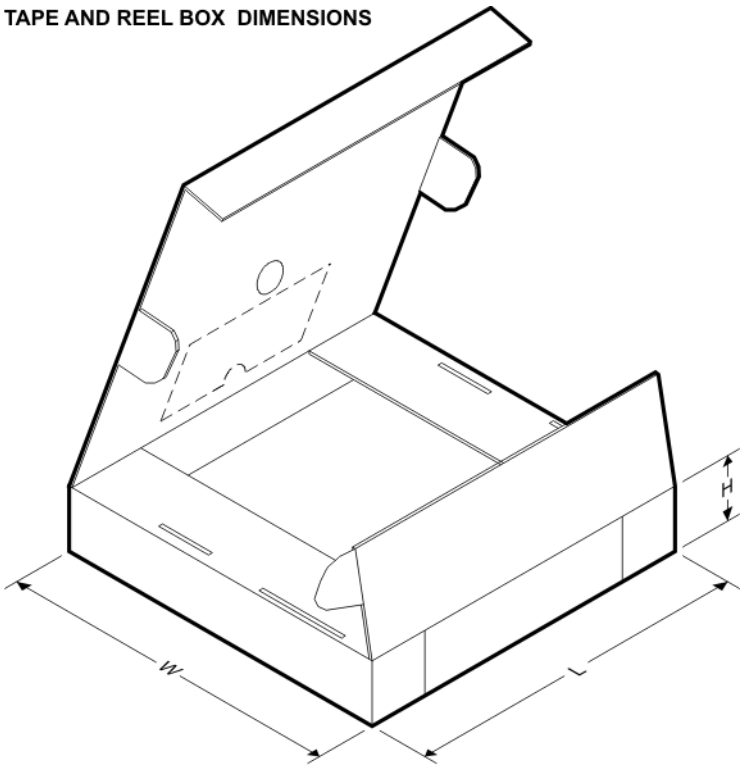
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5013ADQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013ADQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013ADQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013FAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013FAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



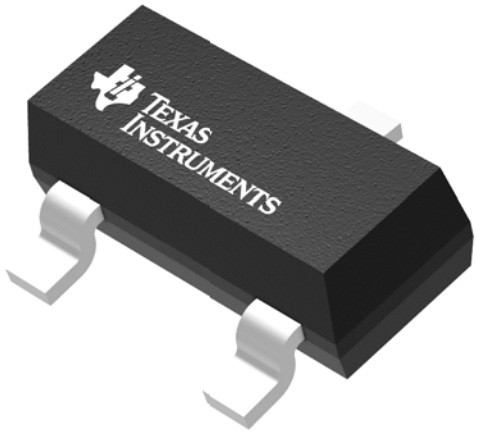
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5013ADQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5013ADQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013ADQDBZT	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013AGQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5013AGQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013AGQDBZT	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013AGQDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
DRV5013BCQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5013BCQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013BCQDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
DRV5013BCQDBZT	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013FAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5013FAQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



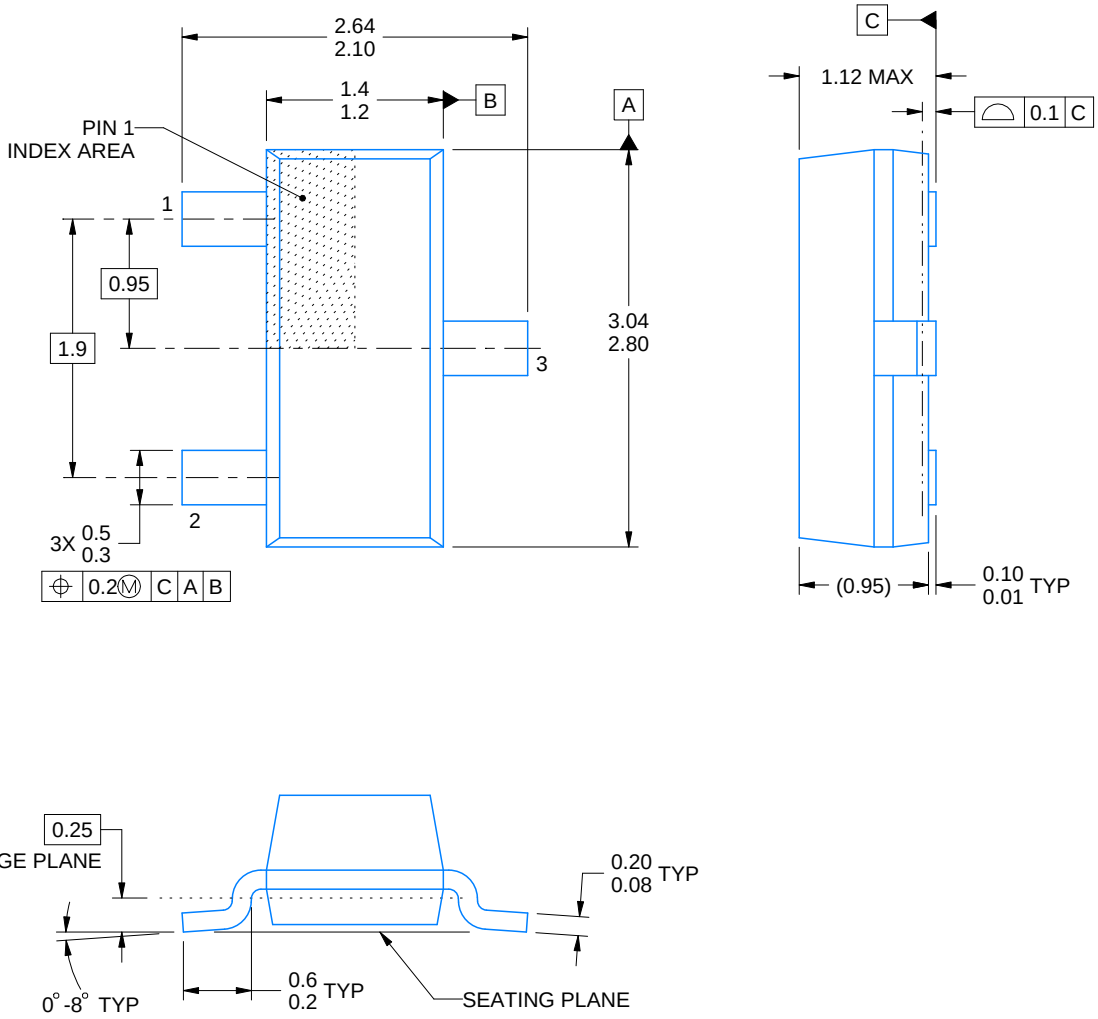
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

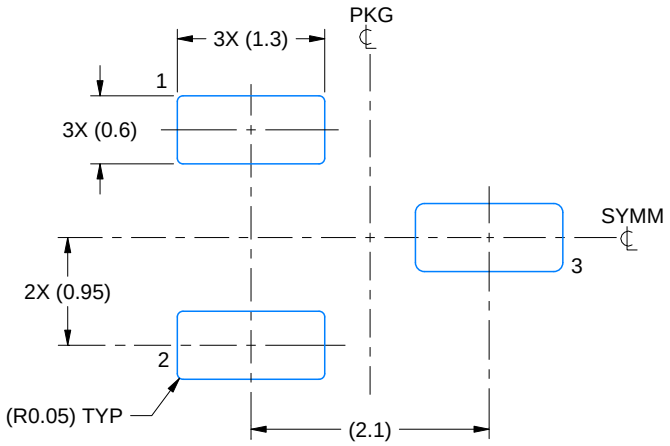
SMALL OUTLINE TRANSISTOR



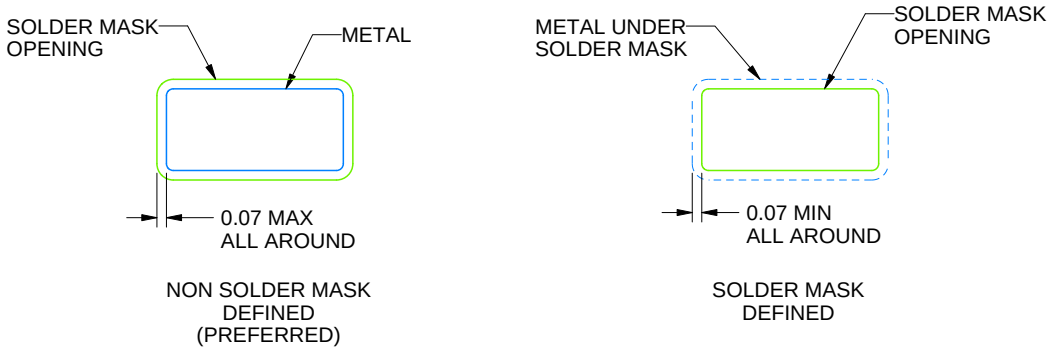
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

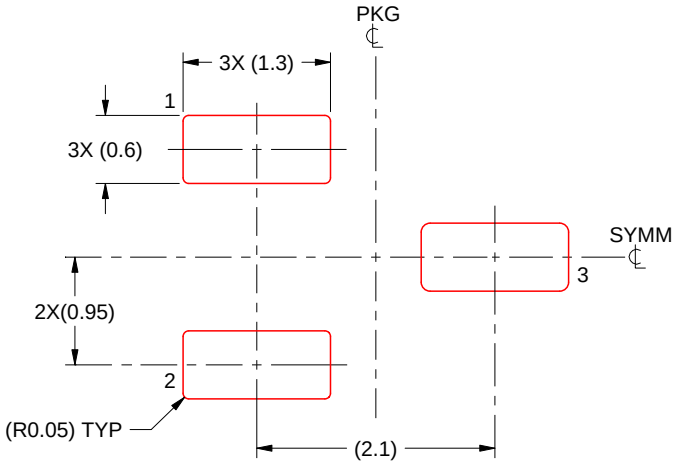


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

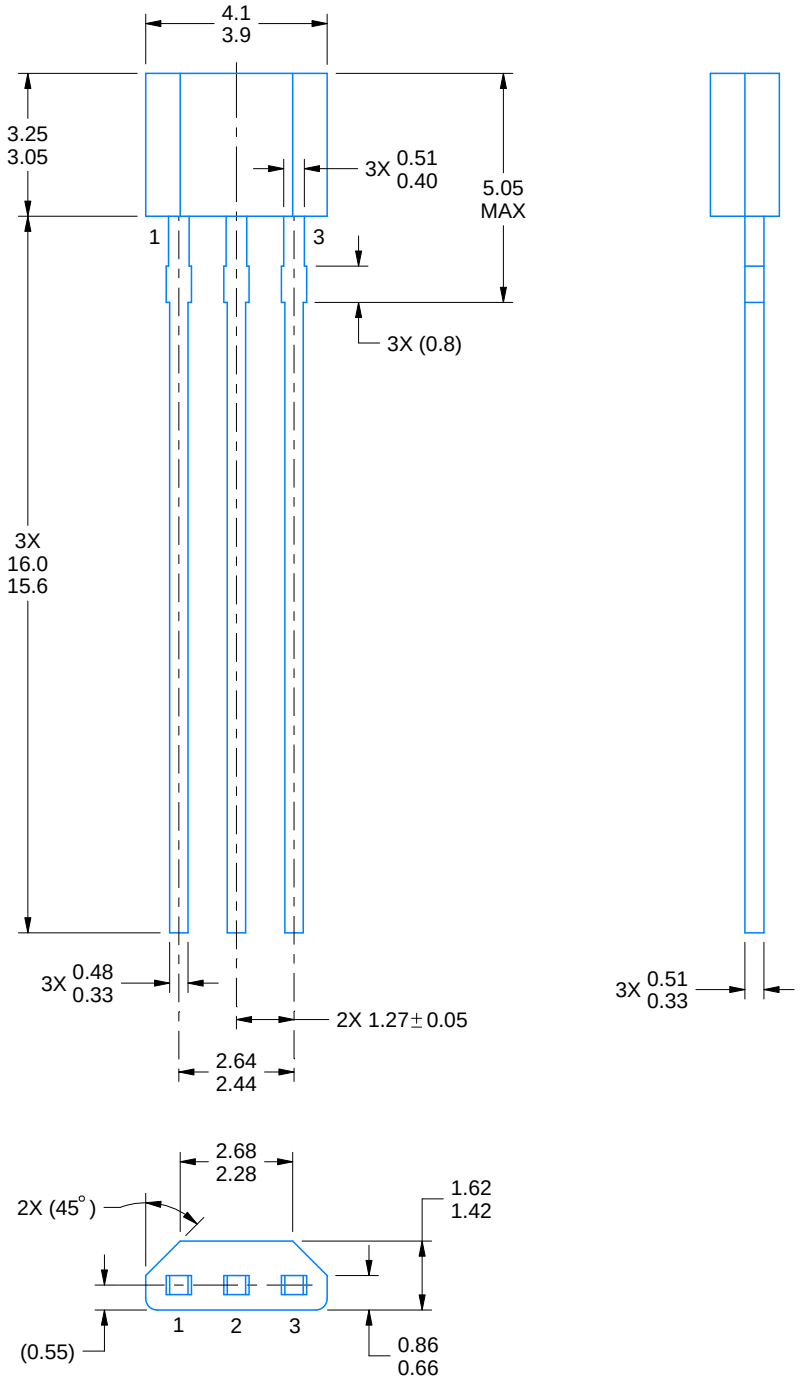
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

LPE0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4224358/A 06/2018

NOTES:

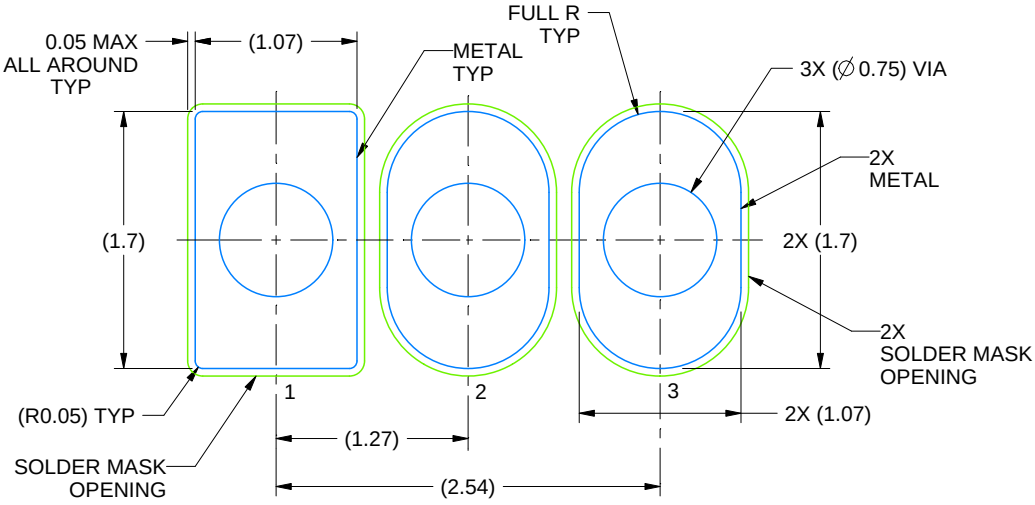
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

LPE0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



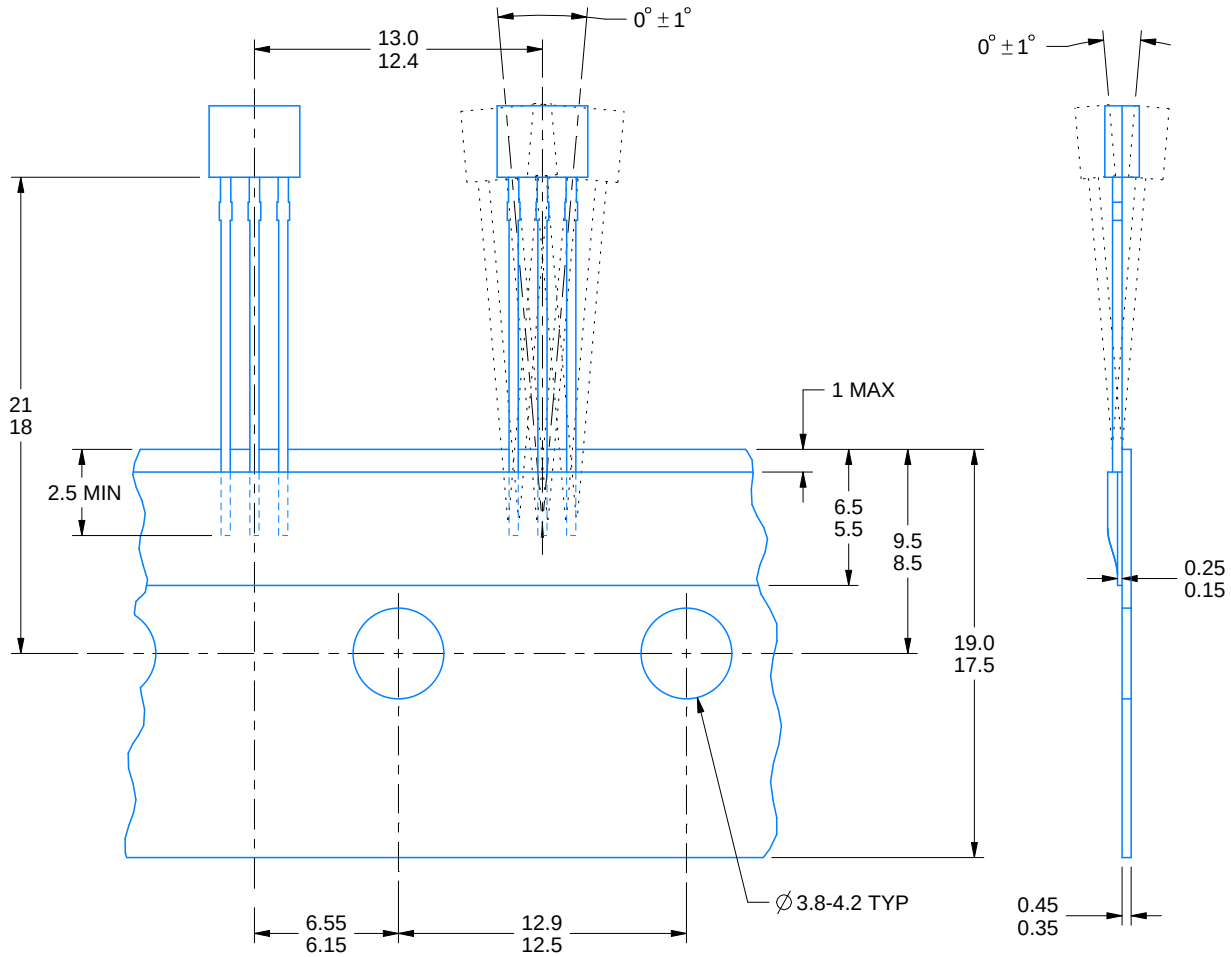
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

4224358/A 06/2018

LPE0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



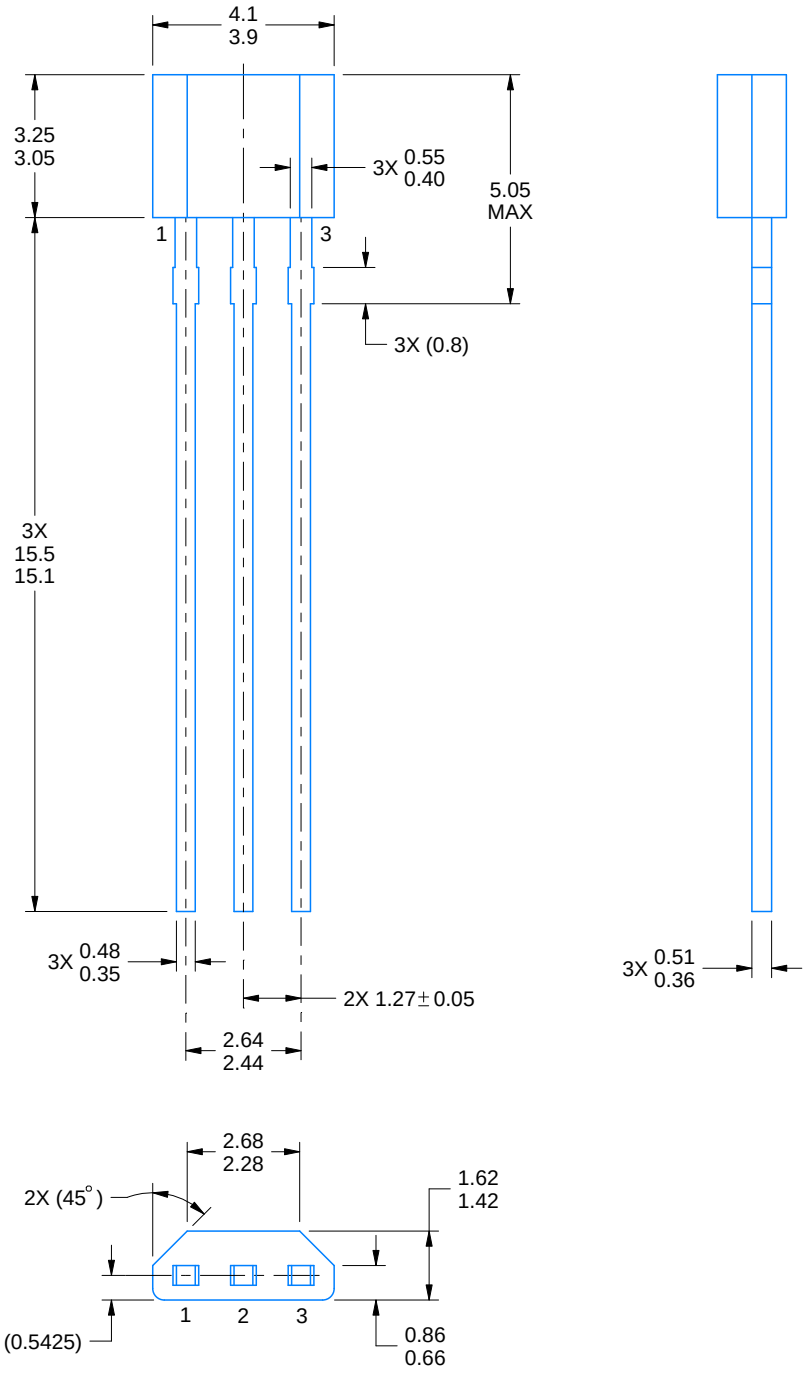
4224358/A 06/2018

PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

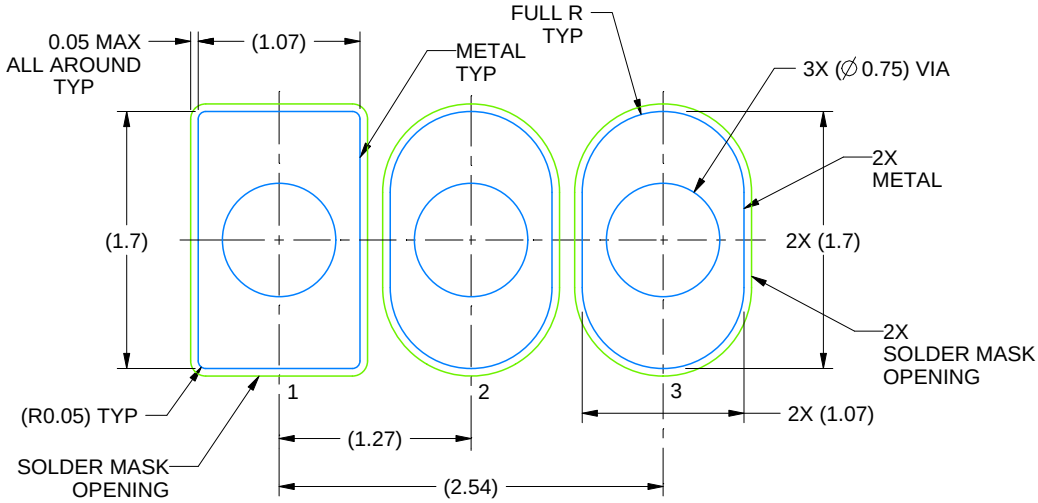
TRANSISTOR OUTLINE



4221343/C 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

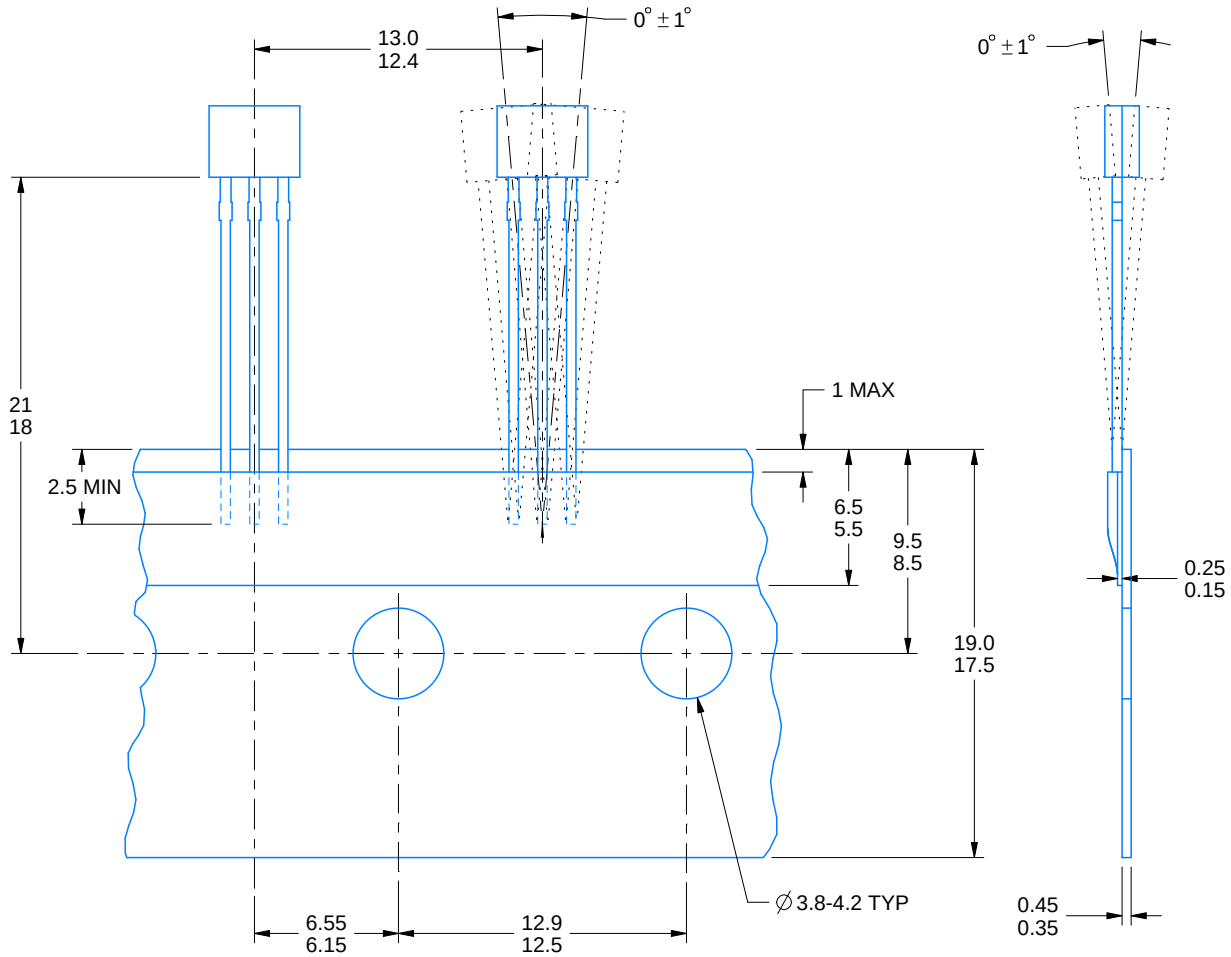
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122