# TPS62840 1.8V 至 6.5V、750mA、60nA $I_Q$ 降压转换器

## 1 特性

- 60nA 工作静态电流
- 100% 占空比模式下，$I_Q$ 为 120nA
- 输入电压范围 $V_{IN}$：1.8V 至 6.5V
- 高达 750mA 的输出电流
- 射频友好型 DCS-Control™
- 1μA $I_{OUT}$（3.6$V_{IN}$ 至 1.8$V_{OUT}$）时的效率为 80%
- 通过 VSET 引脚提供 16 种可选输出电压
- 自动转换 PFM/PWM 或强制 PWM 模式
- 可选的强制 PWM 和 STOP 模式
- 输出放电功能
- 25nA 关断电流
- SON-8、WCSP-6 和热增强型 HVSSOP-8

## 2 应用

- 智能仪表、智能恒温器
- 资产跟踪设备
- 可穿戴电子产品
- 医疗传感器贴片和患者监护仪
- 工业物联网（智能传感器）/窄带物联网
- 测试和测量
- ATEX/本质安全

## 3 说明

TPS62840 是一款高效降压转换器，具有典型值为 60nA 的超低工作静态电流。此器件具有特殊电路，可在 100% 模式下实现仅 120nA 的 $I_Q$，因此可在放电末期进一步延长电池寿命。

此器件采用 DCS-Control 技术，可以为无线电提供干净的电源，工作时具有 1.8MHz 的典型开关频率。在省电模式下，此器件可将轻负载效率向下扩展至 1μA 负载电流及以下。

可以将一个电阻器连接到 VSET 引脚以选择 16 种预定义的输出电压，因此这款器件可以灵活地用于各种 应用 并最大限度地减少了外部组件的数量。

该器件的 STOP 引脚可立即消除所有的开关噪声，从而在测试和测量系统中执行无噪声测量。

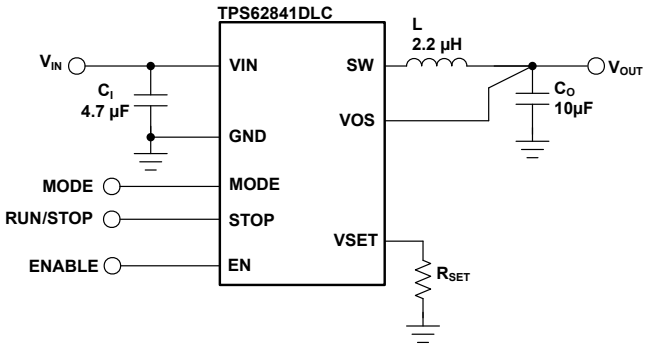
TPS62840 提供了高达 750mA 的输出电流。此器件的输入电压为 1.8V 至 6.5V，支持多种电源，例如 2 节至 4 节碱性电池或 1 节至 2 节锂二氧化锰 (Li-$MnO_2$) 或 1 节锂离子/锂亚硫酰氯 (Li-$SOCl_2$) 电池。

器件信息(1)

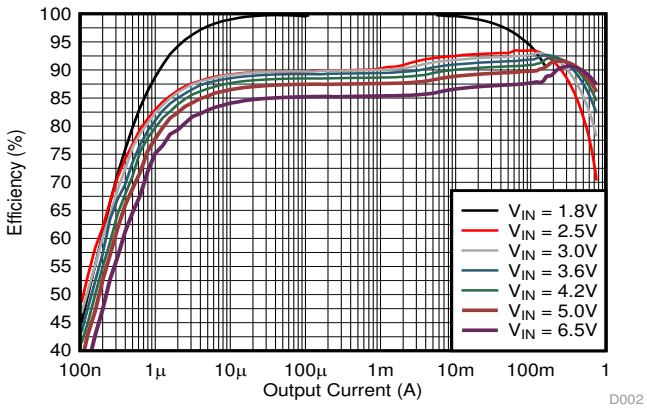
| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS6284x | 8 引脚 DLC (SON) | 1.5mm x 2mm |
| | 6 引脚 YBG (WCSP) | 0.97mm x 1.47mm |
| | 8 引脚 DGR (HVSSOP) | 3mm x 5mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用




效率与负载电流间的关系 ($V_{OUT}$ = 1.8V)



# 目录



## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision C (November 2019) to Revision D** **Page**

- Updated the *Device Comparison Table* ... 3
- Added efficiency graphs to the *Application Curves* ... 20

**Changes from Revision B (August 2019) to Revision C** **Page**

- 将 SON-8、WCSP-6 和热增强型 HVSSOP-8 添加至*特性* ... 1
- 将“ATEX/本质安全”添加到*应用* ... 1
- 更新了典型应用图像以显示 TPS62842DGR 器件 ... 1
- Added orderable part number TPS62841DGR to *Device Comparison Table* ... 3
- Added orderable part number TPS62842DGR to *Device Comparison Table* ... 3
- Updated *Thermal Information* values to support TPS62842DGR ... 6
- Added low-side MOSFET switch current limit to *Electrical Characteristics* ... 8
- Added TPS62841DGR to *Output Voltage Selection* ... 13
- Updated Efficiency Power Save graphs in *Application Curves* ... 20
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- Added PCB layout for DGR package ... 29

**Changes from Revision A (July 2019) to Revision B** **Page**

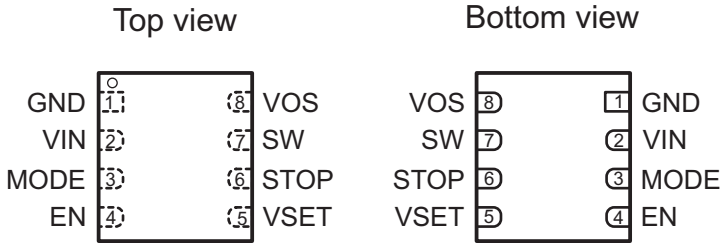
- 将销售状态从“预告信息”更改为“生产数据” ... 1

# 5 Device Comparison Table

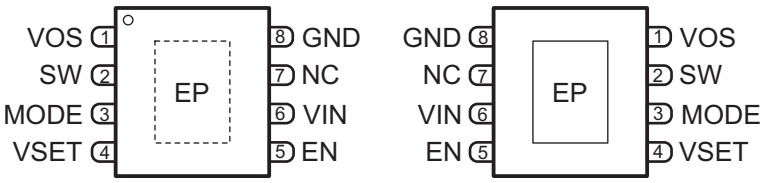
| ORDERABLE PART NUMBER | OUTPUT VOLTAGE | OUTPUT CURRENT | OUTPUT DISCHARGE | MODE PIN | STOP PIN | PACKAGE | PACKAGE MARKING |
|---|---|---|---|---|---|---|---|
| TPS62840DLC | 1.8 V to 3.3 V in 100-mV steps | 750 mA | yes | yes | yes | SON-8 (DLC) | E5 |
| TPS62840YBG | | | | no | no | WCSP-6 (YBG) | 62840 |
| TPS62841DLC | 0.8 V to 1.55 V in 50-mV steps | 750 mA | yes | yes | yes | SON-8 (DLC) | E9 |
| TPS62841YBG | | | | no | no | WCSP-6 (YBG) | 62841 |
| TPS62841DGR | | | | yes | no | HVSSOP-8 (DGR) | 62841 |
| TPS62842DGR | 1.8 V, 2.0 V, 2.2 V, 2.4 V to 3.6 V in 100-mV steps | 750 mA | yes | yes | no | HVSSOP-8 (DGR) | 62842 |
| TPS62849DLC | 3.4-V fixed output voltage | | | | yes | SON-8 (DLC) | FF |

# 6 Pin Configuration and Functions

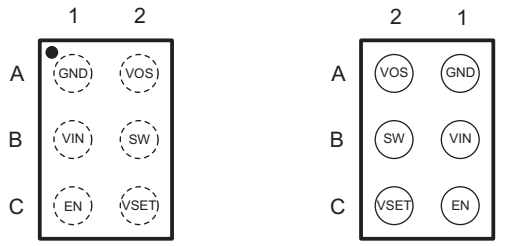
**DLC**
**SON-8**




**DGR**
**HVSSOP-8**




**YBG**
**WCSP-6**



## Pin Functions

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DLC (SON-8) | DGR (HVSSOP-8) | YBG (WCSP-6) | | |
| VIN | 2 | 6 | B1 | PWR | $V_{IN}$ power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A 4.7-µF ceramic capacitor is required. |
| SW | 7 | 2 | B2 | PWR | The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal. |
| GND | 1 | 8 | A1 | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitors. |
| VSET | 5 | 4 | C2 | IN | Connecting a resistor to GND sets the output voltage when the converter is enabled. For the TPS62849, connect this pin to GND. |
| VOS | 8 | 1 | A2 | IN | Output voltage sense pin for the internal feedback divider network and regulation loop. When the converter is disabled, this pin discharges $V_{OUT}$ by an internal MOSFET. Connect this pin directly to the output capacitor with a short trace. |
| EN | 4 | 5 | C1 | IN | Enable pin. A high level enables the device and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up and the output voltage is regulated. The pulldown resistor is activated again, once a low level has been detected. |
| STOP | 6 | n/a | n/a | IN | STOP Switching pin. When this pin is logic high, the converter stops switching in order to provide a quiet supply rail. The output is powered from the charge available in the output capacitor. When this pin is logic low, the device immediately resumes operation. The pin features an internal pulldown resistor, which is disabled once a high level is detected at the input. The pulldown resistor is activated again, once a low level has been detected. |
| MODE | 3 | 3 | n/a | IN | MODE pin. A low level enables Power-Save Mode operation with an automatic transition between PFM and PWM modes. A high level forces the converter to operated in PWM mode. This pin can be toggled during operation. It must be terminated. |
| NC | n/a | 7 | n/a | | This pin is not connected internally. Do not connect this pin. |
| EP | n/a | 9 | n/a | PWR | Exposed thermal pad(1). The PowerPAD must be connected to GND. |

(1) For more information about the PowerPAD, see the *PowerPAD™ Thermally Enhanced Package* application report.

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage(2) | VIN | –0.3 | 7 | V |
| | SW (DC) | –0.3 | $V_{IN}$ + 0.3 | V |
| | SW (AC), less than 10ns(3) | –2.0 | 8.5 | V |
| | EN, MODE, STOP | –0.3 | 6.5 | V |
| | VSET | –0.3 | $V_{IN}$ + 0.3 < 3.6 | V |
| | VOS | –0.3 | 3.7 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) While switching.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage $V_{IN}$ | 1.8 | | 6.5 | V |
| L | Effective inductance | 1.51 | 2.2 | 2.9 | µH |
| $C_{OUT}$ | Effective output capacitance | 3 | 10 | 40 | µF |
| $C_{IN}$ | Effective input capacitance | 1 | 4.7 | | µF |
| $C_{VSET}$ | External parasitic capacitance at VSET pin | | | 100 | pF |
| $R_{SET}$ | Nominal resistance range for external voltage selection resistor (E96 resistor series) | 0.909 | | 267 | kΩ |
| | External voltage selection resistor tolerance | | | 1% | |
| | External voltage selection resistor temperature coefficient | | | ±200 | ppm/°C |
| $T_J$ | Operating junction temperature range | -40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | 8 Pins DLC Package | 6 Pins YBG Package | 8 Pins DGR Package | DGR EVM | UNIT |
|---|---|---|---|---|---|---|
| | | JEDEC PCB 51-7 | | JEDEC PCB 51-5 | TPS62841-2EVM123 | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 105.6 | 133.4 | 54.4 | 46.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 75.7 | 0.4 | 58.1 | N/A | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 31.9 | 39.4 | 25.9 | N/A | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.3 | 0.1 | 1.2 | 0.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 31.5 | 39.4 | 25.9 | 17.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | 11.7 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

$V_{IN}$ = 3.6 V, $T_J$ = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_{Q\_NO\_LOAD}$ | No load<br>operating input current | EN = $V_{IN}$, $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.8V<br>device switching | | 60 | | nA |
| $I_{Q\_NO\_LOAD}$ | No load<br>operating input current | EN = $V_{IN,}$ $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.2V<br>device switching | | 80 | | nA |
| $I_{Q\_NO\_LOAD}$ | No load<br>operating input current<br>(PWM Mode) | EN = $V_{IN}$, $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.8V, MODE = $V_{IN}$<br>device switching | | 3 | | mA |
| $I_{Q\_VIN}$ | Operating quiescent current into pin VIN | EN = $V_{IN}$, $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.55V or $V_{OUT}$ = 1.8V<br>device not switching, $T_J$ = 25°C<br>(DLC package option) | | 36 | 100 | nA |
| $I_{Q\_VOS}$ | Operating quiescent current into pin VOS | EN = $V_{IN}$, $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.55V or $V_{OUT}$ = 1.8V<br>device not switching, $T_J$ = 25°C<br>(DLC package option) | | 56 | 120 | nA |
| $I_{Q\_VIN}$ | Operating quiescent current into pin VIN | EN = $V_{IN}$, $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.55V or $V_{OUT}$ = 1.8V<br>device not switching, $T_J$ = -40°C to 85°C | | 36 | 360 | nA |
| $I_{Q\_VOS}$ | Operating quiescent current into pin VOS | EN = $V_{IN}$, $I_{OUT}$ = 0µA, $V_{OUT}$ = 1.55V or $V_{OUT}$ = 1.8V<br>device not switching, $T_J$ = -40°C to 85°C | | 56 | 170 | nA |
| $I_{Q\_VOS}$ | Operating quiescent current into VOS pin | EN = $V_{IN}$, $V_{OUT}$ = 3.3V<br>device not switching | | 70 | | nA |
| | | EN = $V_{IN}$, $V_{OUT}$ < 1.5 V<br>device not switching | | 5 | | nA |
| | | EN, STOP = $V_{IN}$, 3V < $V_{OUT}$ < 3.3V<br>$T_J$ = -40°C to 85°C | | 5 | 100 | nA |
| $I_{Q\_100\%\_MODE}$ | Operating quiescent current 100% Mode | $V_{IN}$ = $V_{OUT}$ = 3.3V, $T_J$ = -40°C to 85°C | | 120 | | nA |
| $I_{Q\_VIN\_STOP}$ | Operating quiescent current into pin VIN | STOP = High, $V_{OUT}$ = 1.8V, $T_J$ = -40°C to 85°C | | 70 | 175 | µA |
| $I_{SD}$ | Shutdown current | EN = GND, shutdown current into $V_{IN}$<br>VSET = GND, $T_J$ = -40°C to 85°C | | 25 | 300 | nA |
| $V_{TH\_UVLO+}$ | Undervoltage lockout threshold | Rising $V_{IN}$ | | 1.72 | 1.8 | V |
| $V_{TH\_UVLO–}$ | | Falling $V_{IN}$ | | 1.45 | 1.75 | V |
| **EN, MODE, STOP INPUTS** | | | | | | |
| $V_{IH\_TH}$ | High level input voltage | | 1.1 | | | V |
| $V_{IL\_TH}$ | Low level input voltage | | | | 0.4 | V |
| $I_{IN}$ | Input bias current | MODE input, $T_J$ = -40°C to 85°C | | 1 | 25 | nA |
| $R_{PD}$ | Internal pull-down resistance | EN, STOP inputs | 200 | 450 | | kΩ |

## Electrical Characteristics (continued)

$V_{IN}$ = 3.6 V, $T_J$ = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SWITCHES** | | | | | | |
| $R_{DS(ON)}$ | High-side MOSFET on-resistance (DLC, YBG package) | $V_{IN}$ = 3.6V, I = 200mA, $T_J$ = -40°C to 85°C | | 430 | 600 | mΩ |
| | | $V_{IN}$ = 5V, I = 200mA, $T_J$ = -40°C to 85°C | | 340 | 465 | |
| | Low-side MOSFET on-resistance (DLC, YBG package) | $V_{IN}$ = 3.6V, I = 200mA, $T_J$ = -40°C to 85°C | | 170 | 240 | mΩ |
| | | $V_{IN}$ = 5V, I = 200mA, $T_J$ = -40°C to 85°C | | 135 | 180 | |
| | High-side MOSFET on-resistance (DGR package) | $V_{IN}$ = 3.6V, I = 200mA, $T_J$ = -40°C to 85°C | | 460 | 630 | mΩ |
| | | $V_{IN}$ = 5V, I = 200mA, $T_J$ = -40°C to 85°C | | 370 | 495 | |
| | Low-side MOSFET on-resistance (DGR package) | $V_{IN}$ = 3.6V, I = 200mA, $T_J$ = -40°C to 85°C | | 200 | 270 | mΩ |
| | | $V_{IN}$ = 5V, I = 200mA, $T_J$ = -40°C to 85°C | | 165 | 210 | |
| $I_{LIMF\_SS}$ | Soft-start switch current limit(1) | | 0.15 | 0.225 | 0.3 | A |
| $I_{LIMF}$ | High-side MOSFET switch current limit(1) | | 1.0 | 1.2 | 1.4 | A |
| | Low-side MOSFET switch current limit | | | 1.0 | | A |
| $I_{LIMN}$ | Negative current limit | | | 533 | | mA |
| $t_{I\_LIM\_DELAY}$ | Current limit propagation delay | | | 50 | | ns |
| $I_{LKG\_SW}$ | Leakage current into SW pin | $V_{SW}$ = 1.8V, $T_J$ = -40°C to 85°C | | 10 | | nA |
| **OUTPUT VOLTAGE DISCHARGE** | | | | | | |
| $I_{DISCHARGE\_VOS}$ | Output discharge current | EN = GND, sink current into VOS pin, over VIN range $V_{OUT}$ = 1.8V, $T_J$ = -40°C to 85°C | 16 | 35 | 44 | mA |
| **THERMAL PROTECTION** | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature | Rising junction temperature, PWM Mode | | 160 | | °C |
| | Thermal shutdown hysteresis | | | 5 | | °C |
| **OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage accuracy | PWM Mode, $I_{OUT}$ = 0 mA, $V_{OUT}$ >= 1.8 V | -1.5 | 0 | 1.5 | % |
| | | PWM Mode, $I_{OUT}$ = 0 mA, $V_{OUT}$ <= 1.55 V | -2 | 0 | 2 | % |
| $V_{OUT}$ | DC output voltage load regulation | PWM Mode | | 0 | | %/mA |
| | DC output voltage line regulation | PWM Mode $V_{OUT}$ = 1.8V, $I_{OUT}$ = 200 mA, over VIN range | | 0 | | %/V |
| $f_{SW}$ | Switching frequency | $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.8V, MODE = $V_{IN}$ $I_{OUT}$ = 0mA | | 1.8 | | MHz |
| $t_{STARTUP\_DELAY}$ | Regulator start up delay time | $V_{IN}$ = 3.6V, from EN = low to high until device starts switching | | | 200 | µs |
| $t_{STARTUP\_DELAY}$ | Regulator start up delay time | EN ramps with VIN, VIN 0 to 3.6V (< 100us), until device starts switching | | 10 | | ms |
| $t_{SS}$ | Soft-start time | $I_{OUT}$ = 0mA | | 120 | | µs |
| $t_{SS\_ILIMF}$ | Reduced current limit soft-start timeout | | | 700 | 1200 | µs |

(1) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Switch Current Limit / Short Circuit Protection section).

## 7.6 Typical Characteristics

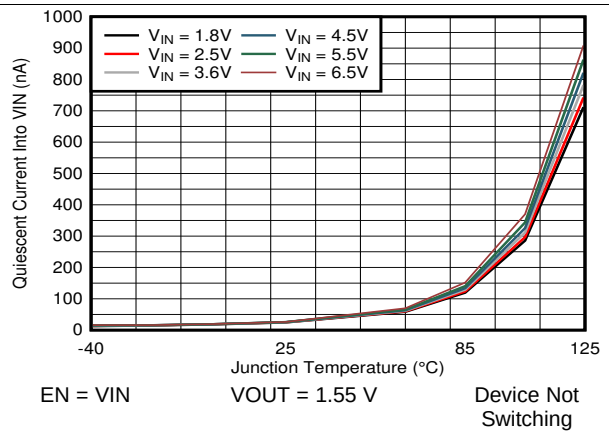



**图 1. Quiescent Current into VIN ($I_{Q\_VIN}$)**

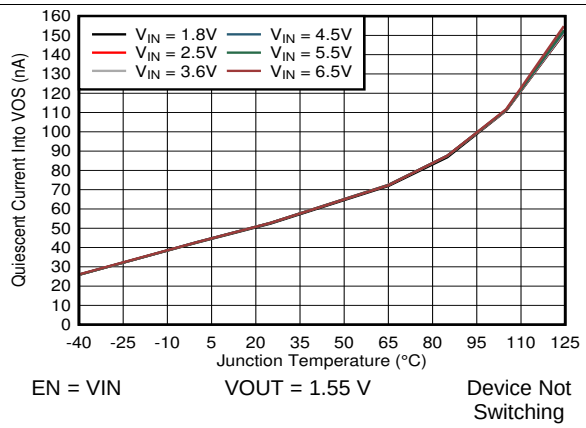



**图 2. Quiescent Current into VOS ($I_{Q\_VOS}$)**

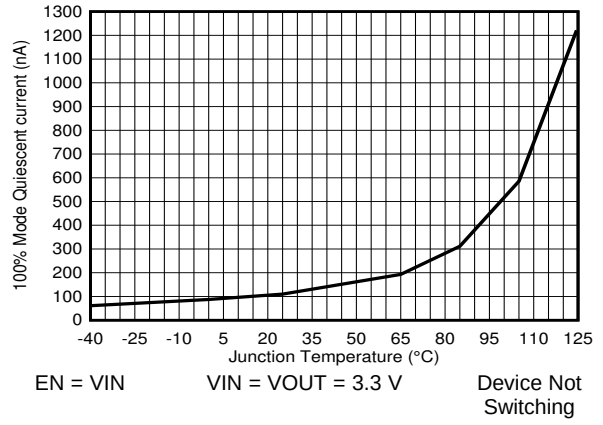



**图 3. 100% Mode Quiescent Current ($I_{Q\_100\%\_MODE}$)**

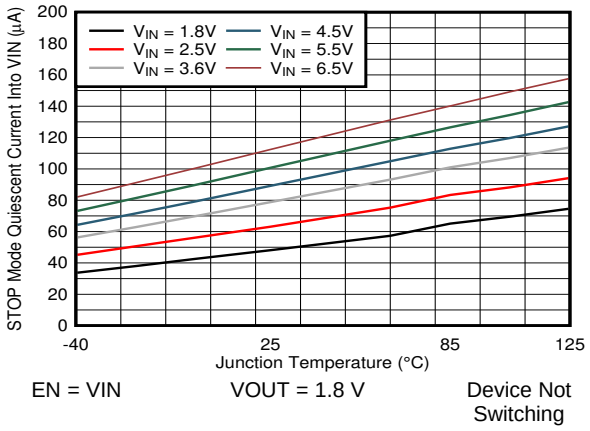



**图 4. STOP Mode Quiescent Current into VIN ($I_{Q\_VIN\_STOP}$)**

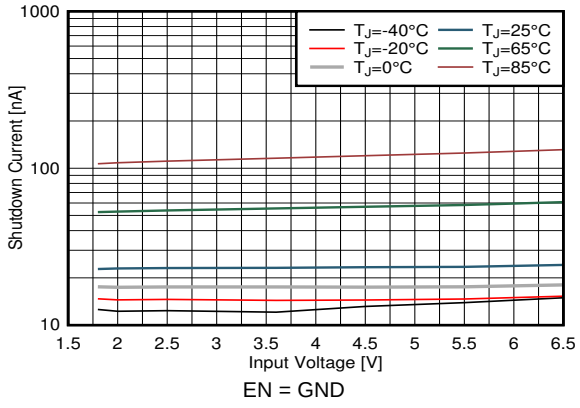



**图 5. Shutdown Current ($I_{SD}$)**

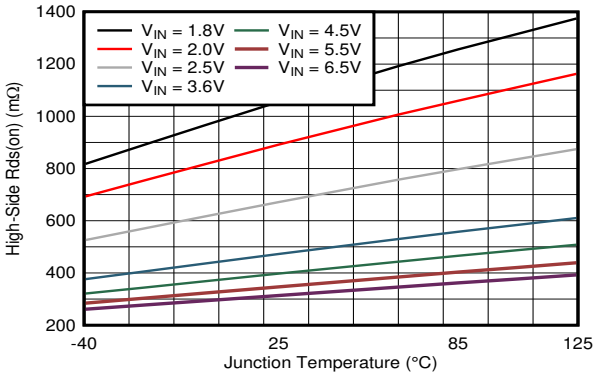



**图 6. High-Side $R_{DSON}$ versus Temperature (DLC, YBG packages)**

## Typical Characteristics (接下页)

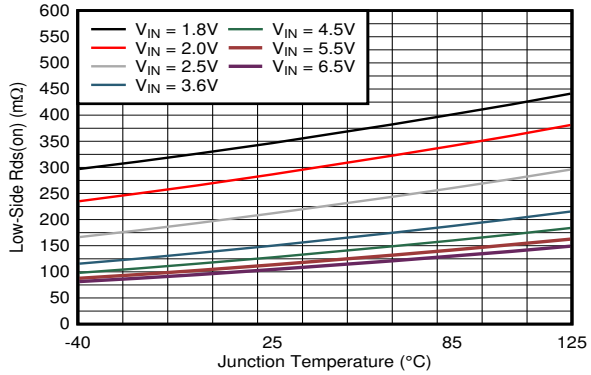



**图 7. Low-Side $R_{DSON}$ versus Temperature (DLC, YBG packages)**

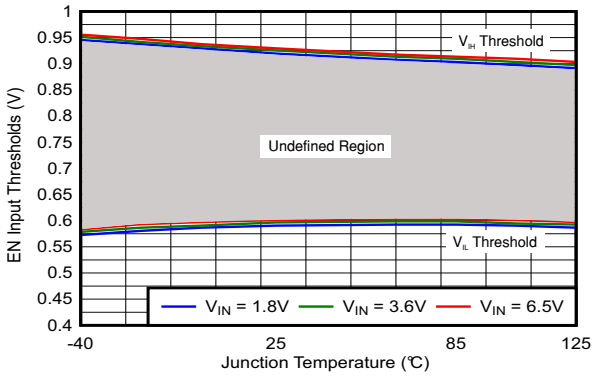



**图 8. EN Input Thresholds versus Temperature**

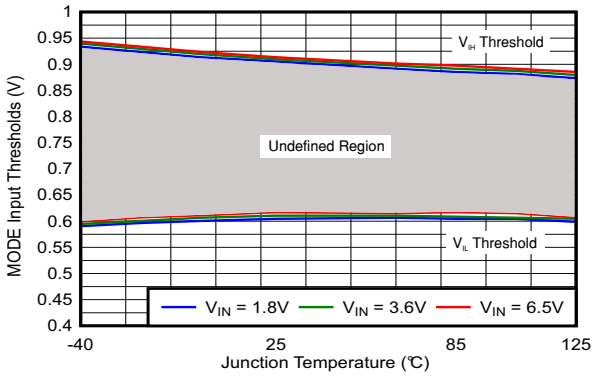



**图 9. MODE Input Thresholds versus Temperature**

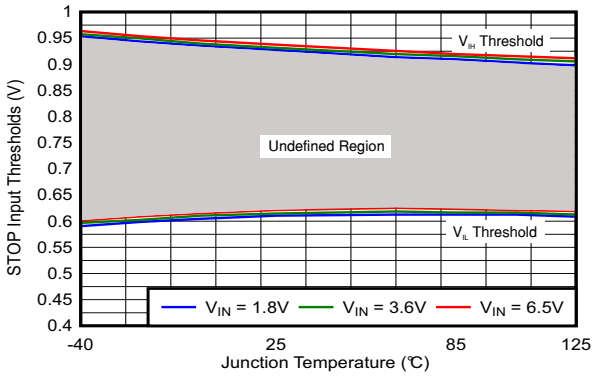



**图 10. STOP Input Thresholds versus Temperature**

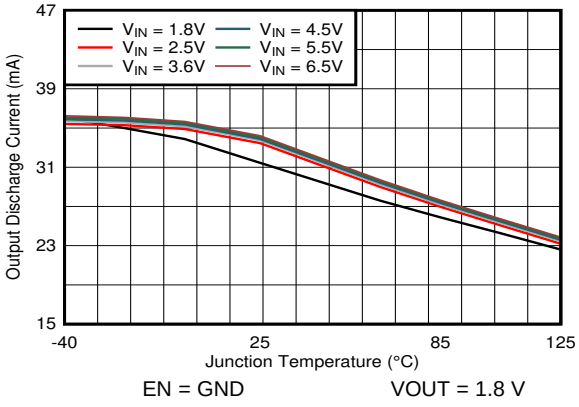



**图 11. Output Discharge Current versus Temperature**

# 8 Detailed Description

## 8.1 Overview

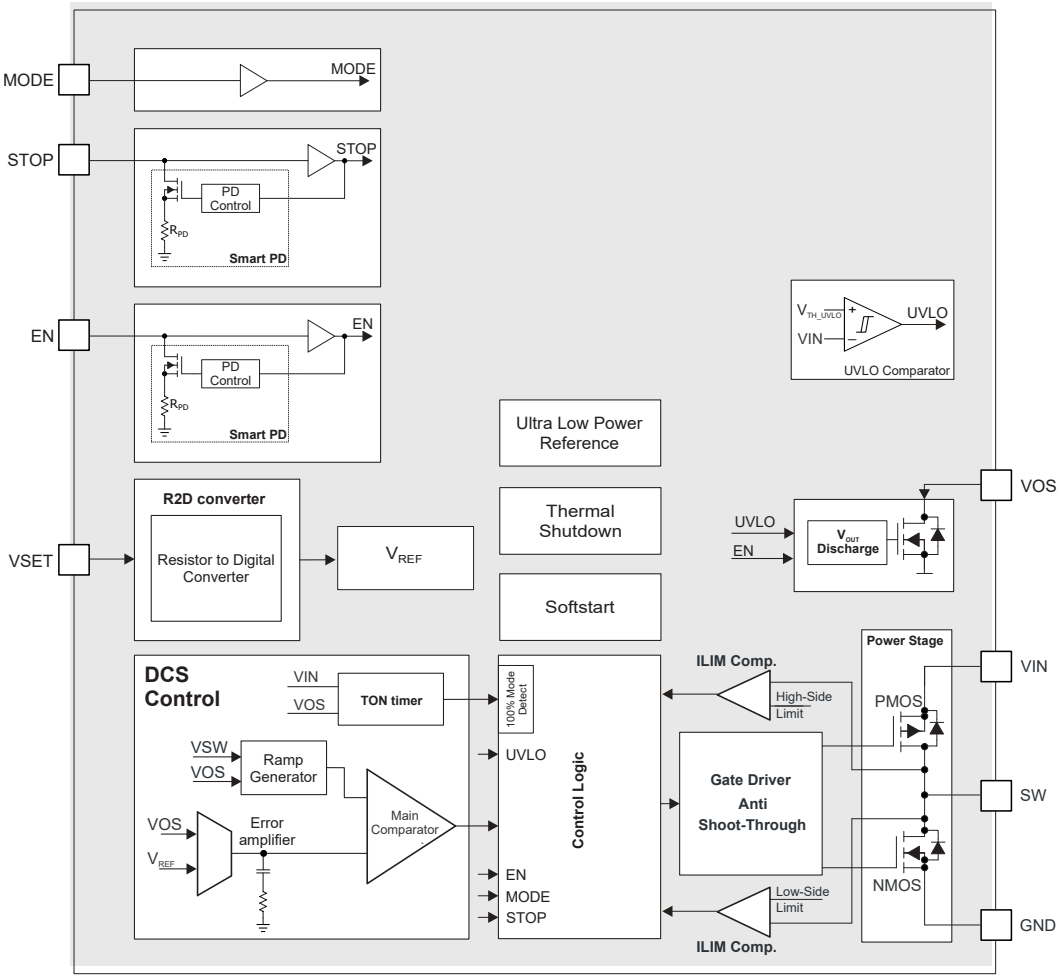
The TPS6284x is a synchronous step-down converter with ultra-low quiescent current consumption. Using TI's DCS-Control topology, the device extends the high efficiency operation area down to micro amperes of load current during Power-Save Mode Operation. Depending on the output voltage, the device consumes quiescent current from both the input and output to reduce the overall input current consumption to 60 nA typical.

DCS-Control™ (Direct Control with Seamless Transition into Power-Save Mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode controls. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM modes. It includes a AC loop which senses the output voltage (VOS pin) and directly feeds this information into a fast comparator stage.

The device operates with a nominal switching frequency of 1.8 MHz. An additional voltage feedback loop is used to achieve accurate DC load regulation. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

In Power-Save Mode, the switching frequency varies linearly with the load current. Since DCS-Control supports both operating modes, the transition from PWM to PFM is seamless with minimum output voltage ripple. The TPS6284x offers both, excellent DC voltage and superior load transient regulation, combined with low output voltage ripple thereby minimizing interferences with Radio Frequency circuits.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Smart Enable and Shutdown

To avoid a floating input, an internal 450-kΩ resistor pulls the EN pin to GND. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven low safely. The device is in shutdown mode when the EN input is logic low.

The device turns on with a logic high EN signal. An internal control circuit disconnects the EN pin pulldown resistor once the device has finished soft start and the output voltage is in regulation. With the EN pin set low, the device enters shutdown mode and the pulldown resistor is activated again.

### 8.3.2 Soft Start

To protect the battery and system from excessive inrush current, the device features a soft start of the output voltage.

Once the device has been enabled, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time ($t_{STARTUP\_DELAY}$). Once this delay expires, the device enters soft start, starts switching, and ramps up the output voltage.

The device operates with a reduced switch current limit ($I_{LIMF\_SS}$) throughout the entire soft-start phase ($t_{SS}$). The switch current limit is increased to its nominal value ($I_{LIMF}$) once the output voltage has reached its nominal value or the reduced current limit soft-start time ($t_{SS\_ILIMF}$) has expired, whichever occurs first. The soft-start phase ($t_{SS}$) can last up to approximately 700 µs. 图 12 shows the start-up procedure.

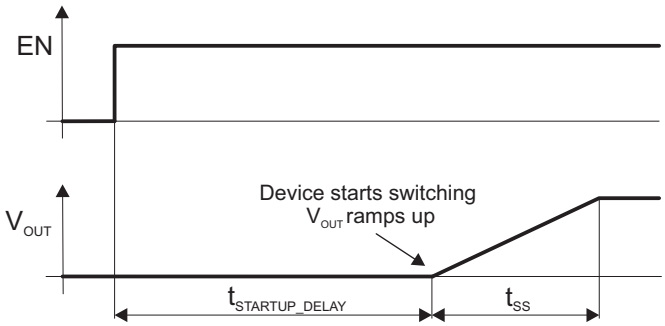



**图 12. Device Start-up**

### 8.3.3 Mode Selection: Power-Save Mode (PFM/PWM) or Forced PWM Operation (FPWM)

Connecting the MODE input to GND enables the automatic PWM and power-save mode operation. The converter operates in PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in PWM mode even at light load currents, allowing lower ripple compared to PFM mode switching. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements. The MODE pin must be terminated.

This pin is not available in the YBG package, where the device automatically transitions between power-save and PWM modes.

### 8.3.4 Output Voltage Selection (VSET)

The output voltage is set with a single external resistor connected between the VSET pin and GND. Once the device has been enabled and the control logic as well as the reference system are powered up, an R2D (resistor to digital) conversion is started to detect the value of the external $R_{SET}$ resistor. A pre-defined fixed output voltage is set based on the $R_{SET}$ value. The output voltage is set once during the start-up delay phase of the device.

## Feature Description (接下页)

Once the output voltage is set, the R2D converter is turned off to avoid current flowing through $R_{SET}$. Care must be taken that no parasitic current, capacitance, or both greater than 100 pF is present between the VSET and GND pins. This can cause false $R_{SET}$ readings and a faulty output voltage to be set. The R2D converter is designed to operate with resistor values out of E96 series. 表 1 shows the allowed $R_{SET}$ values.

**表 1. Output Voltage Setting, $R_{SET}$ Resistor**

| OUTPUT VOLTAGE SETTING $V_{OUT}$ [V] | | | VSET RESISTANCE TO GND - E96 VALUES [Ω] | | |
|---|---|---|---|---|---|
| TPS62841YBG<br>TPS62841DLC<br>TPS62841DGR | TPS62840YBG<br>TPS62840DLC | TPS62842DGR | MIN | NOM | MAX |
| 0.8 | 1.8 | 1.8 | 0 | GND | 0.01 k |
| 0.85 | 1.9 | 2.0 | 0.87 k | 0.909 k | 0.95 k |
| 0.9 | 2.0 | 2.2 | 1.67 k | 1.74 k | 1.81 k |
| 0.95 | 2.1 | 2.4 | 2.76 k | 2.87 k | 2.98 k |
| 1.0 | 2.2 | 2.5 | 4.15 k | 4.32 k | 4.49 k |
| 1.05 | 2.3 | 2.6 | 5.80 k | 6.04 k | 6.28 k |
| 1.1 | 2.4 | 2.7 | 8.11 k | 8.45 k | 8.79 k |
| 1.15 | 2.5 | 2.8 | 11.04 k | 11.5 k | 11.96 k |
| 1.2 | 2.6 | 2.9 | 15.17 k | 15.8 k | 16.43 k |
| 1.25 | 2.7 | 3.0 | 20.64 k | 21.5 k | 22.36 k |
| 1.3 | 2.8 | 3.1 | 27.55 k | 28.7 k | 29.85 k |
| 1.35 | 2.9 | 3.2 | 36.77 k | 38.3 k | 39.83 k |
| 1.4 | 3.0 | 3.3 | 50.21 k | 52.3 k | 54.39 k |
| 1.45 | 3.1 | 3.4 | 68.64 k | 71.5 k | 74.36 k |
| 1.5 | 3.2 | 3.49 | 97.92 k | 102 k | 106.08 k |
| 1.55 | 3.3 | 3.6 | 256.32 k | 267 k | 277.68 k |

The output voltage of the TPS62849 is internally set to 3.4 V. Connect VSET directly to GND for this device.

### 8.3.5 Undervoltage Lockout UVLO

To avoid mis-operation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input below the threshold $V_{TH\_UVLO–}$ with falling $V_{IN}$. The device starts at an input voltage higher than the threshold $V_{TH\_UVLO+}$ with rising $V_{IN}$.

When the device resumes operation from an undervoltage lockout condition, it behaves like being enabled. This means the internal control logic is powered up, the external $R_{SET}$ resistor is read out and a soft-start sequence is initiated.

### 8.3.6 Switch Current Limit / Short Circuit Protection

The TPS6284x integrates a current limit on the high-side as well as on the low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle-by-cycle. If the high-side MOSFET current limit ($I_{LIMF}$) trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp the inductor current down. Once the inductor current decreases below the low-side current limit ($I_{LIMF}$), the low-side MOSFET turns off and the high-side MOSFET turns on again.

During soft start, the current limit is reduced to $I_{LIMF\_SS}$. After soft start has finished, the current limit value increases to the normal value $I_{LIMF}$.

Due to internal propagation delay, the actual inductor current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{I\_LIM\_DELAY} \quad (1)$$

where

- $I_{LIMF}$ is the static current limit, specified in *Electrical Characteristics*
- L is the inductance
- $V_L$ is the voltage across the inductor ($V_{IN}$ - $V_{OUT}$)
- $t_{I\_LIM\_DELAY}$ is the internal propagation delay

In forced PWM mode, a negative current limit ($I_{LIMN}$) is enabled to prevent excessive current flowing backwards to the input. When the inductor current reaches $I_{LIMN}$, the low-side MOSFET turns off and the high-side MOSFET turns on and kept on until TON time expires.

### 8.3.7 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined ramp-down of the output voltage when the device is disabled.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled or if UVLO is entered. It is not active during Thermal Shutdown. The discharge circuit remains active as long as the input voltage is above 0.7 V.

### 8.3.8 Thermal Shutdown

The junction temperature ($T_J$) of the device is monitored by an internal temperature sensor. The device enters thermal shutdown when the junction temperature exceeds the thermal shutdown threshold ($T_{SD}$) of 160°C (typ.). Both the high-side and low-side MOSFETs are turned off. The device resumes its operation when the junction temperature falls below typically 155°C again and begins with a soft-start cycle without reading $R_{SET}$ again. In Power-Save Mode, the thermal shutdown feature is disabled.

### 8.3.9 STOP Mode

The TPS6284x includes the STOP input pin, allowing the user to temporarily stop the switching of the regulator. The STOP pin function does not depend on the setting of the MODE pin. The STOP pin is only present on the DLC package.

When a logic high level is applied to the STOP pin, the regulator is forced to stop switching after the current switching cycle. The application is powered by the charge available in the output capacitor. No switching noise is generated, which can be beneficial in noise-sensitive sampled applications.

An MCU controlling this pin needs to take care to turn the device back on before the output voltage reaches a system critical level. Should this not happen, the output voltage is clamped to about 0.5 V below the set output voltage. In STOP mode, the device consumes typically 70 µA operating quiescent current from the input supply.

When a logic low level is applied to the STOP pin, the regulator immediately resumes switching operation without a start-up delay or soft start. To avoid a floating input, an internal 450-kΩ resistor pulls the STOP pin to GND. A control circuit disconnects the pulldown resistor at the STOP pin once a high level has been detected (similar to the EN pin).

## 8.4 Device Functional Modes

### 8.4.1 Power-Save Mode Operation

The DCS-Control topology supports Power-Save Mode operation. At light loads, the device operates in PFM (Pulse Frequency Modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 60 nA. This low quiescent current consumption is achieved by an ultra-low power reference, an integrated high-impedance feedback divider network, and an optimized Power-Save Mode operation. To achieve a stable switching frequency in steady state operation, the on-time is calculated as in 公式 2.

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 556\text{ns} \tag{2}$$

In PFM Mode, the switching frequency varies linearly with the load current and is calculated in 公式 3. At medium and high load conditions, the device enters automatically PWM (Pulse Width Modulation) mode and operates in continuous conduction mode with a nominal switching frequency ($f_{sw}$). The switching frequency in PWM mode is controlled and depends on $V_{IN}$ and $V_{OUT}$. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

$$f_{PFM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \frac{V_{IN}}{V_{OUT}} \left[ \frac{V_{IN} - V_{OUT}}{L} \right]} \tag{3}$$

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to ultra-light loads. Since DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM modes is seamless with minimum output voltage ripple.

### 8.4.2 Forced PWM Mode Operation

With a high level on the MODE input, the device enters forced PWM Mode and operates with a high switching frequency over the entire load range, even at very light loads. This reduces or eliminates interference with RF and noise-sensitive circuits, but reduces efficiency at light loads. The MODE pin can be changed during operation and must be terminated.

### 8.4.3 100% Mode Operation

In PWM mode, the duty-cycle of a buck converter is given as $D = V_{OUT}/V_{IN}$. The duty-cycle increases as the input voltage comes closer to the output voltage. Once the input voltage decreases to near 100% duty cycle, the output voltage set point is increased by +30 mV. As the input voltage decreases further, the device enters 100% duty-cycle mode and keeps the high-side MOSFET on continuously. The output ($V_{OUT}$) is connected to the input ($V_{IN}$) through the inductor and the internal high-side MOSFET. The minimum input voltage to maintain a given output voltage depends on the load current and is calculated as:

$V_{IN}min = V_{OUT} + I_{OUT} \times (R_{DS(on)}max + R_L)$

where

- $I_{OUT}$ = output current
- $R_{DS(on)}max$ = maximum P-channel switch $R_{DS(on)}$
- $R_L$ = DC resistance of the inductor

The TPS6284x contains special circuitry to keep an ultra-low $I_Q$ of 120 nA during 100% mode operation.

# 9 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

## 9.2 Typical Application

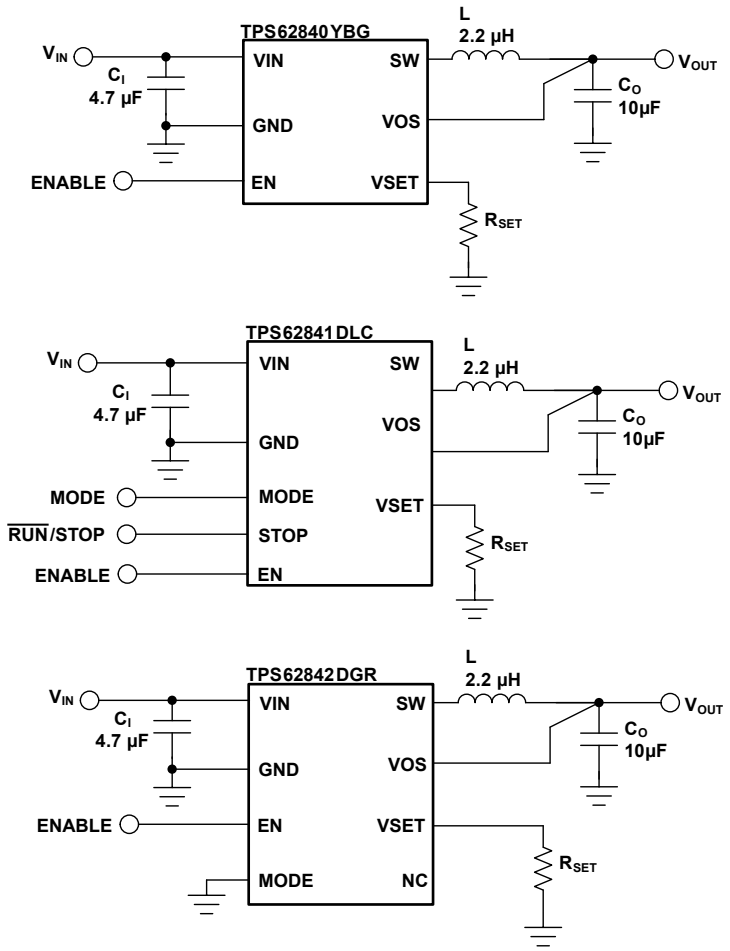



**图 13. TPS6284x Application Circuit**

Additional circuits are shown in the *System Examples*.

### 9.2.1 Design Requirements

表 2 shows the list of components for the application circuit and the characteristic application curves.

## Typical Application (接下页)

**表 2. Components for Application Characteristic Curves**

| REFERENCE | DESCRIPTION | VALUE | SIZE [L x W x T] | MANUFACTURER(1) |
|---|---|---|---|---|
| IC | TPS6284x step-down converter | | | TI |
| $C_I$ | GRM155R61A475MEAAD ceramic capacitor | 4.7 µF / 10 V / X5R | (0402) [1 mm x 0.5 mm x 0.65 mm max.] | muRata |
| $C_O$ | GRM155R60G106ME44D ceramic capacitor | 10 µF / 4 V / X5R | (0402) [1 mm x 0.5 mm x 0.65 mm max.] | muRata |
| L | DFE201612E-2R2M=P2 inductor | 2.2 µH / 116 mΩ DCR | (2016) [2.0 mm x 1.6 mm x 1.2 mm max.] | muRata |
| $R_{SET}$ | Resistor E96 series 1%, TC ±200ppm | See 表 1 | | |

(1) See the *Third-party Products Disclaimer*.

### 9.2.2 Detailed Design Procedure

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 3 outlines possible inductor and capacitor value combinations.

**表 3. Recommended LC Output Filter Combinations**

| INDUCTOR VALUE [µH](1) | OUTPUT CAPACITOR VALUE [µF](2) | |
|---|---|---|
| | 10 µF | 22 µF |
| 2.2 | √(3) | √ |

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -20%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

#### *9.2.2.1 Inductor Selection*

The inductor value affects the peak-to-peak ripple current, PWM-to-PFM transition point, output voltage ripple, and efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current ($\Delta I_L$) decreases with higher inductance and increases with higher $V_{IN}$ or $V_{OUT}$ and can be estimated according to 公式 4.

公式 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current, as calculated with 公式 5. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit, $I_{LIMF}$.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \tag{4}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \tag{5}$$

where

- f is the switching frequency
- L is the inductance
- $\Delta I_L$ is the peak-to-peak inductor ripple current
- $I_{Lmax}$ is the maximum inductor current

表 4 shows a list of possible inductors.

**表 4. List of Possible Inductors(1)**

| INDUCTANCE [µH] | INDUCTOR TYPE | SIZE [L x W x T] | SUPPLIER |
|---|---|---|---|
| 2.2 | DFE201612E | [2.0 mm x 1.6 mm x 1.2 mm max.] | muRata |
| 2.2 | DFE201210S | [2.0 mm x 1.2 mm x 1.0 mm max.] | muRata |

(1) See the *Third-party Products Disclaimer*.

#### 9.2.2.2 Output Capacitor Selection

The DCS-Control scheme of the TPS62840 allows the use of tiny ceramic capacitors. Ceramic capacitors with low-ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric.

At light load currents, the converter operates in Power-Save Mode and the output voltage ripple is dependent on the output capacitor value. Larger output capacitors reduce the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

**表 5. List of Possible Capacitors(1)**

| CAPACITOR VALUE [µF] | CAPACITOR TYPE | SIZE IMPERIAL (METRIC) | SIZE [L x W x T] | SUPPLIER |
|---|---|---|---|---|
| 10 | GRM155R60G106ME44D | 0402 (1005) | [1mm x 0.5mm x 0.65mm max.] | muRata |

(1) See the *Third-party Products Disclaimer*.

#### 9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications, a 4.7-µF input capacitor is sufficient.

When operating from a high impedance source, a larger input buffer capacitor is recommended to avoid voltage drops during start-up and load transients.

The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current. 表 6 shows a selection of input and output capacitors.

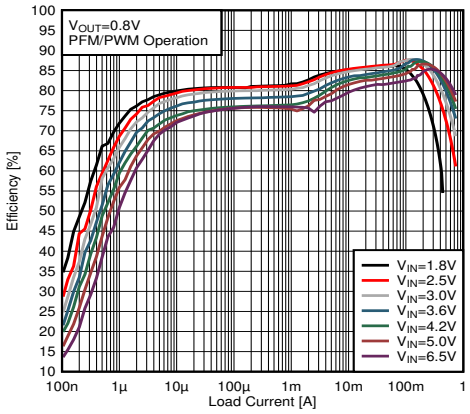
**表 6. List of Possible Capacitors(1)**

| CAPACITOR VALUE [µF] | CAPACITOR TYPE | SIZE IMPERIAL (METRIC) | SIZE [L x W x T] | SUPPLIER |
|---|---|---|---|---|
| 4.7 | GRM155R61A475MEAAD | 0402 (1005) | [1mm x 0.5mm x 0.65mm max.] | muRata |
| 4.7 | GRM31CR71H475MA12L | 1206 (3216) | [3.2mm x 1.6mm x 1.8mm max.] | muRata |
| 4.7 | C1608X7S1A475M080AC | 0603 (1608) | [1.6mm x 0.8mm x 1.0mm max.] | TDK |
| 10 | GRM155R60J106ME15D | 0402 (1005) | [1mm x 0.5mm x 0.65mm max.] | muRata |

(1) See the *Third-party Products Disclaimer*.

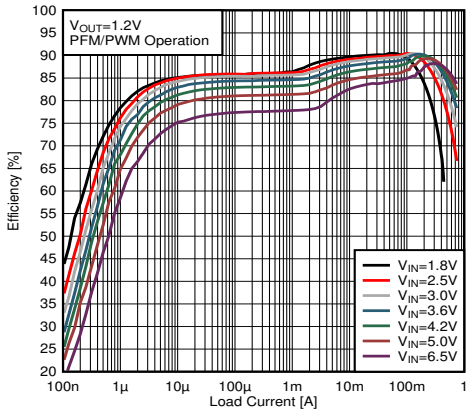
### 9.2.3 Application Curves

The conditions for the following application curves are $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.8 V, MODE = GND, STOP = GND, and the used components listed in 表 2, unless otherwise noted.



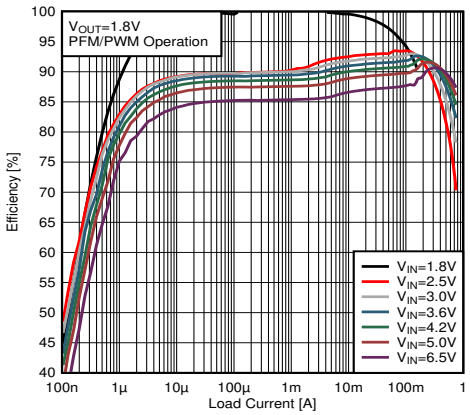

$R_{SET}$ = GND

**图 14. Efficiency Power Save Mode $V_{OUT}$ = 0.8 V**



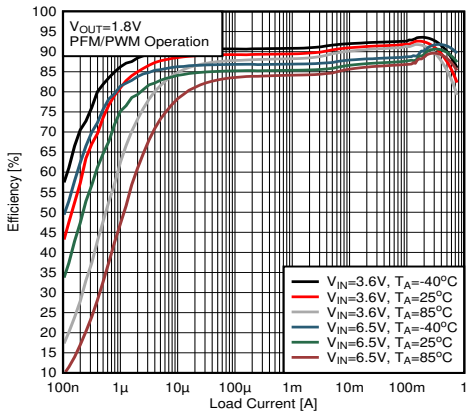

$R_{SET}$ = 15.8 kΩ to GND

**图 15. Efficiency Power Save Mode $V_{OUT}$ = 1.2 V**



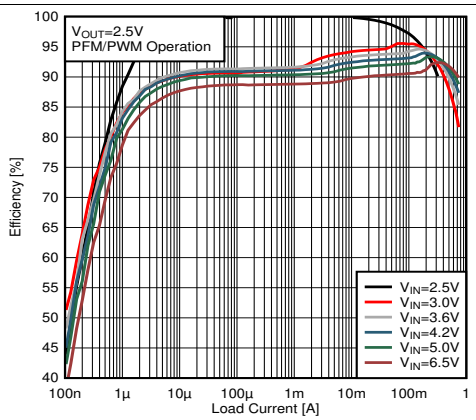

$R_{SET}$ = GND

**图 16. Efficiency Power Save Mode $V_{OUT}$ = 1.8 V**



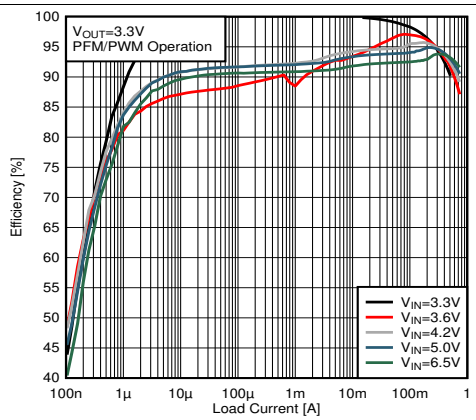

$R_{SET}$ = GND

**图 17. Efficiency Power Save Mode $V_{OUT}$ = 1.8 V**



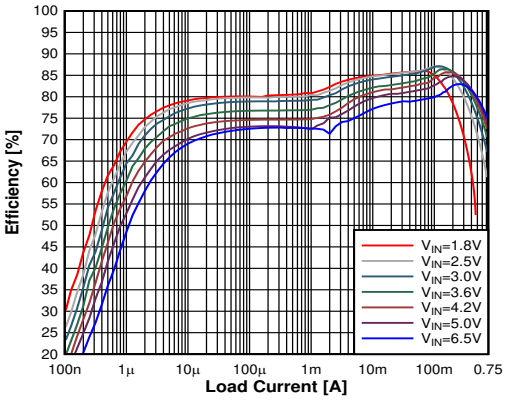

$R_{SET}$ = 11.5 kΩ to GND

**图 18. Efficiency Power Save Mode $V_{OUT}$ = 2.5 V**



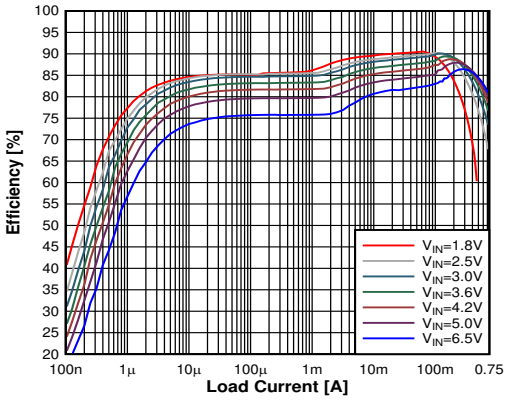

$R_{SET}$ = 267 kΩ to GND

**图 19. Efficiency Power Save Mode $V_{OUT}$ = 3.3 V**



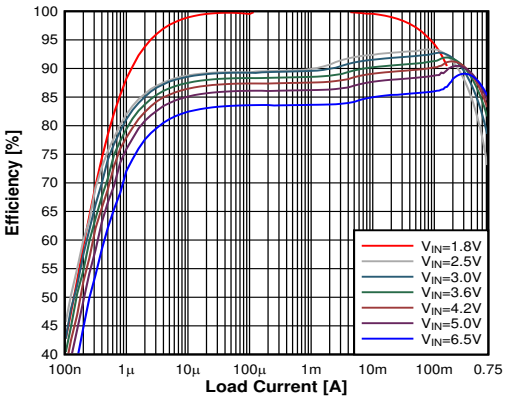

$R_{SET}$ = GND

**图 20. Efficiency Power Save Mode**
**$V_{OUT}$ = 0.8 V for the DGR device**



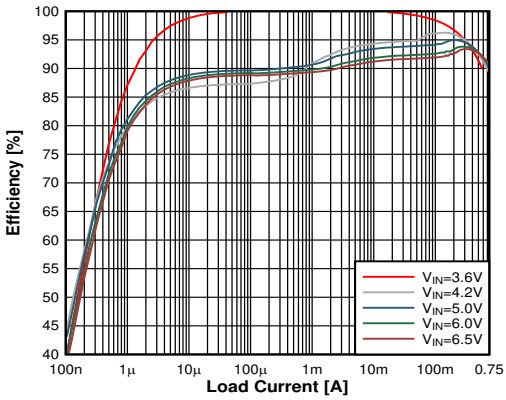

$R_{SET}$ = GND

**图 21. Efficiency Power Save Mode**
**$V_{OUT}$ = 1.2 V for the DGR device**




$R_{SET}$ = GND

**图 22. Efficiency Power Save Mode**
**$V_{OUT}$ = 1.8 V for the DGR device**




$R_{SET}$ = 267 kΩ to GND

**图 23. Efficiency Power Save Mode**
**$V_{OUT}$ = 3.6 V for the DGR device**

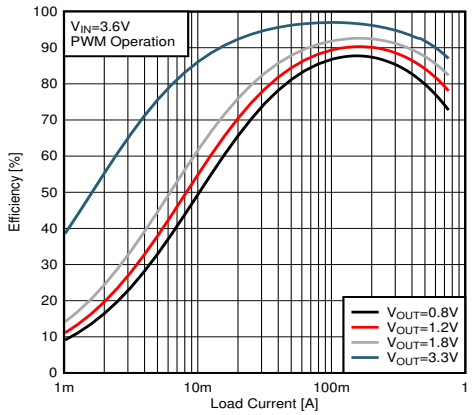
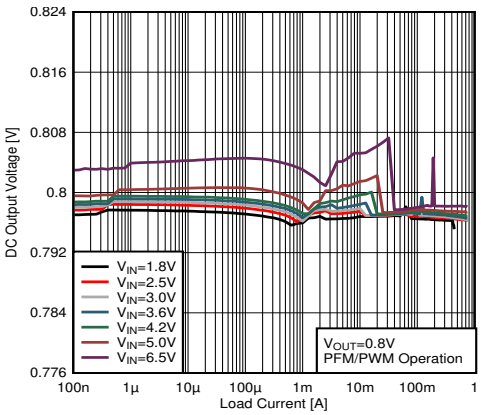
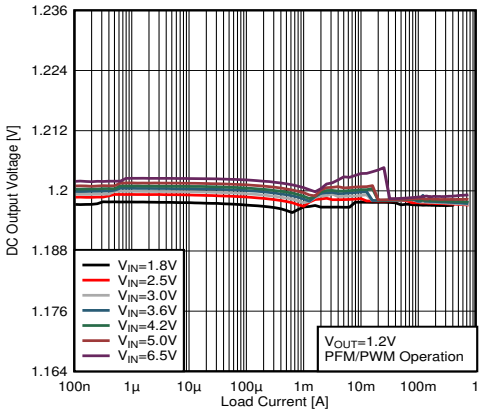



**图 24. Efficiency Forced PWM Mode**
**$V_{OUT}$ = 0.8 V / 1.2 V / 1.8 V / 3.3 V**



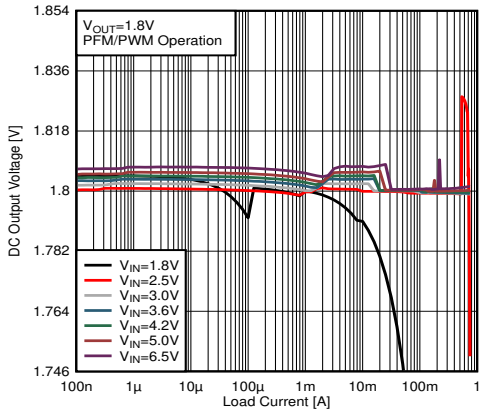

$R_{SET}$ = GND

**图 25. Output Voltage versus Load Current**
**$V_{OUT}$ = 0.8 V**



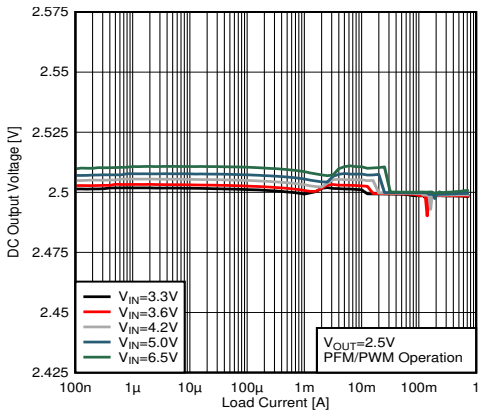

$R_{SET}$ = 15.8k Ω to GND

**图 26. Output Voltage versus Load Current**
**$V_{OUT}$ = 1.2 V**



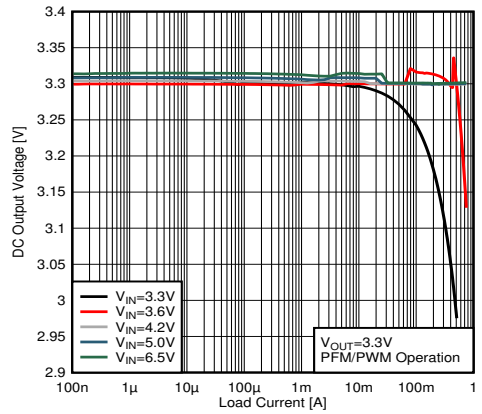

$R_{SET}$ = GND

**图 27. Output Voltage versus Load Current**
**$V_{OUT}$ = 1.8 V**



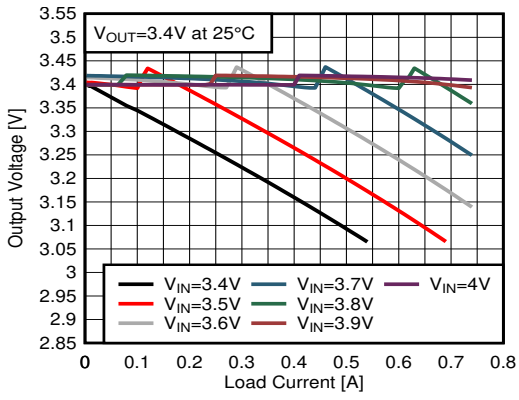

$R_{SET}$ = 11.5 kΩ to GND

**图 28. Output Voltage versus Load Current**
**$V_{OUT}$ = 2.5 V**



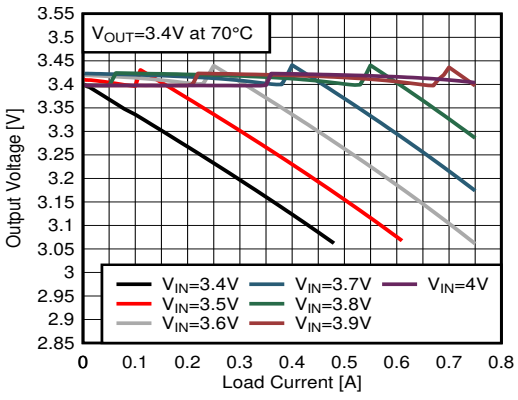

$R_{SET}$ = 267 kΩ to GND

**图 29. Output Voltage versus Load Current**
**$V_{OUT}$ = 3.3 V**




$R_{SET}$ = GND

**图 30. Output Voltage versus Load Current**
**$V_{OUT}$ = 3.4 V**




$R_{SET}$ = GND

**图 31. Output Voltage versus Load Current**
**$V_{OUT}$ = 3.4 V**

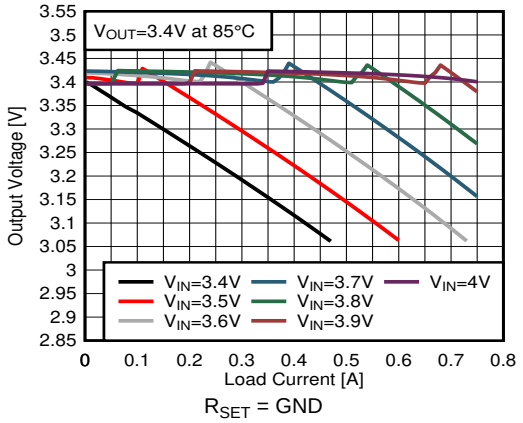



**图 32. Output Voltage versus Load Current**
**$V_{OUT}$ = 3.4 V**

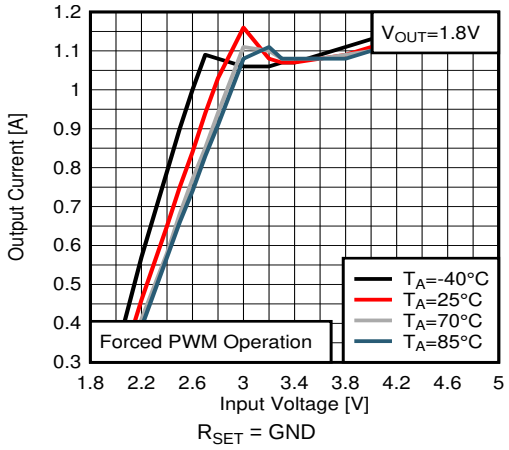



**图 33. Maximum Output Current versus Input Voltage**
**$V_{OUT}$ = 1.8 V**

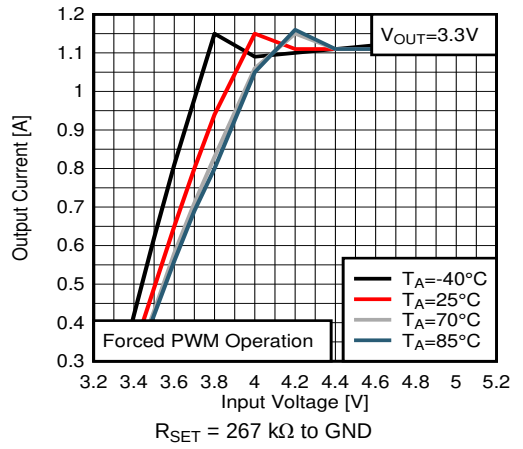



**图 34. Maximum Output Current versus Input Voltage**
**$V_{OUT}$ = 3.3 V**

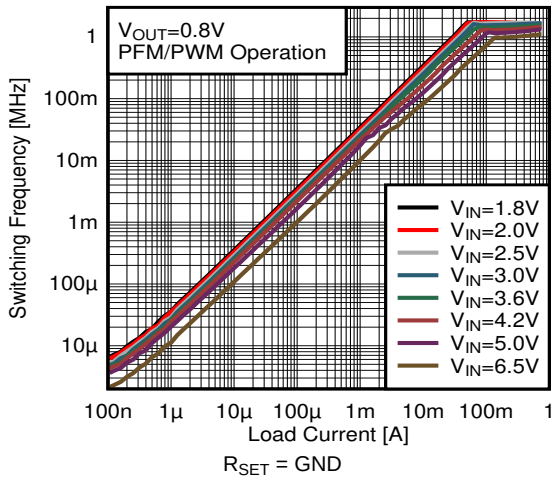



**图 35. Switching Frequency versus Load Current**
**$V_{OUT}$ = 0.8 V**

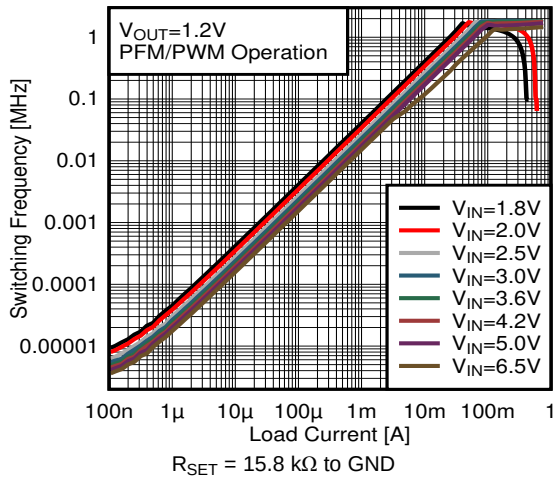



**图 36. Switching Frequency versus Load Current**
**$V_{OUT}$ = 1.2 V**

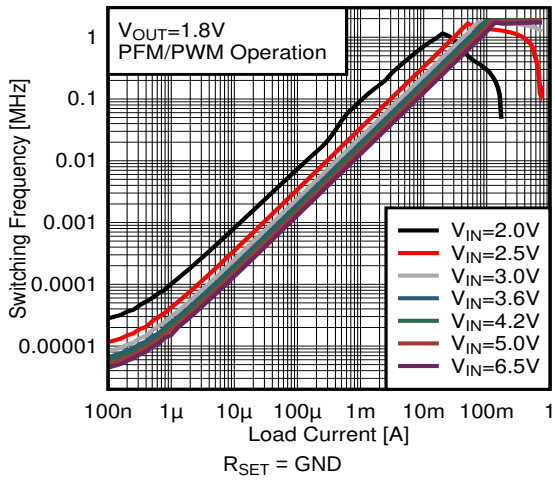
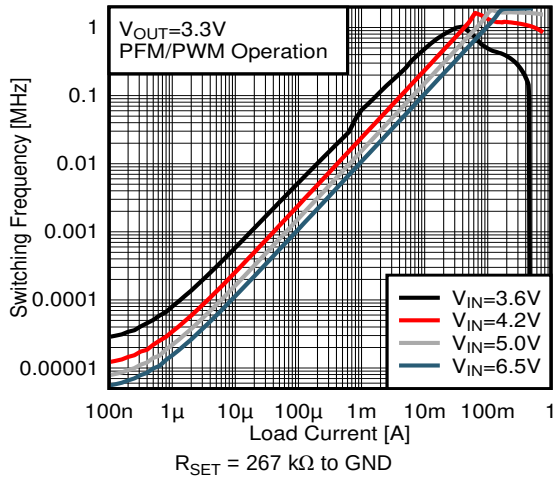
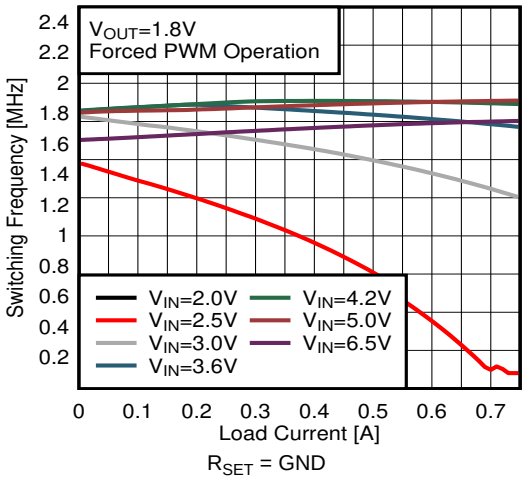



**图 37. Switching Frequency versus Load Current**
**$V_{OUT}$ = 1.8 V**



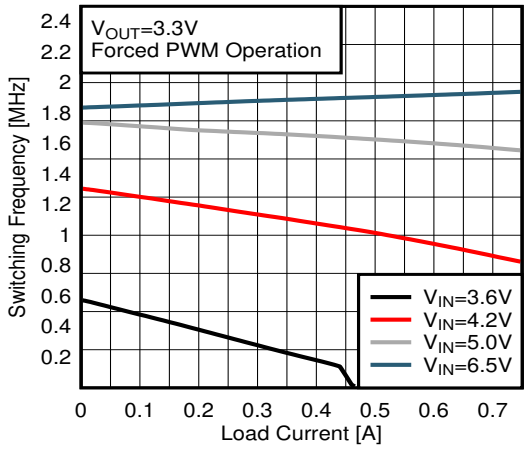

$R_{SET}$ = 267 kΩ to GND

**图 38. Switching Frequency versus Load Current**
**$V_{OUT}$ = 3.3 V**




$R_{SET}$ = GND

**图 39. Switching Frequency versus Load Current**
**$V_{OUT}$ = 1.8 V**




$R_{SET}$ = 267 kΩ to GND

**图 40. Switching Frequency versus Load Current**
**$V_{OUT}$ = 3.3 V**

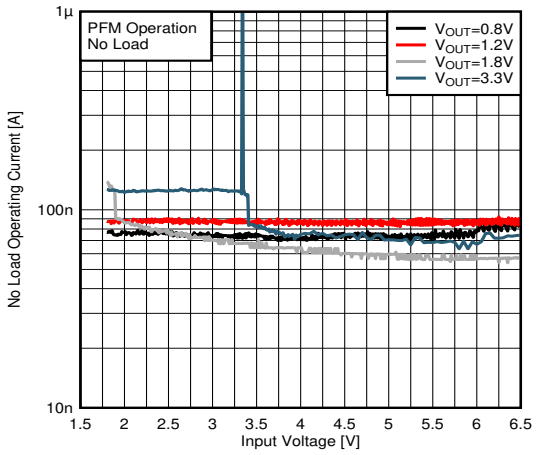



**图 41. No Load Operating Current versus Input Voltage**

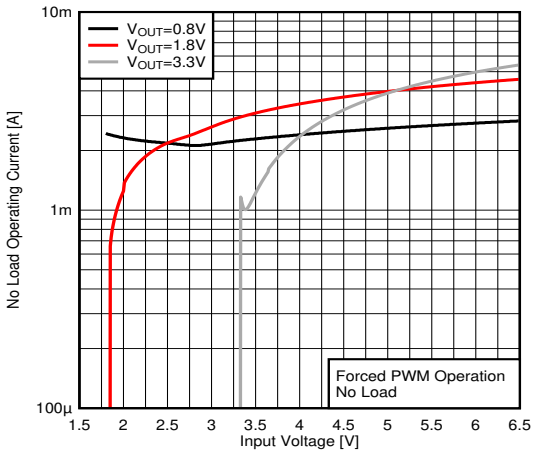
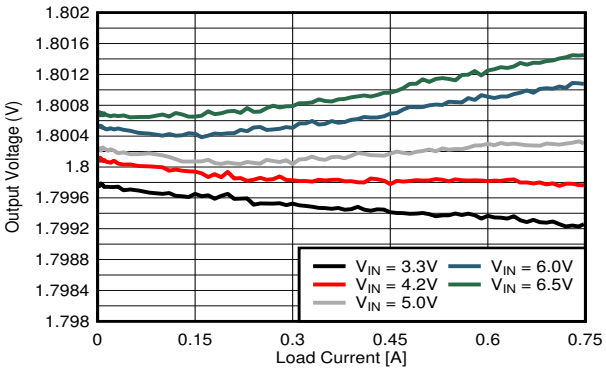
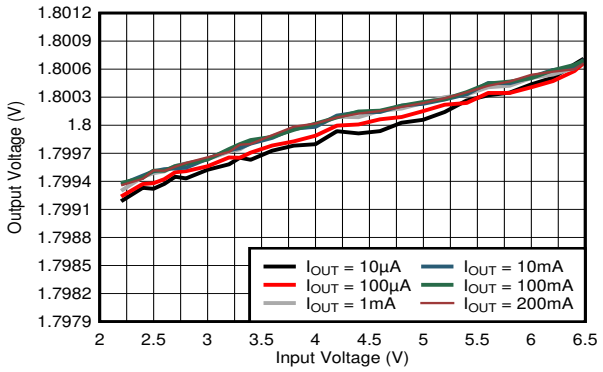



**图 42. No Load Operating Current versus Input Voltage**



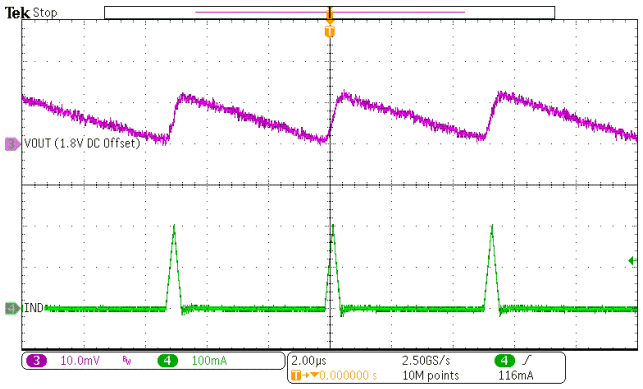

EN = VIN MODE = HIGH

**图 43. Output Voltage Accuracy (Load Regulation)**



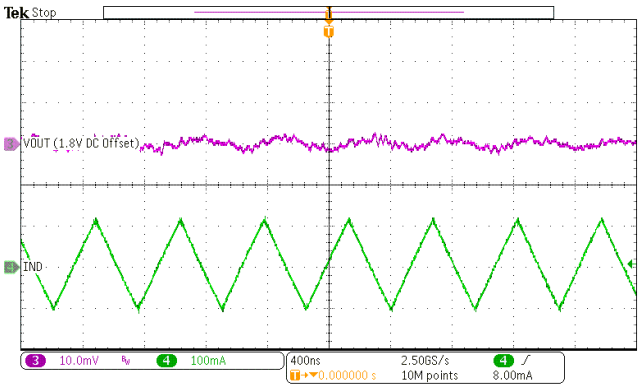

EN = VIN MODE = HIGH

**图 44. Output Voltage Accuracy (Line Regulation)**




$V_{OUT}$ = 1.8 V $I_{OUT}$ = 10 mA

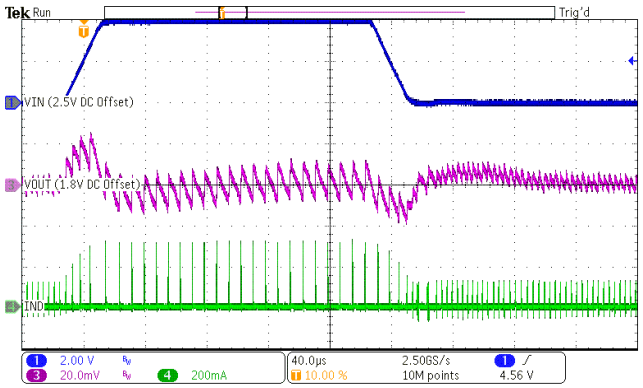
**图 45. Output Voltage Ripple, PFM Operation**




$V_{OUT}$ = 1.8 V
MODE = HIGH

$I_{OUT}$ = 10 mA

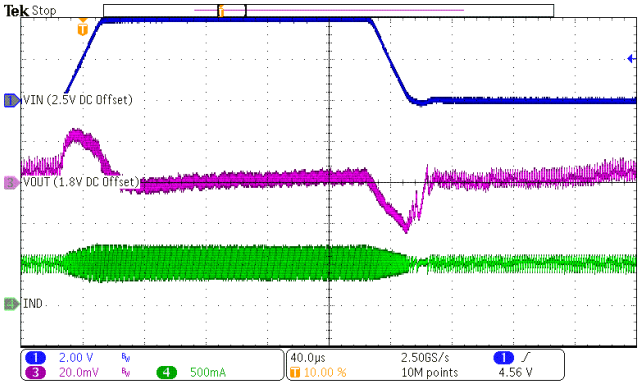
**图 46. Output Voltage Ripple, PWM Operation**




$V_{OUT}$ = 1.8 V
rise/fall time = 20 µs

$V_{IN}$ = 2.5 V to 6.5 V
$I_{OUT}$ = 10 mA

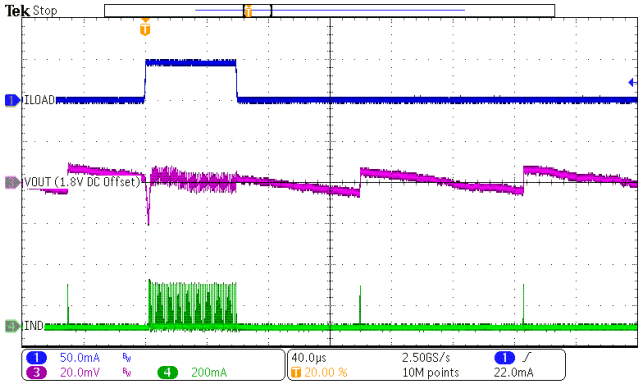
**图 47. Line Transient PFM Mode**




$V_{OUT}$ = 1.8 V
rise/fall time = 20 µs

$V_{IN}$ = 2.5 V to 6.5 V
$I_{OUT}$ = 500 mA

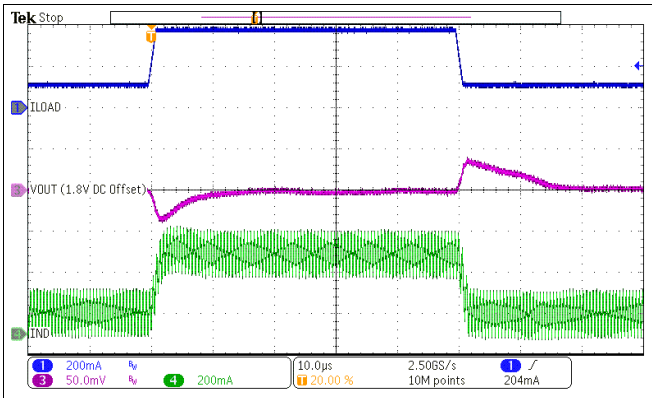
**图 48. Line Transient PWM Mode**




$V_{OUT}$ = 1.8 V
rise/fall time < 1 µs

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 125 µA to 50 mA

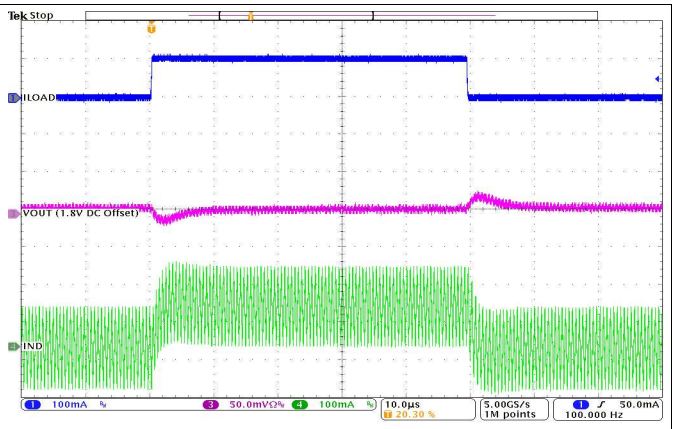
**图 49. Load Transient PFM Mode**




$V_{OUT}$ = 1.8 V
rise/fall time < 1 µs

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 125 mA to 375 mA

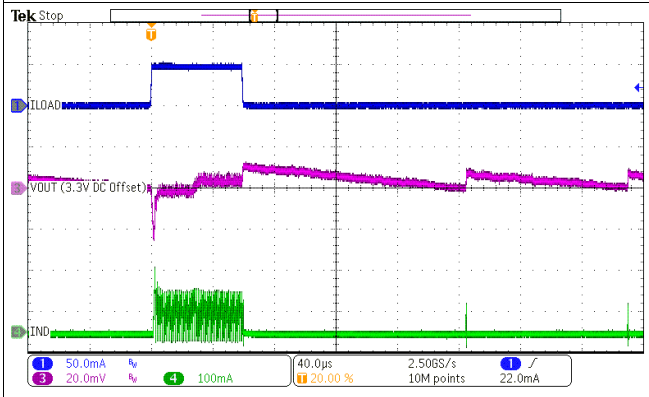
**图 50. Load Transient PFM/PWM Mode**




$V_{OUT}$ = 1.8 V
rise/fall time < 1 µs

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 0 A to 100 mA

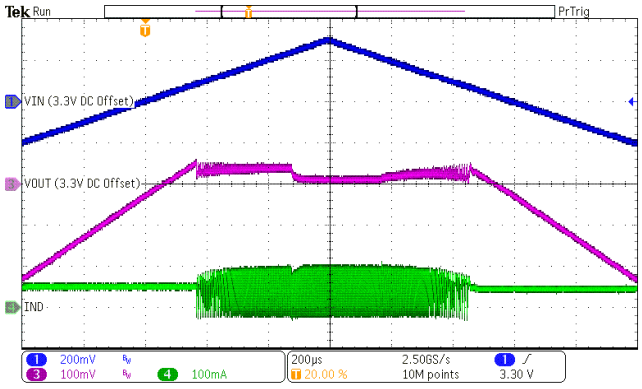
**图 51. Load Transient PWM Mode from No load**




$V_{OUT}$ = 3.3 V
rise/fall time < 1 µs

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 75 µA to 50 mA

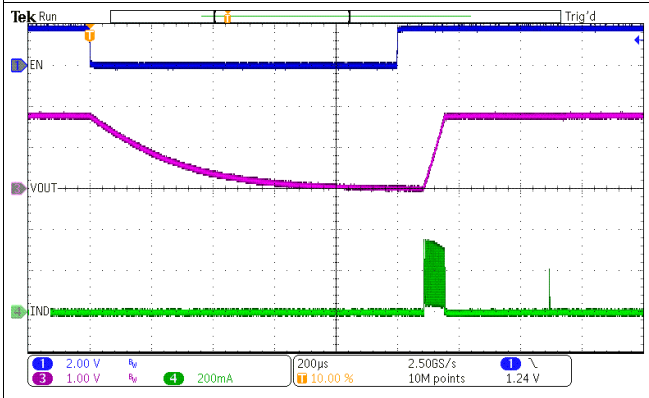
**图 52. Load Transient PFM Mode**




$V_{OUT}$ = 3.3 V

$V_{IN}$ = 3.1 V to 3.6 V
$I_{OUT}$ = 50 mA

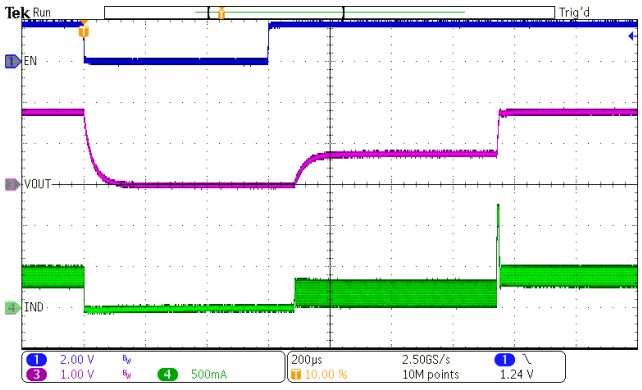
**图 53. 100% Mode Entry/Exit Operation**




$V_{OUT}$ = 1.8 V
Turned on by EN input

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 0 mA

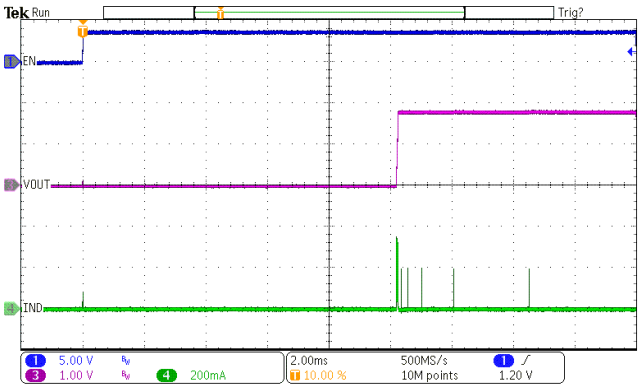
**图 54. Start-up/Shutdown into No Load**




$V_{OUT}$ = 1.8 V
Turned on by EN input

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 400 mA
$R_{LOAD}$ = 4.5 Ω

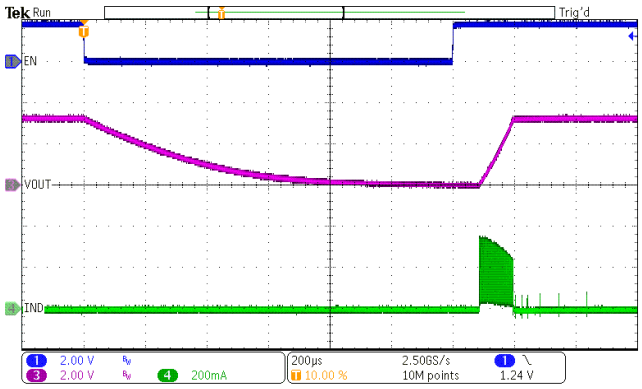
**图 55. Start-up/Shutdown into Load**




$V_{OUT}$ = 1.8 V
$V_{IN}$ rising from 0 V to 3.6 V

EN = $V_{IN}$
$I_{OUT}$ = 0 mA

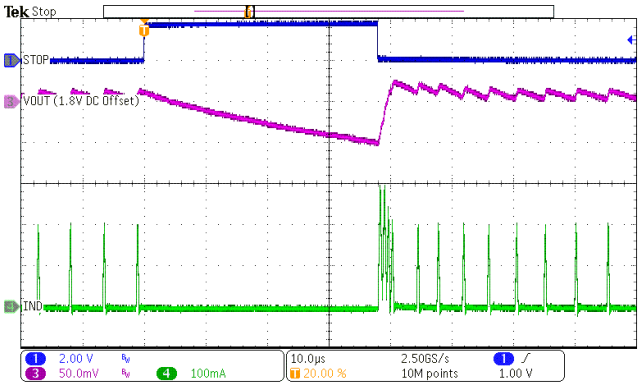
**图 56. Start-up/Shutdown into No Load**




$V_{OUT}$ = 3.3 V
Turned on by EN input

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 0 mA

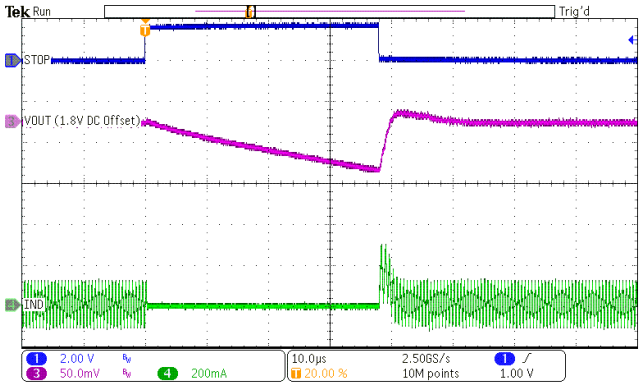
**图 57. Start-up/Shutdown into No Load**




$V_{OUT}$ = 1.8 V
PFM Operation

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 10 mA

**图 58. STOP Mode Operation**




$V_{OUT}$ = 1.8 V
PWM Operation

$V_{IN}$ = 3.6 V
$I_{OUT}$ = 10 mA

**图 59. STOP Mode Operation**

## 9.3 System Example

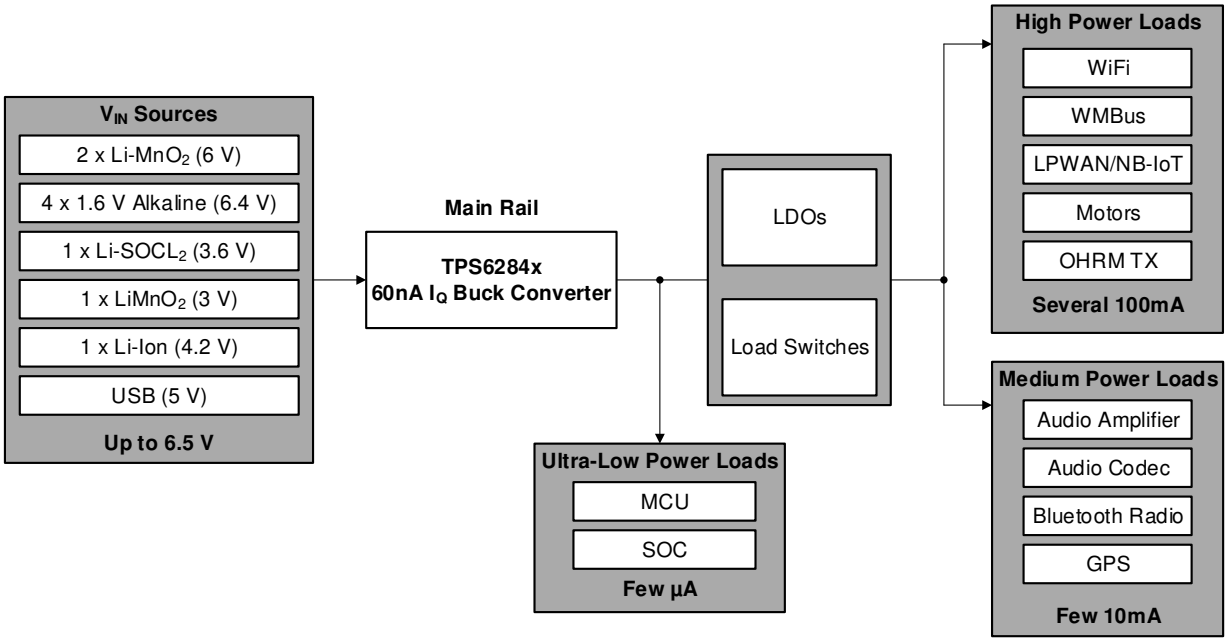



**图 60. The Broad Range of Input Voltage Sources and Various Power Loads that TPS6284x Can Support**

# 10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS62840.

# 11 Layout

## 11.1 Layout Guidelines

The TPS62840 pinout has been optimized to enable a single layer PCB routing of the device and its critical passive components such as $C_{IN}$, $C_{OUT}$, and L.

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor must be placed as close as possible to the VIN and GND pins of the device. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, the SW line) or other noise sources.

## 11.2 Layout Example

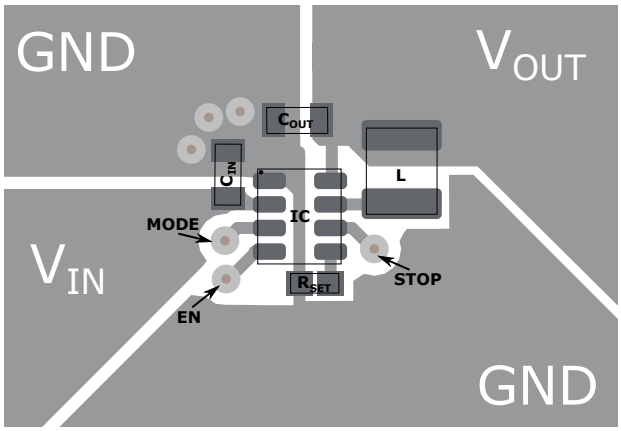



**图 61. Recommended PCB Layout DLC Package**

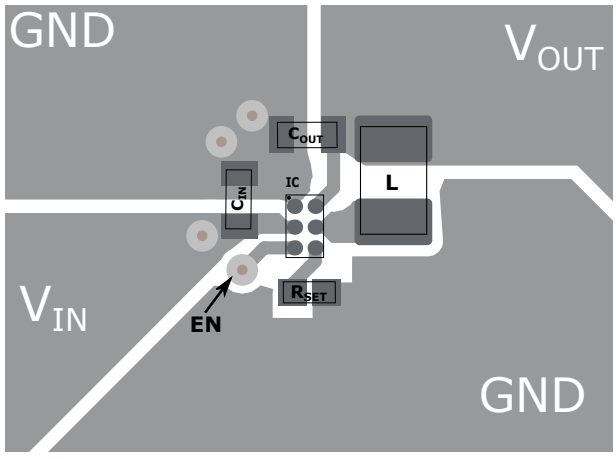



**图 62. Recommended PCB Layout YBG Package**

## Layout Example (接下页)

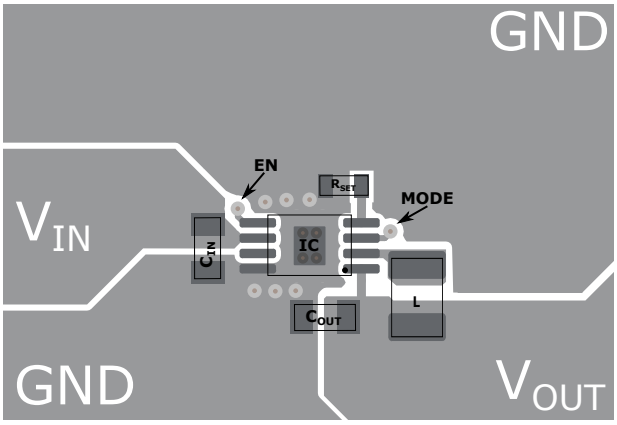



**图 63. Recommended PCB Layout**
**DGR Package**

# 12 器件和文档支持

## 12.1 器件支持

### 12.1.1 第三方产品免责声明

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## 12.2 保障资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62840DLCR | ACTIVE | VSON-HR | DLC | 8 | 3000 | RoHS & Green | Call TI \| NIPDAU | Level-1-260C-UNLIM | -40 to 125 | E5 | Samples |
| TPS62840YBGR | ACTIVE | DSBGA | YBG | 6 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 62840 | Samples |
| TPS62841DGRR | ACTIVE | HVSSOP | DGR | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T841R | Samples |
| TPS62841DLCR | ACTIVE | VSON-HR | DLC | 8 | 3000 | RoHS & Green | Call TI \| NIPDAU | Level-1-260C-UNLIM | -40 to 125 | E9 | Samples |
| TPS62841YBGR | ACTIVE | DSBGA | YBG | 6 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 62841 | Samples |
| TPS62842DGRR | ACTIVE | HVSSOP | DGR | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T842R | Samples |
| TPS62849DLCR | ACTIVE | VSON-HR | DLC | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | FF | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

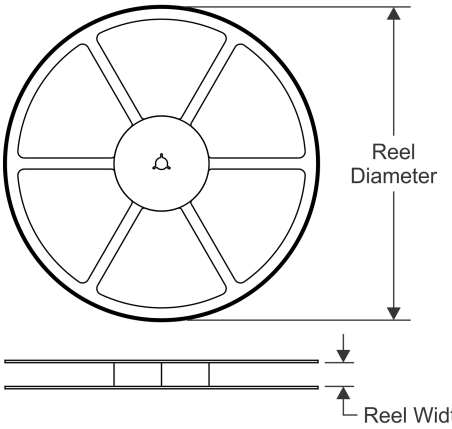
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

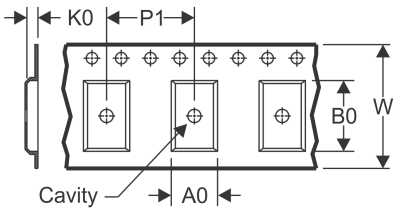
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

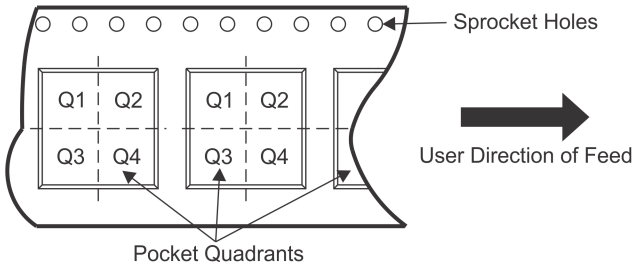



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

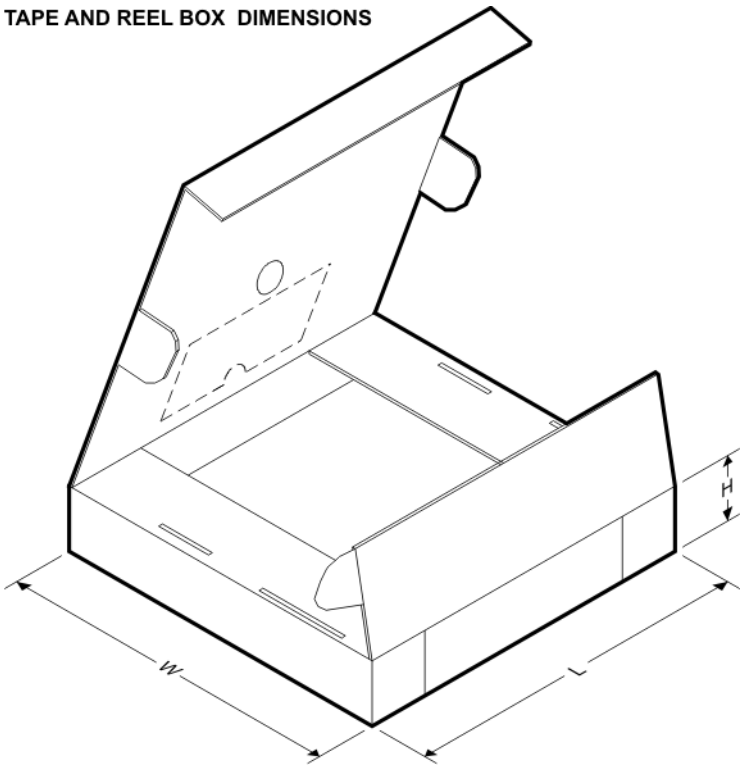
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS62840DLCR | VSON-HR | DLC | 8 | 3000 | 180.0 | 8.4 | 1.8 | 2.25 | 1.15 | 4.0 | 8.0 | Q1 |
| TPS62840YBGR | DSBGA | YBG | 6 | 3000 | 180.0 | 8.4 | 1.14 | 1.64 | 0.59 | 4.0 | 8.0 | Q1 |
| TPS62841DGRR | HVSSOP | DGR | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS62841DLCR | VSON-HR | DLC | 8 | 3000 | 180.0 | 8.4 | 1.8 | 2.25 | 1.15 | 4.0 | 8.0 | Q1 |
| TPS62841YBGR | DSBGA | YBG | 6 | 3000 | 180.0 | 8.4 | 1.14 | 1.64 | 0.59 | 4.0 | 8.0 | Q1 |
| TPS62842DGRR | HVSSOP | DGR | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS62849DLCR | VSON-HR | DLC | 8 | 3000 | 180.0 | 8.4 | 1.8 | 2.25 | 1.15 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



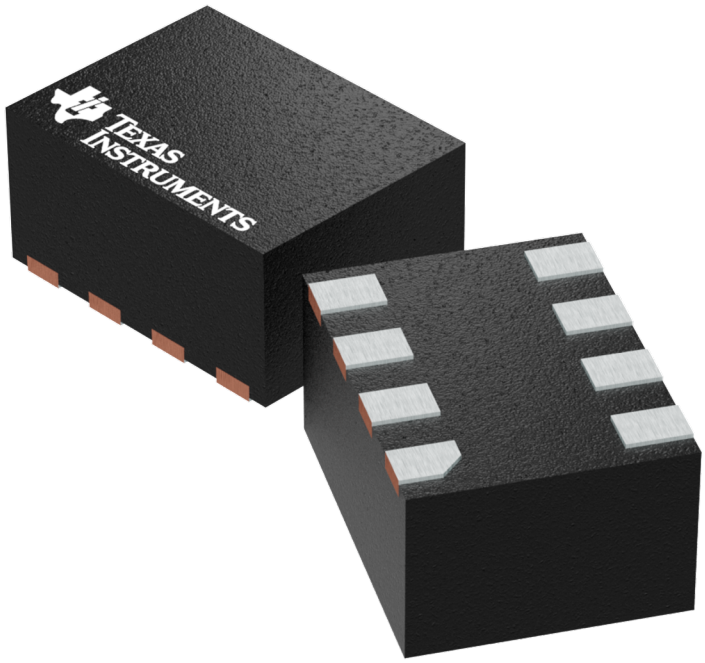

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS62840DLCR | VSON-HR | DLC | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62840YBGR | DSBGA | YBG | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62841DGRR | HVSSOP | DGR | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS62841DLCR | VSON-HR | DLC | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62841YBGR | DSBGA | YBG | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62842DGRR | HVSSOP | DGR | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS62849DLCR | VSON-HR | DLC | 8 | 3000 | 182.0 | 182.0 | 20.0 |

# DLC 8 VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

**2.0 x 1.5 mm, 0.5 mm pitch**



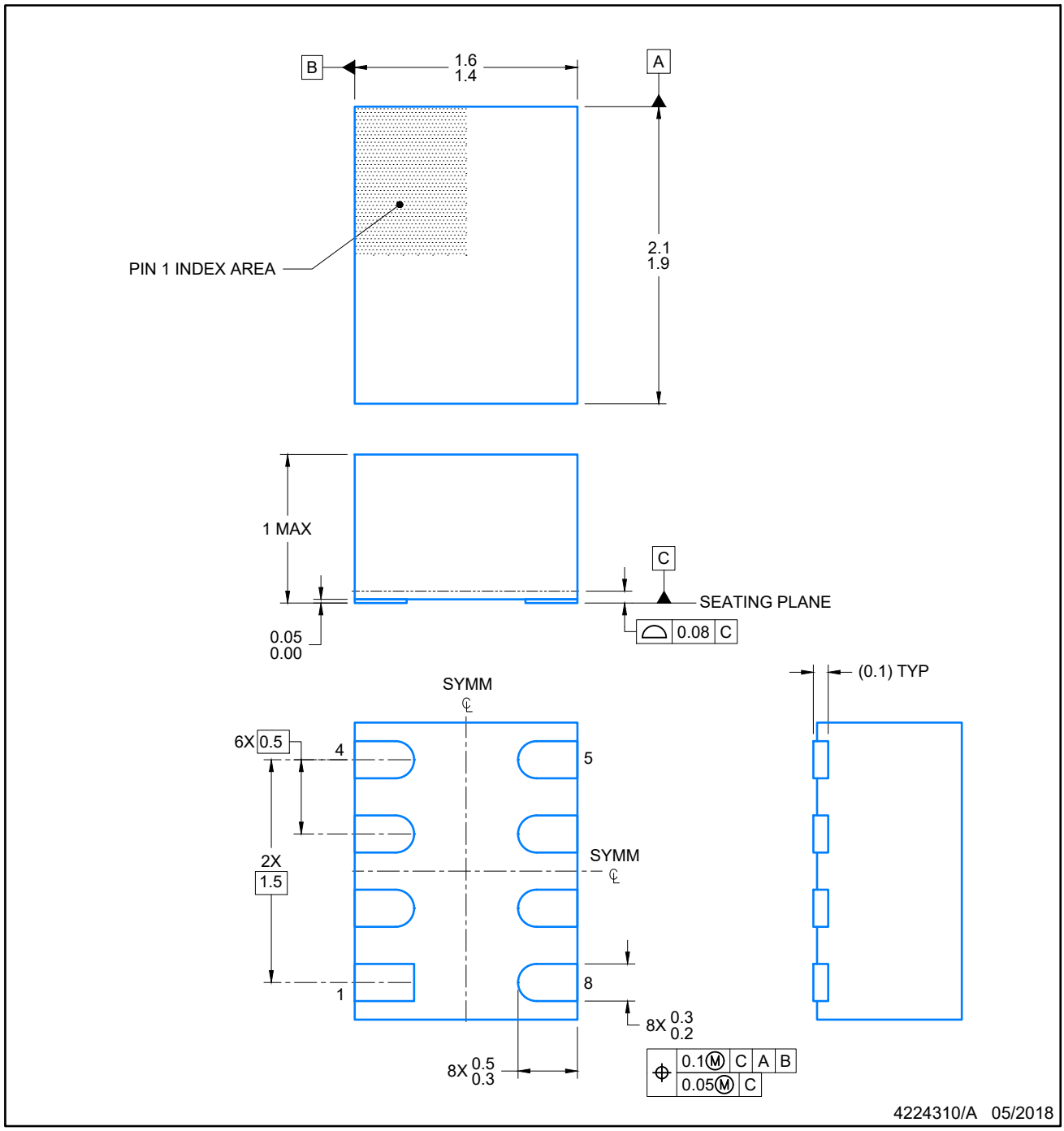

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DLC0008B

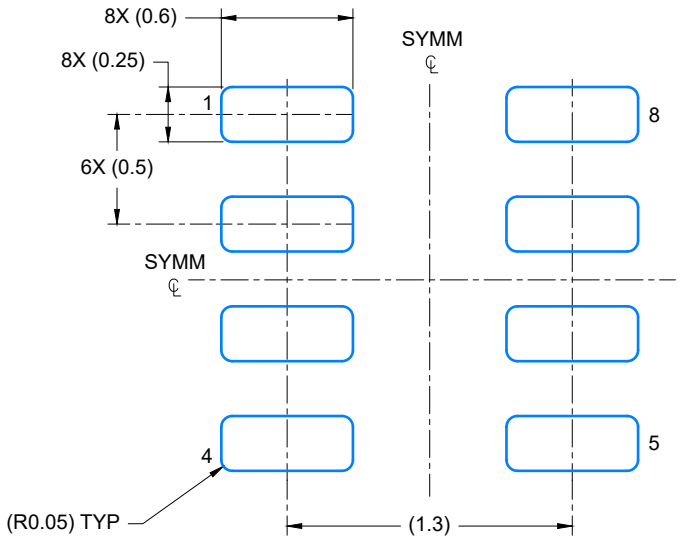
## VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD

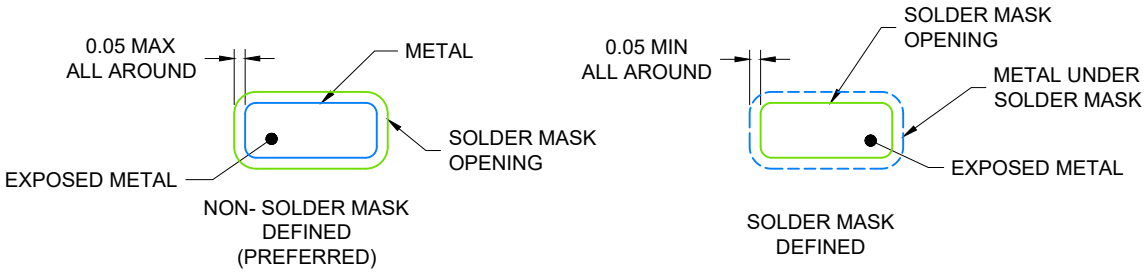



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

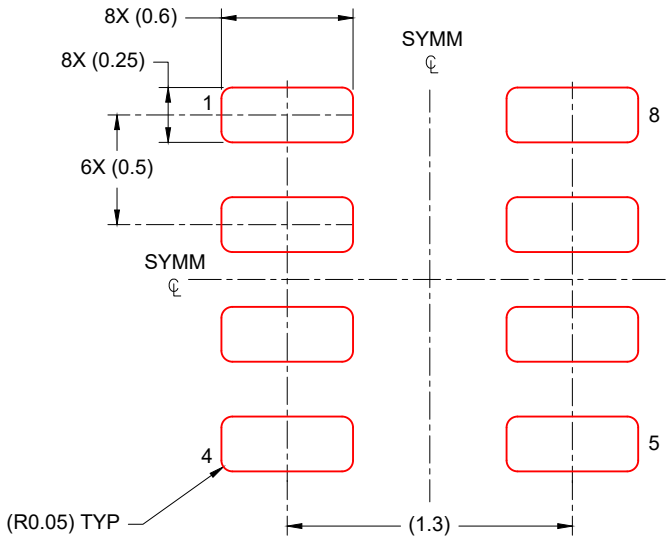



SOLDER MASK DETAILS

4224310/A 05/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224310/A 05/2018

NOTES: (continued)

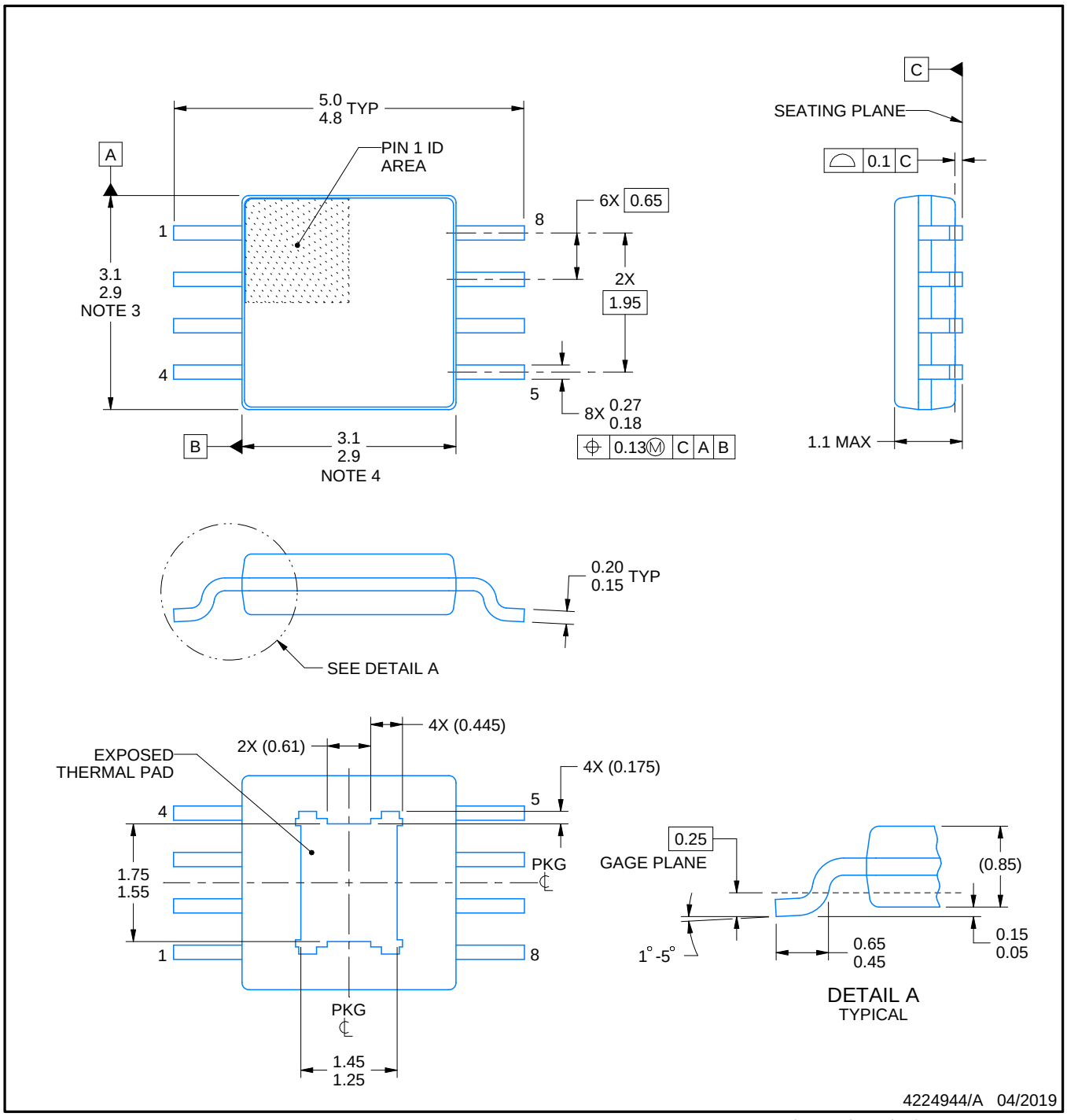
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DGR0008A

## VSSOP PowerPAD™ - 1.1 mm max height

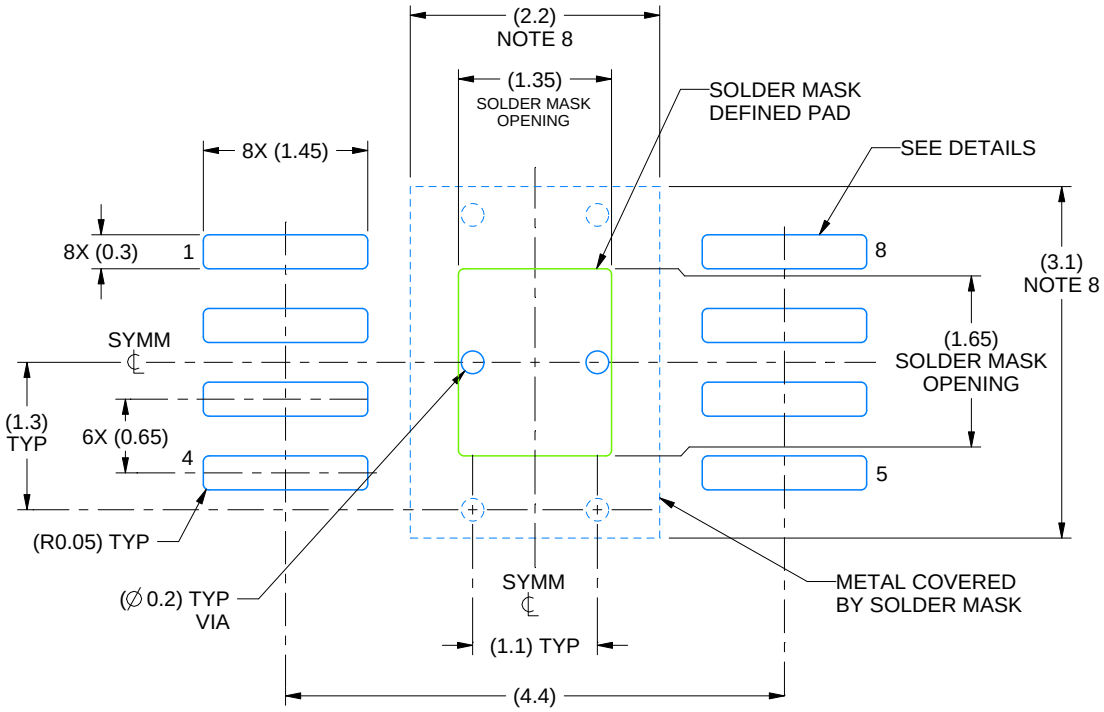
PLASTIC SMALL OUTLINE



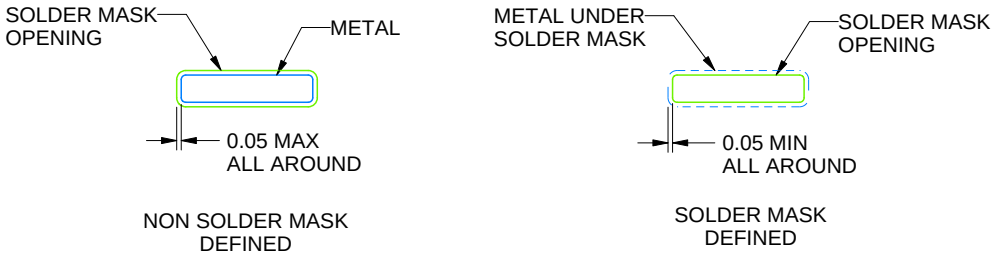

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.3 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

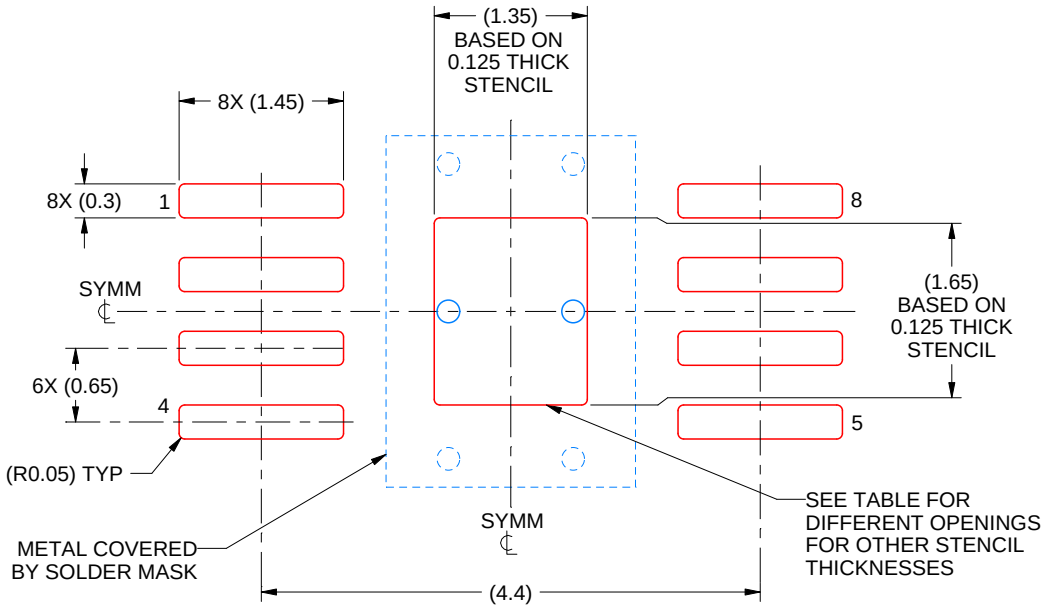



SOLDER MASK DETAILS

4224944/A 04/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.51 X 1.84 |
| 0.125 | 1.35 X 1.65 (SHOWN) |
| 0.150 | 1.23 X 1.51 |
| 0.175 | 1.14 X 1.39 |

4224944/A 04/2019

NOTES: (continued)

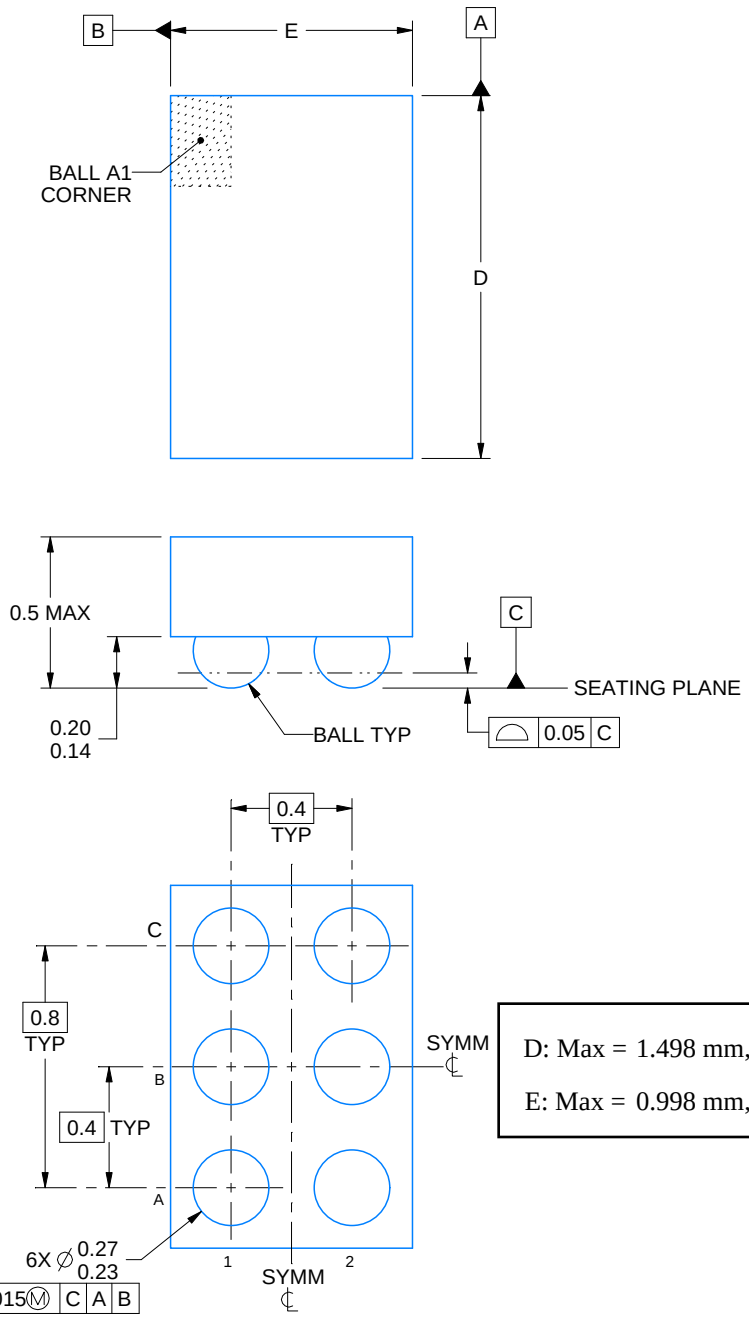
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## YBG0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




4224328/A 05/2018

NOTES:

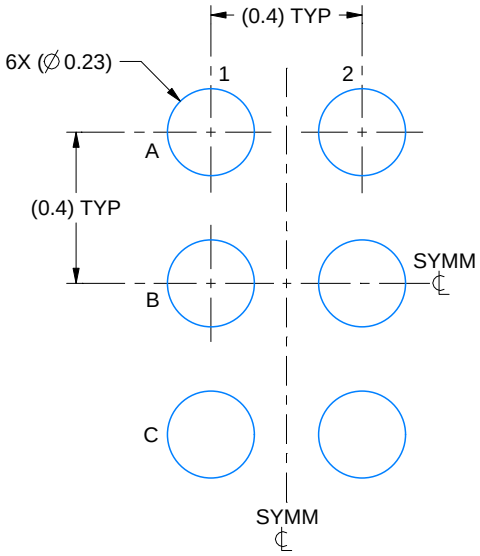
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

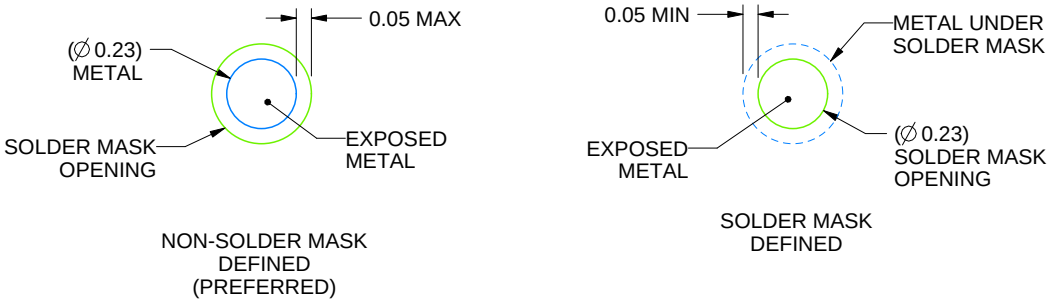
## YBG0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

4224328/A 05/2018

NOTES: (continued)

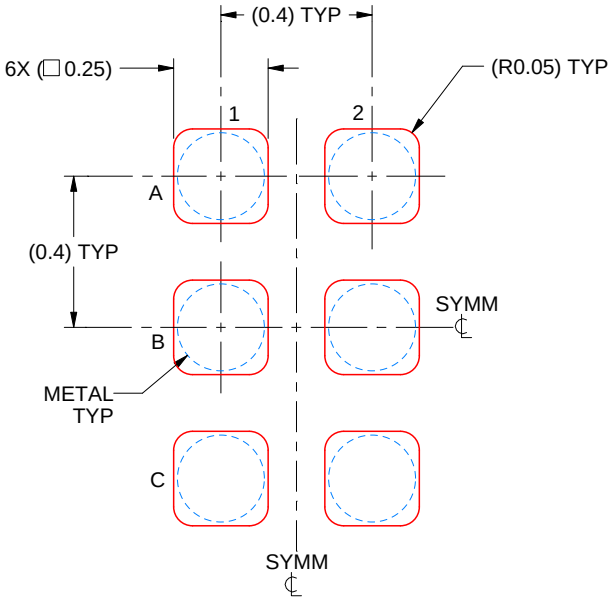
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

# EXAMPLE STENCIL DESIGN

## YBG0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4224328/A 05/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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