

20V N 通道 NexFET™ 功率金属氧化物场效应晶体管 (MOSFET)

 查询样品: **CSD15571Q2**

特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

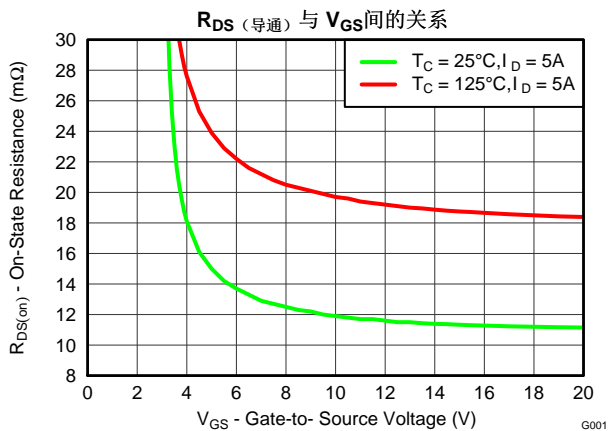
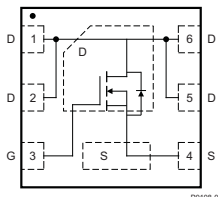
应用范围

- 针对负载开关应用进行了优化
- 存储、平板电脑和手持类器件
- 针对控制场效应晶体管 (FET) 应用进行了优化
- 负载点同步降压转换器

说明

此 NexFET™ 功率 MOSFET 被设计成在功率转换和负载管理应用中大大降低功率损耗。小外形尺寸无引线 (SON) 2mm x 2mm 封装提供针对封装尺寸的出色散热性能。

顶视图



产品概述

V_{DS}	漏源电压	20	V
Q_g	栅极电荷总量 (4.5V)	2.5	nC
Q_{gd}	栅漏栅极电荷	0.66	nC
$R_{DS(on)}$ (导通)	漏源导通电阻	$V_{GS}=4.5\text{V}$	16 mΩ
		$V_{GS}=10\text{V}$	12 mΩ
$V_{GS(th)}$	阈值电压	1.45	V

订购信息

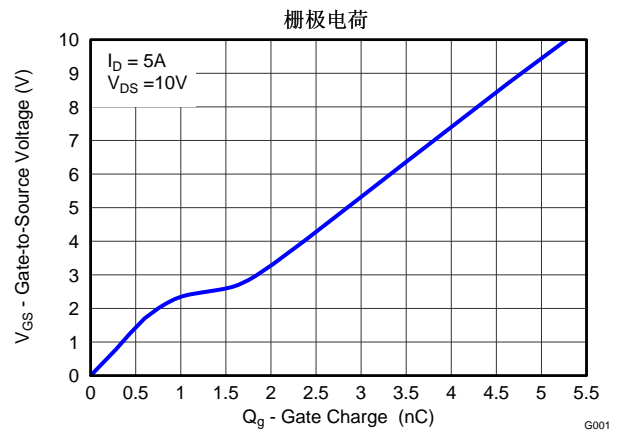
器件	封装	介质	数量	出货
CSD15571Q2	SON 2mm x 2mm 塑料封装	7 英寸卷带	3000	卷带封装

绝对最大额定值

$T_A=25^\circ\text{C}$ 时测得, 除非另外注明		值	单位
V_{DS}	漏源电压	20	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	22	A
	持续漏极电流 ⁽¹⁾	10	A
I_{DM}	脉冲漏极电流, $T_A=25^\circ\text{C}$ 时测得 ⁽²⁾	52	A
P_D	功率耗散 ⁽¹⁾	2.5	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D=19\text{A}, L=0.1\text{mH}, R_G=25\Omega$	18	mJ

(1) $R_{\theta JA} = 50$ 。这是在 1 平方英寸纯铜 (2 盎司), 厚度为 .060" 的环氧板 (FR4) 印刷电路板 (PCB) 上测得的值。

(2) 脉冲持续时间 10 μs , 占空比 $\leq 2\%$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified

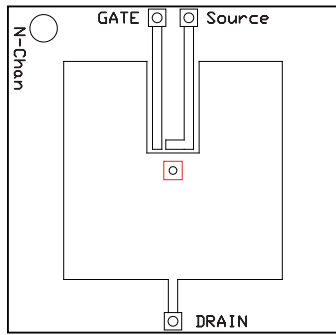
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	20			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\mu A$	1.10	1.45	1.90	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_{DS} = 5A$		16.0	19.2	$m\Omega$
		$V_{GS} = 10V, I_{DS} = 5A$		12.0	15.0	$m\Omega$
g_{fs}	Transconductance	$V_{DS} = 16V, I_{DS} = 5A$		25		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$		320	419	pF
C_{OSS}	Output Capacitance			184	239	pF
C_{RSS}	Reverse Transfer Capacitance			32	42	pF
R_g	Series Gate Resistance			3.8	7.6	Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 10V, I_{DS} = 5A$		2.5	3.3	nC
Q_g	Gate Charge Total (10V)			5.1	6.7	nC
Q_{gd}	Gate Charge – Gate to Drain			0.66		nC
Q_{gs}	Gate Charge Gate to Source			0.93		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.52		nC
Q_{OSS}	Output Charge		$V_{DS} = 10V, V_{GS} = 0V$		4.1	
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 10V, V_{GS} = 4.5V, I_{DS} = 5A$ $R_G = 2\Omega$		4.7		ns
t_r	Rise Time			17.2		ns
$t_{d(off)}$	Turn Off Delay Time			9.9		ns
t_f	Fall Time			4.1		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{DS} = 5A, V_{GS} = 0V$		0.82	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 10V, I_F = 5A, di/dt = 300A/\mu s$		10.7		nC
t_{rr}	Reverse Recovery Time			19		ns

THERMAL CHARACTERISTICS

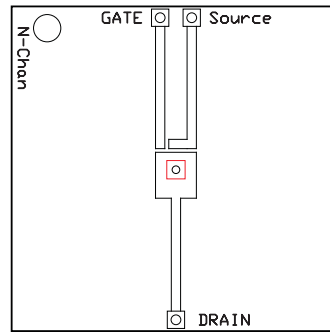
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			4.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			65	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 65$ when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 235$ when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

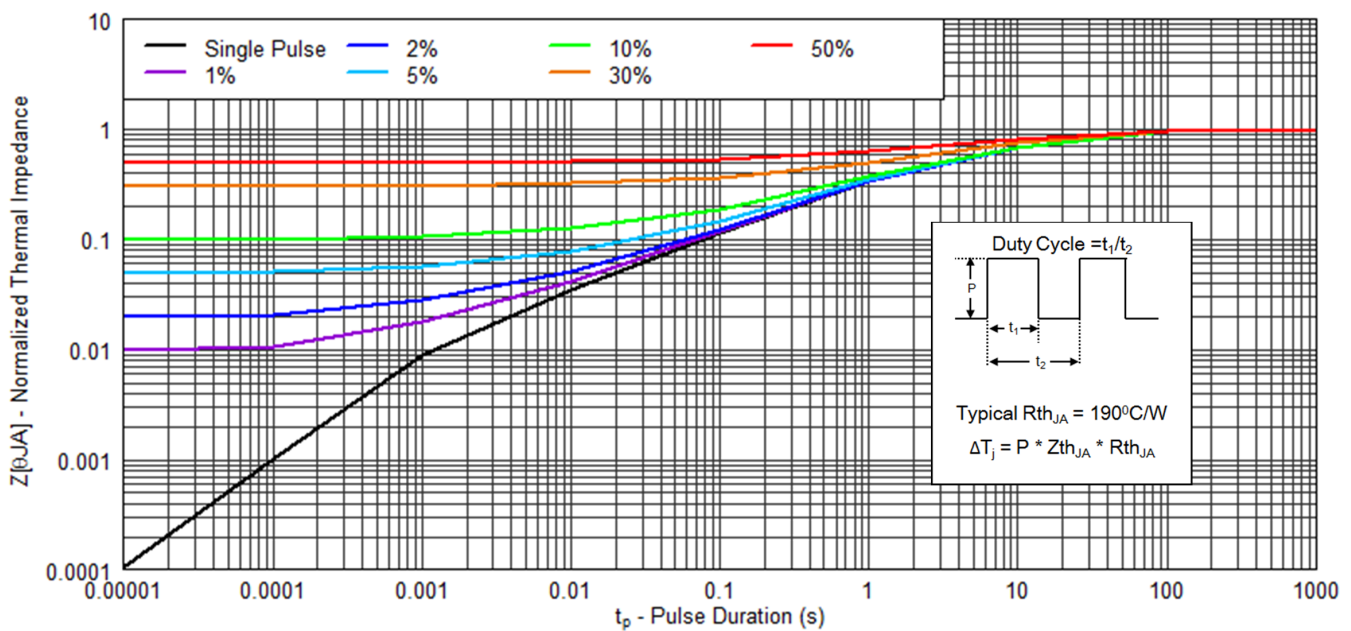


Figure 1. Transient Thermal Impedance

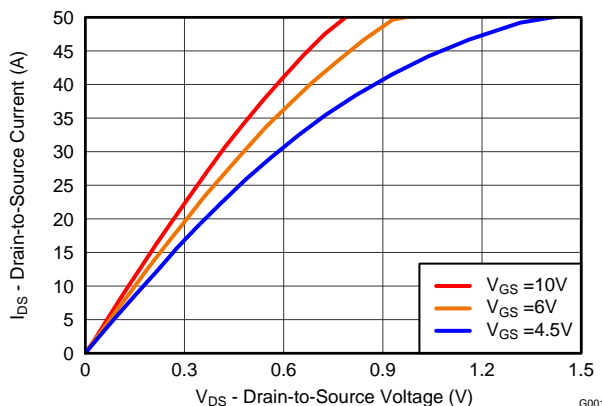


Figure 2. Saturation Characteristics

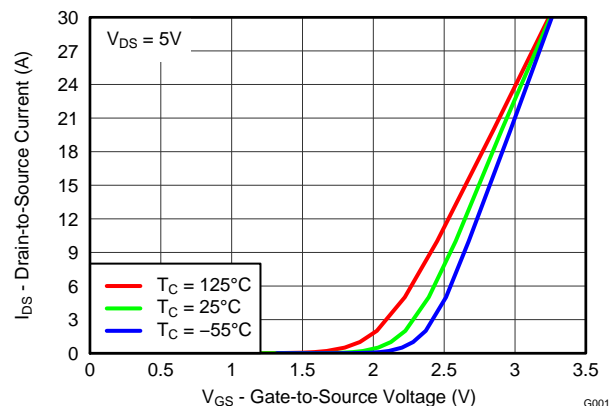


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

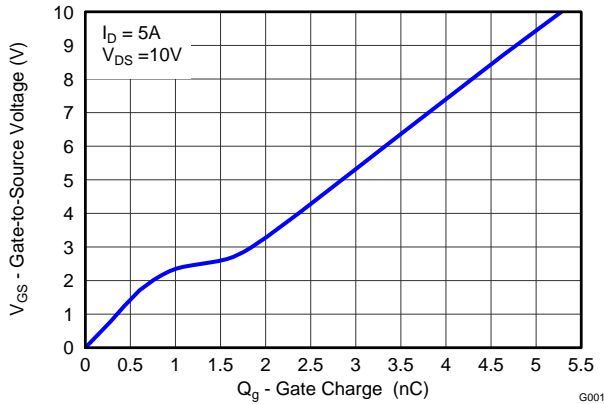


Figure 4. Gate Charge

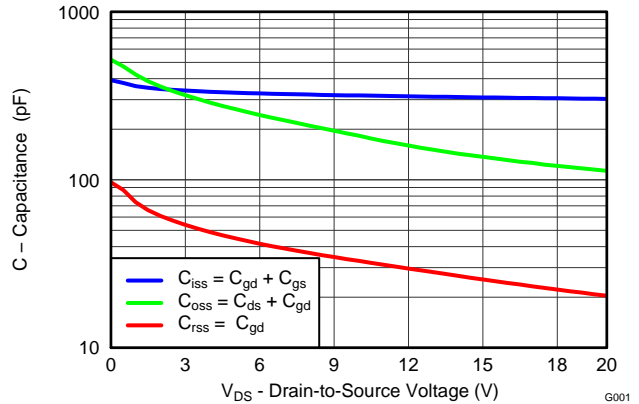


Figure 5. Capacitance

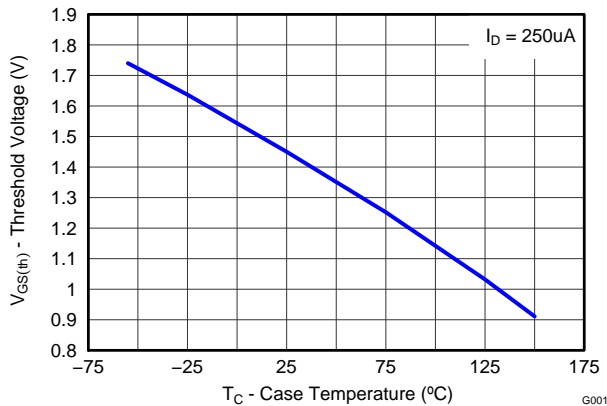


Figure 6. Threshold Voltage vs. Temperature

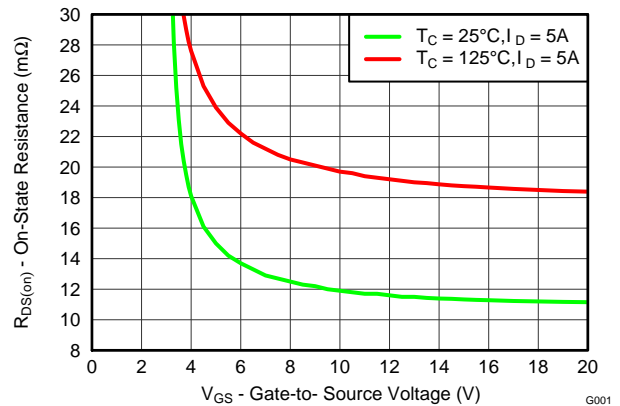


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

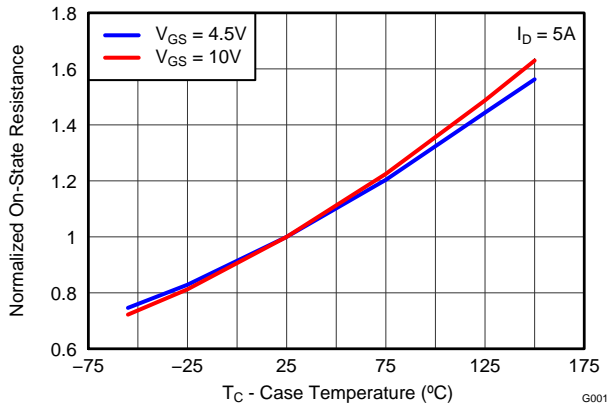


Figure 8. Normalized On-State Resistance vs. Temperature

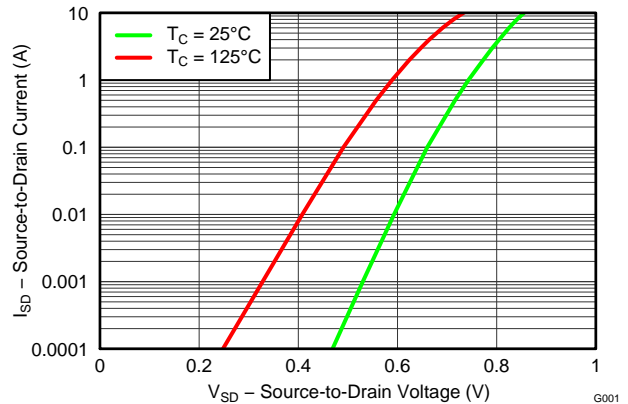


Figure 9. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

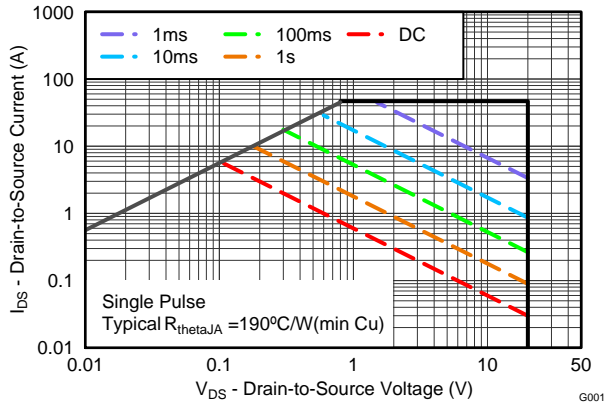


Figure 10. Maximum Safe Operating Area

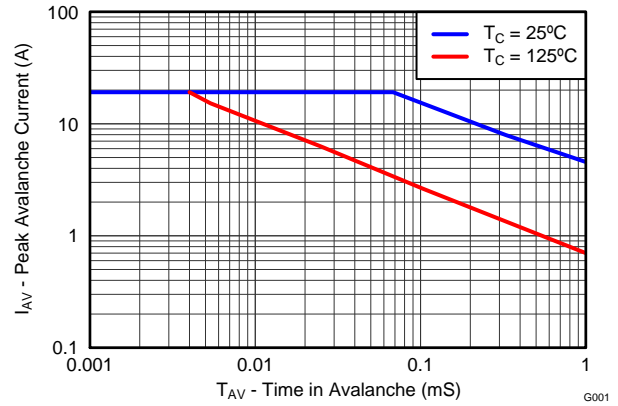


Figure 11. Single Pulse Unclamped Inductive Switching

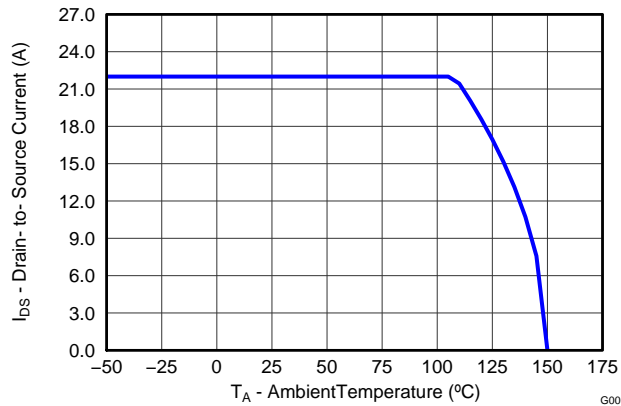
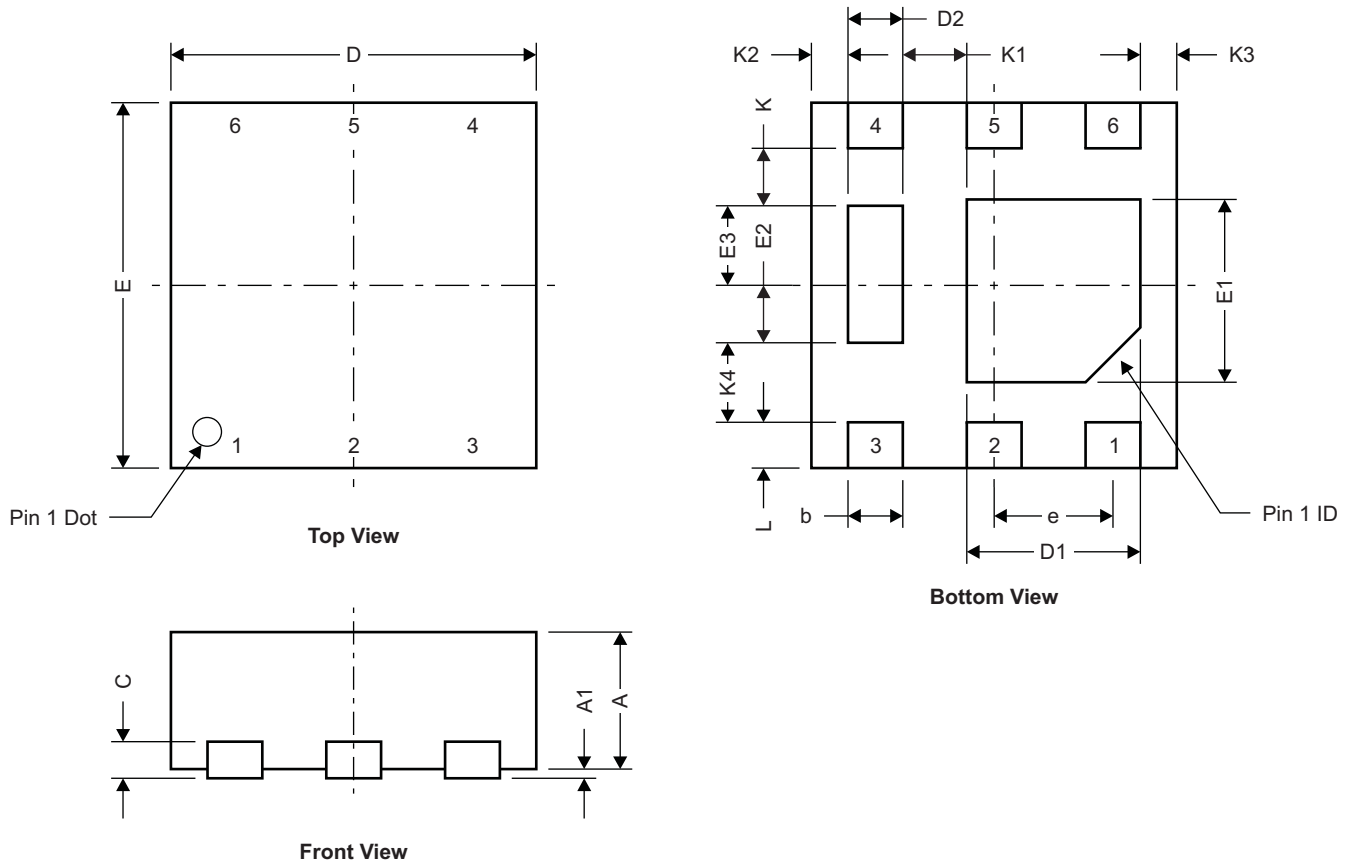


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

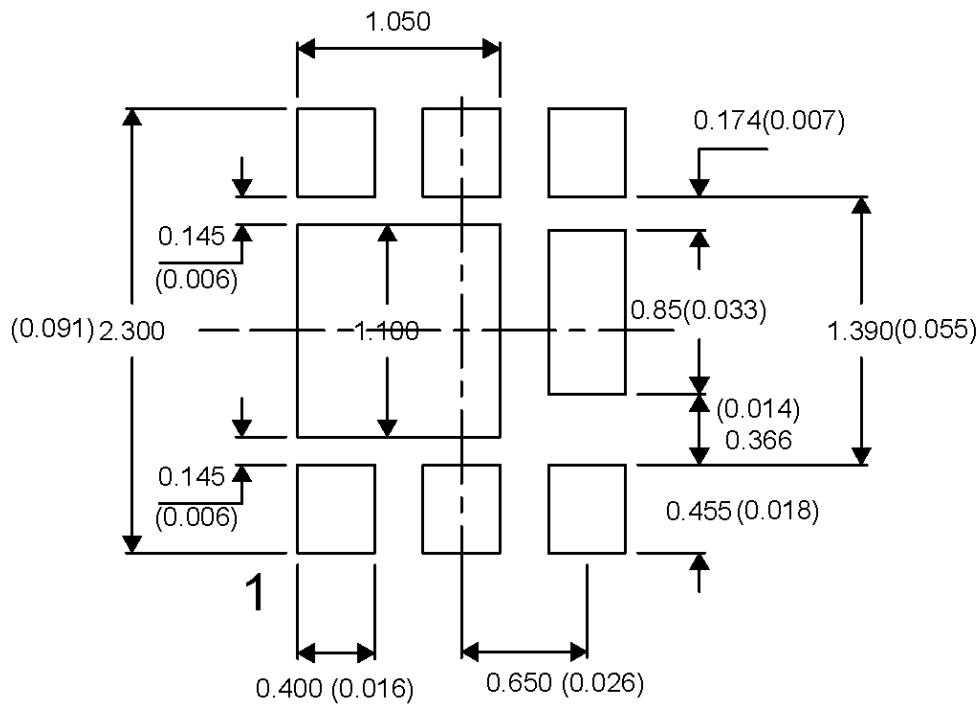
Q2 Package Dimensions



M0165-01

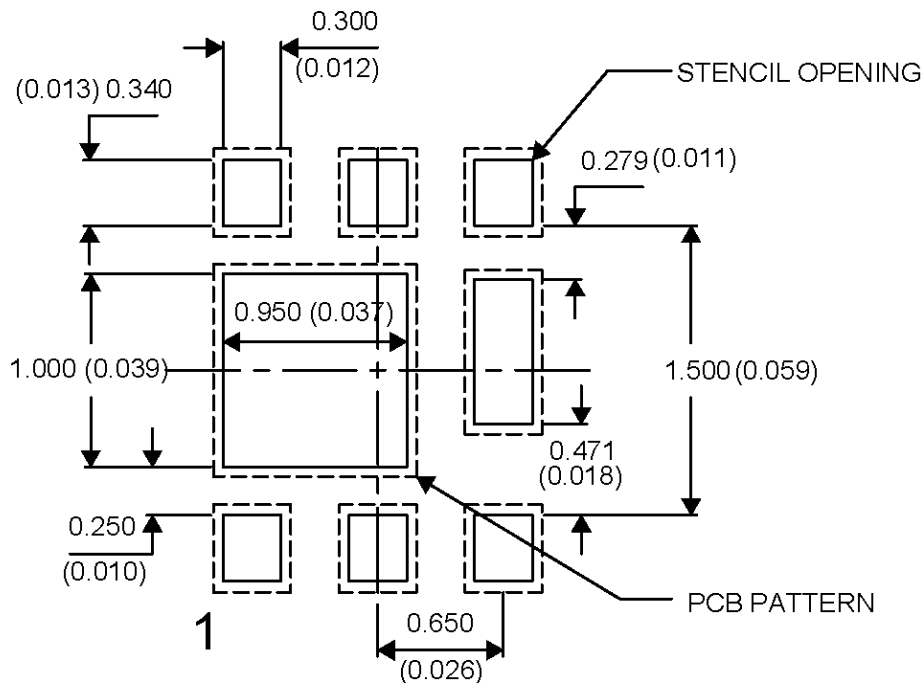
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 BSC			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

Recommended PCB Pattern



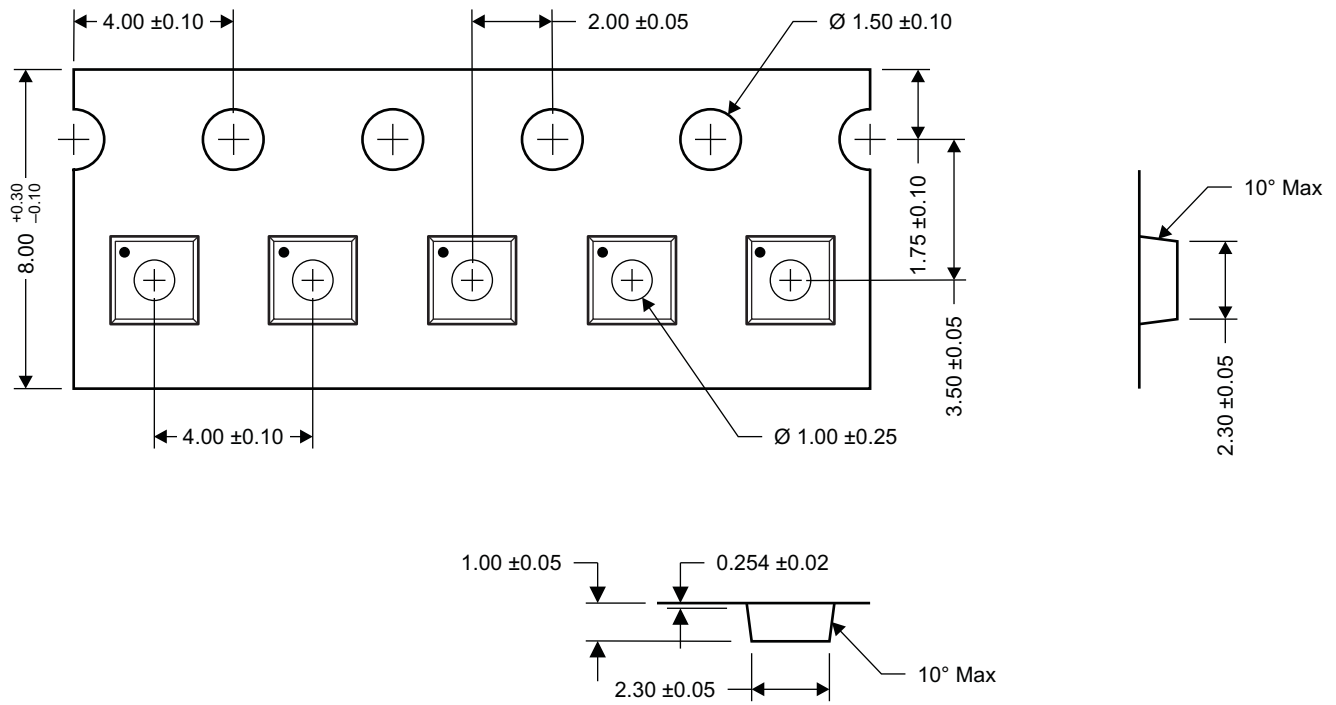
For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

Q2 Tape and Reel Information



- Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
 2. Cumulative tolerance of 10 sprocket holes is ±0.20
 3. Other material available
 4. Typical SR of form tape Max 10⁹ OHM/SQ
 5. All dimensions are in mm, unless otherwise specified.

M0168-01

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD15571Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	1551	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司