

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645 OCTAL BUS TRANSCEIVERS

SDLS189 – APRIL 1979 – REVISED MARCH 1988

- **SN74LS64X-1 Versions Rated at I_{OL} of 48 mA**
- **Bi-directional Bus Transceivers in High-Density 20-Pin Packages**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\bar{G}$) can be used to disable the device so the buses are effectively isolated.

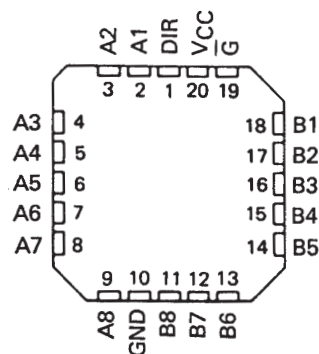
The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C .

SN54LS' . . . J PACKAGE
SN74LS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS' . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

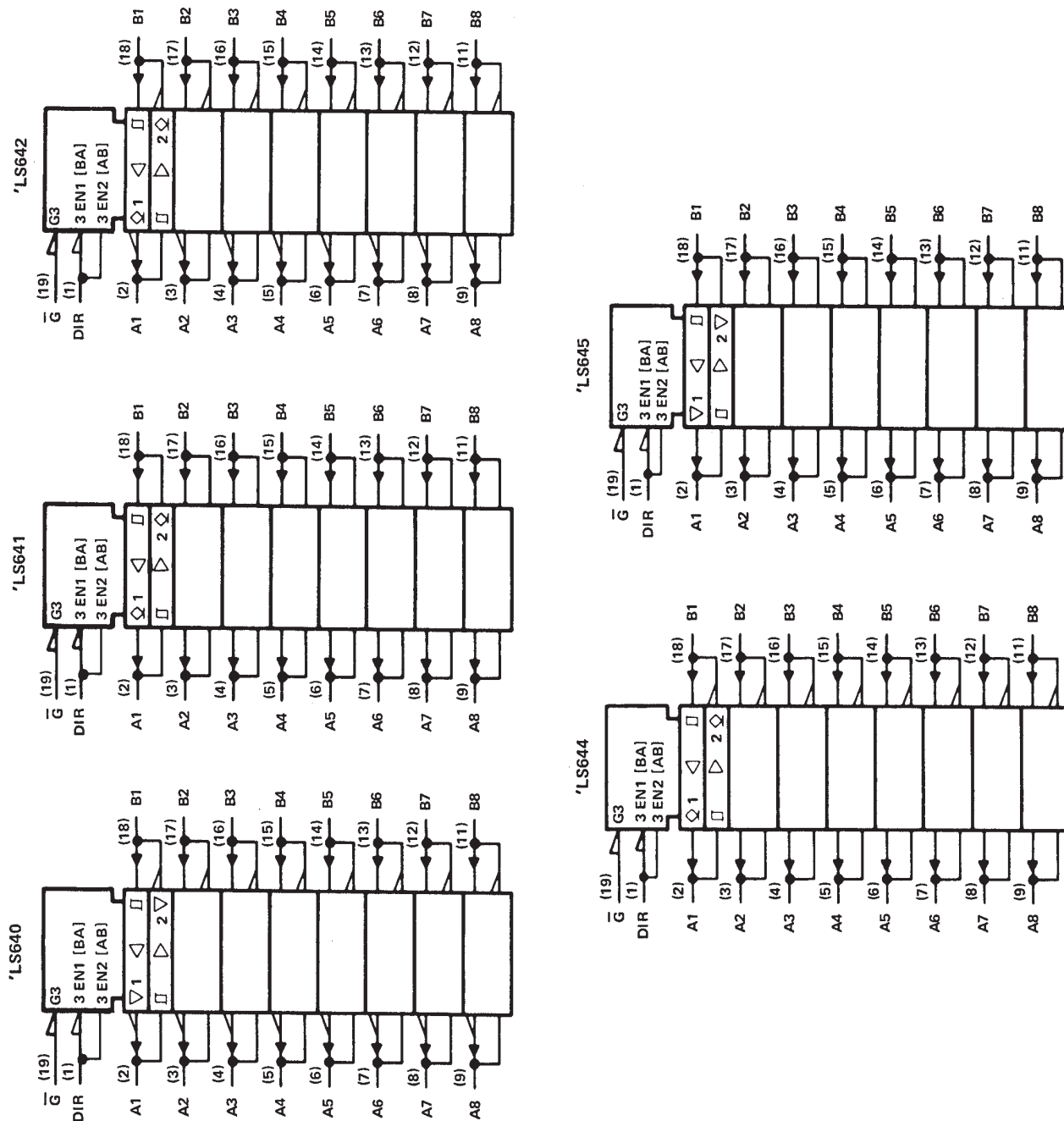
CONTROL INPUTS		OPERATION		
$\bar{G}$	DIR	'LS640 'LS642	'LS641 'LS645	'LS644
L	L	B data to A bus	B data to A bus	B data to A bus
L	H	A data to B bus	A data to B bus	$\bar{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645 OCTAL BUS TRANSCEIVERS

SDLS189 – APRIL 1979 – REVISED MARCH 1988

logic symbols†

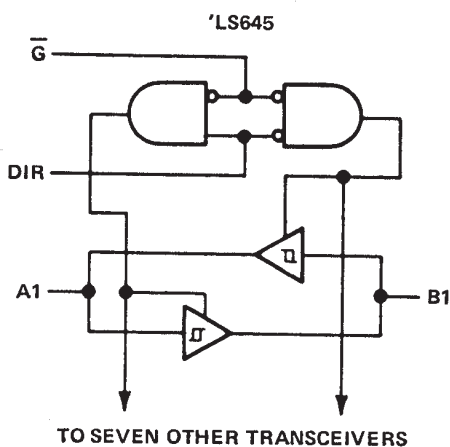
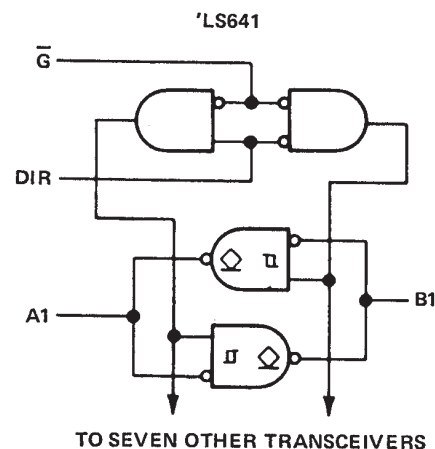
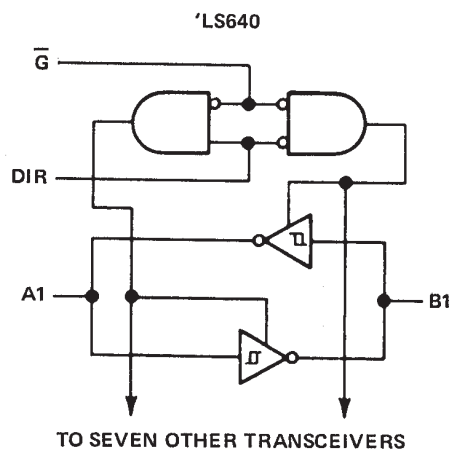


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645
 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645
 OCTAL BUS TRANSCEIVERS

SDLS189 – APRIL 1979 – REVISED MARCH 1988

logic diagrams (positive logic)



SN54LS640, SN54LS645
SN74LS640, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDLS189 – APRIL 1979 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS640, SN54LS645	– 55 °C to 125 °C
SN74LS640, SN74LS645	0 °C to 70 °C
Storage temperature range	– 65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS640 SN54LS645			SN74LS640 SN74LS645			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.5			0.6	V
I_{OH} High-level output current			– 12			– 15	mA
I_{OL} Low-level output current			12			24	mA
						48†	
T_A Operating free-air temperature	– 55		125	0		70	°C

†The 48-mA limit applies for the SN74LS640-1 and SN74LS645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS640 SN54LS645			SN74LS640 SN74LS645			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				– 1.5			– 1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN},$	A or B input	0.1	0.4		0.2	0.4		V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		V
		$I_{OH} = \text{MAX}$	2			2			
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
		$I_{OL} = 24 \text{ mA}$					0.35	0.5	
		$I_{OL} = 48 \text{ mA}^\#$					0.4	0.5	
I_{OZH}	$V_{CC} = \text{MAX}, \bar{G} \text{ at } 2 \text{ V},$	$V_O = 2.7 \text{ V}$			20			20	µA
I_{OZL}	$V_{CC} = \text{MAX}, \bar{G} \text{ at } 2 \text{ V},$	$V_O = 0.4 \text{ V}$			– 0.4			– 0.4	mA
I_I	A or B DIR or $\bar{G}$	$V_{CC} = \text{MAX}$			0.1			0.1	mA
		$V_I = 5.5 \text{ V}$			0.1			0.1	
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.7 \text{ V}$				20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$				– 0.4			– 0.4	mA
$I_{OS}^\dagger$	$V_{CC} = \text{MAX}$		– 40		– 225	– 40		– 225	mA
I_{CC}	Outputs high	$V_{CC} = \text{MAX},$ Outputs open			48			48	mA
	Outputs low				62			62	
	Outputs at Hi-Z				64			64	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

†Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

‡The 48-mA condition applies for the SN74LS640-1 and SN74LS645-1 only.

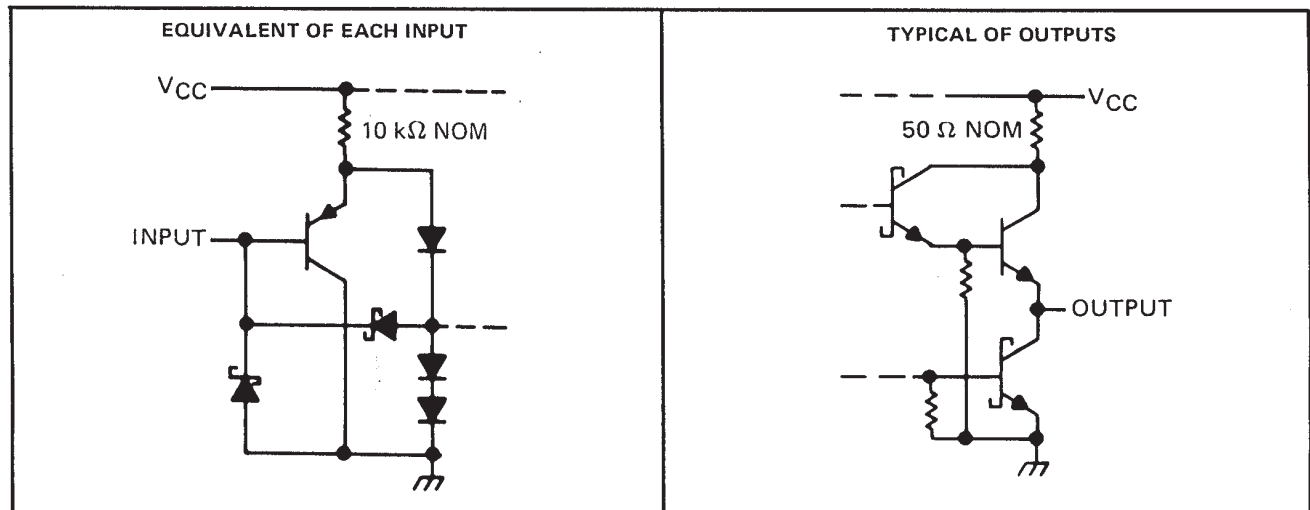


switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640-1			'LS645, 'LS645-1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$, See Note 2		6	10		8	15	ns
	B	A			6	10		8	15	
t_{PHL} Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
	B	A			8	15		11	15	
t_{PZL} Output enable time to low level	$\overline{G}$	A			31	40		31	40	ns
	$\overline{G}$	B			31	40		31	40	
t_{PZH} Output enable time to high level	$\overline{G}$	A			23	40		26	40	ns
	$\overline{G}$	B			23	40		26	40	
t_{PLZ} Output disable time from low level	$\overline{G}$	A	$C_L = 5\text{ pF}$, $R_L = 667\ \Omega$, See Note 2		15	25		15	25	ns
	$\overline{G}$	B			15	25		15	25	
t_{PHZ} Output disable time from high level	$\overline{G}$	A			15	25		15	25	ns
	$\overline{G}$	B			15	25		15	25	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



SN54LS640, SN54LS645
SN74LS640, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDLS189 – APRIL 1979 – REVISED MARCH 1988

TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE

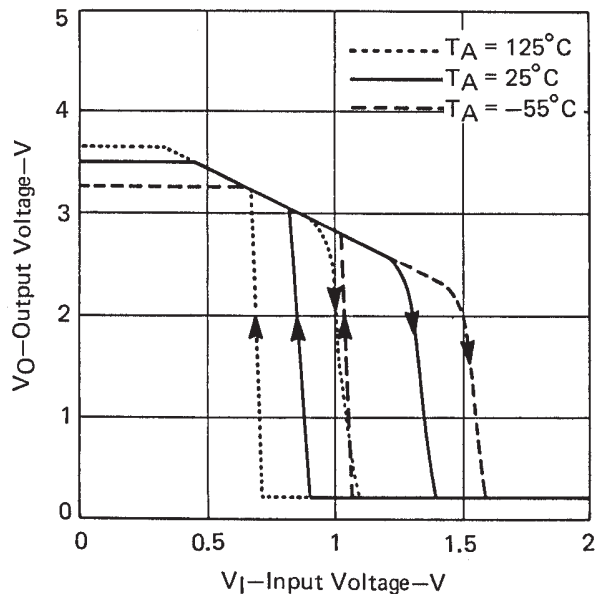


FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE

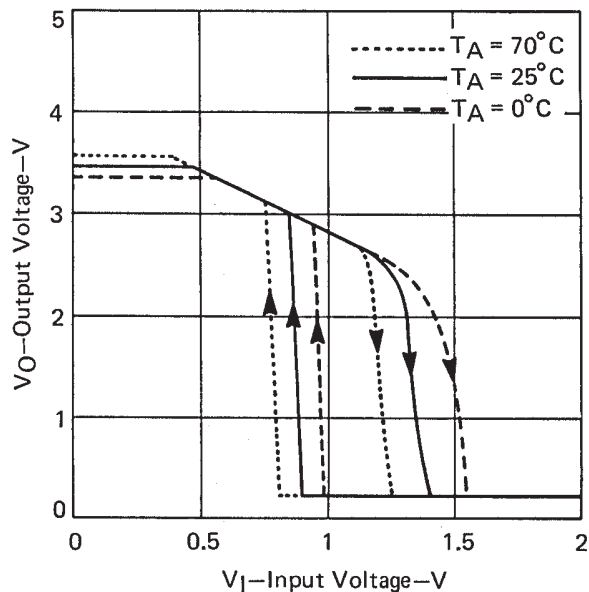


FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE

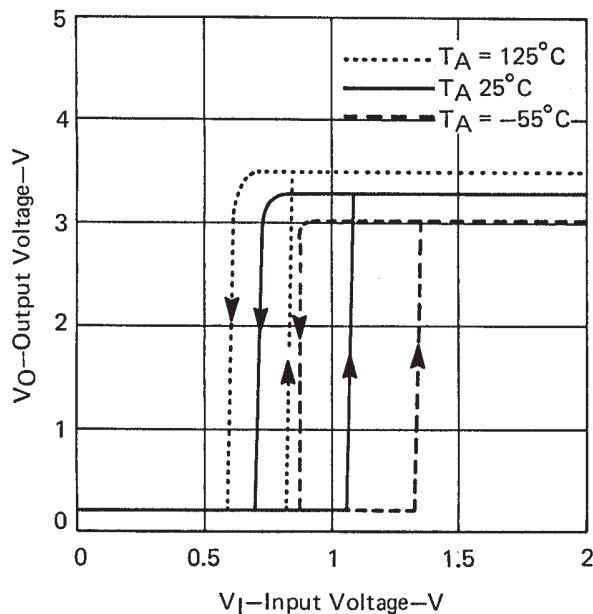


FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE

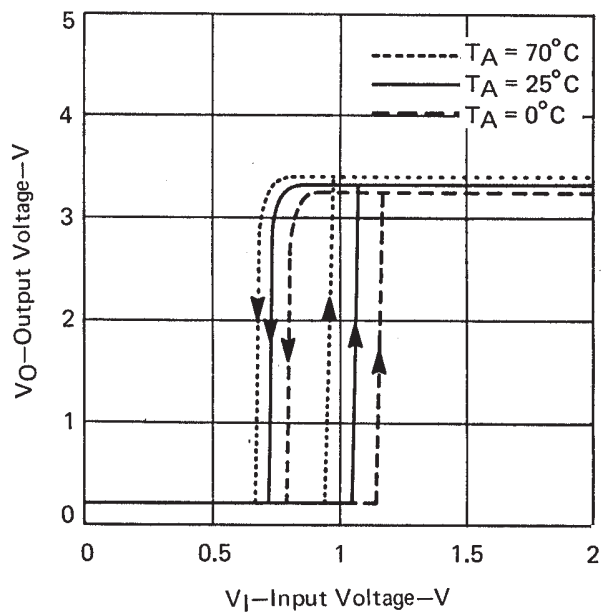


FIGURE 4

NOTE 1: Voltage values are with respect to network ground terminal.

PARAMETER	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.5			0.6	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current		12			24		mA
					48 §		
T _A Operating free-air temperature	− 55		125	0		70	°C

PARAMETER		TEST CONDITIONS†	SN54LS641 SN54LS642 SN54LS644		SN74LS641 SN74LS642 SN74LS644		UNIT			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V_{IK}			$V_{CC} = \text{MIN},$	$I_I = -18 \text{ mA}$		-1.5		-1.5		V
Hysteresis ($V_{T+} - V_{T-}$)			$V_{CC} = \text{MIN},$	A or B input		0.1	0.4	0.2	0.4	V
I_{OH}			$V_{CC} = \text{MIN},$ $V_{IH} = 2 \text{ V},$ $V_{IL} = \text{MAX},$ $V_{OH} = 5.5 \text{ V}$			0.1		0.1		mA
V_{OL}			$V_{CC} = \text{MIN},$ $V_{IH} = 2 \text{ V},$ $V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4	0.25	0.4	V
				$I_{OL} = 24 \text{ mA}$				0.35	0.5	
				$I_{OL} = 48 \text{ mA}§$				0.4	0.5	
I_I	A or B	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$		0.1		0.1		mA	
	DIR or $\overline{G}$		$V_I = 7 \text{ V}$		0.1		0.1			
I_{IH}		$V_{CC} = \text{MAX},$	$V_I = 2.7 \text{ V}$		20		20		μA	
I_{IL}		$V_{CC} = \text{MAX},$	$V_I = 0.4 \text{ V}$		-0.4		-0.4		mA	
I_{CC}	Outputs high	$V_{CC} = \text{MAX},$	Outputs open		48	70	48	70	mA	
	Outputs low				62	90	62	90		
	Outputs at Hi-Z				64	95	64	95		

§The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

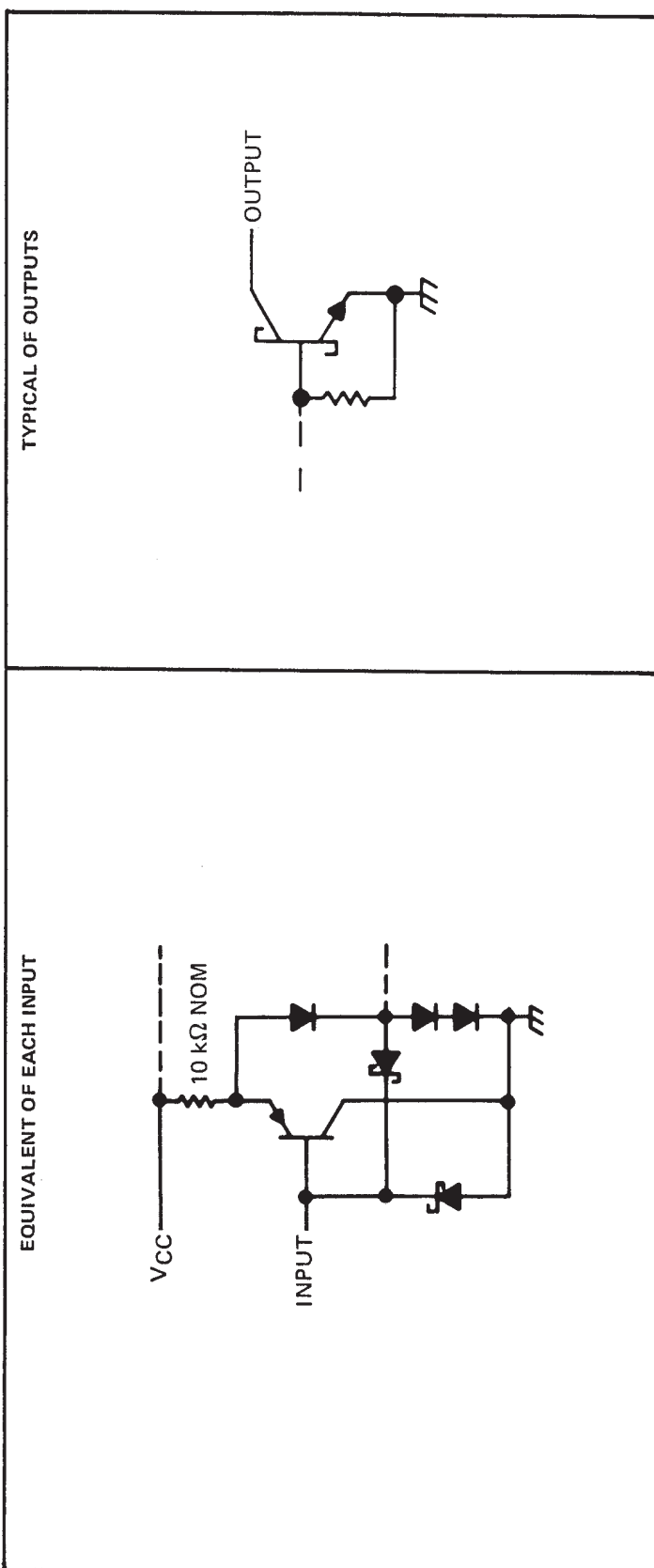
SDLS189 – APRIL 1979 – REVISED MARCH 1988

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS641, 'LS641-1		'LS642, 'LS642-1		'LS644, 'LS644-1		UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} Propagation delay time, low-to-high-level output	A	B	C _L = 45 pF, R _L = 667 Ω, See Note 2	17	25	19	25	17	25	ns
	B	A		17	25	19	25	19	25	
t _{PHL} Propagation delay time, high-to-low-level output	A	B		16	25	14	25	14	25	ns
	B	A		16	25	14	25	16	25	
t _{PLH} Output disable time from low level	$\bar{G}$, DIR	A	23	40	26	40	26	40	ns	
	$\bar{G}$, DIR	B	25	40	28	40	25	40		
t _{PHL} Output enable time from high level	$\bar{G}$, DIR	A	34	50	43	60	43	60	ns	
	$\bar{G}$, DIR	B	37	50	39	60	37	50		

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84161012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84161012A SNJ54LS 640FK	Samples
8416101RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8416101RA SNJ54LS640J	Samples
SN54LS640J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS640J	Samples
SN54LS645J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS645J	Samples
SN74LS640-1DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS640-1	Samples
SN74LS640-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS640-1N	Samples
SN74LS640-1NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS640-1	Samples
SN74LS640DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS640	Samples
SN74LS640DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS640	Samples
SN74LS640N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS640N	Samples
SN74LS640NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS640	Samples
SN74LS641-1DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS641-1	Samples
SN74LS641-1DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS641-1	Samples
SN74LS641-1DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS641-1	Samples
SN74LS641-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS641-1N	Samples
SN74LS641DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS641	Samples
SN74LS641N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS641N	Samples
SN74LS641NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS641	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS642-1DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS642-1	Samples
SN74LS642-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS642-1N	Samples
SN74LS642DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS642	Samples
SN74LS642N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS642N	Samples
SN74LS642NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS642	Samples
SN74LS645-1DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS645-1	Samples
SN74LS645-1DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS645-1	Samples
SN74LS645-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS645-1N	Samples
SN74LS645-1NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS645-1	Samples
SN74LS645DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS645	Samples
SN74LS645N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS645N	Samples
SN74LS645NE4	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS645N	Samples
SN74LS645NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS645	Samples
SNJ54LS640FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84161012A SNJ54LS 640FK	Samples
SNJ54LS640J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8416101RA SNJ54LS640J	Samples
SNJ54LS645J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS645J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS640, SN54LS645, SN74LS640, SN74LS645 :

● Catalog : [SN74LS640](#), [SN74LS645](#)

● Military : [SN54LS640](#), [SN54LS645](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

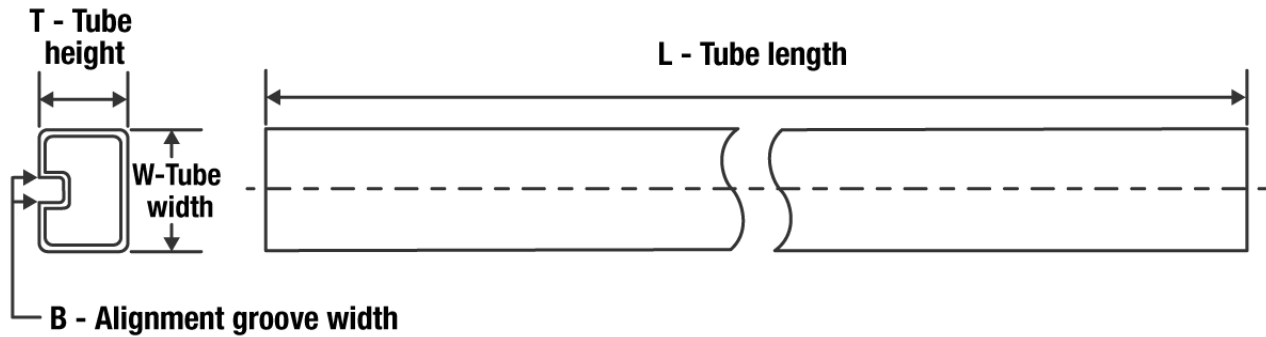
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS640-1NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS640DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS640NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS641-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS641NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS642NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS645-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS645-1NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS645NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS640-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS640DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS640NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS641-1DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS641NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS642NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS645-1DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS645-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS645NSR	SO	NS	20	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84161012A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74LS640-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS640-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS640DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS640N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS641-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS641-1DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS641-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS641DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS641N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS642-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS642-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS642DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS642N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS645-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS645-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS645DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS645N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS645NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS640FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



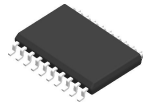
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



NOTES:

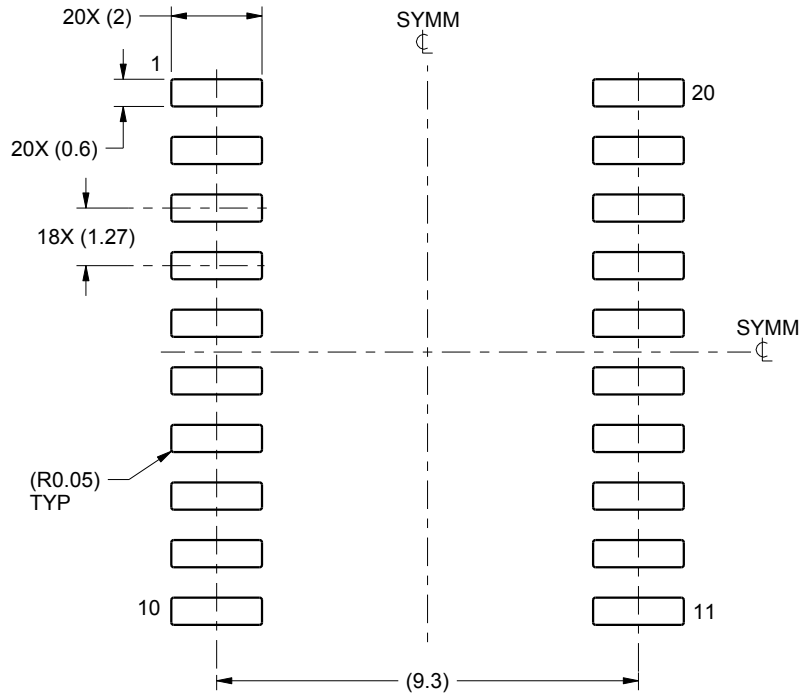
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

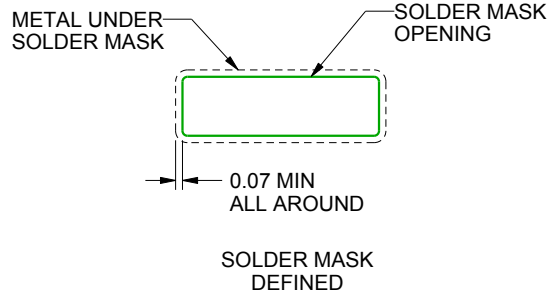
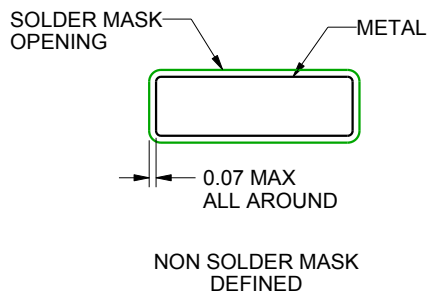
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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