



# INA125

## INSTRUMENTATION AMPLIFIER With Precision Voltage Reference

### FEATURES

- LOW QUIESCENT CURRENT: 460 $\mu$ A
- PRECISION VOLTAGE REFERENCE:  
1.24V, 2.5V, 5V or 10V
- SLEEP MODE
- LOW OFFSET VOLTAGE: 250 $\mu$ V max
- LOW OFFSET DRIFT: 2 $\mu$ V/ $^{\circ}$ C max
- LOW INPUT BIAS CURRENT: 20nA max
- HIGH CMR: 100dB min
- LOW NOISE: 38nV/ $\sqrt{\text{Hz}}$  at f = 1kHz
- INPUT PROTECTION TO  $\pm 40$ V
- WIDE SUPPLY RANGE  
Single Supply: 2.7V to 36V  
Dual Supply:  $\pm 1.35$ V to  $\pm 18$ V
- 16-PIN DIP AND SO-16 SOIC PACKAGES

### DESCRIPTION

The INA125 is a low power, high accuracy instrumentation amplifier with a precision voltage reference. It provides complete bridge excitation and precision differential-input amplification on a single integrated circuit.

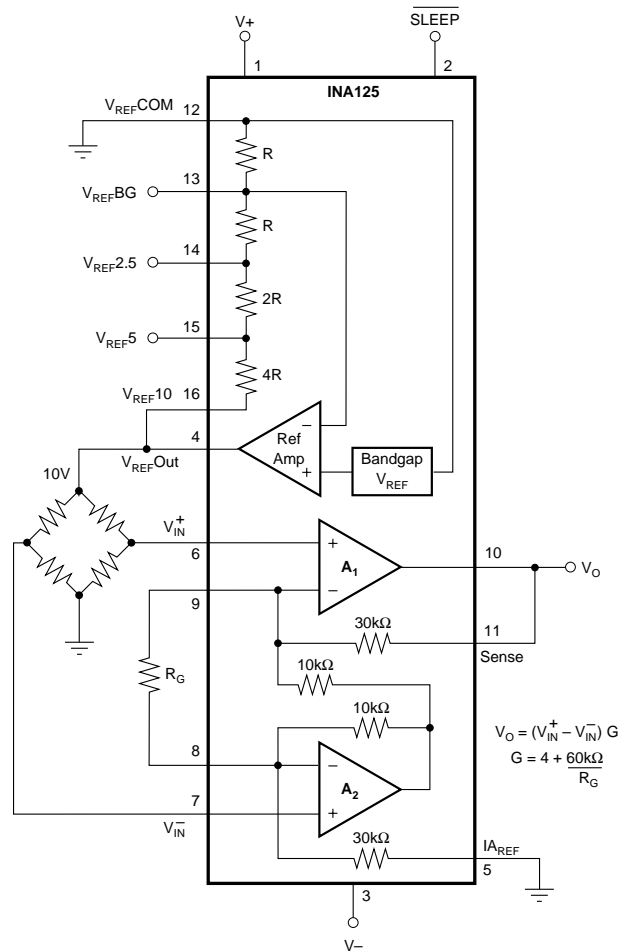
A single external resistor sets any gain from 4 to 10,000. The INA125 is laser-trimmed for low offset voltage (250 $\mu$ V), low offset drift (2 $\mu$ V/ $^{\circ}$ C), and high common-mode rejection (100dB at G = 100). It operates on single (+2.7V to +36V) or dual ( $\pm 1.35$ V to  $\pm 18$ V) supplies.

The voltage reference is externally adjustable with pin-selectable voltages of 2.5V, 5V, or 10V, allowing use with a variety of transducers. The reference voltage is accurate to  $\pm 0.5\%$  (max) with  $\pm 35$ ppm/ $^{\circ}$ C drift (max). Sleep mode allows shutdown and duty cycle operation to save power.

The INA125 is available in 16-pin plastic DIP and SO-16 surface-mount packages and is specified for the  $-40^{\circ}$ C to  $+85^{\circ}$ C industrial temperature range.

### APPLICATIONS

- PRESSURE AND TEMPERATURE BRIDGE AMPLIFIERS
- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- MULTI-CHANNEL DATA ACQUISITION
- BATTERY OPERATED SYSTEMS
- GENERAL PURPOSE INSTRUMENTATION



# SPECIFICATIONS: $V_S = \pm 15V$

At  $T_A = +25^\circ C$ ,  $V_S = \pm 15V$ ,  $I_A$  common = 0V,  $V_{REF}$  common = 0V, and  $R_L = 10k\Omega$ , unless otherwise noted.

PARAMETER	CONDITIONS	INA125P, U			INA125PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
Offset Voltage, RTI	$V_S = \pm 1.35V$ to $\pm 18V$ , $G = 4$		$\pm 50$	$\pm 250$		*	$\pm 500$	$\mu V$
Initial			$\pm 0.25$	$\pm 2$		*	$\pm 5$	$\mu V/^\circ C$
vs Temperature			$\pm 3$	$\pm 20$		*	$\pm 50$	$\mu V/V$
vs Power Supply			$\pm 0.2$			*		$\mu V/mo$
Long-Term Stability			$10^{11} \parallel 2$			*		$\Omega \parallel pF$
Impedance, Differential	$V_{CM} = -10.7V$ to $+10.2V$		$10^{11} \parallel 9$			*		$\Omega \parallel pF$
Common-Mode			See Text	$\pm 40$		*	*	V
Safe Input Voltage								
Input Voltage Range								
Common-Mode Rejection								
	$G = 4$	78	84		72	*		dB
	$G = 10$	86	94		80	*		dB
	$G = 100$	100	114		90	*		dB
	$G = 500$	100	114		90	*		dB
<b>BIAS CURRENT</b>	$V_{CM} = 0V$		10	25		*	50	nA
vs Temperature			$\pm 60$			*		$pA/^\circ C$
Offset Current			$\pm 0.5$	$\pm 2.5$		*	$\pm 5$	nA
vs Temperature			$\pm 0.5$			*		$pA/^\circ C$
<b>NOISE, RTI</b>	$R_S = 0\Omega$							
Voltage Noise, $f = 10Hz$			40			*		$nV/\sqrt{Hz}$
$f = 100Hz$			38			*		$nV/\sqrt{Hz}$
$f = 1kHz$			38			*		$nV/\sqrt{Hz}$
$f = 0.1Hz$ to $10Hz$			0.8			*		$\mu Vp-p$
Current Noise, $f = 10Hz$			170			*		$fA/\sqrt{Hz}$
$f = 1kHz$			56			*		$fA/\sqrt{Hz}$
$f = 0.1Hz$ to $10Hz$			5			*		$pAp-p$
<b>GAIN</b>								
Gain Equation	$V_O = -14V$ to $+13.3V$	4	$4 + 60k\Omega/R_G$	10,000	*	*	*	V/V
Range of Gain								V/V
Gain Error			$\pm 0.01$	$\pm 0.075$		*	$\pm 0.1$	%
			$\pm 0.03$	$\pm 0.3$		*	$\pm 0.5$	%
			$\pm 0.05$	$\pm 0.5$		*	$\pm 1$	%
Gain vs Temperature	$G = 500$		$\pm 0.1$			*		%
	$G = 4$		$\pm 1$	$\pm 15$		*	*	$ppm/^\circ C$
	$G > 4^{(1)}$		$\pm 25$	$\pm 100$		*	*	$ppm/^\circ C$
Nonlinearity	$V_O = -14V$ to $+13.3V$							
			$\pm 0.0004$	$\pm 0.002$		*	$\pm 0.004$	% of FS
			$\pm 0.0004$	$\pm 0.002$		*	$\pm 0.004$	% of FS
			$\pm 0.001$	$\pm 0.01$		*	*	% of FS
			$\pm 0.002$			*		% of FS
<b>OUTPUT</b>								
Voltage: Positive		$(V+) - 1.7$	$(V+) - 0.9$		*	*		V
Negative		$(V-) + 1$	$(V-) + 0.4$		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			$-9/+12$			*		mA
<b>VOLTAGE REFERENCE</b>	$V_{REF} = +2.5V, +5V, +10V$							
Accuracy	$I_L = 0$		$\pm 0.15$	$\pm 0.5$		*	$\pm 1$	%
vs Temperature	$I_L = 0$		$\pm 18$	$\pm 35$		*	$\pm 100$	$ppm/^\circ C$
vs Power Supply, $V+$	$V+ = (V_{REF} + 1.25V)$ to $+36V$		$\pm 20$	$\pm 50$		*	$\pm 100$	$ppm/V$
vs Load	$I_L = 0$ to $5mA$		3	75		*	*	$ppm/mA$
Dropout Voltage, $(V+) - V_{REF}^{(2)}$	Ref Load = $2k\Omega$	1.25	1		*	*		V
Bandgap Voltage Reference			1.24			*		V
Accuracy	$I_L = 0$		$\pm 0.5$			*		%
vs Temperature	$I_L = 0$		$\pm 18$			*		$ppm/^\circ C$

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## SPECIFICATIONS: $V_S = \pm 15V$ (CONT)

At  $T_A = +25^\circ C$ ,  $V_S = \pm 15V$ ,  $I_A$  common = 0V,  $V_{REF}$  common = 0V, and  $R_L = 10k\Omega$ , unless otherwise noted.

PARAMETER CONDITIONS		INA125P, U			INA125PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>FREQUENCY RESPONSE</b> Bandwidth, -3dB	$G = 4$ $G = 10$ $G = 100$ $G = 500$		150 45 4.5 0.9			* * * *		kHz kHz kHz kHz
Slew Rate	$G = 4$ , 10V Step		0.2			*		V/ $\mu s$
Settling Time, 0.01%	$G = 4$ , 10V Step $G = 10$ , 10V Step $G = 100$ , 10V Step $G = 500$ , 10V Step		60 83 375 1700			* * * *		$\mu s$ $\mu s$ $\mu s$ $\mu s$
Overload Recovery	50% Overdrive		5			*		$\mu s$
<b>POWER SUPPLY</b> Specified Operating Voltage Specified Voltage Range Quiescent Current, Positive Negative Reference Ground Current <sup>(3)</sup> Sleep Current ( $V_{SLEEP} \leq 100mV$ )	$I_O = I_{REF} = 0mA$ $I_O = I_{REF} = 0mA$ $R_L = 10k\Omega$ , Ref Load = 2k $\Omega$	$\pm 1.35$	$\pm 15$ 460 -280 180 $\pm 1$	$\pm 18$ 525 -325 180 $\pm 25$	*	* * * * *	* * * * *	V V $\mu A$ $\mu A$ $\mu A$ $\mu A$
<b>SLEEP MODE PIN<sup>(4)</sup></b> $V_{IH}$ (Logic high input voltage) $V_{IL}$ (Logic low input voltage) $I_{IH}$ (Logic high input current) $I_{IL}$ (Logic low input current) Wake-up Time <sup>(5)</sup>		+2.7 0	15 0 150	V+ +0.1	* *	* * * *	* * * *	V V $\mu A$ $\mu A$ $\mu s$
<b>TEMPERATURE RANGE</b> Specification Range Operation Range Storage Range Thermal Resistance, $\theta_{JA}$ 16-Pin DIP SO-16 Surface-Mount		-40 -55 -55		+85 +125 +125	* * *		* * *	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$

\* Specification same as INA125P, U.

NOTES: (1) Temperature coefficient of the "Internal Resistor" in the gain equation. Does not include TCR of gain-setting resistor,  $R_G$ . (2) Dropout voltage is the positive supply voltage minus the reference voltage that produces a 1% decrease in reference voltage. (3)  $V_{REFCOM}$  pin. (4) Voltage measured with respect to Reference Common. Logic low input selects Sleep mode. (5)  $I_A$  and Reference, see Typical Performance Curves.

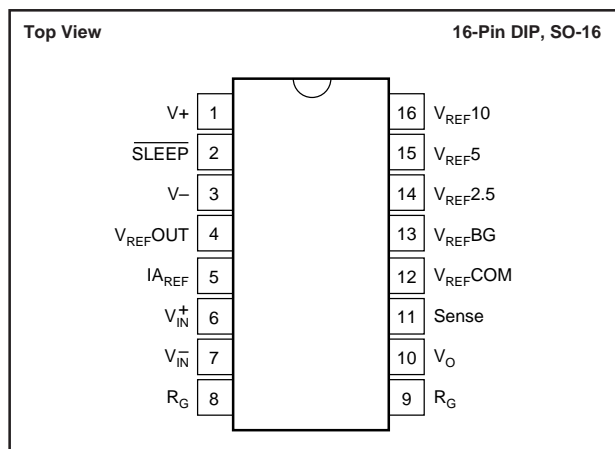
## SPECIFICATIONS: $V_S = +5V$

At  $T_A = +25^\circ C$ ,  $V_S = +5V$ ,  $I_A$  common at  $V_S/2$ ,  $V_{REF}$  common =  $V_S/2$ ,  $V_{CM} = V_S/2$ , and  $R_L = 10k\Omega$  to  $V_S/2$ , unless otherwise noted.

PARAMETER	CONDITIONS	INA125P, U			INA125PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b> Offset Voltage, RTI Initial vs Temperature vs Power Supply Input Voltage Range Common-Mode Rejection	$V_S = +2.7V$ to +36V  $V_{CM} = +1.1V$ to +3.6V $G = 4$ $G = 10$ $G = 100$ $G = 500$		$\pm 75$ $\pm 0.25$ 3 See Text	$\pm 500$ 20		* * * *	$\pm 750$ 50	$\mu V$ $\mu V/^\circ C$ $\mu V/V$
		78 86 100 100	84 94 114 114		72 80 90 90	* * * *		dB dB dB dB
<b>GAIN</b> Gain Error	$V_O = +0.3V$ to +3.8V $G = 4$		$\pm 0.01$			*		%
<b>OUTPUT</b> Voltage, Positive Negative		(V+)-1.2 (V-)+0.3	(V+)-0.8 (V-)+0.15		* *	* *		V V
<b>POWER SUPPLY</b> Specified Operating Voltage Operating Voltage Range Quiescent Current Sleep Current ( $V_{SLEEP} \leq 100mV$ )	$I_O = I_{REF} = 0mA$ $R_L = 10k\Omega$ , Ref Load = 2k $\Omega$	+2.7	+5 460 $\pm 1$	+36 525 $\pm 25$	*	* * * *	* * * *	V V $\mu A$ $\mu A$

\* Specification same as INA125P, U.

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Power Supply Voltage, V+ to V-	36V
Input Signal Voltage	±40V
Output Short Circuit	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above these ratings may cause permanent damage.

## PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
INA125PA	16-Pin Plastic DIP	180
INA125P	16-Pin Plastic DIP	180
INA125UA	SO-16 Surface-Mount	265
INA125U	SO-16 Surface-Mount	265

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



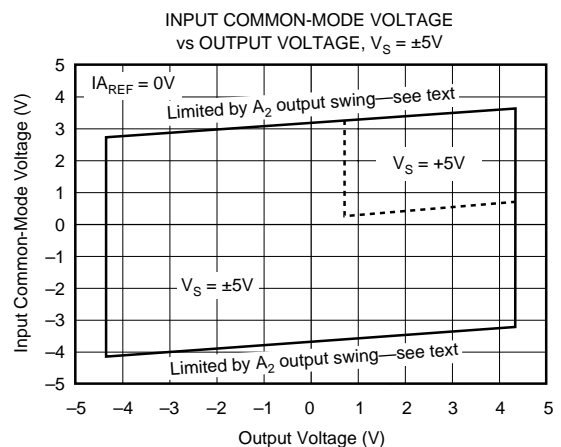
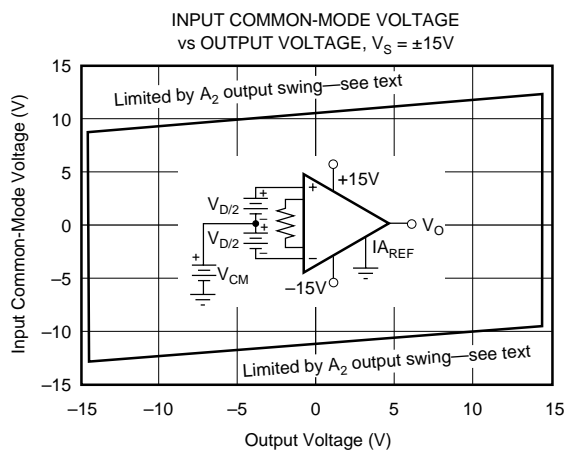
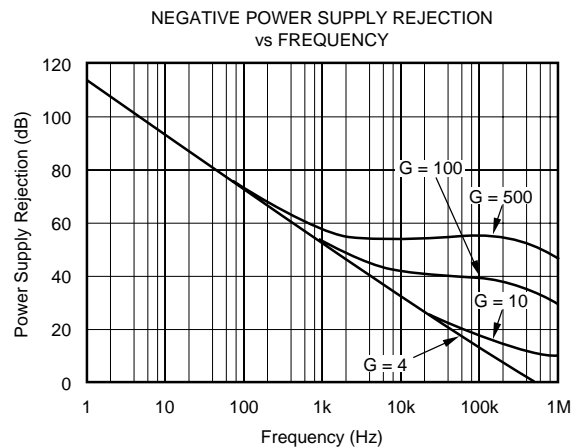
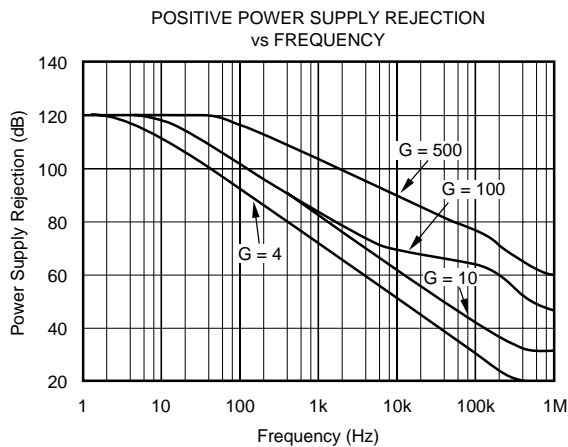
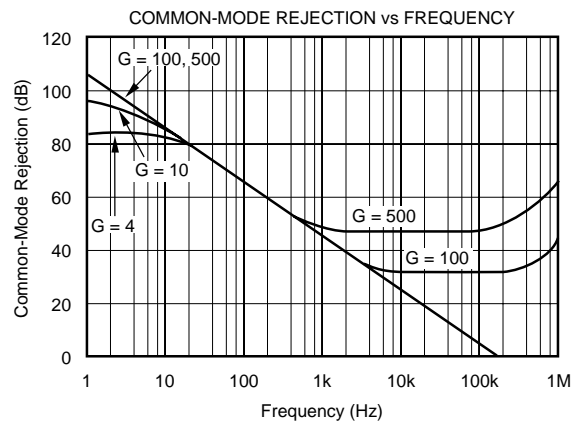
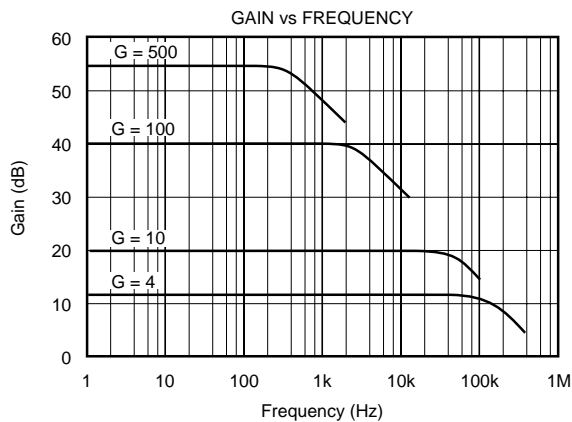
## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

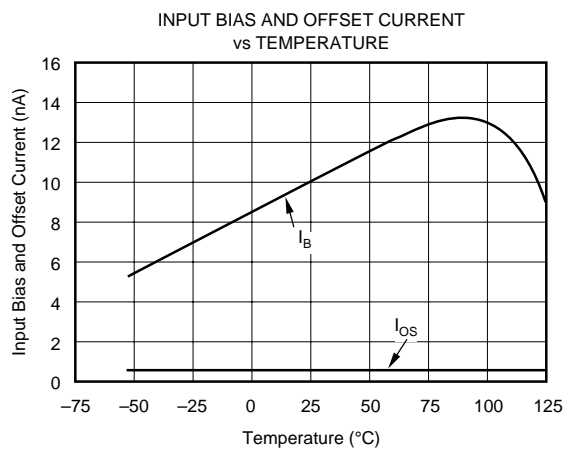
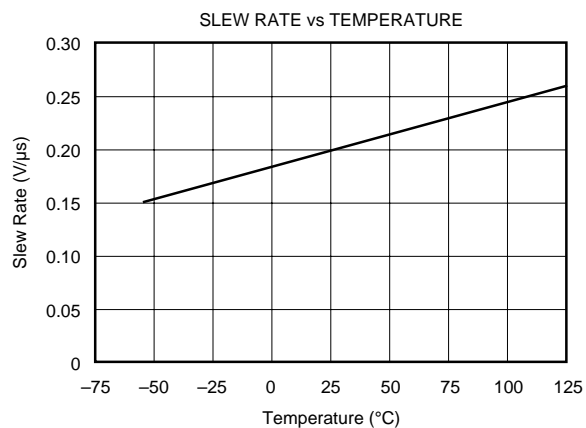
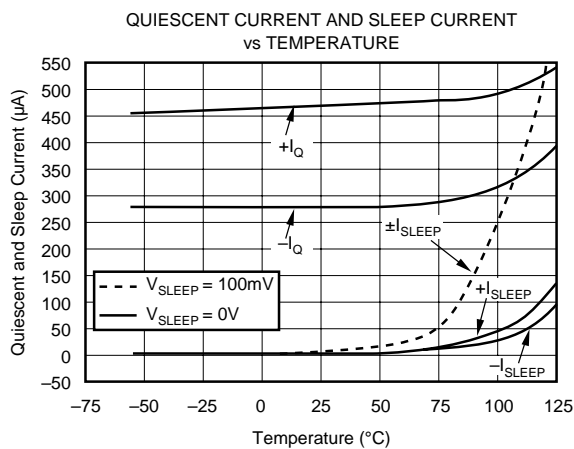
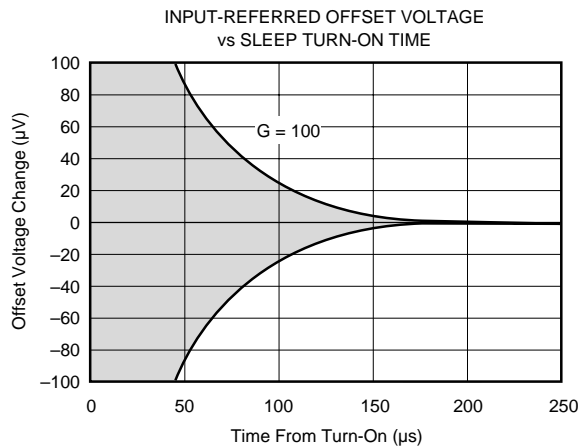
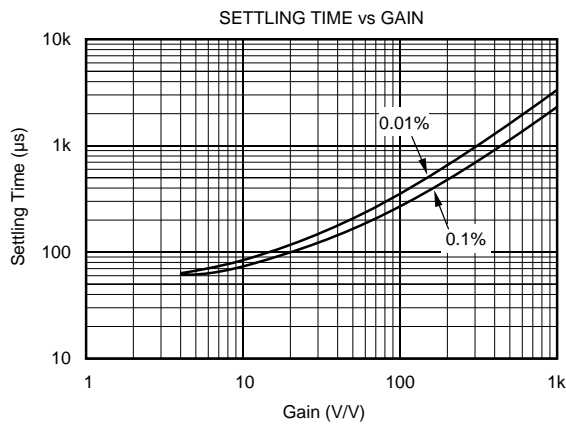
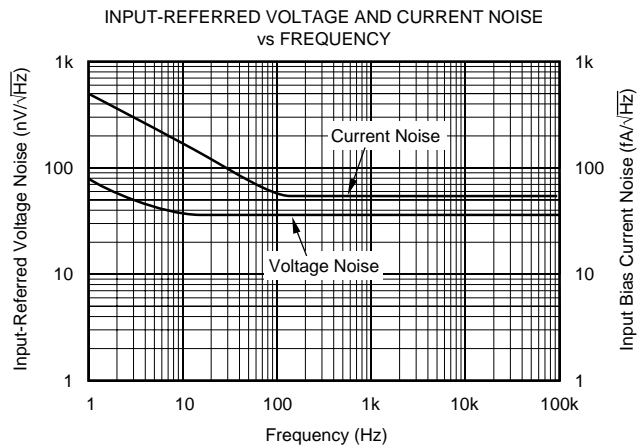
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

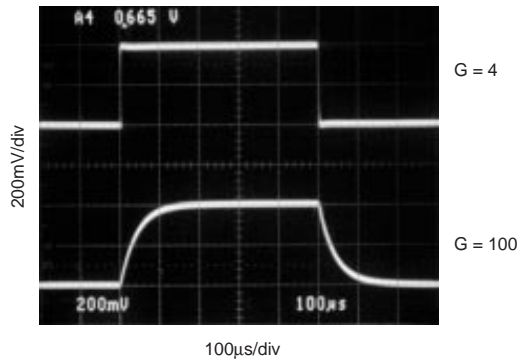
At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



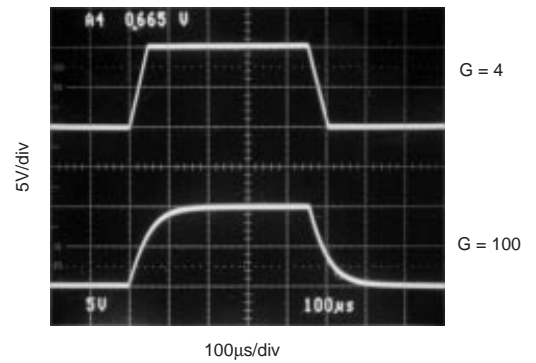
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

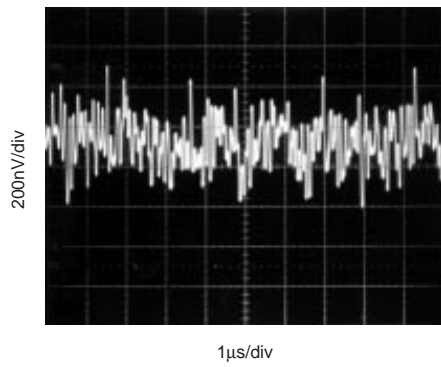
SMALL-SIGNAL RESPONSE



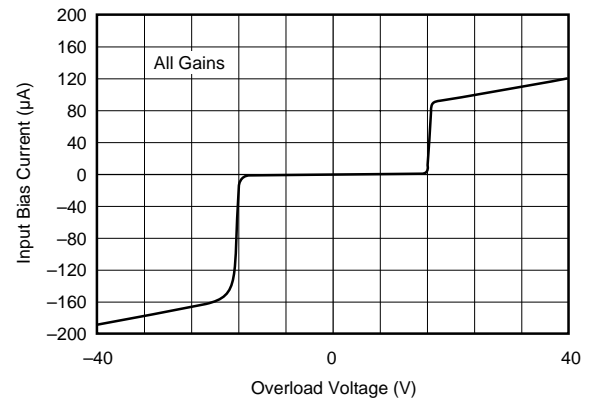
LARGE-SIGNAL RESPONSE



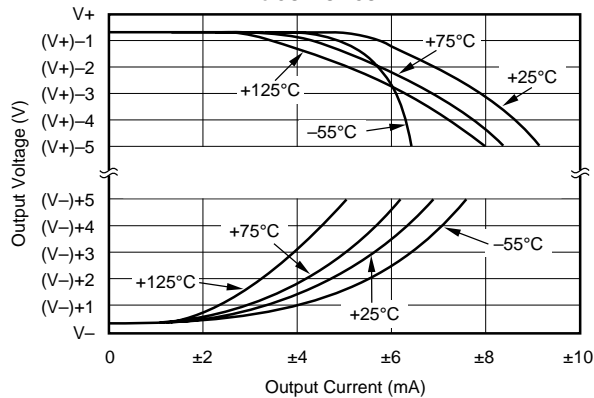
INPUT-REFERRED NOISE, 0.1Hz to 10Hz



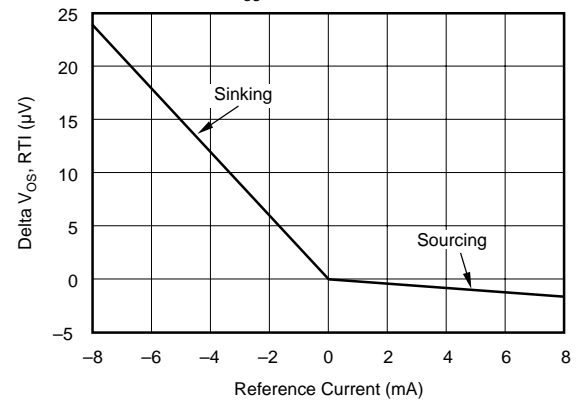
INPUT BIAS CURRENT  
vs INPUT OVERLOAD VOLTAGE



OUTPUT VOLTAGE SWING  
vs OUTPUT CURRENT

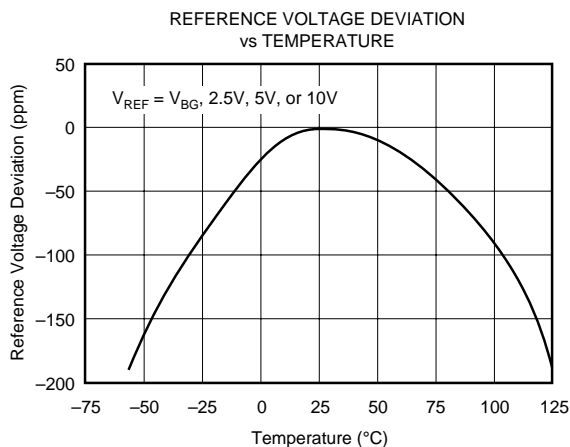
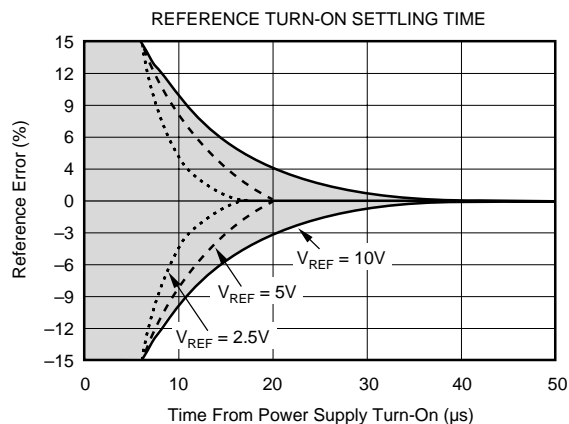
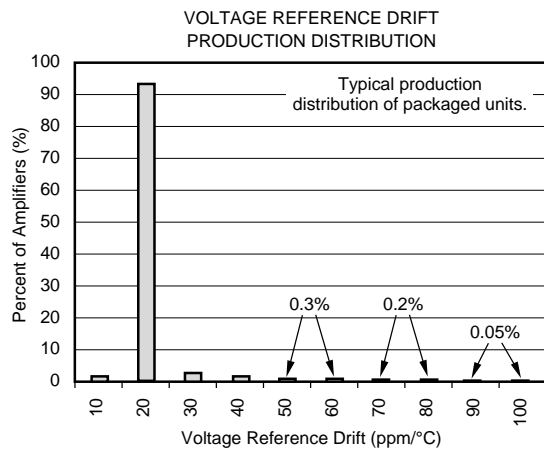
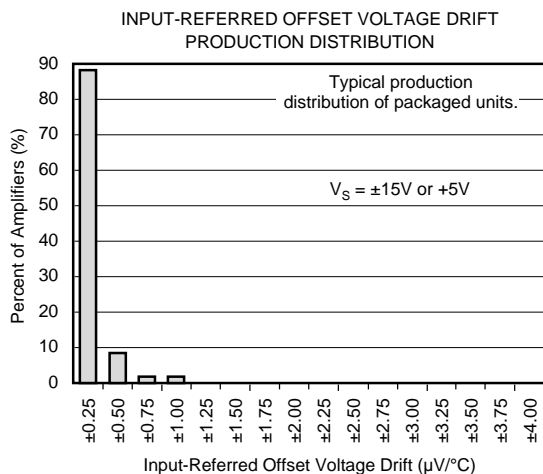
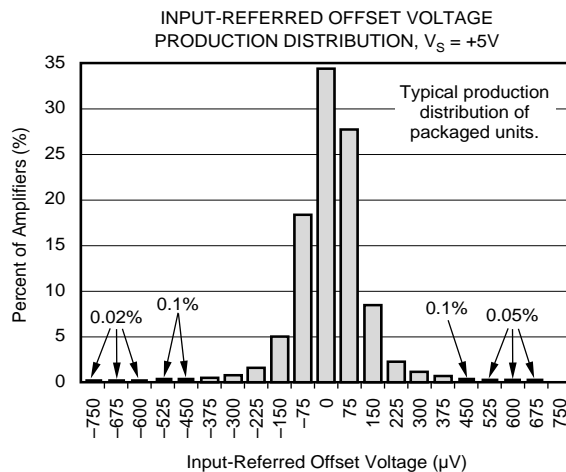
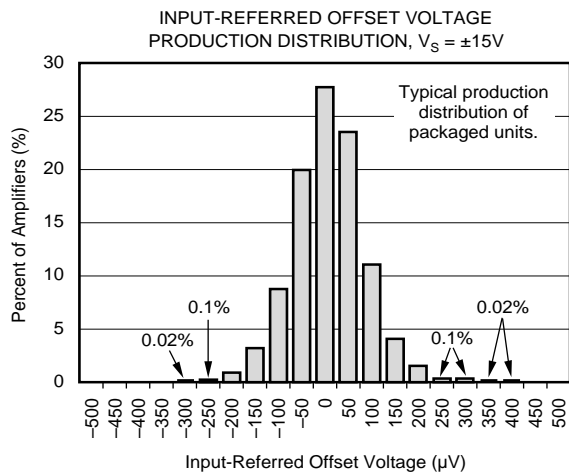


DELTA  $V_{OS}$  vs REFERENCE CURRENT



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

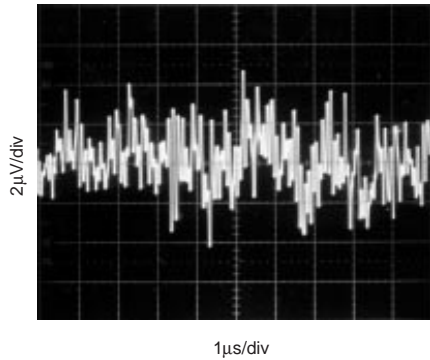




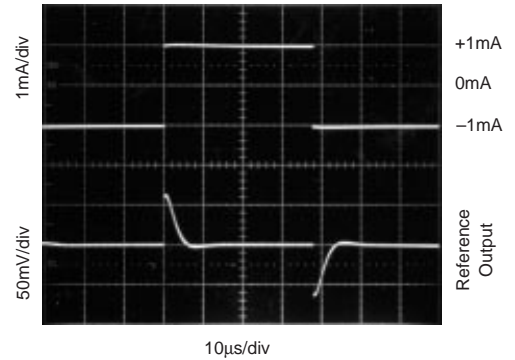
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$  and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

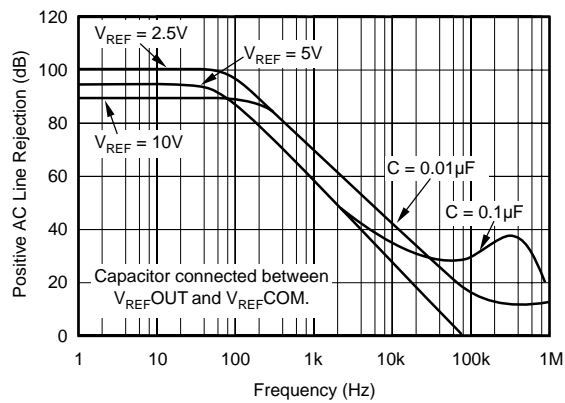
0.1Hz to 10Hz REFERENCE NOISE  
 $V_{REF} = 2.5\text{V}$ ,  $C_L = 100\text{pF}$



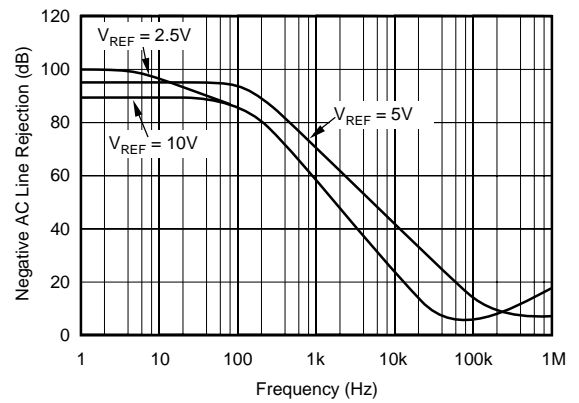
REFERENCE TRANSIENT RESPONSE  
 $V_{REF} = 2.5\text{V}$ ,  $C_L = 100\text{pF}$



POSITIVE REFERENCE AC LINE REJECTION  
vs FREQUENCY



NEGATIVE REFERENCE AC LINE REJECTION  
vs FREQUENCY



## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA125. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the instrumentation amplifier reference ( $IA_{REF}$ ) terminal which is normally grounded. This must be a low impedance connection to assure good common-mode rejection. A resistance of  $12\Omega$  in series with the  $IA_{REF}$  pin will cause a typical device to degrade to approximately 80dB CMR ( $G = 4$ ).

Connecting  $V_{REF}OUT$  (pin 4) to one of the four available reference voltage pins ( $V_{REF}BG$ ,  $V_{REF}2.5$ ,  $V_{REF}5$ , or  $V_{REF}10$ ) provides an accurate voltage source for bridge applications.

For example, in Figure 1  $V_{REF}OUT$  is connected to  $V_{REF}10$  thus supplying 10V to the bridge. It is recommended that  $V_{REF}OUT$  be connected to one of the reference voltage pins even when the reference is not being utilized to avoid saturating the reference amplifier. Driving the  $SLEEP$  pin LOW puts the INA125 in a shutdown mode.

### SETTING THE GAIN

Gain of the INA125 is set by connecting a single external resistor,  $R_G$ , between pins 8 and 9:

$$G = 4 + \frac{60k\Omega}{R_G} \quad (1)$$

Commonly used gains and  $R_G$  resistor values are shown in Figure 1.

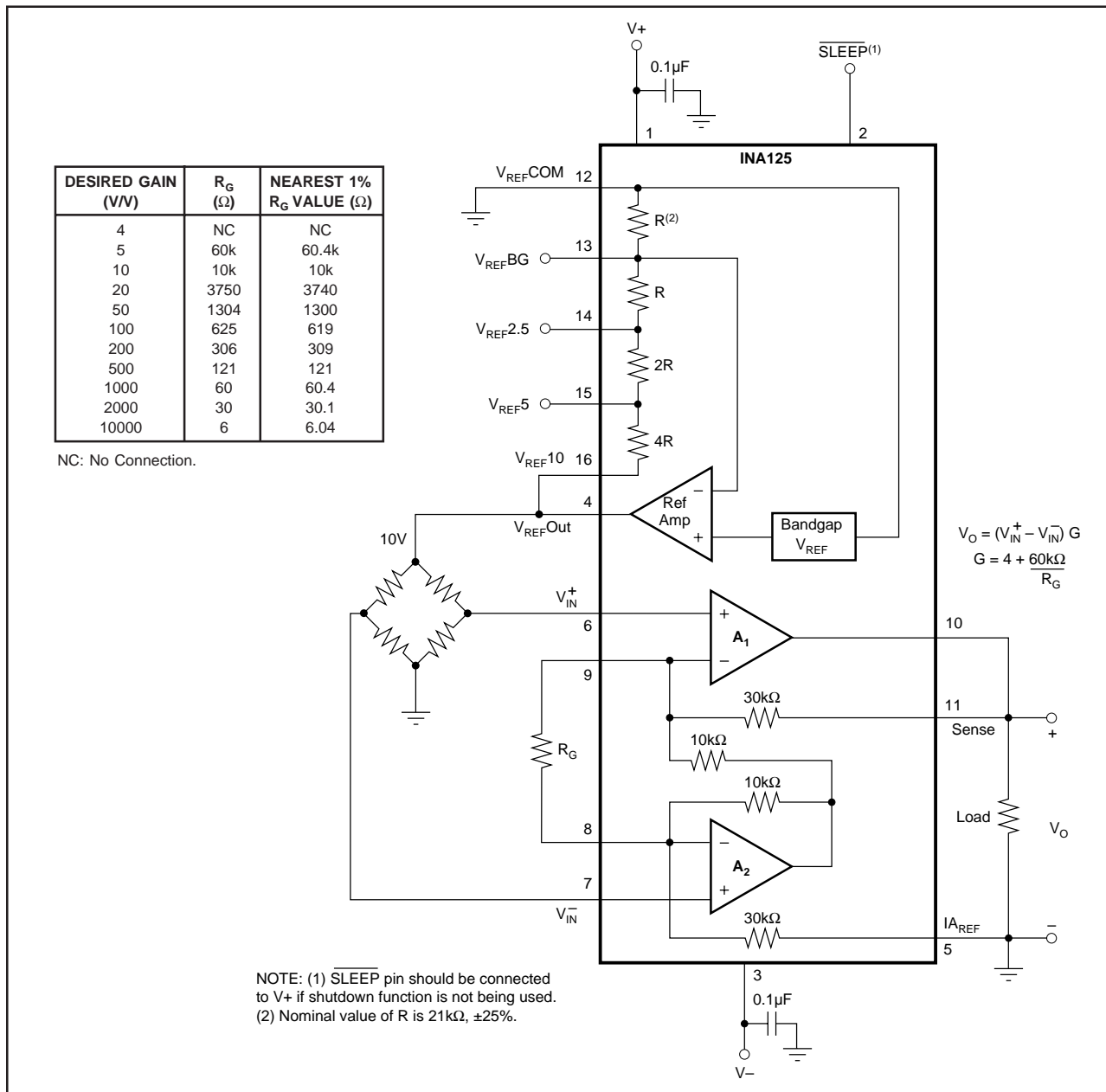


FIGURE 1. Basic Connections.

The 60k $\Omega$  term in equation 1 comes from the internal metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA125.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain.  $R_G$ 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

## OFFSET TRIMMING

The INA125 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the  $IA_{REF}$  terminal is added to the output signal. The op amp buffer is used to provide low impedance at the  $IA_{REF}$  terminal to preserve good common-mode rejection.

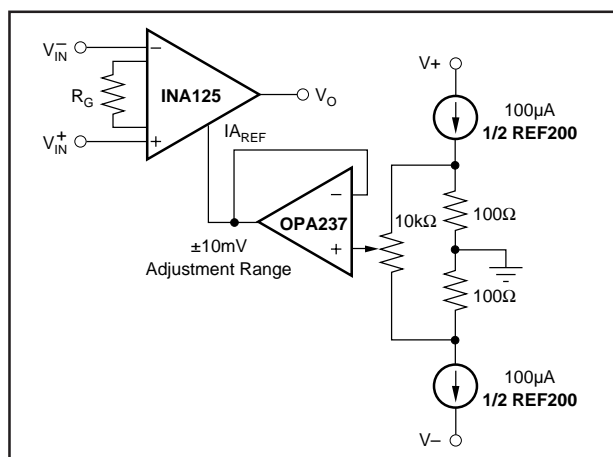


FIGURE 2. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN

The input impedance of the INA125 is extremely high—approximately  $10^{11}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current flows out of the device and is approximately 10nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high frequency common-mode rejection.

## INPUT COMMON-MODE RANGE

The input common-mode range of the INA125 is shown in the typical performance curves. The common-mode range is limited on the negative side by the output voltage swing of  $A_2$ , an internal circuit node that cannot be measured on an external pin. The output voltage of  $A_2$  can be expressed as:

$$V_{O2} = 1.3V_{IN}^- - (V_{IN}^+ - V_{IN}^-) (10k\Omega/R_G)$$

(voltages referred to  $IA_{REF}$  terminal, pin 5)

The internal op amp  $A_2$  is identical to  $A_1$ . Its output swing is limited to approximately 0.8V from the positive supply and 0.25V from the negative supply. When the input common-mode range is exceeded ( $A_2$ 's output is saturated),  $A_1$  can still be in linear operation, responding to changes in the non-inverting input voltage. The output voltage, however, will be invalid.

## PRECISION VOLTAGE REFERENCE

The on-board precision voltage reference provides an accurate voltage source for bridge and other transducer applications or ratiometric conversion with analog-to-digital converters. A reference output of 2.5V, 5V or 10V is available by connecting  $V_{REFOUT}$  (pin 4) to one of the  $V_{REF}$  pins ( $V_{REF2.5}$ ,  $V_{REF5}$ , or  $V_{REF10}$ ). Reference voltages are laser-trimmed for low initial error and low temperature drift. Connecting  $V_{REFOUT}$  to  $V_{REFBG}$  (pin 13) produces the bandgap reference voltage ( $1.24V \pm 0.5\%$ ) at the reference output.

Positive supply voltage must be 1.25V above the desired reference voltage. For example, with  $V+ = 2.7V$ , only the 1.24V reference ( $V_{REFBG}$ ) can be used. If using dual supplies  $V_{REFCOM}$  can be connected to  $V-$ , increasing the

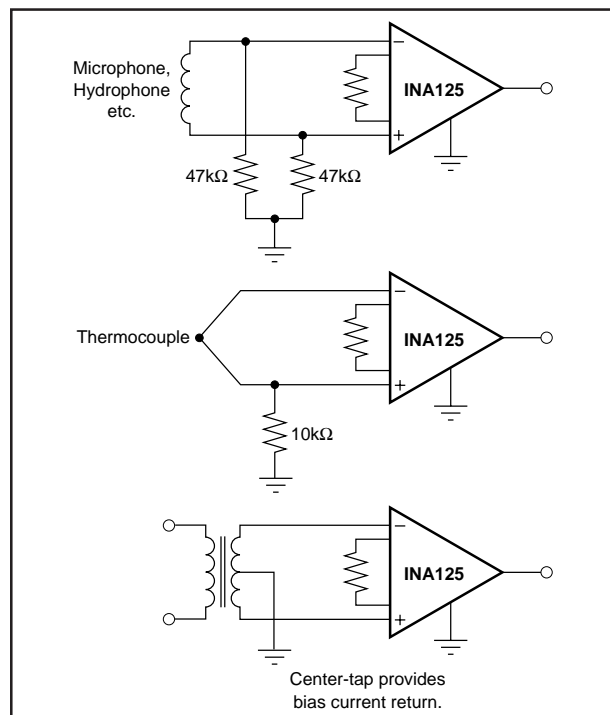


FIGURE 3. Providing an Input Common-Mode Current Path.

amount of supply voltage headroom available to the reference. Approximately 180 $\mu$ A flows out of the  $V_{REF}COM$  terminal, therefore, it is recommended that it be connected through a low impedance path to sensor common to avoid possible ground loop problems.

Reference noise is proportional to the reference voltage selected. With  $V_{REF} = 2.5V$ , 0.1Hz to 10Hz peak-to-peak noise is approximately 9 $\mu$ Vp-p. Noise increases to 36 $\mu$ Vp-p for the 10V reference. Output drive capability of the voltage reference is improved by connecting a transistor as shown in Figure 4. The external transistor also serves to remove power from the INA125.

Internal resistors that set the voltage reference output are ratio-trimmed for accurate output voltages ( $\pm 0.5\%$  max). The absolute resistance values, however, may vary  $\pm 25\%$ . Adjustment of the reference output voltage with an external resistor is not recommended because the required resistor value is uncertain.

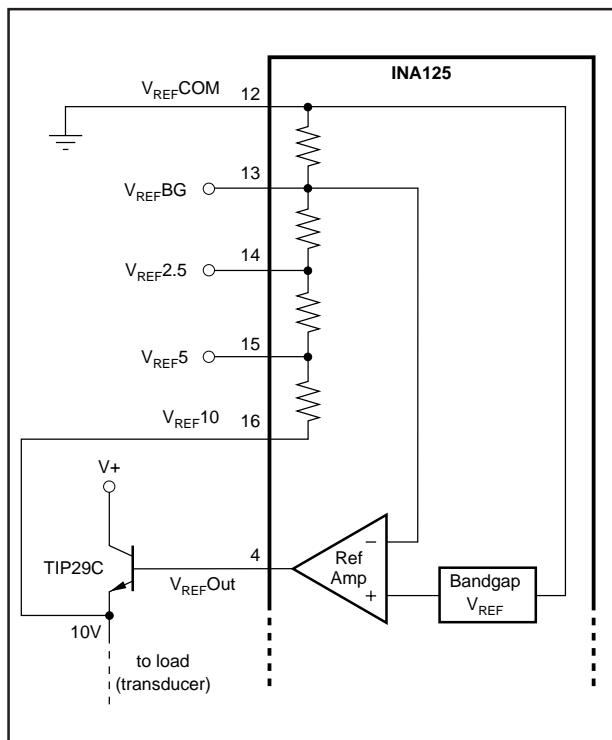


FIGURE 4. Reference Current Boost.

## SHUTDOWN

The INA125 has a shutdown option. When the  $\overline{SLEEP}$  pin is LOW (100mV or less), the supply current drops to approximately 1 $\mu$ A and output impedance becomes approximately 80k $\Omega$ . Best performance is achieved with CMOS logic. To maintain low sleep current at high temperatures,  $V_{SLEEP}$  should be as close to 0V as possible. This should not be a problem if using CMOS logic unless the CMOS gate is driving other currents. Refer to the typical performance curve, "Sleep Current vs Temperature."

A transition region exists when  $V_{SLEEP}$  is between 400mV and 2.7V (with respect to  $V_{REF}COM$ ) where the output is unpredictable. Operation in this region is not recommended. The INA125 achieves high accuracy quickly following wake-up ( $V_{SLEEP} \geq 2.7V$ ). See the typical performance curve "Input-Referred Offset Voltage vs Sleep Turn-on Time." If shutdown is not being used, connect the  $\overline{SLEEP}$  pin to  $V+$ .

## LOW VOLTAGE OPERATION

The INA125 can be operated on power supplies as low as  $\pm 1.35V$ . Performance remains excellent with power supplies ranging from  $\pm 1.35V$  to  $\pm 18V$ . Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to ensure that the common-mode voltage remains within its linear range. See "Input Common-Mode Voltage Range." As previously mentioned, when using the on-board reference with low supply voltages, it may be necessary to connect  $V_{REF}COM$  to  $V-$  to ensure  $V_S - V_{REF} \geq 1.25V$ .

## SINGLE SUPPLY OPERATION

The INA125 can be used on single power supplies of +2.7V to +36V. Figure 5 shows a basic single supply circuit. The  $IA_{REF}$ ,  $V_{REF}COM$ , and  $V-$  terminals are connected to ground. Zero differential input voltage will demand an output voltage of 0V (ground). When the load is referred to ground as shown, actual output voltage swing is limited to approximately 150mV above ground. The typical performance curve "Output Voltage Swing vs Output Current" shows how the output swing varies with output current.

With single supply operation, careful attention should be paid to input common-mode range, output voltage swing of both op amps, and the voltage applied to the  $IA_{REF}$  terminal.  $V_{IN+}$  and  $V_{IN-}$  must both be 1V above ground for linear operation. You cannot, for instance, connect the inverting input to ground and measure a voltage connected to the non-inverting input.

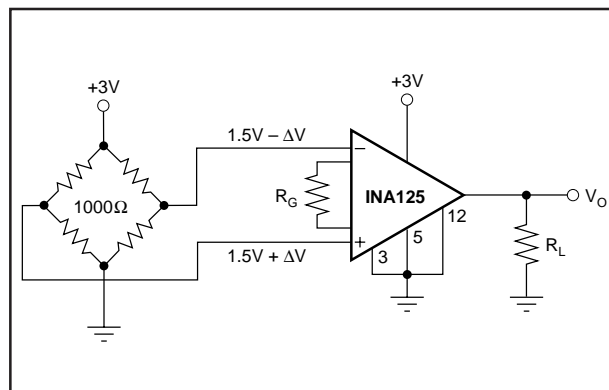


FIGURE 5. Single Supply Bridge Amplifier.

## INPUT PROTECTION

The inputs of the INA125 are individually protected for voltage up to  $\pm 40\text{V}$ . For example, a condition of  $-40\text{V}$  on one input and  $+40\text{V}$  on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute

excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately  $120\mu\text{A}$  to  $190\mu\text{A}$ . The typical performance curve “Input Bias Current vs Input Overload Voltage” shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

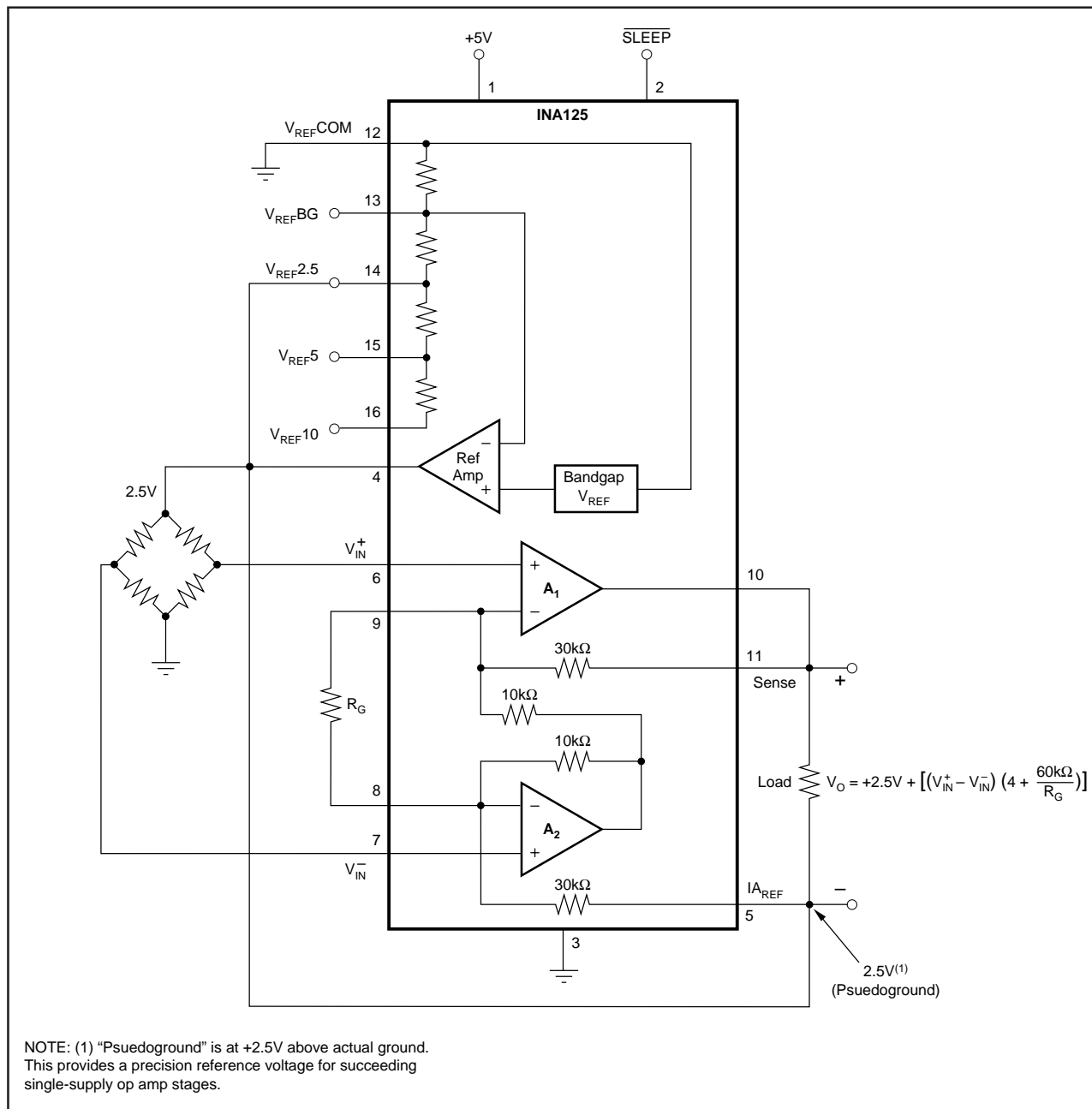


FIGURE 6. Psuedoground Bridge Measurement, 5V Single Supply.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA125P	ACTIVE	PDIP	N	16	25	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA125P	<a href="#">Samples</a>
INA125PA	ACTIVE	PDIP	N	16	25	RoHS & Green	Call TI	N / A for Pkg Type		INA125P A	<a href="#">Samples</a>
INA125PAG4	ACTIVE	PDIP	N	16	25	RoHS & Green	Call TI	N / A for Pkg Type		INA125P A	<a href="#">Samples</a>
INA125U	ACTIVE	SOIC	D	16	40	RoHS & Green	Call TI	Level-3-260C-168 HR		INA125U A	<a href="#">Samples</a>
INA125U/2K5	ACTIVE	SOIC	D	16	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA125U A	<a href="#">Samples</a>
INA125UA	ACTIVE	SOIC	D	16	40	RoHS & Green	Call TI	Level-3-260C-168 HR		INA125U A	<a href="#">Samples</a>
INA125UA/2K5	ACTIVE	SOIC	D	16	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA125U A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

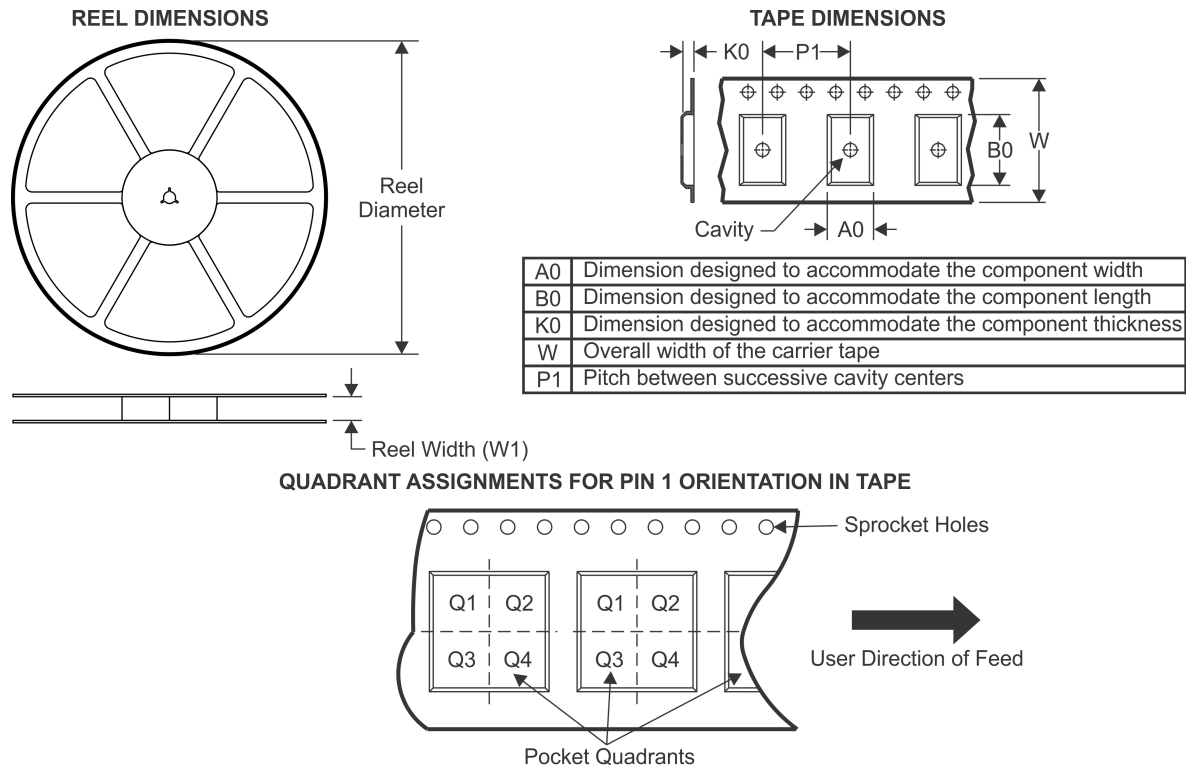
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

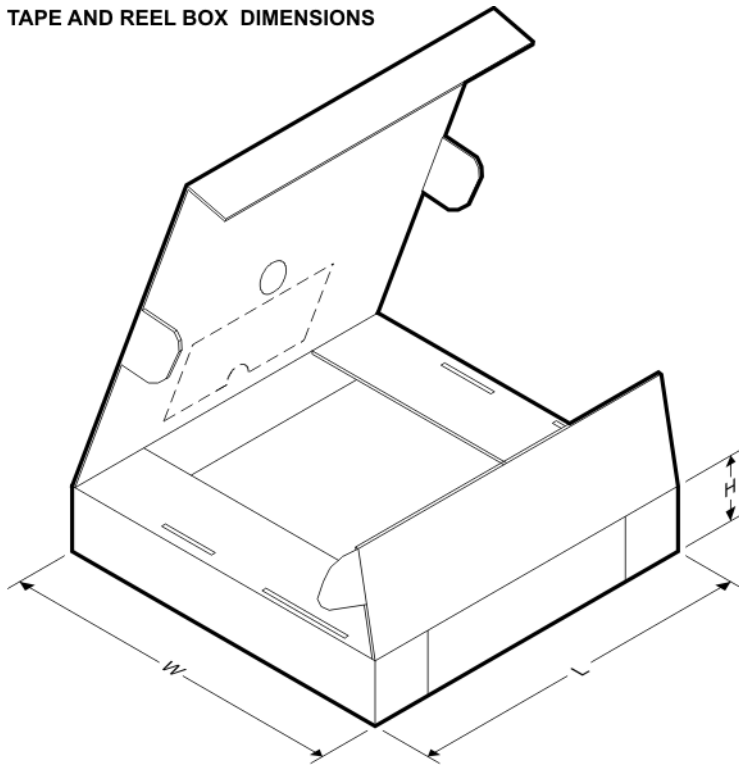


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA125U/2K5	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
INA125UA/2K5	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



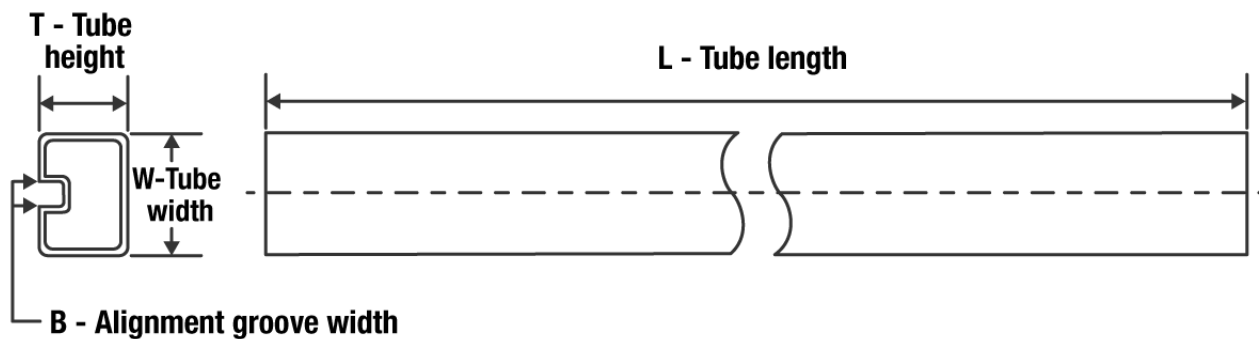
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA125U/2K5	SOIC	D	16	2500	853.0	449.0	35.0
INA125UA/2K5	SOIC	D	16	2500	853.0	449.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA125P	N	PDIP	16	25	506	13.97	11230	4.32
INA125PA	N	PDIP	16	25	506	13.97	11230	4.32
INA125PAG4	N	PDIP	16	25	506	13.97	11230	4.32
INA125U	D	SOIC	16	40	506.6	8	3940	4.32
INA125UA	D	SOIC	16	40	506.6	8	3940	4.32

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated