TPS389x 采用超小型封装的单通道可调电压监视器

1 特性

- 超小型 USON (1.45mm × 1.00mm) 封装
- 可调阈值低至 500mV
- 阈值精度：整个温度范围内为 1%
- 电容可调式延迟时间
- 低静态电流：6μA（典型值）
- 外部使能输入
- 开漏（额定值 18V）和推挽式输出选项
- 温度范围：–40°C 至 125℃
- 与 MAX6895/6/7/8 引脚到引脚兼容

2 应用

- 数字信号处理器 (DSP)、微控制器和微处理器
- 笔记本和台式计算机
- PDA 和手持式产品
- 便携式和电池供电类产品
- FPGA 和 ASIC

3 说明

TPS3895、TPS3896、TPS3897 和 TPS3898 器件（TPS389x 系列）为超小型监控电路，用于监视高于 500mV 的电压，阈值精度为 0.25%（典型值），且可通过外部电容调整延迟时间。 TPS389x 系列还具有用于导通和关断输出的逻辑使能引脚（ENABLE 或 $\overline{\text{ENABLE}}$）。 以 TPS3895 为例，当输入电压引脚 (SENSE) 的电压超出阈值且 ENABLE 引脚为高电平时，输出引脚 (SENSE_OUT) 将在一段电容可调式延迟时间后变为高电平。 当 SENSE 的电压降至阈值以下或 ENABLE 为低电平时，SENSE_OUT 将变为低电平。 有关真值表的信息，请参见表 1 和表 2。

对于 TPS389xA 版本，SENSE 和 ENABLE 均具有电容可调式延迟。 当 SENSE 和 ENABLE 输入正常时，输出将在经过这段电容可调式延迟时间后置为有效。对于 TPS389xP 器件，如果 SENSE 的电压超出阈值，则将使能引脚置为有效后，将经过短暂的 0.2μs 传播延迟后，输出引脚才会置为有效。

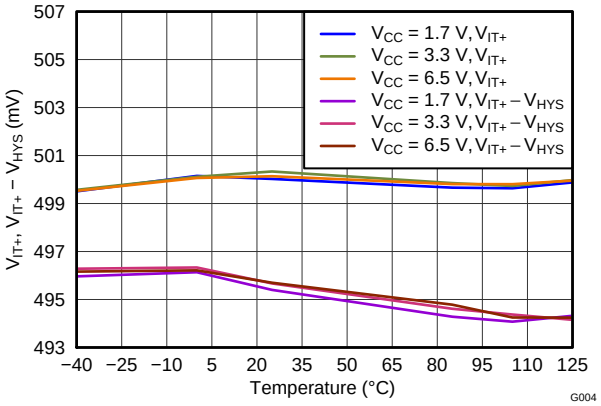
所有器件的工作电压范围均为 1.7V 至 6.5V，且具有 6μA 的静态电流典型值，开漏输出额定值为 18V。TPS389x 采用超小型 USON 封装，额定工作温度范围 T_J = –40°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS389x	USON (6)	1.45mm x 1.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

感测阈值电压和温度间的关系



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

Changes from Revision A (September 2011) to Revision B **Page**

- 已更改 *说明*部分的第 1 段；已修改说明 ... 1
- Changed *Pin Configuration and Functions* section; updated table format, renamed pin packages to meet new standards ... 4

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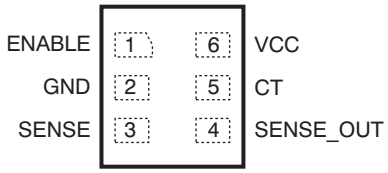
5 Device Comparison Table

DEVICE	ENABLE	OUTPUT	INPUT (SENSE) DELAY	ENABLE DELAY
TPS3895A	Active high	Active high, push-pull	Capacitor adjustable	Capacitor adjustable
TPS3895P	Active high	Active high, push-pull	Capacitor adjustable	0.2 µs
TPS3896A	Active low	Active low, push-pull	Capacitor adjustable	Capacitor adjustable
TPS3896P	Active low	Active low, push-pull	Capacitor adjustable	0.2 µs
TPS3897A	Active high	Active high, open drain	Capacitor adjustable	Capacitor adjustable
TPS3897P	Active high	Active high, open drain	Capacitor adjustable	0.2 µs
TPS3898A	Active low	Active low, open drain	Capacitor adjustable	Capacitor adjustable
TPS3898P	Active low	Active low, open drain	Capacitor adjustable	0.2 µs

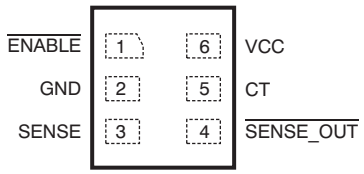
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6 Pin Configuration and Functions

DRY Package: TPS3895, TPS3897
6-Pin USON
Top View



DRY Package: TPS3896, TPS3898
6-Pin USON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	USON			
	TPS3895/ TPS3897	TPS3896/ TPS3898		
CT	5	5	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for SENSE rising above 0.5 V to SENSE_OUT asserting (or ENABLE asserting to SENSE_OUT asserting for A version devices). $t_{pd(r)}$ (s) = [C_{CT} (µF) × 4] + 40 µs
ENABLE	1	—	I	Active high input. Driving ENABLE low immediately makes SENSE_OUT go low, independent of $V_{(SENSE)}$. With $V_{(SENSE)}$ already above V_{IT+}, drive ENABLE high to make SENSE_OUT go high after the capacitor-adjustable delay time (A version) or 0.2 µs (P version).
$\overline{\text{ENABLE}}$	—	1	I	Active low input. Driving $\overline{\text{ENABLE}}$ high immediately makes $\overline{\text{SENSE_OUT}}$ go high, independent of $V_{(SENSE)}$. With $V_{(SENSE)}$ already above V_{IT+}, drive $\overline{\text{ENABLE}}$ low to make $\overline{\text{SENSE_OUT}}$ go low after the capacitor-adjustable delay time (A version) or 0.2 µs (P version).
GND	2	2	—	Ground
SENSE	3	3	I	This pin is connected to the voltage that is monitored with the use of an external resistor. The output asserts after the capacitor-adjustable delay time when $V_{(SENSE)}$ rises above 0.5 V and ENABLE is asserted. The output deasserts after a minimal propagation delay (16 µs) when $V_{(SENSE)}$ falls below $V_{IT+} – V_{hys}$.
SENSE_OUT	4	—	O	SENSE_OUT is an open-drain and push-pull output that is immediately driven low after $V_{(SENSE)}$ falls below ($V_{IT+} – V_{hys}$) or the ENABLE input is low. SENSE_OUT goes high after the capacitor-adjustable delay time when $V_{(SENSE)}$ is greater than V_{IT+} and the ENABLE pin is high. Open-drain devices (TPS3897/8) can be pulled up to 18 V independent of V_{CC}; pullup resistors are required for these devices.
$\overline{\text{SENSE_OUT}}$	—	4	O	$\overline{\text{SENSE_OUT}}$ is an open-drain and push-pull output that is immediately driven high after $V_{(SENSE)}$ falls below ($V_{IT+} – V_{hys}$) or the $\overline{\text{ENABLE}}$ input is high. $\overline{\text{SENSE_OUT}}$ goes low after the capacitor-adjustable delay time when $V_{(SENSE)}$ is greater than V_{IT+} and the $\overline{\text{ENABLE}}$ pin is low. Open-drain devices (TPS3897/8) can be pulled up to 18 V independent of V_{CC}; pullup resistors are required for these devices.
VCC	6	6	I	Supply voltage input. Connect a 1.7-V to 6.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage(2)	VCC	–0.3	7	V
	CT	–0.3	V_{CC} + 0.3	
	ENABLE, SENSE, SENSE_OUT (push-pull)	–0.3	7	
	SENSE_OUT (open drain)	–0.3	20	
	SENSE_OUT (push-pull)	–0.3	7	
Current	SENSE_OUT		±10	mA
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input supply voltage	1.7		6.5	V
V_{ENABLE}, $V_{\overline{ENABLE}}$	ENABLE and $\overline{ENABLE}$ pin voltage	0		6.5	V
V_{SENSE}	SENSE pin voltage	0		6.5	V
V_{SENSE_OUT}, $V_{\overline{SENSE_OUT}\ (open\ drain)}$	SENSE_OUT, $\overline{SENSE_OUT}$ pin voltage	0		18	V
V_{SENSE_OUT}, $V_{\overline{SENSE_OUT}\ (push\text{-}pull)}$	SENSE_OUT, $\overline{SENSE_OUT}$ pin voltage	0		V_{CC}	V
I_{SENSE_OUT}, $I_{\overline{SENSE_OUT}}$	SENSE_OUT, $\overline{SENSE_OUT}$ pin current	0.0003		1	mA

7.4 Thermal Information

THERMAL METRIC(1)		TPS389x DRY (USON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	293.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	165.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	160.8	
ψ_{JT}	Junction-to-top characterization parameter	27.3	
ψ_{JB}	Junction-to-board characterization parameter	65.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	65.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, and 1.7 V < V_{CC}< 6.5 V, unless otherwise noted. Typical values are at T_J = 25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	T_J = –40°C to 125°C	1.7		6.5	V
		T_J = 0°C to 85°C	1.65		6.5	
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} (max) = 0.2 V , $I_{(SENSE_OUT)}$ = 15 µA			0.8	V
I_{CC}	Supply current (into VCC pin)	V_{CC} = 3.3 V , no load		6	12	µA
		V_{CC} = 6.5 V , no load		7	12	
V_{IT+}	Positive-going input threshold voltage	$V_{(SENSE)}$ rising	0.495	0.5	0.505	V
V_{hys}	Hysteresis voltage	$V_{(SENSE)}$ falling		5		mV
$I_{(SENSE)}$	Input current(2)	$V_{(SENSE)}$ = 0 V or V_{CC}	–15		15	nA
$I_{(CT)}$	CT pin charge current		260	310	360	nA
$V_{(CT)}$	CT pin comparator threshold voltage		1.18	1.238	1.299	V
$R_{(CT)}$	CT pin pulldown resistance			200		Ω
V_{IL}	Low-level input voltage (ENABLE pin)				0.4	V
V_{IH}	High-level input voltage (ENABLE pin)		1.4			V
UVLO	Undervoltage lockout(3)	V_{CC} falling	1.3		1.7	V
I_{lkg}	Leakage current	ENABLE = V_{CC} or GND	–100		100	nA
V_{OL}	Low-level output voltage	V_{CC} ≥ 1.2 V, I_{SINK} = 90 µA (TPS3895/7 only)			0.3	V
		V_{CC} ≥ 2.25 V, I_{SINK} = 0.5 mA			0.3	
		V_{CC} ≥ 4.5 V, I_{SINK} = 1 mA			0.4	
V_{OH}	High-level output voltage (push-pull)	V_{CC} ≥ 2.25 V, I_{SOURCE} = 0.5 mA	0.8V_{CC}			V
		V_{CC} ≥ 4.5 V, I_{SOURCE} = 1 mA	0.8V_{CC}			
$I_{lkg(OD)}$	Open-drain output leakage current	$V_{(SENSE_OUT)}$ high impedance = 18 V			300	nA

(1) The lowest supply voltage (V_{CC}) at which output is active (SENSE_OUT is low, $\overline{\text{SENSE_OUT}}$ is high); $t_r(V_{CC})$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) Specified by design.
(3) When V_{CC} falls below the UVLO threshold, the output deasserts (SENSE_OUT goes low, $\overline{\text{SENSE_OUT}}$ goes high). Below $V_{(POR)}$, the output cannot be determined.

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7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
$t_{pd(r)}$	SENSE (rising) to SENSE_OUT propagation delay	$V_{(SENSE)}$ rising, $C_{(CT)}$ = open		40		µs
		$V_{(SENSE)}$ rising, $C_{(CT)}$ = 0.047 µF		190		ms
$t_{pd(f)}$	SENSE (falling) to SENSE_OUT propagation delay	$V_{(SENSE)}$ falling		16		µs
	Start-up delay(1)			50		µs
t_w	ENABLE pin minimum pulse duration		1			µs
	ENABLE pin glitch rejection			100		ns
$t_{d(OFF)}$	ENABLE to SENSE_OUT delay time (output disabled)	ENABLE deasserted to output deasserted		200		ns
$t_{d(P)}$	ENABLE to SENSE_OUT delay time (P version)	ENABLE asserted to output asserted delay (P version)		200		ns
$t_{d(A)}$	ENABLE to SENSE_OUT delay time (A version)	ENABLE asserted to output asserted delay (A version), $C_{(CT)}$ = open		20		µs
		ENABLE asserted to output asserted delay (A version), $C_{(CT)}$ = 0.047 µF		190		ms

(1) During power on, V_{CC} must exceed 1.7 V for at least 50 µs (plus propagation delay time, $t_{pd(r)}$) before output is in the correct state.

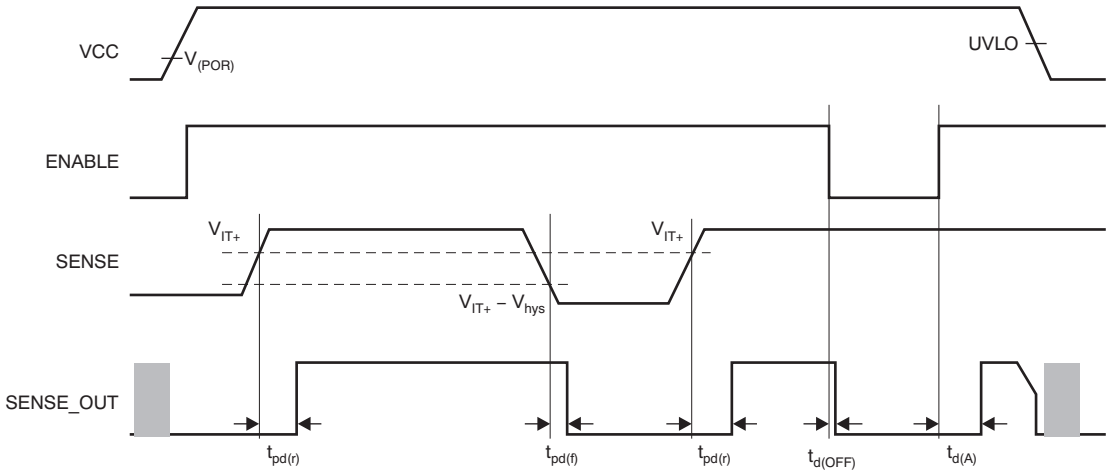


图 1. TPS3895A and TPS3897A Timing

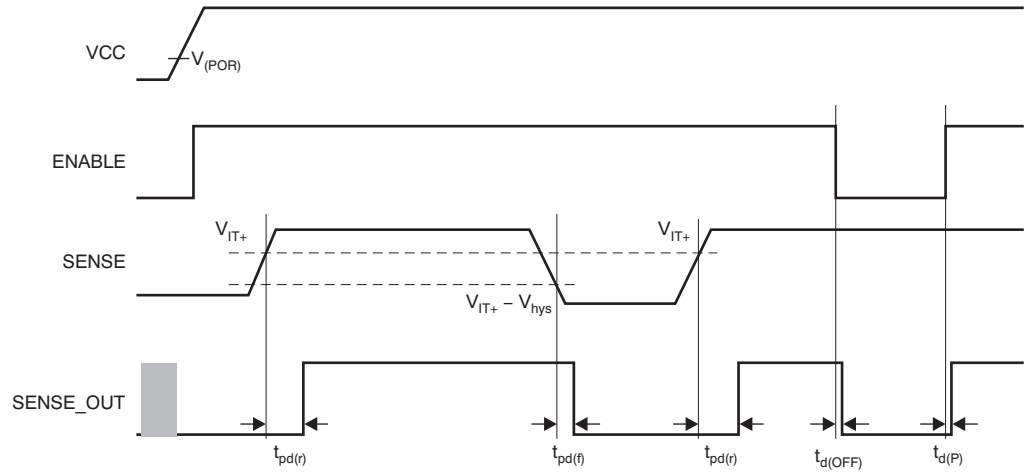


图 2. TPS3895P and TPS3897P Timing

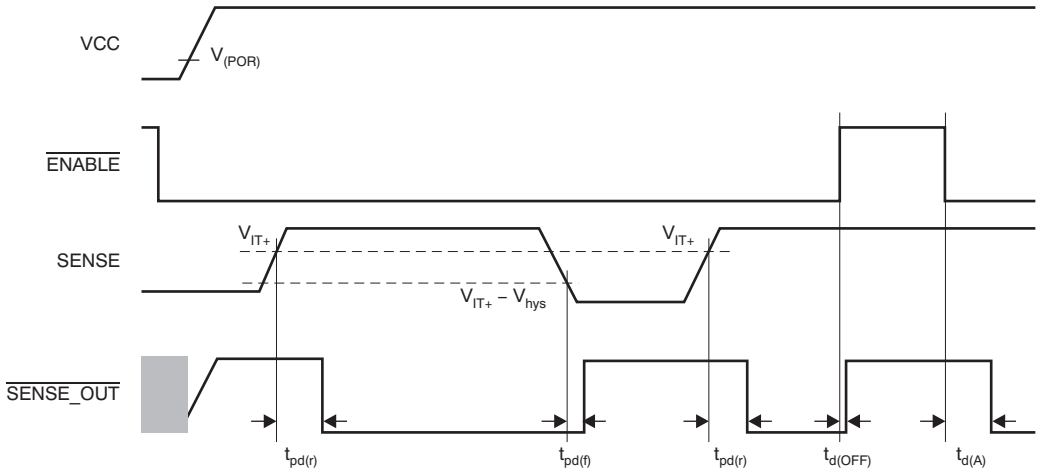


图 3. TPS3896A and TPS3898A Timing

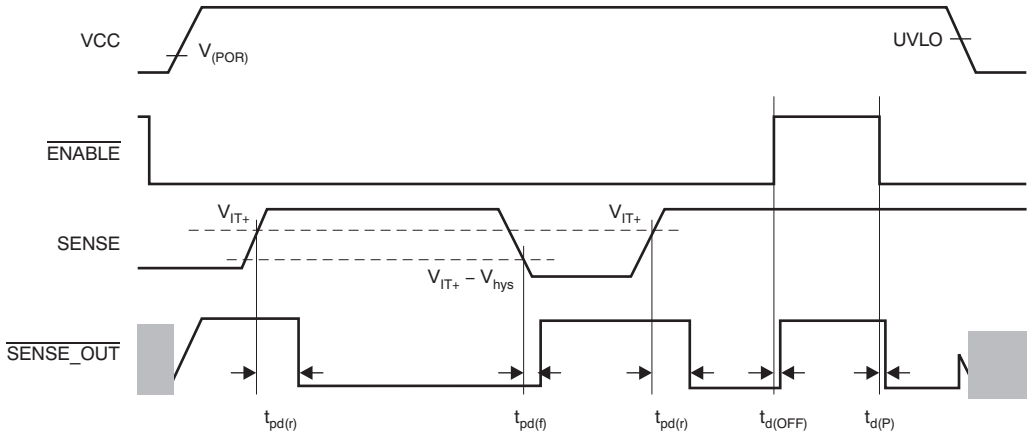


图 4. TPS3896P and TPS3898P Timing

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7.7 Typical Characteristics

At T_A = 25°C, and V_{CC} = 3.3 V, unless otherwise noted.

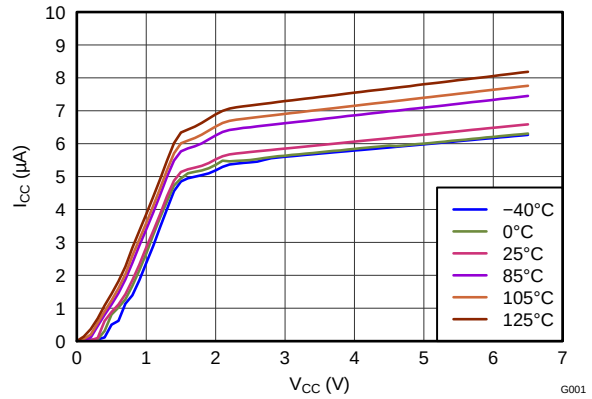


图 5. Supply Current vs Supply Voltage

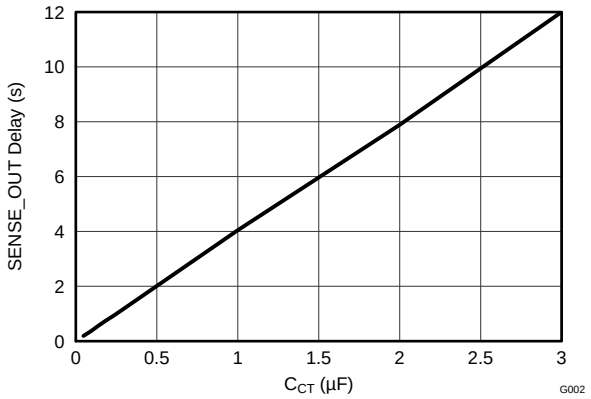


图 6. SENSE_OUT Time-Out Period vs C_{CT}

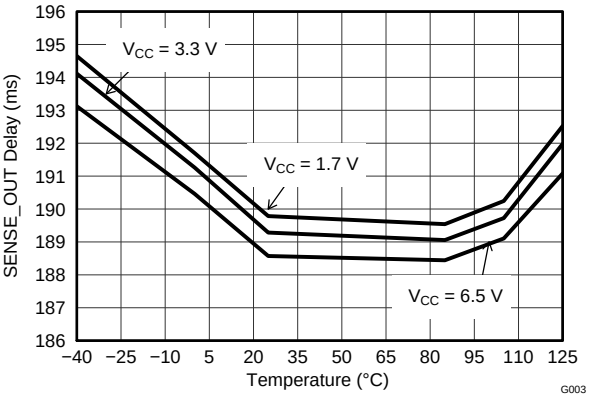


图 7. SENSE_OUT Time-Out Period vs Temperature (C_{CT} = 47 nF)

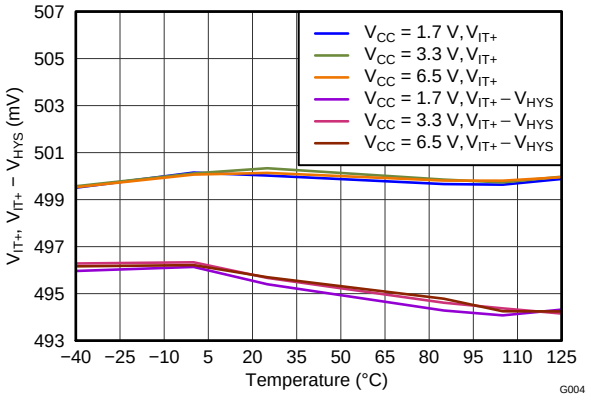


图 8. SENSE Threshold Voltage vs Temperature

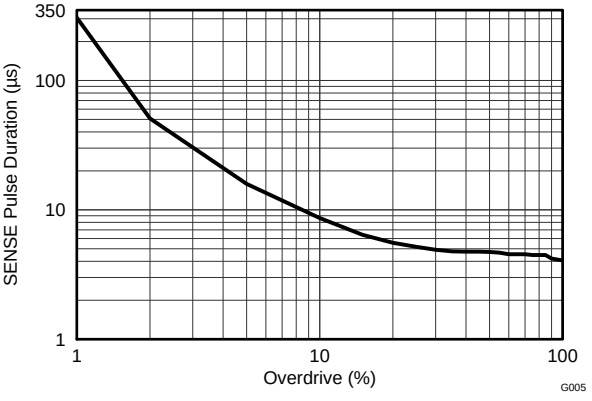


图 9. SENSE Minimum Pulse Duration vs SENSE Threshold Overdrive Voltage

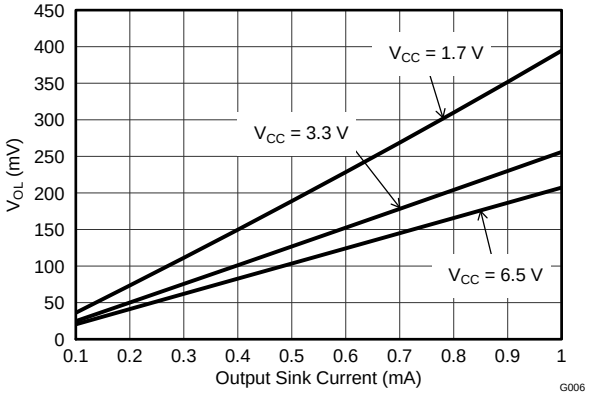


图 10. Output Voltage Low vs Output Current (0 mA to 1 mA)

Typical Characteristics (接下页)

At T_A = 25°C, and V_{CC} = 3.3 V, unless otherwise noted.

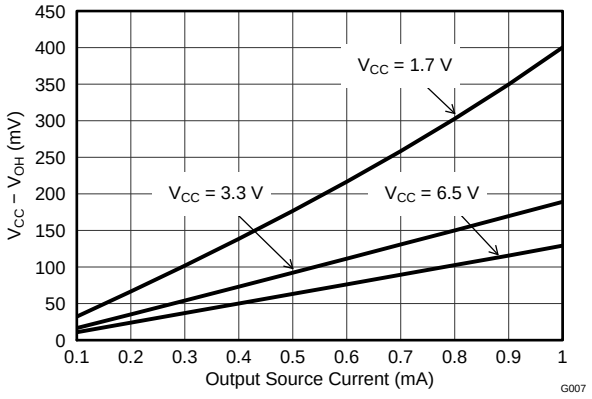


图 11. Output Voltage High vs Output Current (0 mA to 1 mA)

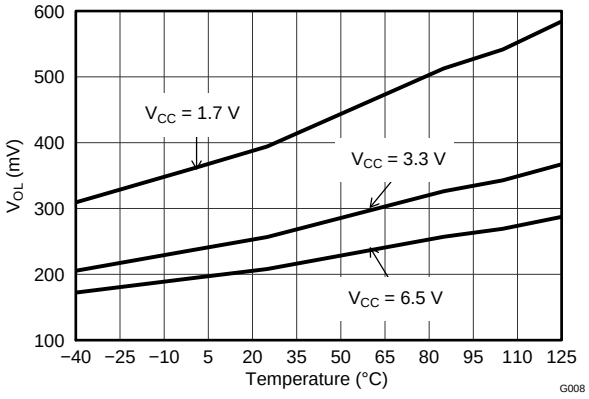


图 12. Output Voltage Low at 1 mA vs Temperature

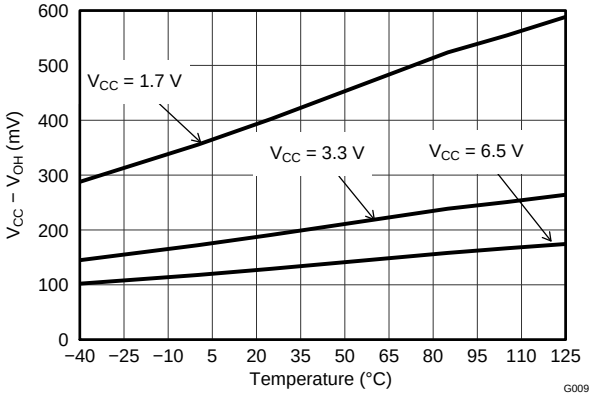


图 13. Output Voltage High at 1 mA vs Temperature

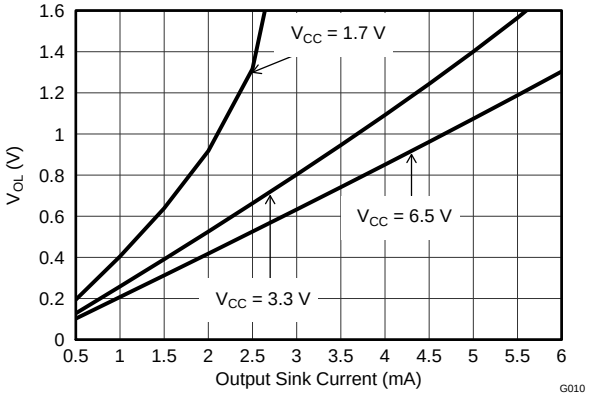


图 14. Output Voltage Low vs Output Current

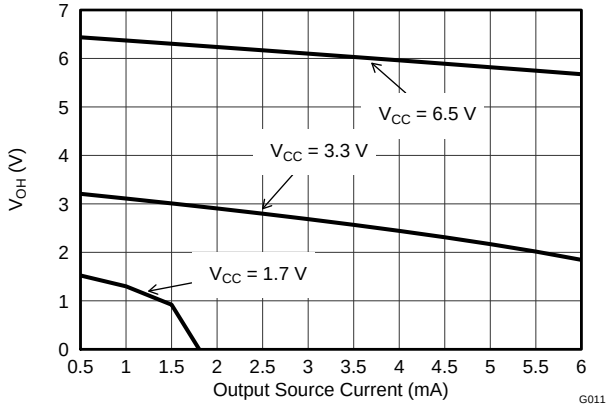


图 15. Output Voltage High vs Output Current

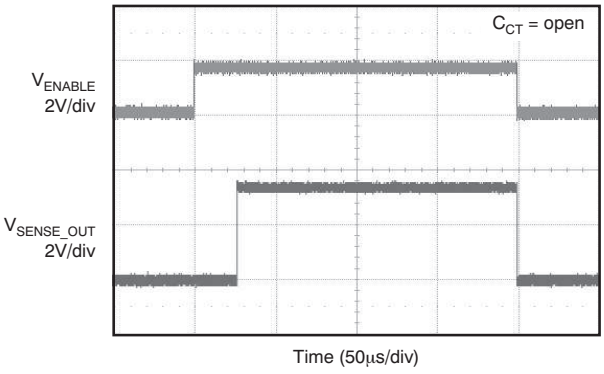


图 16. Enable Power On and Power Off Delay (TPS3895A)

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Typical Characteristics (接下页)

At T_A = 25°C, and V_{CC} = 3.3 V, unless otherwise noted.

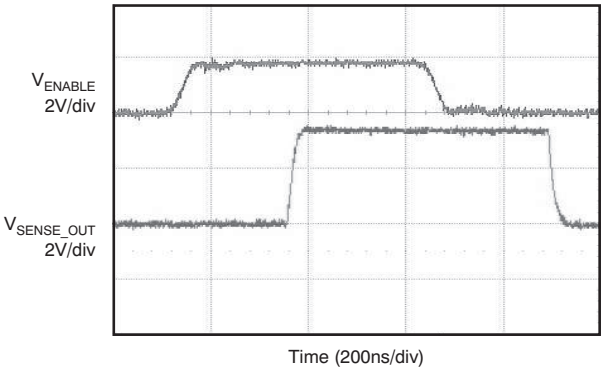


图 17. Enable Power On and Power Off Delay (TPS3895P)

8 Detailed Description

8.1 Overview

The TPS3895, TPS3896, TPS3897, and TPS3898 devices (TPS389x) are a family of ultra-small supervisory circuits. The TPS389x is designed to assert the SENSE_OUT or $\overline{\text{SENSE_OUT}}$ signal, as shown in 表 1 and 表 2. When the SENSE pin rises above 0.5 V and the enable input is asserted (ENABLE = high or $\overline{\text{ENABLE}}$ = low) , the output asserts (SENSE_OUT goes high or $\overline{\text{SENSE_OUT}}$ goes low) after the capacitor-adjustable delay time. The SENSE pin can be set to any voltage threshold above 0.5 V using an external resistor divider. A broad range of output delay times and voltage thresholds can be supported, allowing these devices to be used in wide array of applications.

表 1. TPS3895/7 Truth Table

CONDITIONS		OUTPUT	STATUS
ENABLE = high	SENSE < V_{IT+}	SENSE_OUT = low	Output not asserted
ENABLE = low	SENSE < V_{IT+}	SENSE_OUT = low	Output not asserted
ENABLE = low	SENSE > V_{IT+}	SENSE_OUT = low	Output not asserted
ENABLE = high	SENSE > V_{IT+}	SENSE_OUT = high	Output asserted after delay

表 2. TPS3896/8 Truth Table

CONDITIONS		OUTPUT	STATUS
$\overline{\text{ENABLE}}$ = low	SENSE < V_{IT+}	$\overline{\text{SENSE_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = high	SENSE < V_{IT+}	$\overline{\text{SENSE_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = high	SENSE > V_{IT+}	$\overline{\text{SENSE_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = low	SENSE > V_{IT+}	$\overline{\text{SENSE_OUT}}$ = low	Output asserted after delay

8.2 Functional Block Diagram

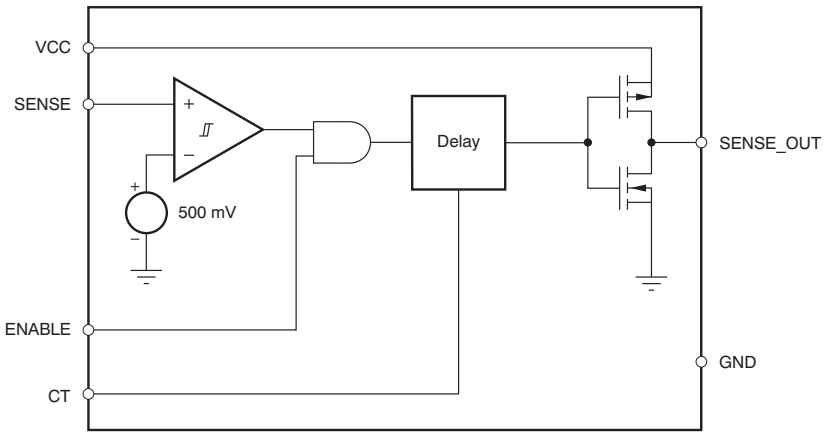


图 18. TPS3895A Block Diagram

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Functional Block Diagram (接下页)

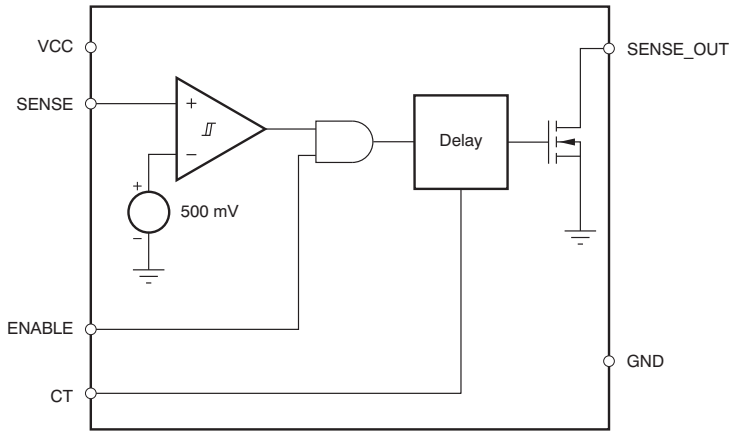


图 19. TPS3897A Block Diagram

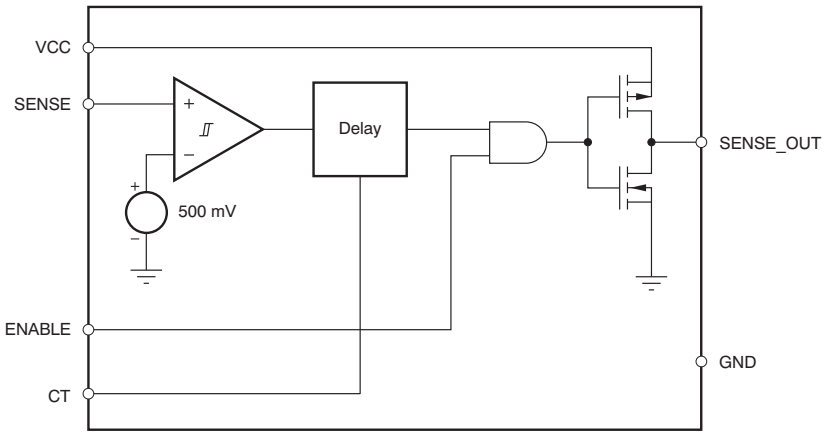


图 20. TPS3895P Block Diagram

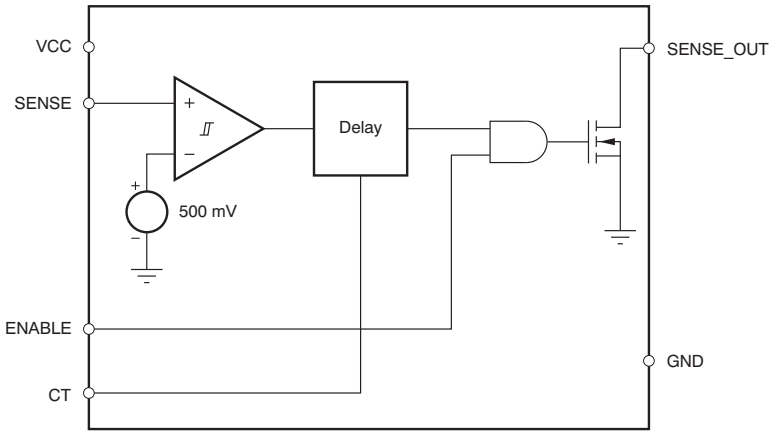


图 21. TPS3897P Block Diagram

8.3 Feature Description

8.3.1 Input Pin (SENSE)

The SENSE input pin allows any system voltage above 0.5 V to be monitored. If the voltage at the SENSE pin exceeds V_{IT+}, and provided that the enable pin is asserted (ENABLE = high or $\overline{\text{ENABLE}}$ = low), then the output is asserted after the capacitor-adjustable delay time elapses. When the voltage at the SENSE pin drops below (V_{IT+} – V_{hys}), then the output is deasserted. The comparator has a built-in hysteresis to ensure smooth output assertions and deassertions. Although not required in most cases, for extremely noisy applications, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the SENSE input in order to reduce sensitivity to transients and layout parasitics.

The TPS389x family monitor the voltage at SENSE with the use of external resistor divider, as shown in 图 22.

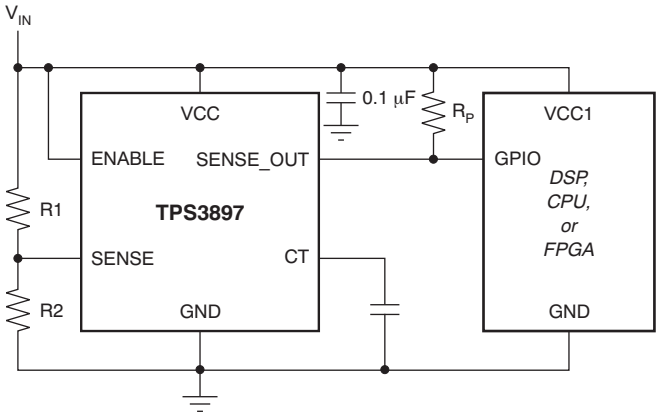


图 22. Using TPS3897 to Monitor User-Defined Threshold Voltage

The target threshold voltage can be calculated by using 公式 1:

$$V_{TARGET} = (1+R1/R2) \times 0.5\ (V) \quad (1)$$

When the input voltage (V_{IN}) shown in 图 22 is greater than V_{TARGET}, then the output is asserted, provided that the enable pin is asserted (ENABLE = high or $\overline{\text{ENABLE}}$ = low). R1 and R2 can have high values (> 100 kΩ) to minimize current consumption as a result of a low SENSE input current without adding significant error to the resistive divider. Refer to application note SLVA450 to learn more about sizing sense-point resistors.

8.3.2 Enable Pin (ENABLE)

The enable input allows an external logic signal from other processors, logic circuits, and/or discrete sensors to turn on or turn off the output. The TPS3895 and TPS3897 offer an active-high enable input (ENABLE). The TPS3896 and TPS3898 offer an active-low enable input ($\overline{\text{ENABLE}}$). Driving ENABLE low (or $\overline{\text{ENABLE}}$ high) forces SENSE_OUT to go low (or $\overline{\text{SENSE_OUT}}$ to go high). The 0.4-V (maximum) low and 1.4-V (minimum) high allow ENABLE to be driven with a 1.5-V or greater system supply.

The TPS389x family is available in two versions: the TPS389xA and TPS389xP. For TPS389xA devices with $V_{SENSE} > V_{IT+}$, driving ENABLE high (or $\overline{\text{ENABLE}}$ = low) makes SENSE_OUT go high (or $\overline{\text{SENSE_OUT}}$ go low) after the capacitor-adjustable delay time. For the TPS389xP versions with $V_{SENSE} > V_{IT+}$, driving ENABLE high (or $\overline{\text{ENABLE}}$ low) makes SENSE_OUT go high (or $\overline{\text{SENSE_OUT}}$ go low) after a 0.2-µs delay.

8.3.3 Output Pin (SENSE_OUT)

In a typical TPS389x application, the SENSE_OUT or $\overline{\text{SENSE_OUT}}$ outputs are connected to a reset/enable input of the processor (DSP, CPU, FPGA, ASIC, and so on) or connected to the enable input of a voltage regulator.

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Feature Description (接下页)

The TPS3897 and TPS3898 provide open-drain outputs. Pullup resistors must be used to hold these lines high when SENSE_OUT is asserted or $\overline{\text{SENSE_OUT}}$ is not asserted. By connecting the pullup resistors to the proper voltage rails, SENSE_OUT or $\overline{\text{SENSE_OUT}}$ can be connected to other devices at the correct interface voltage levels. The outputs can be pulled up to 18 V independent of the supply voltage (V_{CC}). To ensure proper voltage levels, some thought should be given to choosing the correct pullup resistor values. The ability to sink current is determined by the supply voltage; therefore, if V_{CC} = 5 V and the desired output pullup is 18 V, then to obtain a sink current of 1 mA or less (as mentioned in the *Electrical Characteristics*), the pullup resistor value should be greater than 18 kΩ. By using wired-OR logic, any combination of SENSE_OUT can be merged into one logic signal.

The TPS3895 and TPS3896 provide push-pull outputs. The logic high level of the outputs is determined by the VCC pin voltage. With this configuration, pullup resistors are not required and some board area can be saved. However, all the interface logic levels must be examined. All the SENSE_OUT and $\overline{\text{SENSE_OUT}}$ connections must be compatible with the VCC pin logic level.

The SENSE_OUT or $\overline{\text{SENSE_OUT}}$ outputs are defined for a VCC voltage higher than 0.8 V. 表 1 and 表 2 are truth tables that describe how the outputs are asserted or deasserted. When the conditions are met, the device changes state from deasserted to asserted after a preconfigured delay time. However, the transitions from asserted to deasserted are performed almost immediately with minimal propagation delay of 16 µs (typical). 图 1 to 图 4 show the timing diagrams and describe the relationship between the threshold voltages (V_{IT+} and V_{hys}), enable inputs, and respective outputs.

8.3.4 Output Delay Time Pin (CT)

To program a user-defined, adjustable delay time, an external capacitor must be connected between the CT pin and GND. If the CT pin is left open, there will be a delay of 40 µs. The adjustable delay time can be calculated through 公式 2:

$$t_{pd(r)}\ (s) = [C_{CT}\ (\mu F) \times 4] + 40\ \mu s \quad (2)$$

The reset delay time is determined by the time it takes an on-chip, precision 310-nA current source to charge the external capacitor to 1.24 V. When SENSE > V_{IT+} and with ENABLE high (or $\overline{\text{ENABLE}}$ low), the internal current sources are enabled and begin to charge the external capacitors. When the CT*n* voltage on a capacitor reaches 1.24 V, the corresponding SENSE_OUT or $\overline{\text{SENSE_OUT}}$ is asserted. Note that a low-leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

8.3.5 Immunity To Sense Pin Voltage Transients

The TPS389x is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients depends on threshold overdrive, as shown in the typical characteristic graph *Minimum Pulse Duration vs Threshold Overdrive Voltage* (图 9).

8.4 Device Functional Modes

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When the voltage on VDD is greater than $V_{DD(min)}$, the output corresponds to the voltages on the VDD and ENABLE pins relative to V_{IT-}.

8.4.2 Below $V_{DD(min)}$ ($V_{(POR)} < V_{DD} < V_{DD(min)}$)

When the voltage on VDD is less than $V_{DD(min)}$ but greater than the power-on reset voltage ($V_{(POR)}$), the output is deasserted (V_{SENSE_OUT} is low and $V_{\overline{SENSE_OUT}}$ is high.

8.4.3 Below Power-On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the power-on reset voltage ($V_{(POR)}$), the output is undefined. Do not rely on the output for proper device function under this condition.

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9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

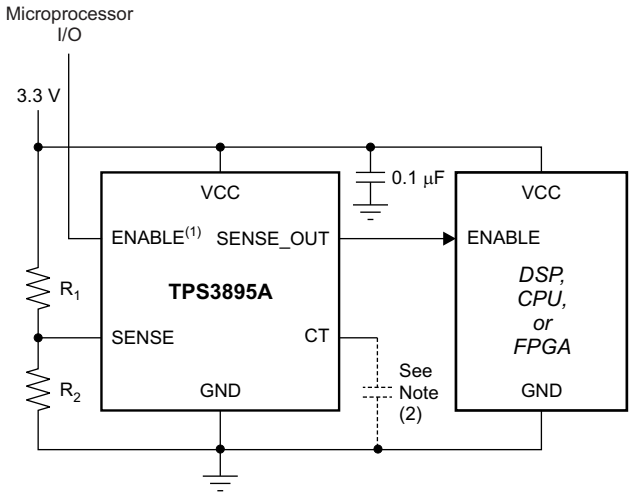
The TPS389x family of devices are very small supervisory circuits that monitor voltages greater than 500 mV and offer an adjustable delay time using external capacitors. The TPS389x family operates from 1.7 V to 6.5 V and also has an enable pin to power on/off the output. Orderable options include versions with either push-pull or open-drain outputs as well as versions that use active-high or active-low logic for the output and enable signals.

9.2 Typical Applications

9.2.1 Single-Rail Monitoring

The TPS3895P can be used to monitor the supply rail for devices such as digital signal processors (DSPs), central processing units (CPUs), or field-programmable gate arrays (FPGAs). The downstream device is enabled by the TPS3895P once the voltage on the SENSE pin (V_{SENSE}) is above the threshold voltage (V_{IT+}) set by the resistor divider. The downstream device is disabled by the TPS3895P when V_{SENSE} is falls below the threshold voltage minus the hysteresis voltage ($V_{IT+} – V_{hys}$).

If active low inputs or outputs are needed, replace the TPS3895P devices with TPS3896P devices. 图 23 shows the TPS3895P in a typical application.



(1) ENABLE can also be driven with a separate 1.5-V or greater power supply.

(2) Capacitor is optional. If a capacitor is not used, leave the CT pin open for a 40-µs delay.

图 23. TPS3895 Typical Application

9.2.1.1 Design Requirements

The TPS3895P must drive the enable pin of devices using a logic-high signal to signify that the supply voltage is above the minimum operating voltage of the device.

9.2.1.2 Detailed Design Procedure

Select R_1 and R_2 so the voltage at SENSE (V_{SENSE}) is above the positive-going threshold voltage (V_{IT+}) at the supply voltage required for proper device operation (that is, proper operation of the DSP, CPU, FPGA, and so on). Also, ensure that the current that flows from the supply voltage to ground through the resistor divider is at least 100 times larger than the input current (I_{SENSE}).

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Typical Applications (接下页)

If an output delay time is required, connect a capacitor from CT to GND; see the *Output Delay Time Pin (CT)* section for more information. If no CT cap is connected, the delay time is 40 µs.

9.2.1.3 Application Curve

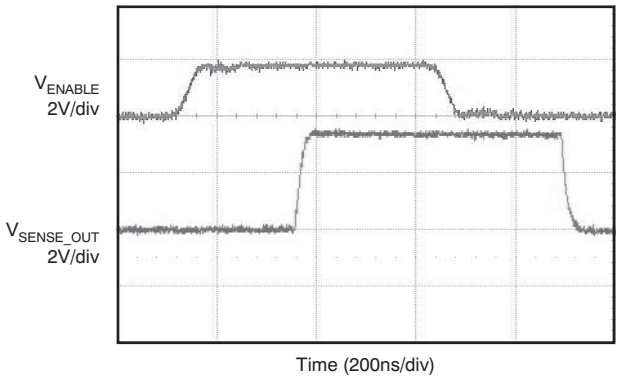


图 24. Enable Power On and Power Off Delay (TPS3895P)

9.2.2 Multiple Voltage Monitoring Sequential Delay

Multiple TPS3895As can be used to monitor multiple supply rails with a single output signifying whether or not all rails are above the respective thresholds. Some applications may need a minimum total delay time that is the sum of all the delay times of the supply monitor. To achieve this configuration, connect the output of one TPS3895A to the ENABLE pin of the next TPS3895A, and repeat until the last TPS3895A is connected to the device that receives the final Wired-AND signal. The downstream device receives a signal from the last TPS3895A once V_{SENSE} on all SENSE pins is above the V_{IT+} set by the resistor dividers. The downstream device is disabled by the last TPS3895A if the voltage on any SENSE pin in the chain falls below (V_{IT+} – V_{hys}).

图 25 shows an example of a configuration for dual-supply monitoring; this concept can be expanded for as many rails as a given application requires.

If active low inputs or outputs are needed, replace the TPS3895A devices with TPS3896A devices.

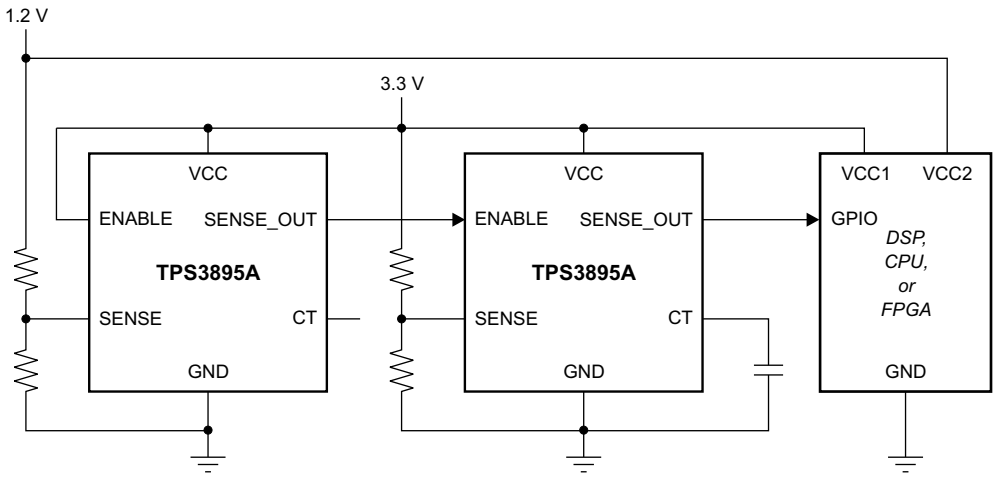


图 25. Multiple Voltage Monitoring Using ENABLE Pin

9.2.2.1 Design Requirements

Two rails must be monitored to ensure that both are above the respective minimum operating voltage for proper operation pf the device. The TPS3895As must drive a GPIO pin of the final downstream device, and use a logic-high signal to signify that the supply voltages are above the minimum operating voltage of the given device.

Typical Applications (接下页)

9.2.2.2 Detailed Design Procedure

Select the resistor divider of each TPS3895A so the voltage at SENSE (V_{SENSE}) is above the positive-going threshold voltage (V_{IT+}) at the point where the monitored voltage is required for proper device operation (that is, proper operation of the DSP, CPU, FPGA, and so on). Also, ensure that the currents that flow from the monitored voltage to ground through the resistor dividers are at least 100 times larger than the input current (I_{SENSE}).

If an output delay time is required for any of the TPS3895As, connect a capacitor from the CT pin of that TPS3895A to GND; see the *Output Delay Time Pin (CT)* section for more information. If no CT caps are connected, the delay time is 40 µs for each TPS3895A in the chain. Because each of the ENABLE pins is tied to the TPS3895A preceding it (other than the first), at a minimum the total delay time is the sum of all the delay times set by the CT pins in the design.

9.2.2.3 Application Curve

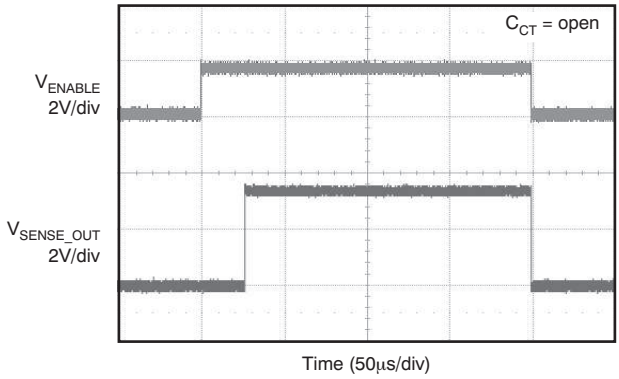


图 26. Enable Power On and Power Off Delay (TPS3895A)

9.2.3 Multiple Voltage Monitoring Minimum Delay

Multiple TPS3897Ps can be used to monitor multiple supply rails with a single output that signals if all rails are above the respective thresholds. Some applications may need a minimum total delay time that is equal to the delay time of only the final supply monitor to power up. To achieve this configuration, connect the outputs of all the TPS3897Ps to the device that must receive the final Wired-AND signal and connect that same node to the appropriate logic-high voltage via a resistor. The downstream device receives a signal once V_{SENSE} on all SENSE pins are above the V_{IT+} set by the resistor dividers. The downstream device is disabled if the voltage on any SENSE pin falls below ($V_{IT+} – V_{hys}$).

See 图 27 for an example of a configuration for dual-supply monitoring. This concept can be expanded for as many rails as a given application requires.

If active low inputs/outputs are required, replace the TPS3897P devices with TPS3898P devices.

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Typical Applications (接下页)

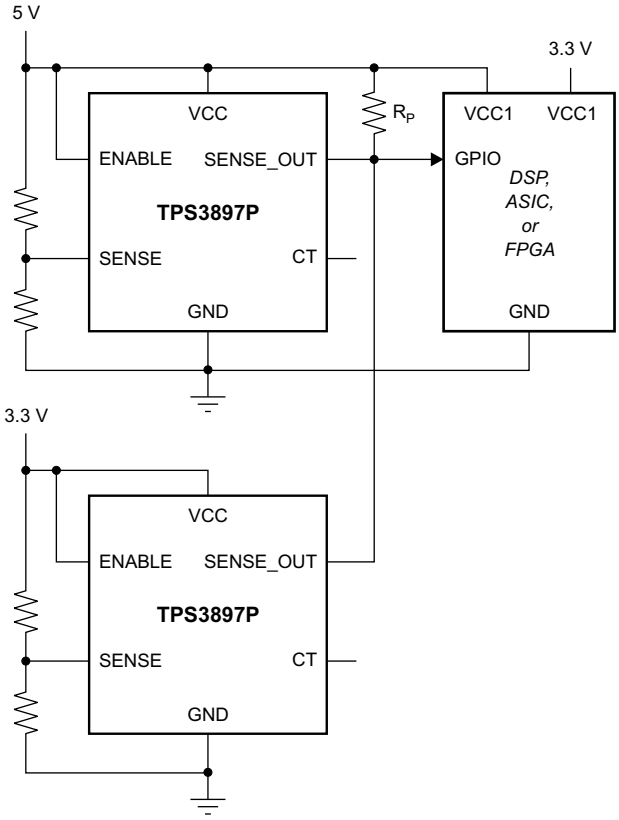


图 27. Multiple Voltage Monitoring Using Wired-OR Logic at SENSE_OUT

9.2.3.1 Design Requirements

Two rails must be monitored to ensure that both rails are above the respective minimum operating voltage for proper operation of the device. The TPS3897Ps must drive a GPIO pin of the final downstream device and use a logic-high signal to signify that the supply voltages are above the minimum operating voltage of the device.

9.2.3.2 Detailed Design Procedure

Select the resistor divider of each TPS3897P so the voltage at SENSE (V_{SENSE}) is above the positive-going threshold voltage (V_{IT+}) at the point where the monitored voltage is required for proper device operation (that is, proper operation of the DSP, CPU, FPGA, and so on). Also, ensure that the currents that flow from the monitored voltage to ground through the resistor dividers are at least 100 times larger than the input current (I_{SENSE}).

If an output delay time is required for any of the TPS3897Ps, connect a capacitor from the CT pin of that TPS3897P to GND; see the *Output Delay Time Pin (CT)* section for more information. If no CT caps are connected, the delay time is 40 µs.

Determine the logic-high voltage by selecting the voltage that the pullup resistor (denoted R_P in 图 29) is connected to. Select R_P so that current that flows to ground allows for a low-level output voltage that is low enough for the specific application. See the *Output Pin (SENSE_OUT)* section for more information.

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Typical Applications (接下页)

9.2.3.3 Application Curves

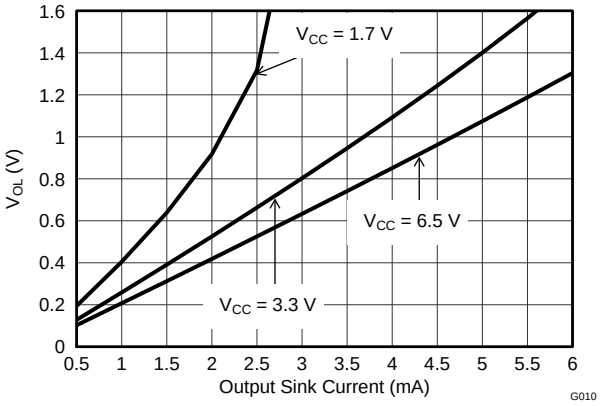


图 28. Output Voltage Low vs Output Current

9.2.4 Voltage Sequencing

TPS3895As can be used to implement voltage rail sequencing by connecting a resistor divider and the SENSE pin of a TPS3895A to the first rail to be monitored, and then feeding the output from the first TPS3895A to the ENABLE pin of the next voltage rail. The downstream voltage rail is enabled by the TPS3895A once the voltage on the SENSE pin (V_{SENSE}) is above the threshold voltage (V_{IT+}) set by the resistor divider. This process can be repeated for as many rails as the application requires. The downstream voltage rail is disabled by the TPS3895A when V_{SENSE} falls below the threshold voltage minus the hysteresis voltage ($V_{IT+} – V_{hys}$).

If active low inputs/outputs are required, replace the TPS3895A devices with TPS3896A devices.

See 图 29 for an example for a system with four voltage rails that must sequence the three LDOs.

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Typical Applications (接下页)

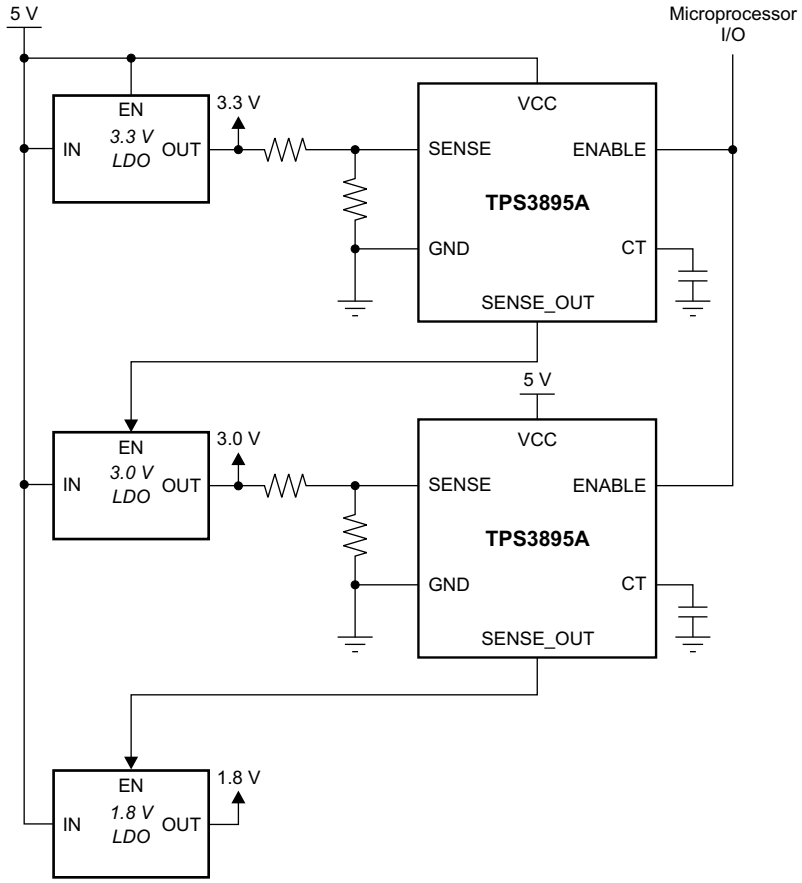


图 29. Voltage Sequencing (5 V → 3.3 V → 3 V → 1.8 V)

9.2.4.1 Design Requirements

Three rails must be sequenced to ensure proper start-up sequencing. The TPS3895As must drive the ENABLE pins of each LDO, and use a logic-high signal to signify that the supply preceding it is above the desired operating voltage for that rail. The ENABLE pin of the TPS3895As must be controlled by a microprocessor to allow it to be shut down even when the rails are above the threshold.

9.2.4.2 Detailed Design Procedure

Select the resistor divider of each TPS3895A so the voltage at SENSE (V_{SENSE}) is above the positive-going threshold voltage (V_{IT+}) at the point where the monitored voltage is required for proper device operation (that is, proper operation of the DSP, CPU, FPGA, and so on). Also, ensure that the currents that flow from the monitored voltage to ground through the resistor dividers are at least 100 times larger than the input current (I_{SENSE}).

If an output delay time is required for any of the TPS3895As, connect a capacitor from the CT pin of that TPS3895A to GND; see the *Output Delay Time Pin (CT)* section for more information. If no CT caps are connected, the delay time is 40 µs for each TPS3895A in the chain. Because each of the ENABLE pins is tied to the TPS3895A that precedes it (other than the first device in the chain), at a minimum the total delay time is the sum of all the delay times set by the CT pins.

Typical Applications (接下页)

9.2.4.3 Application Curve

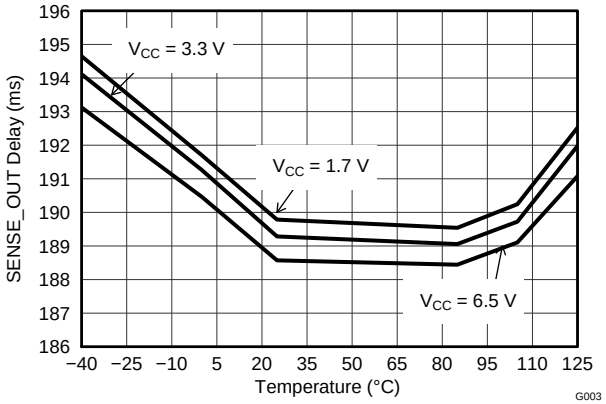


图 30. SENSE_OUT Time-out Period vs Temperature (C_{CT} = 47 nF)

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10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 1.7 V to 6.5 V. Though not required, it is good analog design practice to place a 0.1-µF ceramic capacitor close to the VCC pin.

11 Layout

11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the TPS389x family of devices.

- Place the VCC decoupling capacitor close to the device.
- Avoid using long traces for the VCC supply node. The VCC capacitor (C_{VCC}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum VCC voltage.

11.2 Layout Example

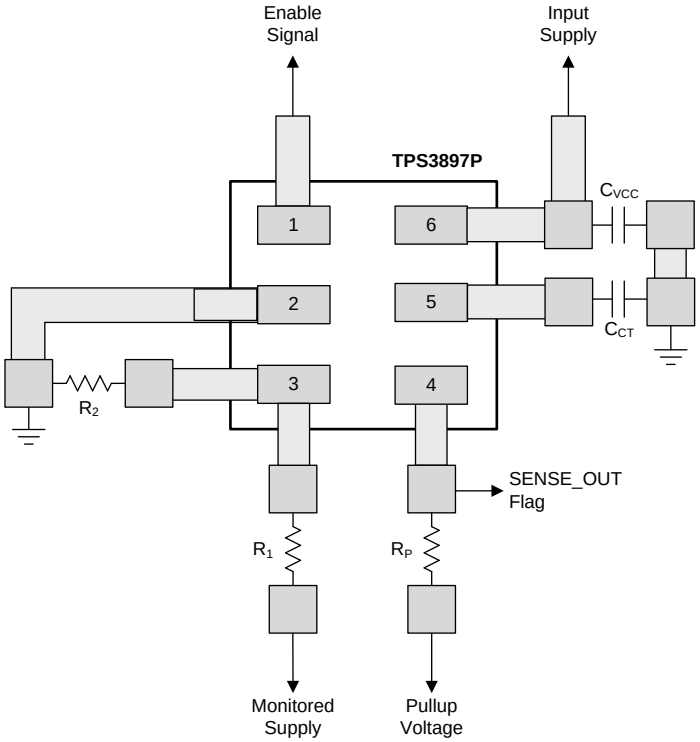


图 31. TPS3897P Layout Example (DRY Package)

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 评估模块

评估模块 (EVM) 可与 TPS389x 配套使用，帮助评估初始电路性能。 TPS3897A-6P-EVM047 评估模块（和相关的用户指南）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI 网上商店购买。

12.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。 您可以从产品文件夹中的*工具和软件*下获取 TPS389x 的 SPICE 模型。

12.1.2 器件命名规则

表 **3.** 器件命名规则

产品	说明
TPS389**wxyyyz**	**w** 为输出配置（请参见Device Comparison Table） **x** 为使能引脚的不同延迟（请参见Device Comparison Table） **yyy** 为封装标识符 **z** 为封装数量

12.2 文档支持

12.2.1 相关文档

- *《为开漏输出选择合适的上拉/下拉电阻》*，SLVA485
- *《TPS3897A-6P-EVM047 用户指南》*，SLVU524

12.3 商标

All trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3895ADRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UN	Samples
TPS3895ADRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UN	Samples
TPS3895PDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UO	Samples
TPS3895PDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UO	Samples
TPS3896ADRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UJ	Samples
TPS3896ADRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UJ	Samples
TPS3896PDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UK	Samples
TPS3896PDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UK	Samples
TPS3897ADRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-1-260C-UNLIM	-40 to 125	UL	Samples
TPS3897ADRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UL	Samples
TPS3897PDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UM	Samples
TPS3897PDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UM	Samples
TPS3898ADRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UH	Samples
TPS3898ADRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UH	Samples
TPS3898PDRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UI	Samples
TPS3898PDRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

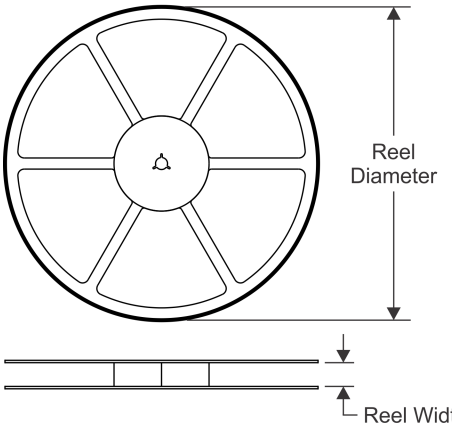
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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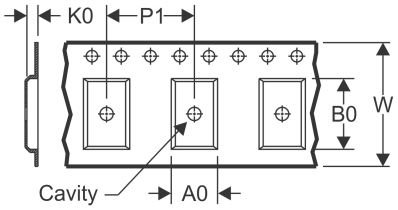
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

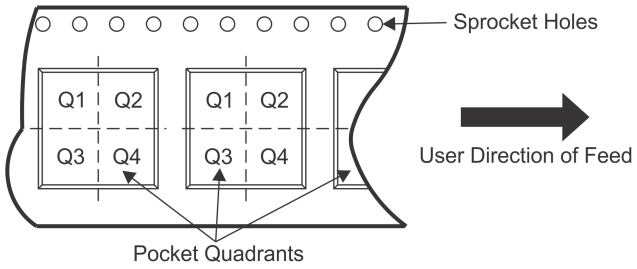


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

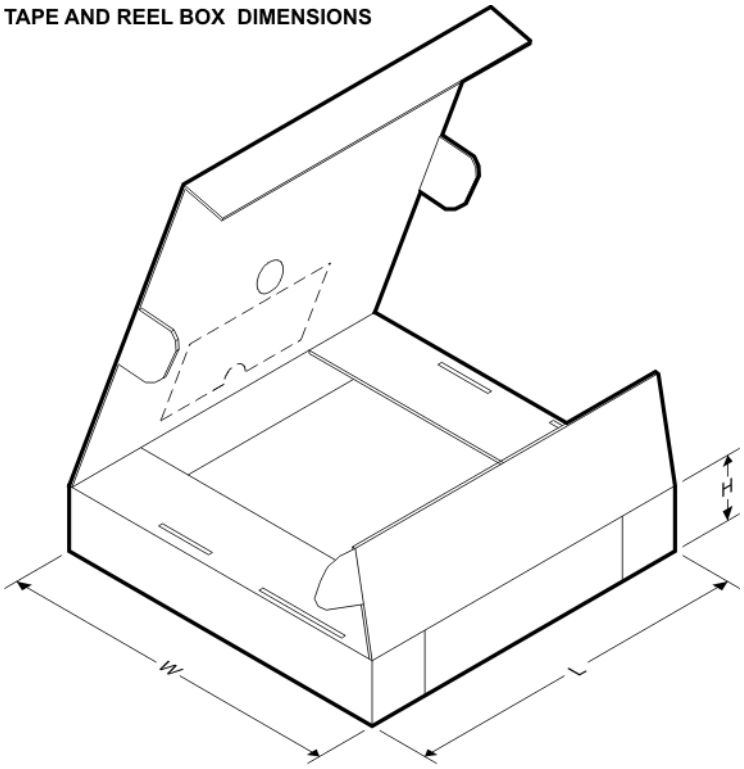


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3895ADRYR	SON	DRY	6	5000	180.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3895ADRYT	SON	DRY	6	250	180.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3895PDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3895PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3896ADRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3896ADRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3896PDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3896PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3897ADRYR	SON	DRY	6	5000	178.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897ADRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897ADRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3897ADRYT	SON	DRY	6	250	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897ADRYT	SON	DRY	6	250	178.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897PDRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897PDRYR	SON	DRY	6	5000	178.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897PDRYT	SON	DRY	6	250	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
TPS3897PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3897PDRYT	SON	DRY	6	250	178.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3898ADRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3898ADRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3898PDRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS3898PDRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3895ADRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3895ADRYT	SON	DRY	6	250	200.0	183.0	25.0
TPS3895PDRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3895PDRYT	SON	DRY	6	250	200.0	183.0	25.0
TPS3896ADRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3896ADRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3896PDRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3896PDRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3897ADRYR	SON	DRY	6	5000	205.0	200.0	33.0
TPS3897ADRYR	SON	DRY	6	5000	189.0	185.0	36.0
TPS3897ADRYT	SON	DRY	6	250	200.0	183.0	25.0
TPS3897ADRYT	SON	DRY	6	250	189.0	185.0	36.0
TPS3897ADRYT	SON	DRY	6	250	205.0	200.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3897PDRYR	SON	DRY	6	5000	189.0	185.0	36.0
TPS3897PDRYR	SON	DRY	6	5000	205.0	200.0	33.0
TPS3897PDRYT	SON	DRY	6	250	189.0	185.0	36.0
TPS3897PDRYT	SON	DRY	6	250	200.0	183.0	25.0
TPS3897PDRYT	SON	DRY	6	250	205.0	200.0	33.0
TPS3898ADRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3898ADRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS3898PDRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS3898PDRYT	SON	DRY	6	250	200.0	183.0	25.0

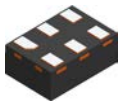
DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

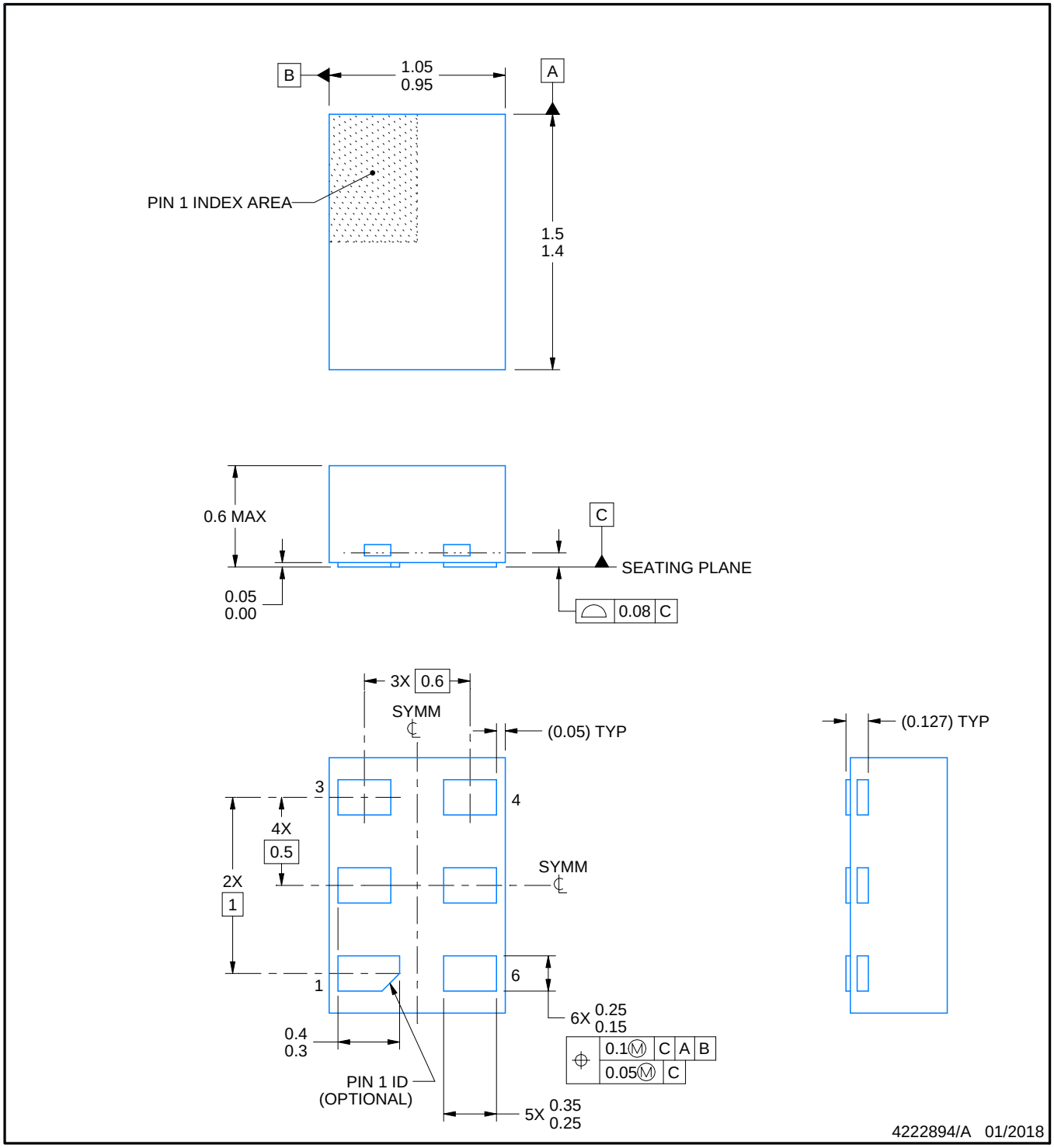
DRY0006A



PACKAGE OUTLINE

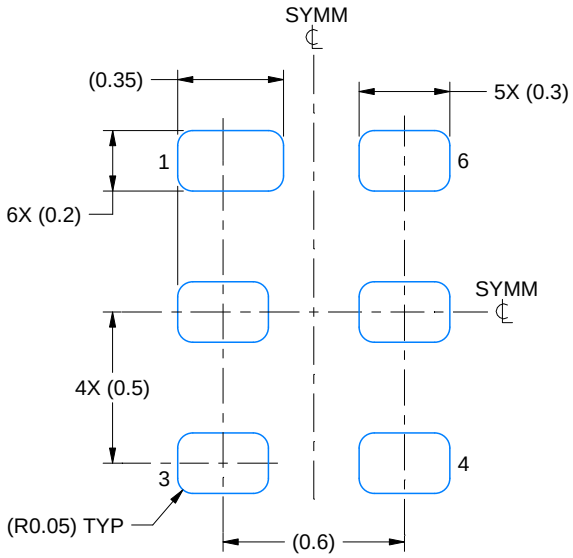
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

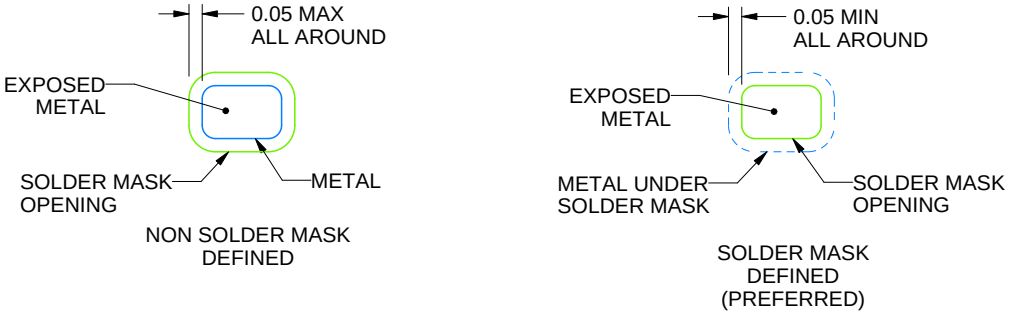


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

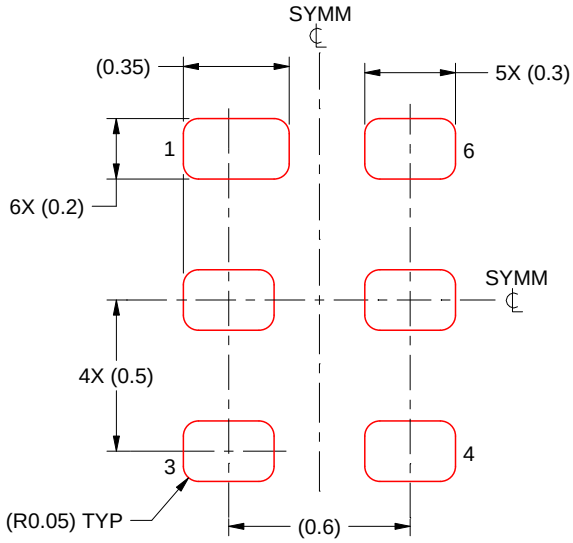
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

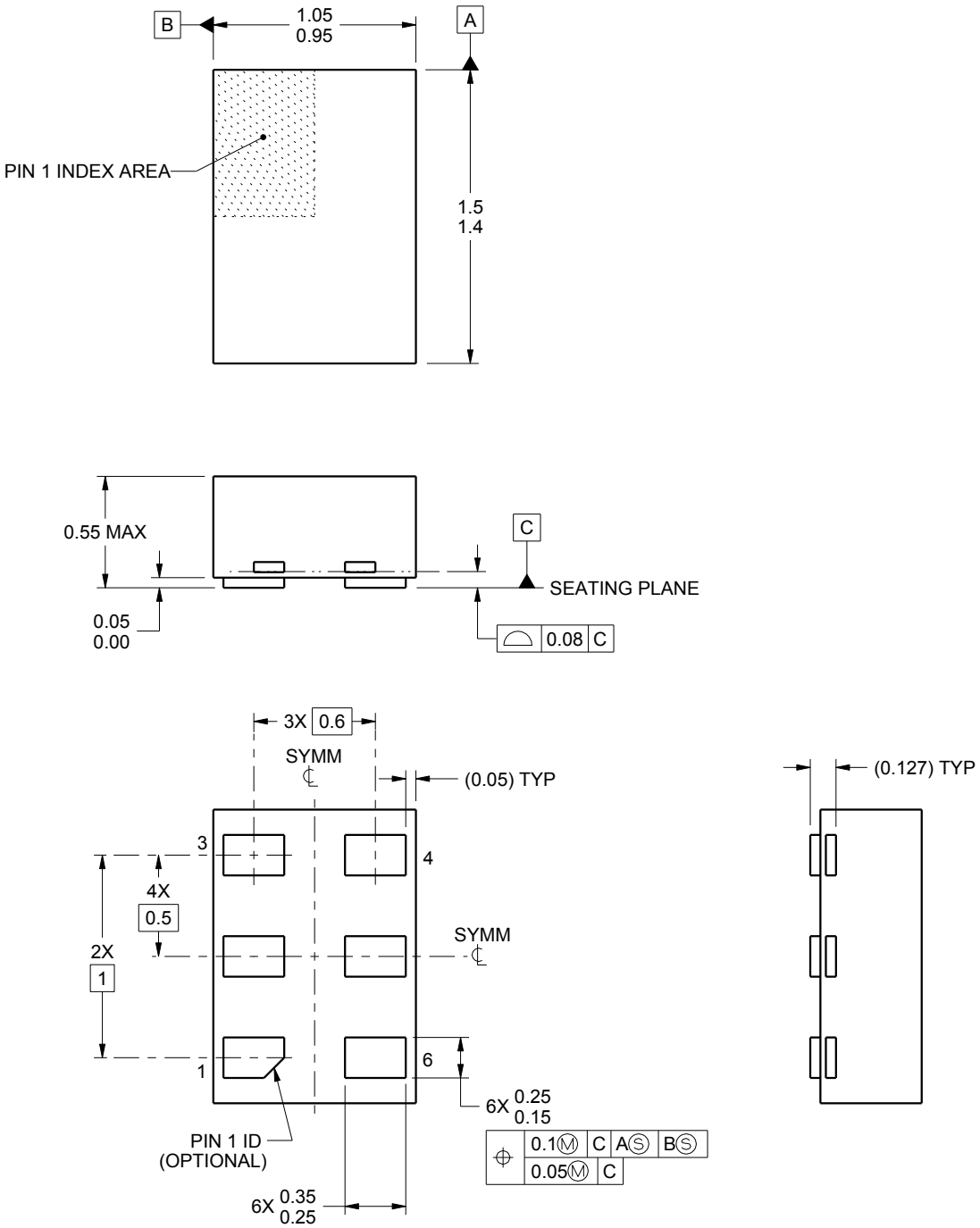
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRY0006B

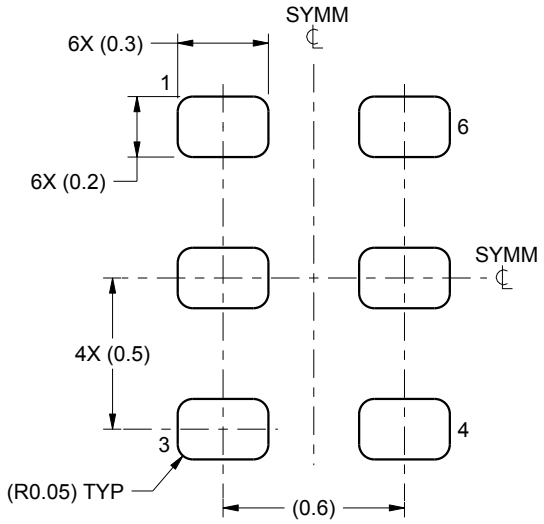
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

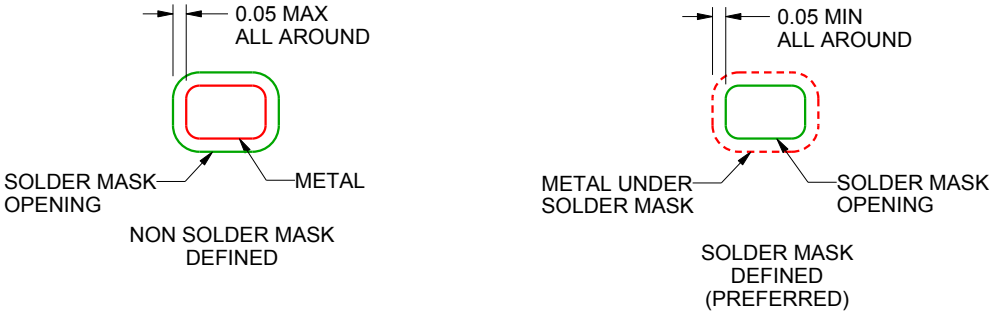


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

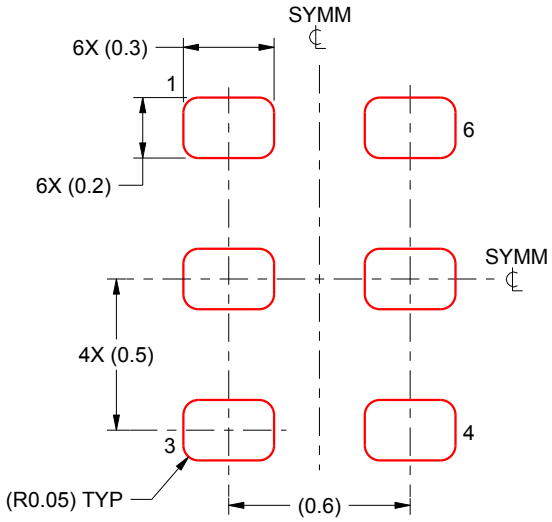
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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