具有优异 EMC 性能的 ISO7741E-Q1 0 级高速四通道增强型数字隔离器

1 特性

- 符合汽车类 应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 0：-40°C 至 150°C 环境工作温度范围
- 100Mbps 数据速率
- 稳健可靠的隔离栅：
  - 1500V_{RMS} 工作电压下，可实现 100 年以上的预期使用寿命
  - 高达 5000V_{RMS} 隔离额定值
  - 高达 12.8kV 的浪涌能力
  - ±100kV/µs 典型 CMTI
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 至 5.5V 电平转换
- 默认输出*高电平* (ISO7741) 和*低电平* (ISO7741F) 选项
- 低功耗，1Mbps 时每通道的电流典型值为 1.5mA
- 低传播延迟：典型值为 10.7ns（由 5V 电源供电）
- 优异的电磁兼容性 (EMC)
  - 系统级 ESD、EFT 和浪涌抗扰性
  - ±8kV IEC 61000-4-2 跨隔离栅接触放电保护
  - 低辐射
- Wide-SOIC (DW-16) 封装
- 安全相关认证：
  - DIN VDE V 0884-11:2017-01
  - UL 1577 组件认证计划
  - 获得 CSA 认证，符合 IEC 60950-1、IEC 62368-1、IEC 61010-1 和 IEC 60601-1 终端设备标准
  - 符合 GB4943.1-2011 的 CQC 认证
  - 符合 EN 60950-1、EN 62368-1 和 EN 61010-1 标准的 TUV 认证

2 应用

- 混合动力、电动和动力传动系统 (EV/HEV)
  - 电池管理系统 (BMS)
  - 车载充电器
  - 牵引逆变器
  - 直流/直流转换器
  - 起动机/发电机
- 车身电子装置
  - 汽车泊车加热器模块
  - HVAC 压缩机模块
  - HVAC 控制模块
  - HVAC 传感器
  - 车内加热器模块

3 说明

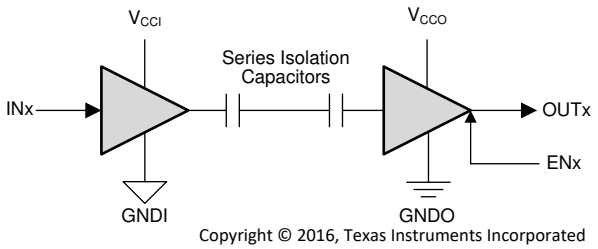
ISO7741E-Q1 器件是 0 级高性能四通道数字隔离器，可提供符合 UL 1577 标准的 5000V_{RMS}隔离额定值。该器件具有符合 VDE、CSA、TUV 和 CQC 标准的增强型隔离额定值。此器件的高温范围高达 150°C，非常适合环境温度可能超过 125°C 的 应用 ，例如带式起动发电机、水泵、冷却风扇、烟尘传感器等等。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7741E-Q1	SOIC (DW)	10.30mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



V_{CCI} = 输入电源，V_{CCO} = 输出电源
GNDI=输入接地，GNDO=输出接地

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2019) to Revision A	Page
• 已更改 将器件状态更改为“生产数据”	1

5 说明（续）

ISO7741E-Q1 器件能够以较低的功耗提供高电磁抗扰度和低辐射，同时还能够隔离 CMOS 或 LVCMOS 数字 I/O。每条隔离通道的逻辑输入和输出缓冲器均由双电容二氧化硅 (SiO_2) 绝缘栅相隔离。该器件配有使能引脚，可用于将多主驱动 应用 中的相应输出置于高阻抗状态，也可用于降低功耗。ISO7741E-Q1 器件具有三条正向通道和一条反向通道。如果输入功率或信号出现损失，不带后缀 F 的器件默认输出*高电平*，带后缀 F 的器件默认输出*低电平*。有关更多详细信息，请参阅 *Device Functional Modes*器件功能模式 部分。

这些器件与隔离式电源搭配使用，有助于防止数据总线（例如，CAN）或其他电路上的噪声电流进入本地接地以及干扰或损坏敏感电路。凭借创新型芯片设计和布局技术，ISO7741E-Q1 器件的电磁兼容性得到了显著增强，可轻松满足系统级 ESD、EFT、浪涌和辐射方面的合规要求。ISO7741E-Q1 器件采用 16 引脚 SOIC 封装。

6 Pin Configuration and Functions

ISO7741E-Q1 DW Package
16-Pin SOIC-WB
Top View

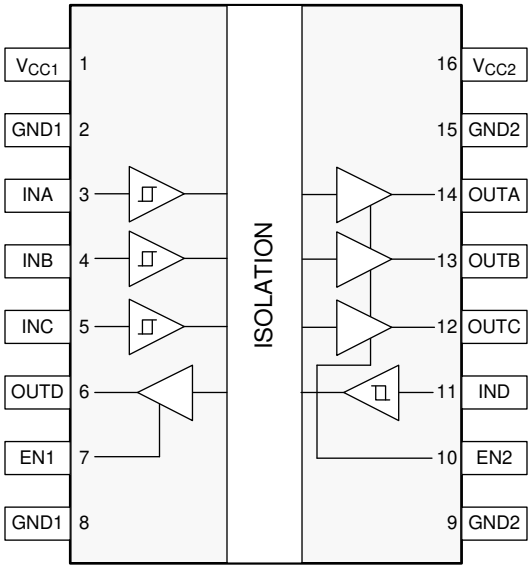


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	—	Ground connection for V_{CC1}
	8		
GND2	9	—	Ground connection for V_{CC2}
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

7 Specifications

7.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	–0.5	6	V
V	Voltage at INx, OUTx, ENx	–0.5	V_{CCX} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Junction temperature		175	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	
		Contact Discharge per IEC 61000-4-2 Isolation Barrier Withstand Test(2)(3)	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	V_{CCO}(1) = 5 V	–4			mA
		V_{CCO} = 3.3 V	–2			
		V_{CCO} = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI}(1)		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}	V
DR	Data rate		0		100	Mbps
T_A	Ambient temperature		-40	25	150	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

7.4 Thermal Information

THERMAL METRIC[1]		ISO7741E-Q1 DW (SOIC) 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 175°C, C_L = 15 pF, Input a 50-MHz 50% duty cycle square wave			200	mW
P_{D1}	Maximum power dissipation by side-1				75	mW
P_{D2}	Maximum power dissipation by side-2				125	mW

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See 图 22	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 x sin (2pft), f = 1 MHz	~1	pF
R_{IO}	Isolation resistance(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/150/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
Maximum transient isolation voltage, 8000 V_{PK} Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1:2014 800 V_{RMS} max working voltage (pollution degree 2, material group I); Reinforced insulation per CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed. 300 V_{RMS} max working voltage (overvoltage category III)	Single protection, 5000 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage;	5000 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A2:2013 up to working voltage of 800 V_{RMS}
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

7.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 83.4 °C/W, V_I = 5.5 V, T_J = 175°C, T_A = 25°C, see 图 1			327	mA
		$R_{\theta JA}$ = 83.4 °C/W, V_I = 3.6 V, T_J = 175°C, T_A = 25°C, see 图 1			500	
		$R_{\theta JA}$ = 83.4 °C/W, V_I = 2.75 V, T_J = 175°C, T_A = 25°C, see 图 1			654	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 83.4 °C/W, T_J = 175°C, T_A = 25°C, see 图 2			1799	mW
T_S	Maximum safety temperature				175	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

7.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 图 9	V_{CCO}(1) – 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 图 9		0.2	0.4	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see 图 12	85	100		kV/µs
C_I	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to ground.

7.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - Disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7741E-Q1); V_I = 0 V (ISO7741E-Q1 with F suffix)		I_{CC1}		1	1.7	mA
			I_{CC2}		0.7	1.3	
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7741E-Q1); V_I = V_{CCI} (ISO7741E-Q1 with F suffix)		I_{CC1}		4.3	6.5	
			I_{CC2}		1.8	2.9	
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7741E-Q1); V_I = 0 V (ISO7741E-Q1 with F suffix)		I_{CC1}		1.5	2.4	
			I_{CC2}		2	3.5	
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7741E-Q1); V_I = V_{CCI} (ISO7741E-Q1 with F suffix)		I_{CC1}		4.8	7.3	
			I_{CC2}		3.2	5.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.2	5	
			I_{CC2}		2.8	4.4	
		10 Mbps	I_{CC1}		3.7	5.2	
			I_{CC2}		4.2	6.2	
		100 Mbps	I_{CC1}		8.6	11.3	
			I_{CC2}		18	22	

(1) V_{CCI} = Input-side V_{CC}

7.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see 图 9	V_{CCO}(1) – 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see 图 9		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see 图 12	85	100		kV/μs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

7.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - Disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7741E-Q1); V_I = 0 V (ISO7741E-Q1 with F suffix)		I_{CC1}		1	1.7	mA
			I_{CC2}		0.7	1.3	
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7741E-Q1); V_I = V_{CCI} (ISO7741E-Q1 with F suffix)		I_{CC1}		4.3	6.4	
			I_{CC2}		1.9	2.8	
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7741E-Q1); V_I = 0 V (ISO7741E-Q1 with F suffix)		I_{CC1}		1.5	2.4	
			I_{CC2}		2	3.5	
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7741E-Q1); V_I = V_{CCI} (ISO7741E-Q1 with F suffix)		I_{CC1}		4.8	7.2	
			I_{CC2}		3.2	5.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.2	4.6	
			I_{CC2}		2.7	4.3	
		10 Mbps	I_{CC1}		3.5	5	
			I_{CC2}		3.7	5.4	
		100 Mbps	I_{CC1}		6.8	9.3	
			I_{CC2}		13.7	16.5	

(1) V_{CCI} = Input-side V_{CC}

7.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see 图 9	V_{CCO}(1) – 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see 图 9		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see 图 12	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

7.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - Disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7741E-Q1); V_I = 0 V (ISO7741E-Q1 with F suffix)		I_{CC1}		1	1.7	mA
			I_{CC2}		0.7	1.2	
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7741E-Q1); V_I = V_{CCI} (ISO7741E-Q1 with F suffix)		I_{CC1}		4.3	6.4	
			I_{CC2}		1.8	2.8	
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7741E-Q1); V_I = 0 V (ISO7741E-Q1 with F suffix)		I_{CC1}		1.4	2.4	
			I_{CC2}		2	3.4	
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7741E-Q1); V_I = V_{CCI} (ISO7741E-Q1 with F suffix)		I_{CC1}		4.7	7.2	
			I_{CC2}		3.2	5.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.1	5	
			I_{CC2}		2.7	4.4	
		10 Mbps	I_{CC1}		3.4	4.9	
			I_{CC2}		3.5	5.1	
		100 Mbps	I_{CC1}		6.2	8.3	
			I_{CC2}		10.8	13.8	

(1) V_{CCI} = Input-side V_{CC}

7.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	6	10.7	16.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0	4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.4	ns
t_r	Output signal rise time	See 图 9		2.4	4.1	ns
t_f	Output signal fall time			2.4	4.1	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 图 10		9	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			9	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1			7	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1 with F suffix			3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1			3	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1 with F suffix			7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See 图 12		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.8		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	6	11	16.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See 图 9		1.3	3.1	ns
t_f	Output signal fall time			1.3	3.1	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 图 10		17	30	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1			17	30	ns
	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1 with F suffix			3.2	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1			3.2	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1 with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See 图 12		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.9		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 图 9	7.5	12	19	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction Channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.6	ns
t_r	Output signal rise time	See 图 9		1	3.6	ns
t_f	Output signal fall time			1	3.6	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 图 10		22	40	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1			18	40	ns
	Enable propagation delay, high impedance-to-high output for ISO7741E-Q1 with F suffix			3.3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1			3.3	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7741E-Q1 with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See 图 12		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.7		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.18 Insulation Characteristics Curves

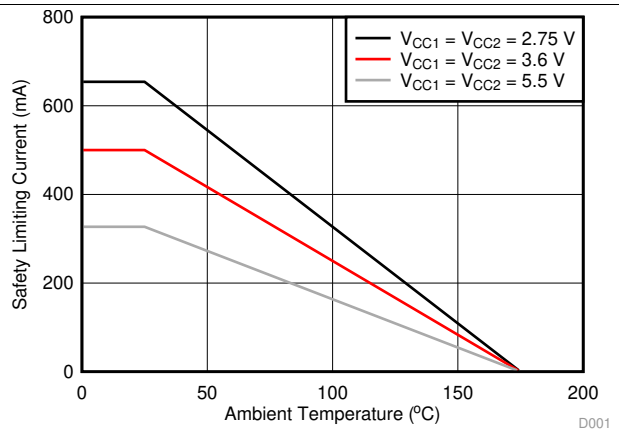


图 1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

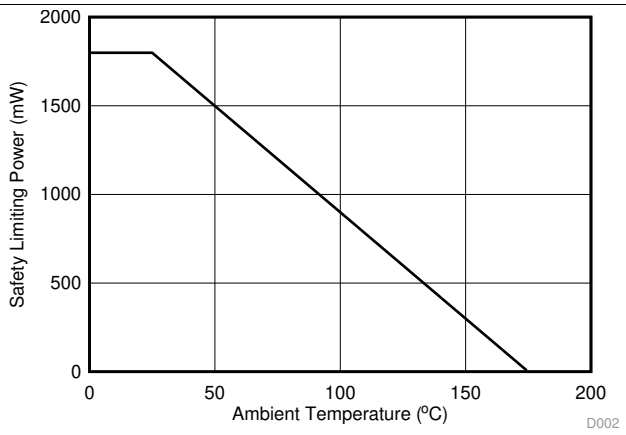
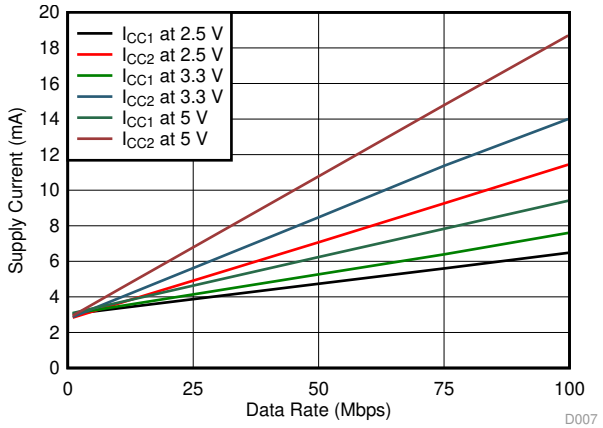


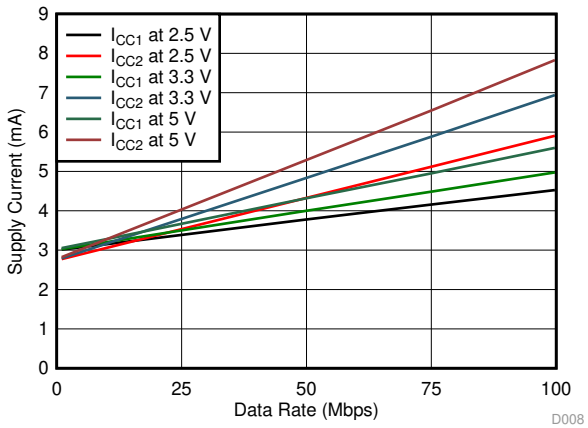
图 2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

7.19 Typical Characteristics



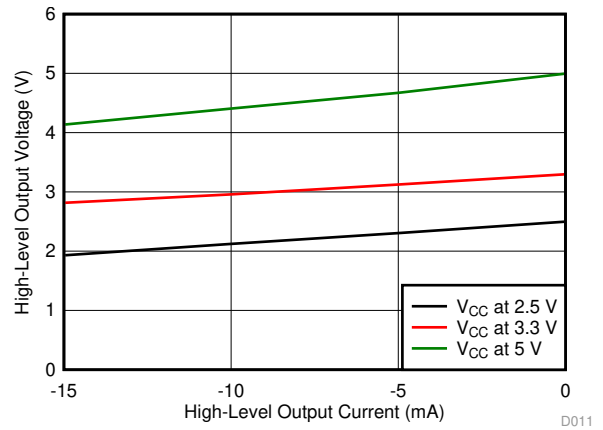
T_A = 25°C C_L = 15 pF

图 3. Supply Current vs Data Rate (With 15-pF Load)



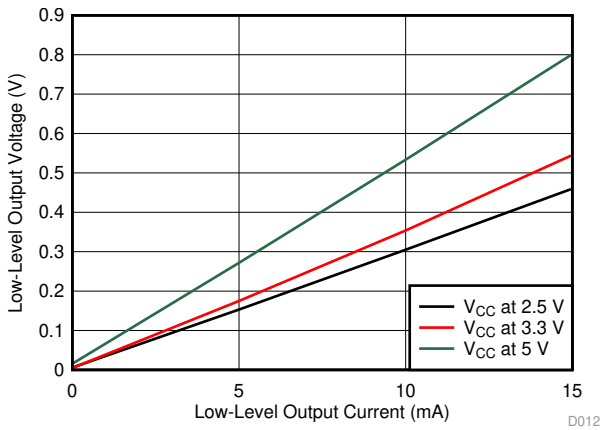
T_A = 25°C C_L = No Load

图 4. Supply Current vs Data Rate (With No Load)



T_A = 25°C

图 5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

图 6. Low-Level Output Voltage vs Low-Level Output Current

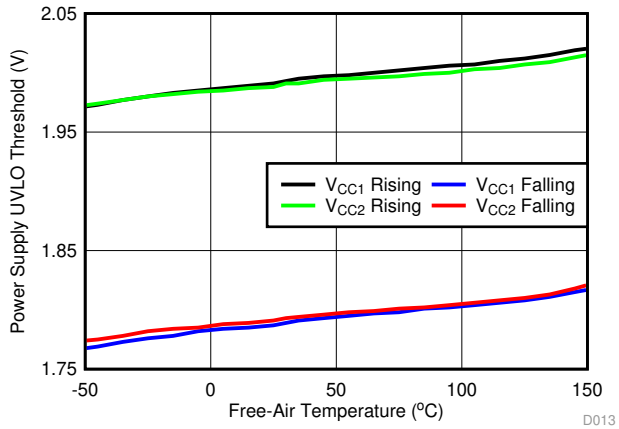


图 7. Power Supply Undervoltage Threshold vs Free-Air Temperature

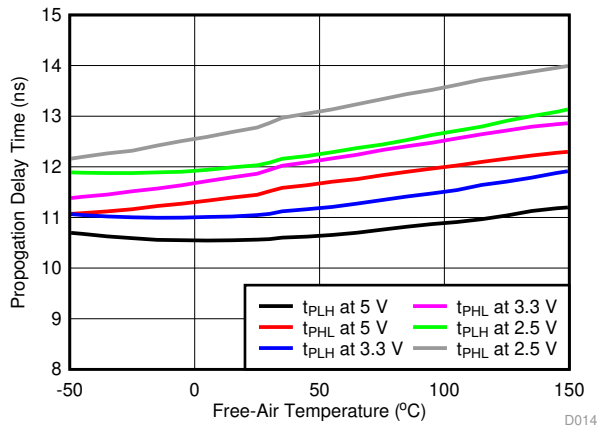
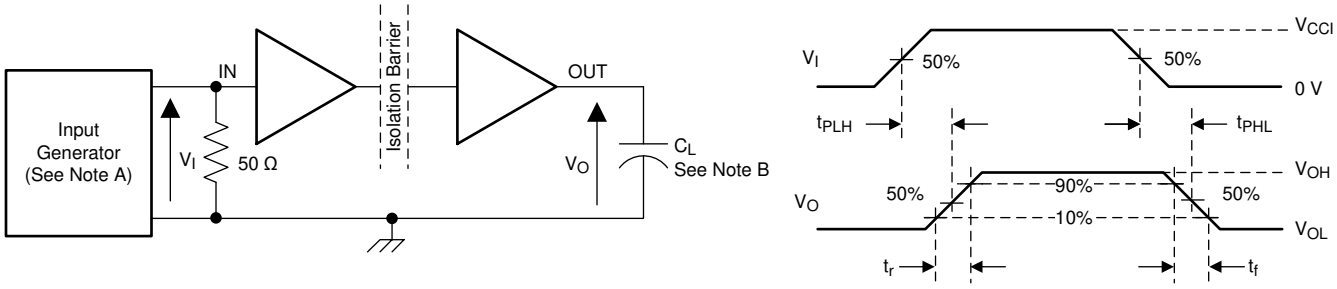


图 8. Propagation Delay Time vs Free-Air Temperature

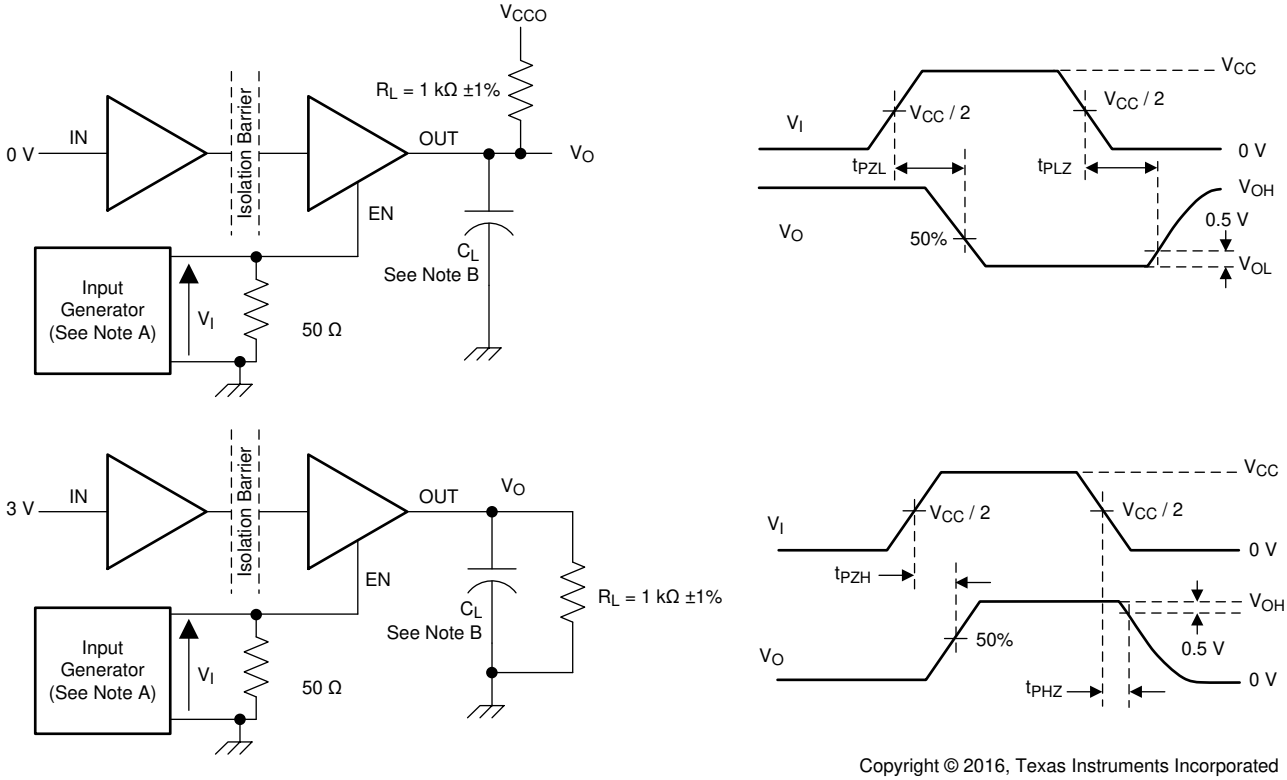
8 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 9. Switching Characteristics Test Circuit and Voltage Waveforms

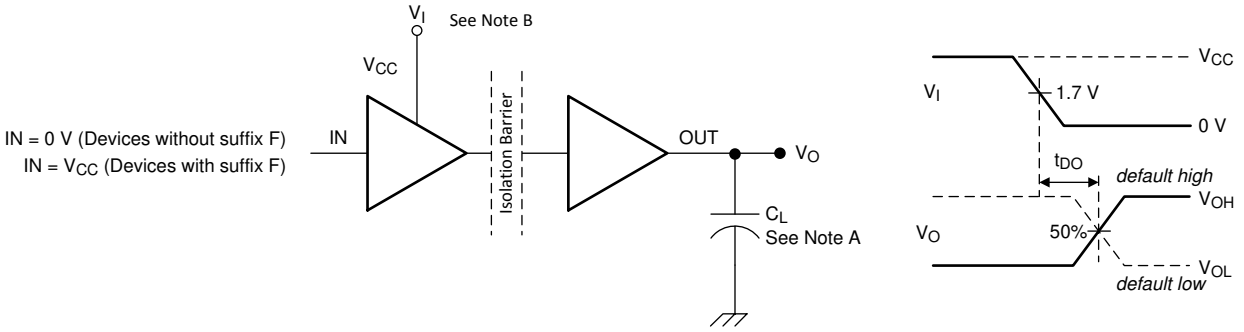


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 10. Enable/Disable Propagation Delay Time Test Circuit and Waveform

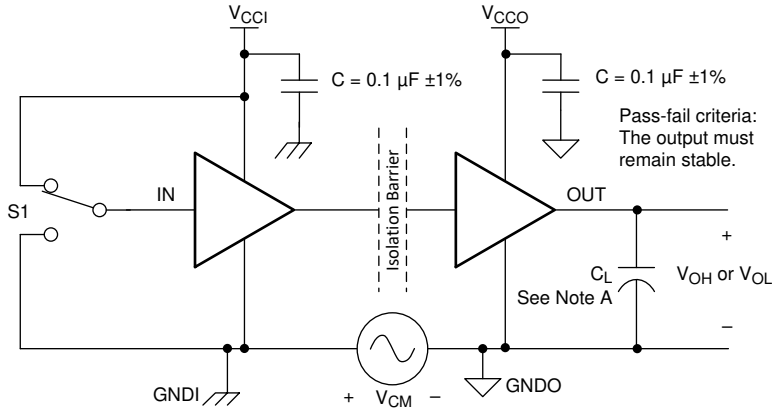
Parameter Measurement Information (接下页)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

图 11. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 12. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ISO7741E-Q1 device has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO7741E-Q1 device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 图 13, shows a functional block diagram of a typical channel.

9.2 Functional Block Diagram

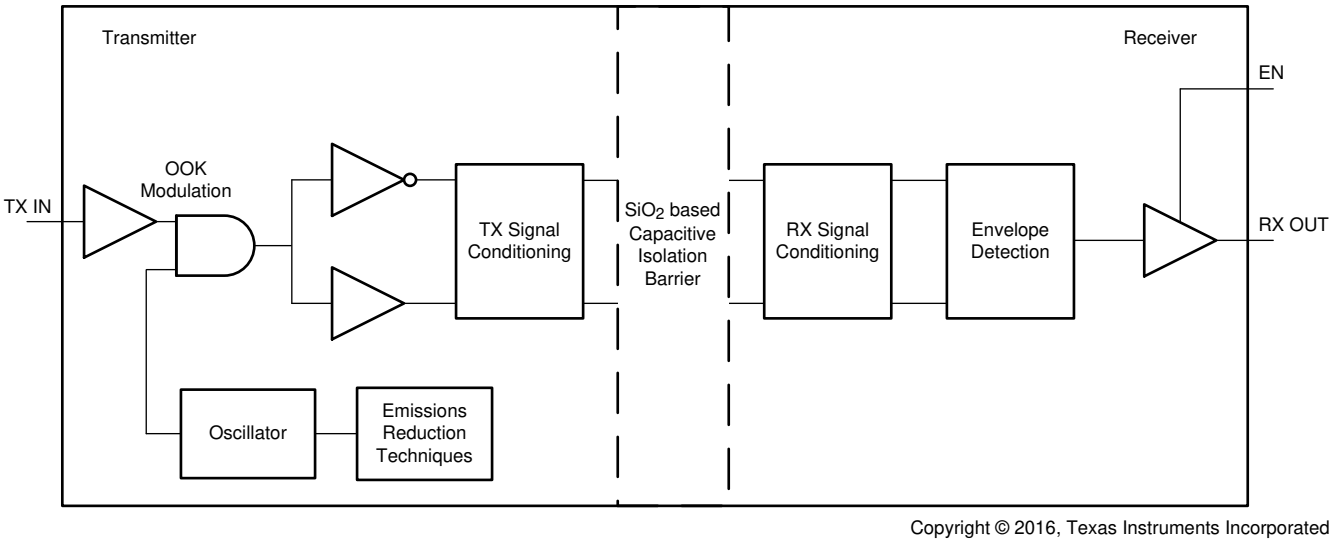


图 13. Conceptual Block Diagram of a Digital Capacitive Isolator

图 14 shows a conceptual detail of how the ON-OFF keying scheme works.

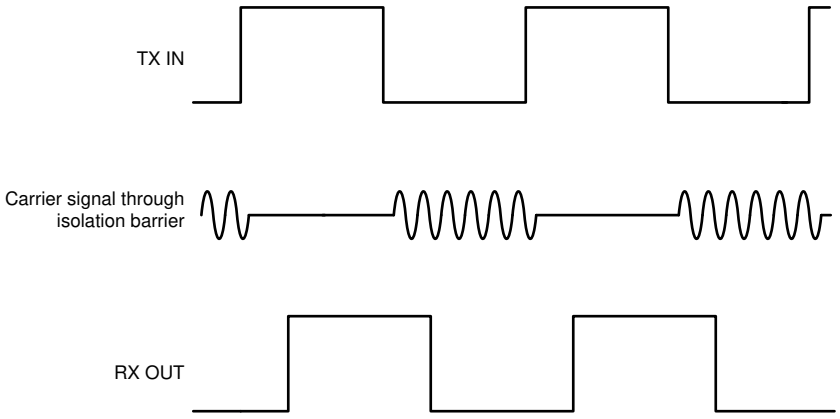


图 14. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

provides an overview of the device features.

表 2. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7741E-Q1	3 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
ISO7741E-Q1 with F suffix	3 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}

9.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7741E-Q1 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.4 Device Functional Modes

表 3 lists the functional modes for the ISO7741E-Q1 device.

表 3. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO7741E-Q1 and *Low* for ISO7741E-Q1 with F suffix.
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO7741E-Q1 and *Low* for ISO7741E-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

9.4.1 Device I/O Schematics

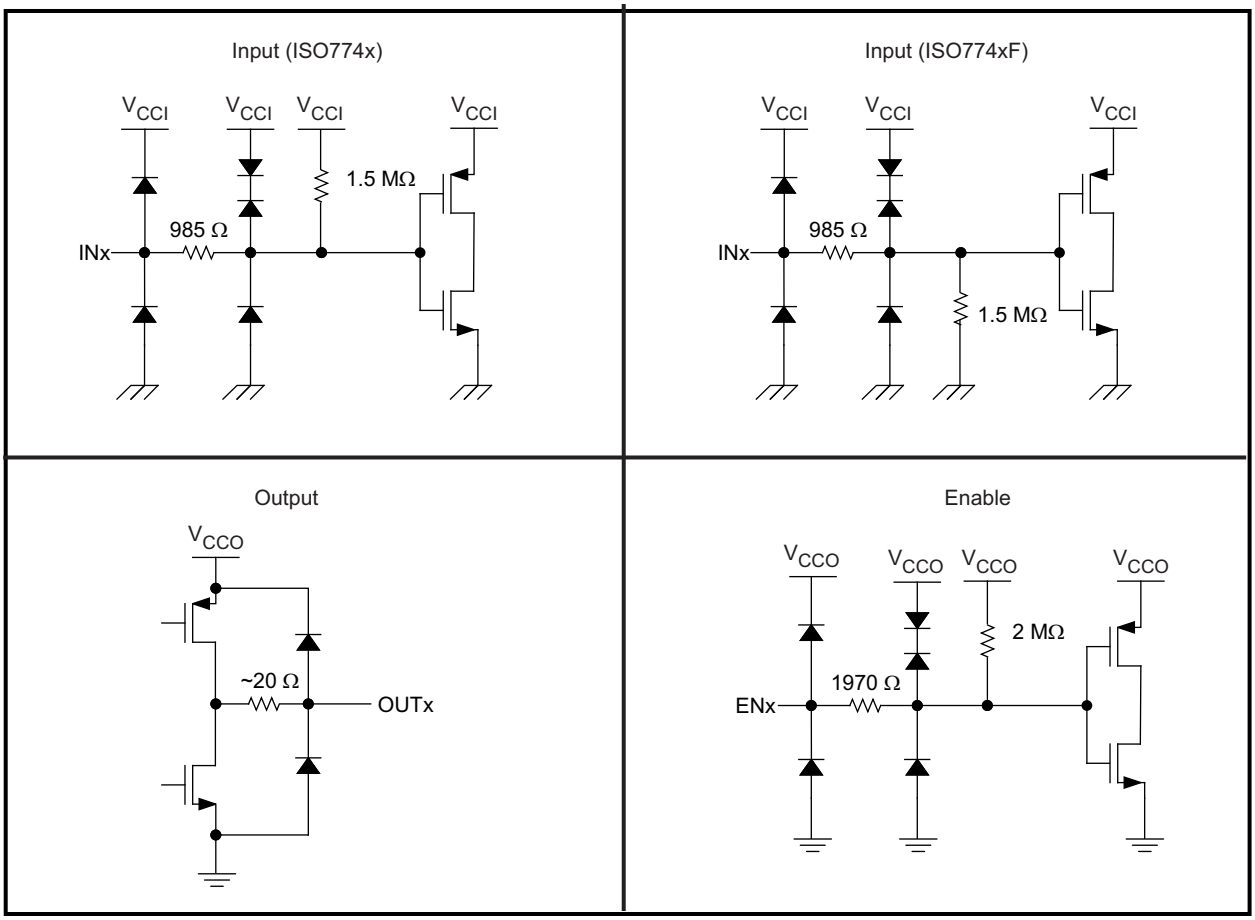


图 15. Device I/O Schematics

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO7741E-Q1 devices are high-performance, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and reduce power consumption. The ISO7741E-Q1 devices use single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

10.2 Typical Application

图 16 shows ISO7741E-Q1 in belt starter generator application.

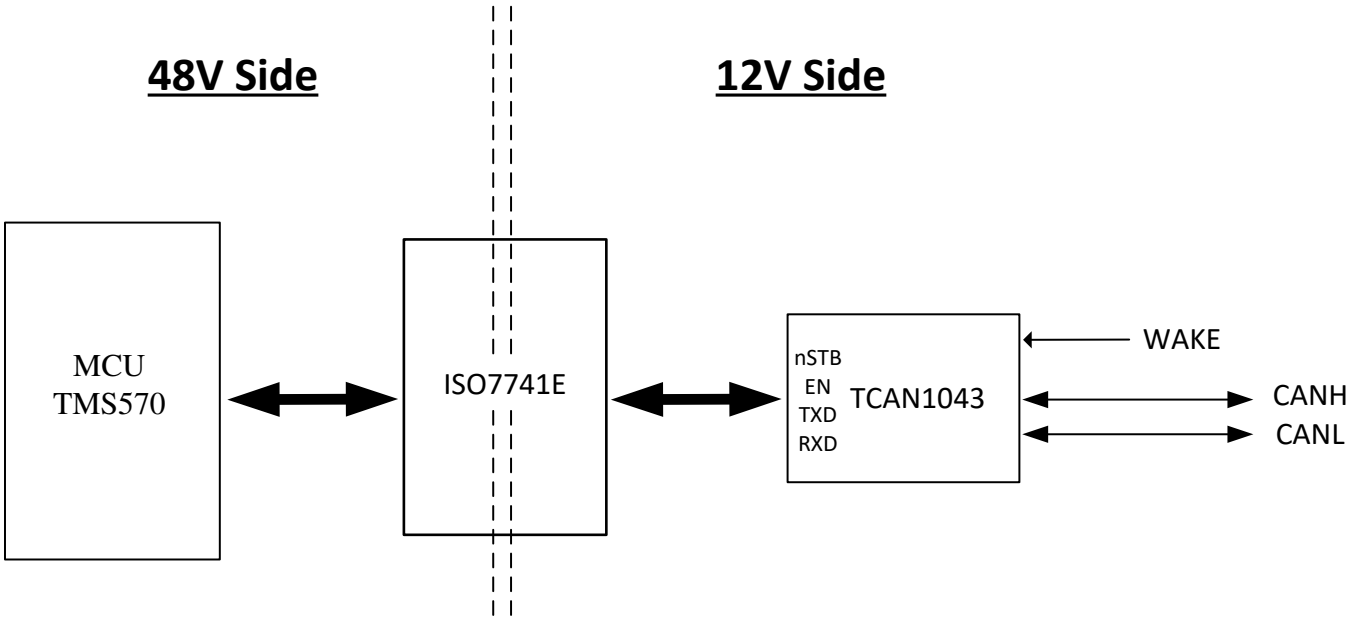


图 16. Belt Starter Generator Application

Typical Application (接下页)

10.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 4.

表 4. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

10.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7741E-Q1 device only require two external bypass capacitors to operate.

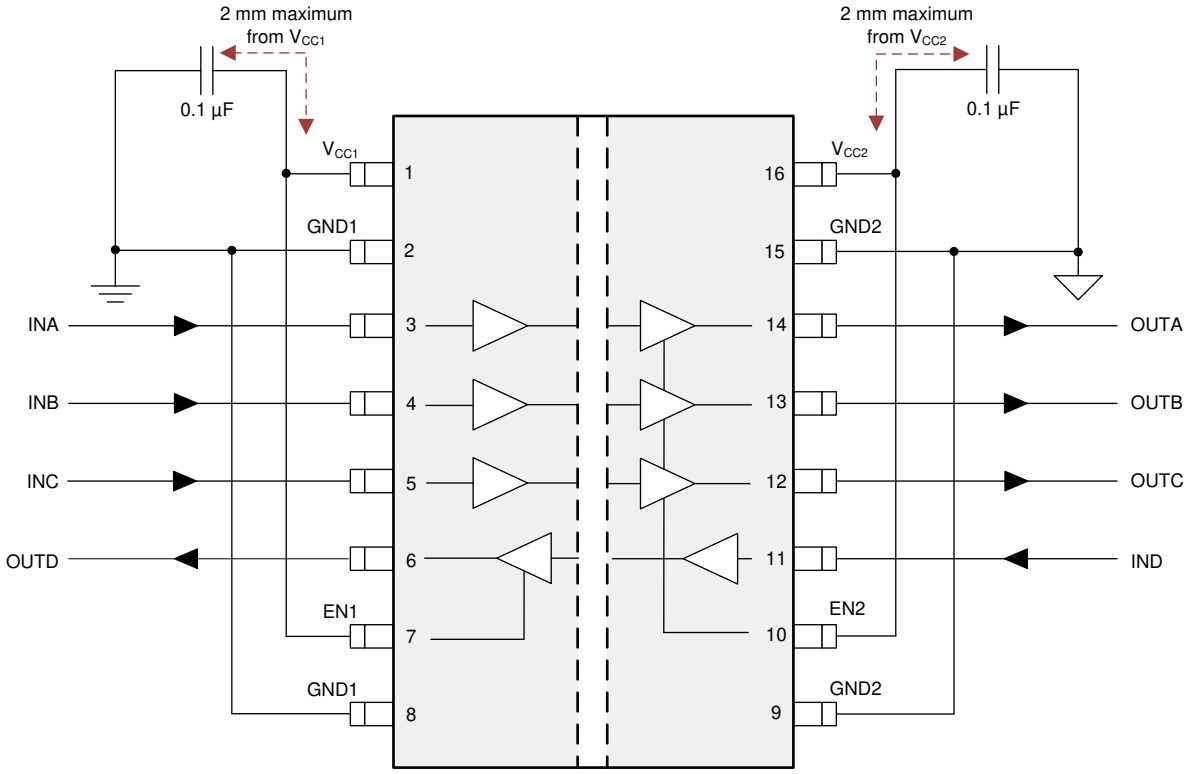


图 17. Typical ISO7741E-Q1 Circuit Hook-up

10.2.3 Application Curve

The following typical eye diagrams of the ISO7741E-Q1 device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

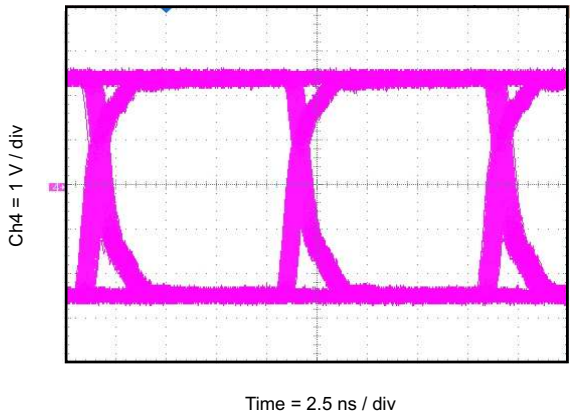


图 18. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 5 V and 25°C

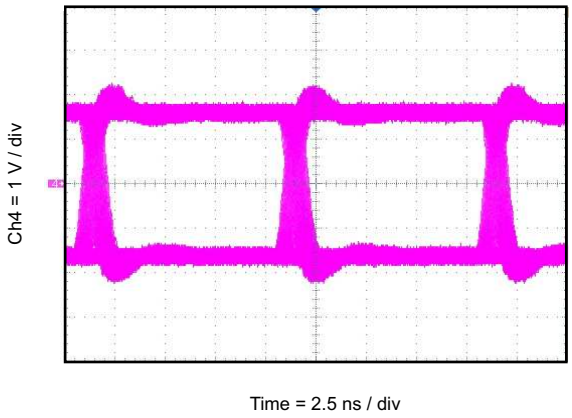


图 19. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

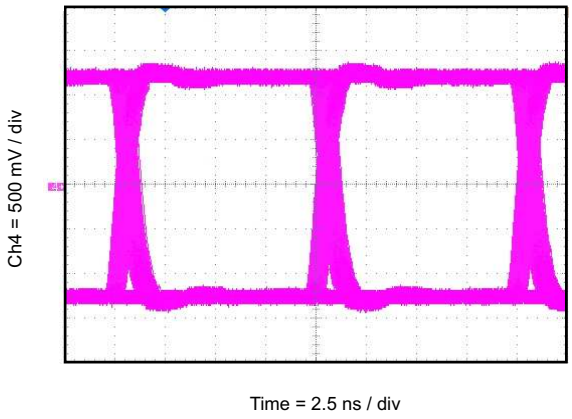


图 20. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

10.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 图 21 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

图 22 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 135 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS} and DBQ-16 package up to 400 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 135 years.

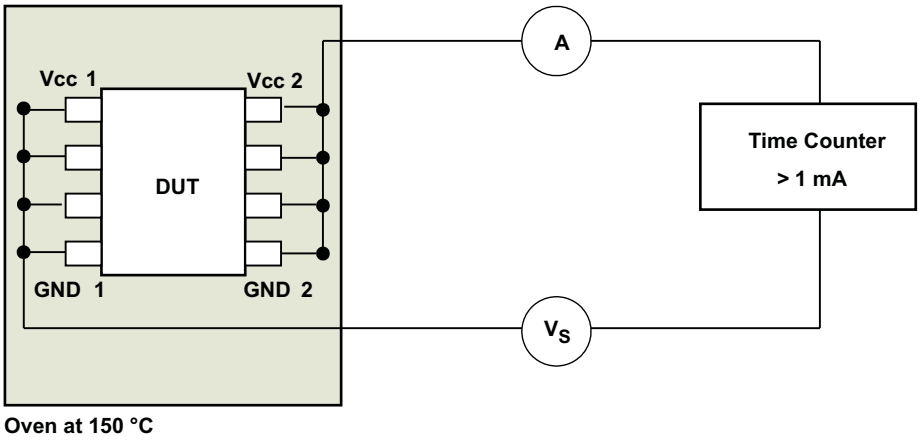


图 21. Test Setup for Insulation Lifetime Measurement

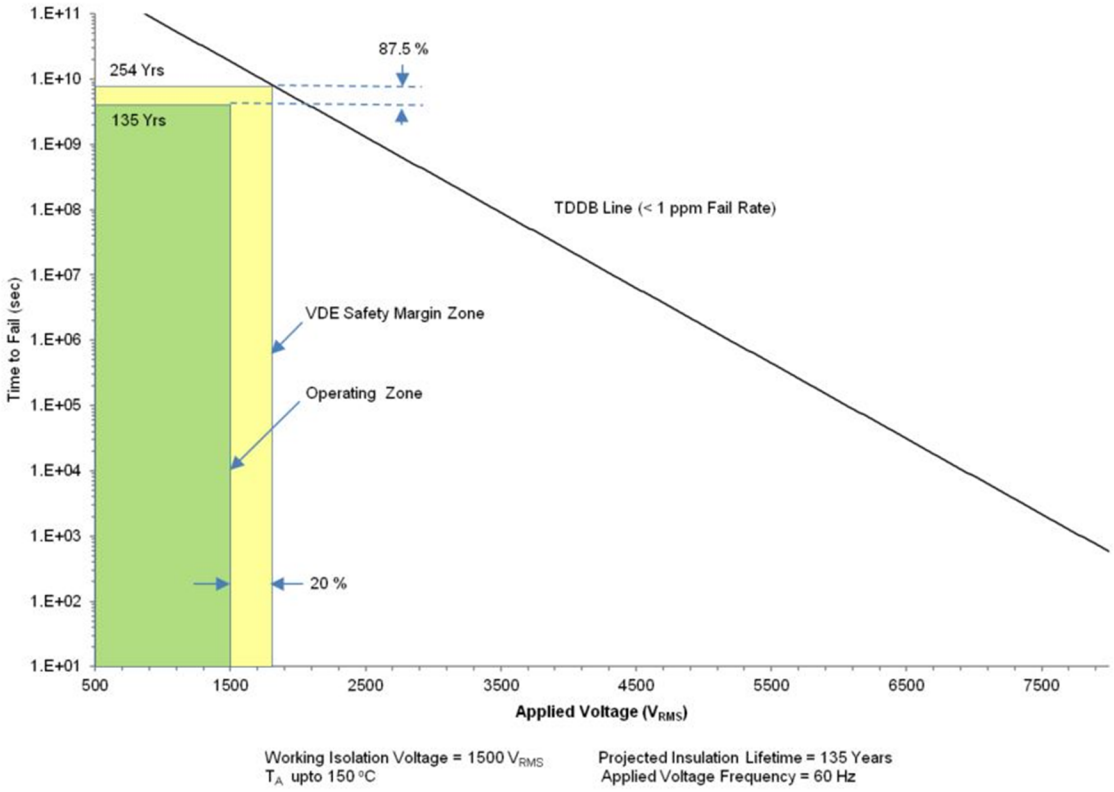


图 22. Insulation Lifetime Projection Data

11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet.

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 图 23). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

12.2 Layout Example

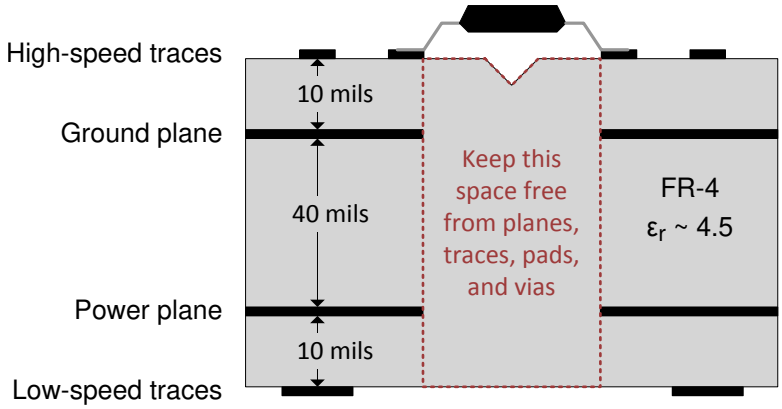


图 23. Layout Example Schematic

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《数字隔离器设计指南》*
- 德州仪器 (TI)，*《隔离相关术语》*
- 德州仪器 (TI)，*《如何通过隔离改善工业系统的 ESD、EFT 和浪涌抗扰性》*应用报告*如何通过隔离改善工业系统的 ESD、EFT 和浪涌抗扰性*"应用报告*如何通过隔离改善工业系统的 ESD、EFT 和浪涌抗扰性*"应用报告
- 德州仪器 (TI)，《具有 CAN FD 和唤醒功能的 TCAN1043xx-Q1 *低功耗故障保护 CAN 收发器》*数据表
- 德州仪器 (TI)，《TMS570LS0714 *16 位和 32 位 RISC 闪存微控制器》*数据表

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

13.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 商标

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All other trademarks are the property of their respective owners.

13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7741EDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	ISO7741E	Samples
ISO7741EDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	ISO7741E	Samples
ISO7741FEDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	ISO7741FE	Samples
ISO7741FEDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	ISO7741FE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

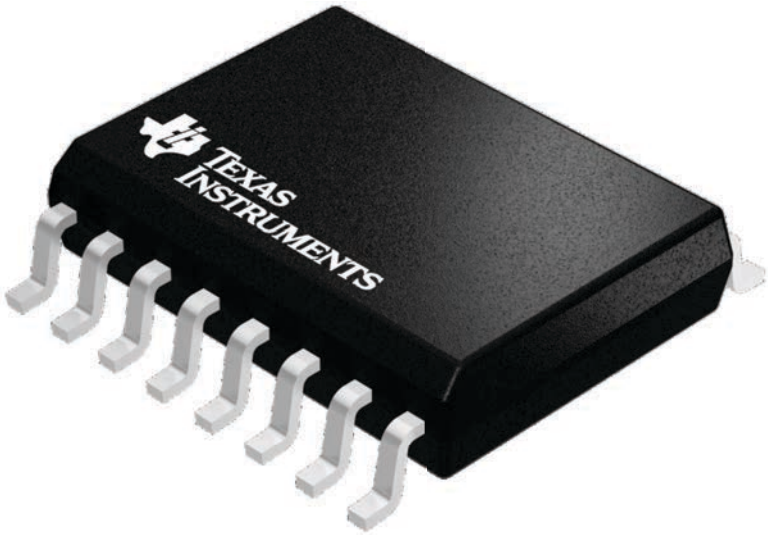
DW 16

SOIC - 2.65 mm max height

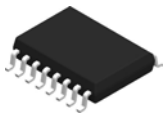
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

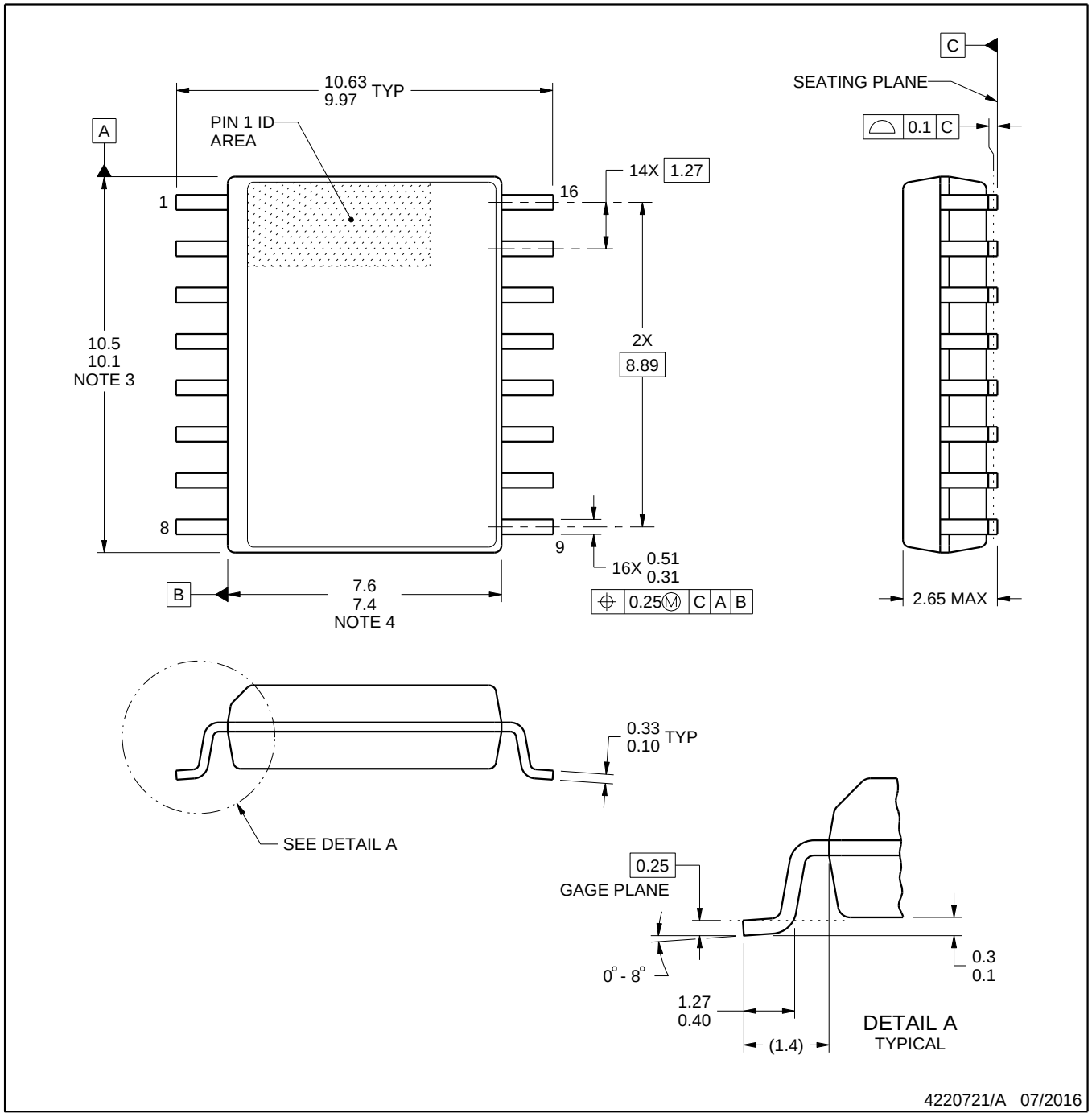


PACKAGE OUTLINE

DW0016A

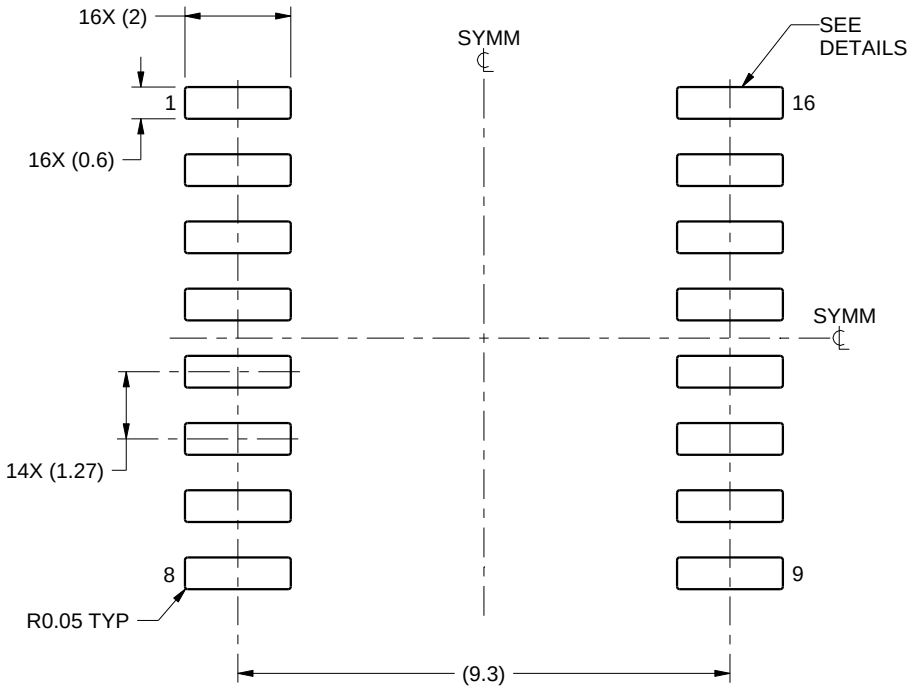
SOIC - 2.65 mm max height

SOIC

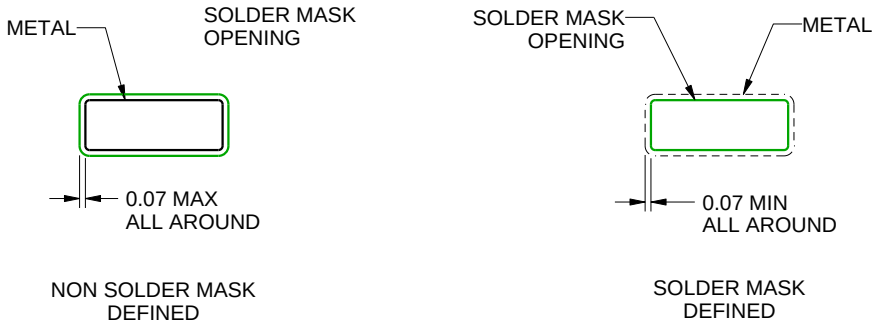


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

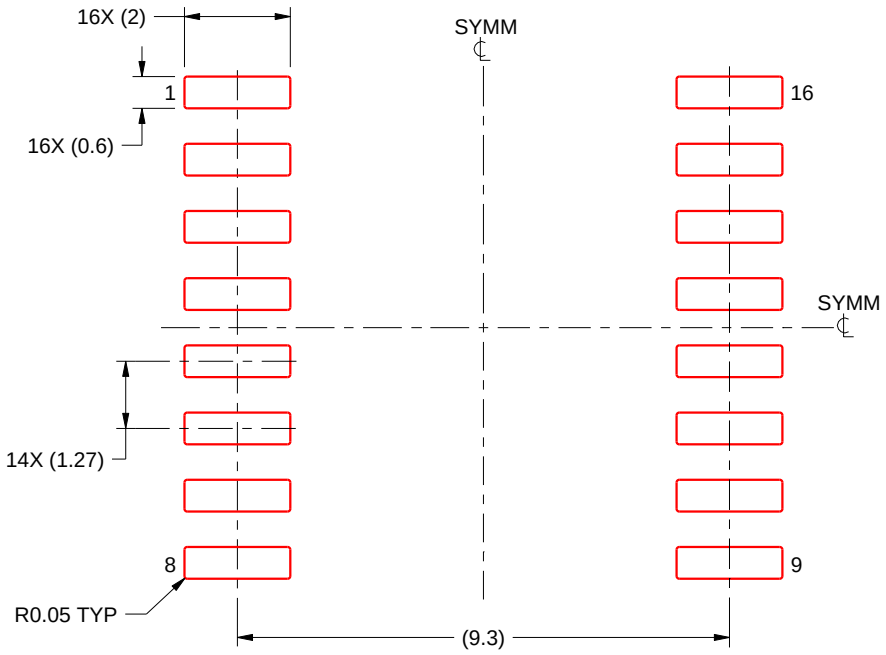


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



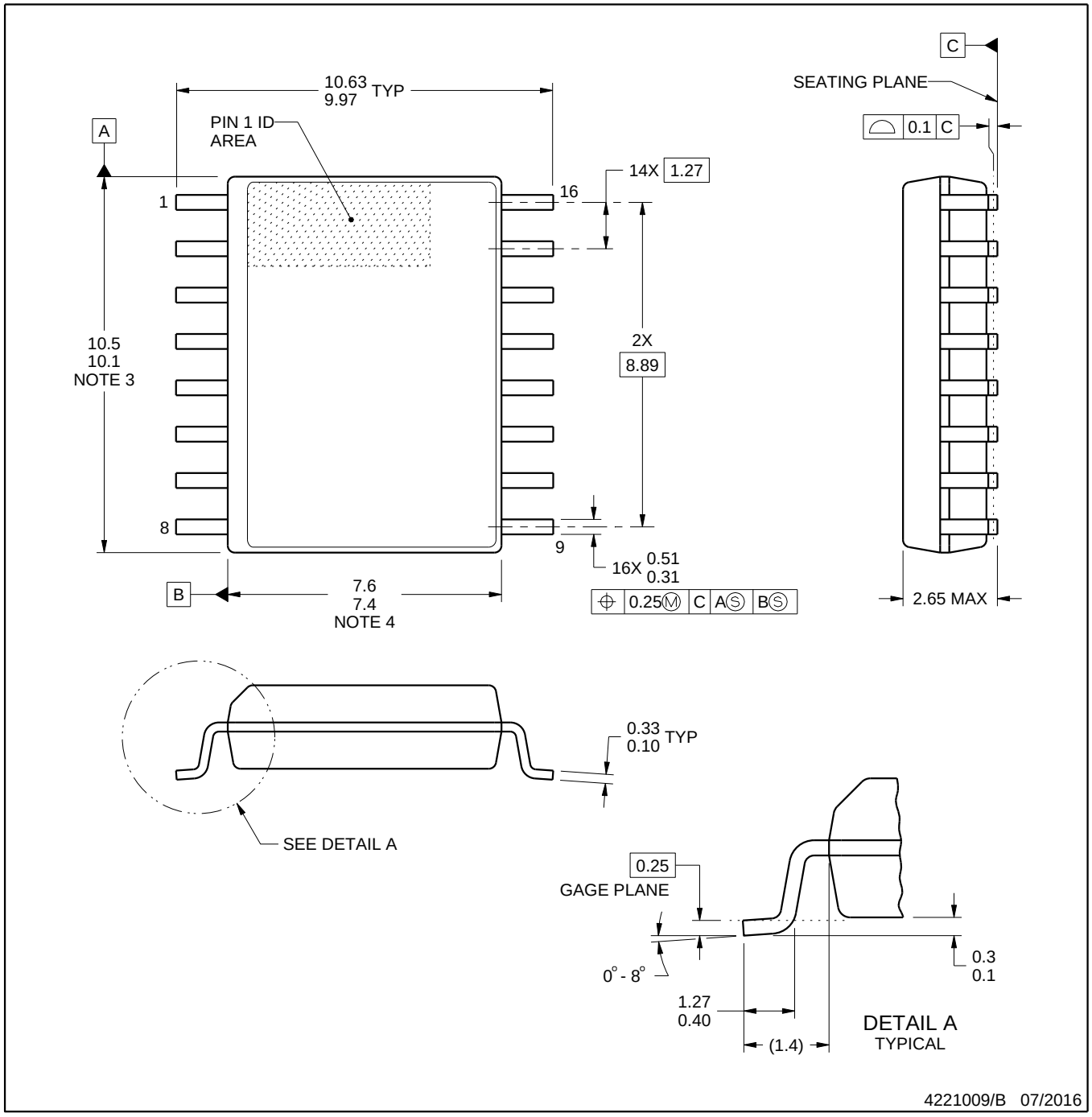
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

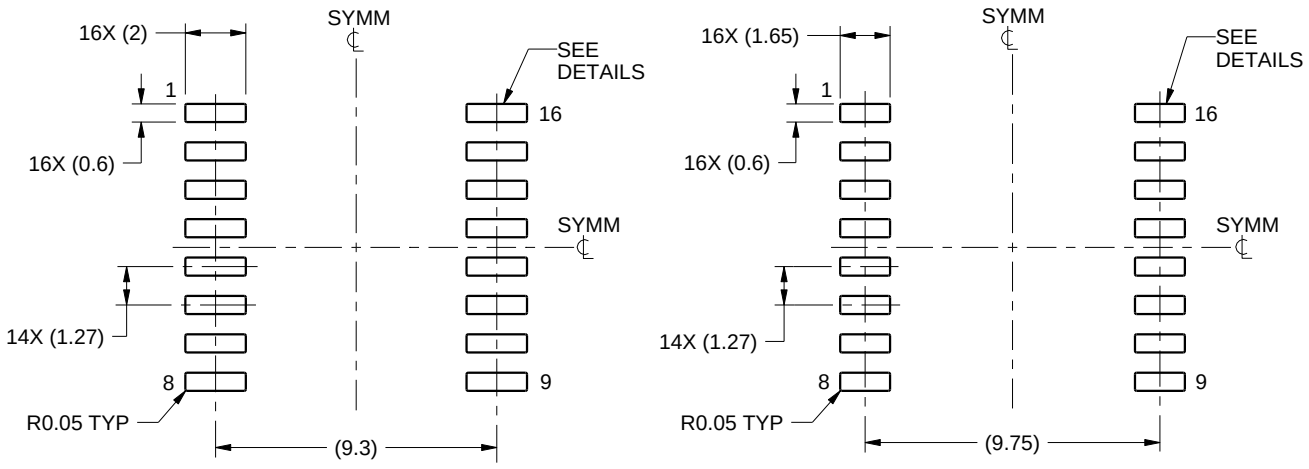
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

SOIC



NOTES:

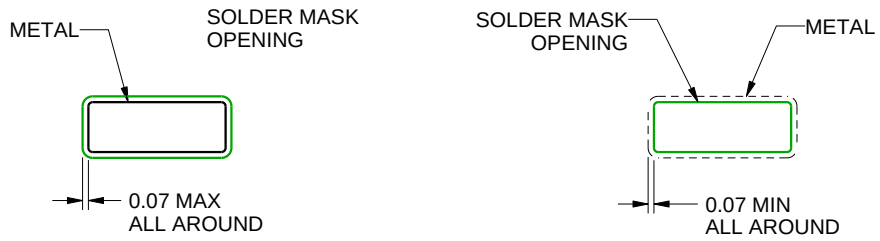
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

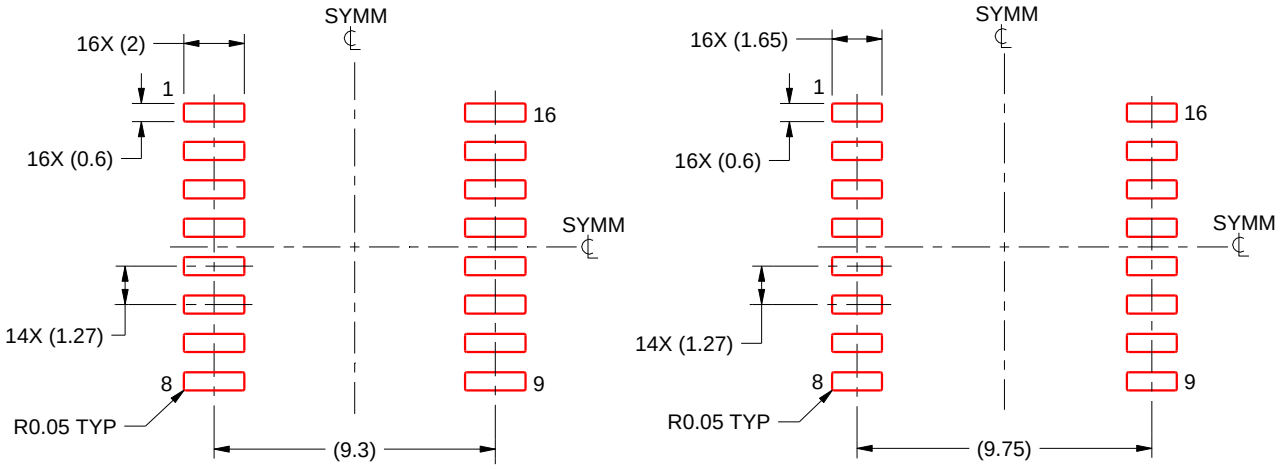
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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