

具有三态输出的 CD74HC125-Q1 汽车类四路缓冲器

1 特性

- 符合 AEC-Q100 车规认证：
 - 器件温度等级 1：
 - 40°C 至 +125°C, T_A
- 缓冲输入
- 正负输入钳位二极管
- 宽工作电压范围：2V 至 6V
- 支持多达 10 个 LSTTL 负载的扇出
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗

2 应用

- 使能数字信号

3 说明

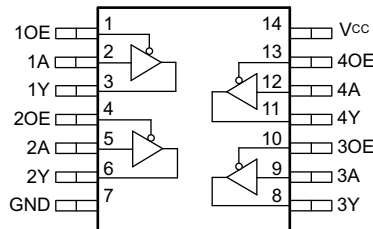
此器件包含四个具有三态输出的独立缓冲器。每个逻辑门以正逻辑执行布尔函数 $Y = A$ 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
CD74HC125QM96G4 Q1	SOIC (14)	8.70mm × 3.90mm
CD74HC125QPWRQ1	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

CD74HC125-Q1 的功能引脚



目录

1	特性	1	8.3	Feature Description	8
2	应用	1	8.4	Device Functional Modes	9
3	说明	1	9	Application and Implementation	10
4	修订历史记录	2	9.1	Application Information	10
5	Pin Configuration and Functions	3	9.2	Typical Application	10
6	Specifications	3	10	Power Supply Recommendations	12
6.1	Absolute Maximum Ratings	3	11	Layout	12
6.2	ESD Ratings	4	11.1	Layout Guidelines	12
6.3	Recommended Operating Conditions	4	11.2	Layout Example	12
6.4	Thermal Information	4	12	器件和文档支持	13
6.5	Electrical Characteristics	5	12.1	文档支持	13
6.6	Switching Characteristics	5	12.2	相关链接	13
6.7	Operating Characteristics	6	12.3	社区资源	13
6.8	Typical Characteristics	6	12.4	商标	13
7	Parameter Measurement Information	6	12.5	静电放电警告	13
8	Detailed Description	8	12.6	Glossary	13
8.1	Overview	8	13	机械、封装和可订购信息	13
8.2	Functional Block Diagram	8			

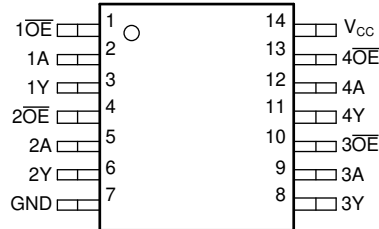
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (September 2008) to Revision B	Page
• 更新至全新数据表标准	1
• Changed $R_{\theta JA}$ for PW package from 113 °C/W to 151.7 °C/W	4
• Changed $R_{\theta JA}$ for D package from 86 °C/W to 133.6 °C/W	4

5 Pin Configuration and Functions

**D or PW Package
14-Pin SOIC or TSSOP
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1 \overline{OE}	1	Input	Channel 1, Output Enable, Active Low
1A	2	Input	Channel 1, Input A
1Y	3	Output	Channel 1, Output Y
2 \overline{OE}	4	Input	Channel 2, Output Enable, Active Low
2A	5	Input	Channel 2, Input A
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3 \overline{OE}	10	Input	Channel 3, Output Enable, Active Low
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4 \overline{OE}	13	Input	Channel 4, Output Enable, Active Low
V _{CC}	14	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		–0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < –0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < –0.5 V or V _O > V _{CC} + 0.5 V		±20	mA
I _O	Continuous output current	V _O > –0.5 V or V _O < V _{CC} + 0.5 V		±25	mA
	Continuous current through V _{CC} or GND			±70	mA
T _J	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 6\text{ V}$	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$			0.5	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 6\text{ V}$			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate	$V_{CC} = 2\text{ V}$			1000	ns
		$V_{CC} = 4.5\text{ V}$			500	
		$V_{CC} = 6\text{ V}$			400	
T_A	Operating free-air temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC		CD74HC125-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V _{CC}	Operating free-air temperature (T _A)						UNIT	
					25°C			-40°C to 125°C				
					MIN	TYP	MAX	MIN	TYP	MAX		
V _{OH}	High-level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9			1.9			V	
				4.5 V	4.4			4.4				
				6 V	5.9			5.9				
			I _{OH} = -6 mA	4.5 V	3.98			3.7				
			I _{OH} = -7.8 mA	6 V	5.48			5.2				
V _{OL}	Low-level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V				0.1			V	
				4.5 V				0.1				0.1
			I _{OL} = 20 μA	6 V			0.1			0.1		
			I _{OL} = 6 mA	4.5 V			0.26			0.4		
			I _{OL} = 7.8 mA	6 V			0.26			0.4		
I _I	Input leakage current	V _I = V _{CC} or GND		6 V				±0.1			±1	μA
I _{CC}	Supply current	V _I = V _{CC} or GND	I _O = 0 mA	6 V				8			160	μA
I _{OZ}	Off-state output current	V _I = V _{IL} or V _{IH}		6 V				±0.5			±10	μA
C _i	Input capacitance			2 V to 6 V				10			10	pF
C _O	Output capacitance	3-state						20			20	pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	CONDITIONS	V _{CC}	Operating free-air temperature (T _A)						UNIT
						25°C			−40°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	
t _{pd}	Propagation delay	A	Y	C _L = 50 pF	2 V	100			150			ns
					4.5 V	20			30			
					6 V	17			26			
				C _L = 15 pF	5 V	8						
t _{en}	Enable time	$\overline{\text{OE}}$	Y	C _L = 50 pF	2 V	125			190			ns
					4.5 V	25			38			
					6 V	21			32			
				C _L = 15 pF	5 V	10						
t _{dis}	Disable time	$\overline{\text{OE}}$	Y	C _L = 50 pF	2 V	125			190			ns
					4.5 V	25			38			
					6 V	21			32			
				C _L = 15 pF	5 V	10						
t _t	Transition-time		Y	C _L = 50 pF	2 V	60			90			ns
					4.5 V	12			18			
					6 V	10			15			

6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load		29		pF

6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$

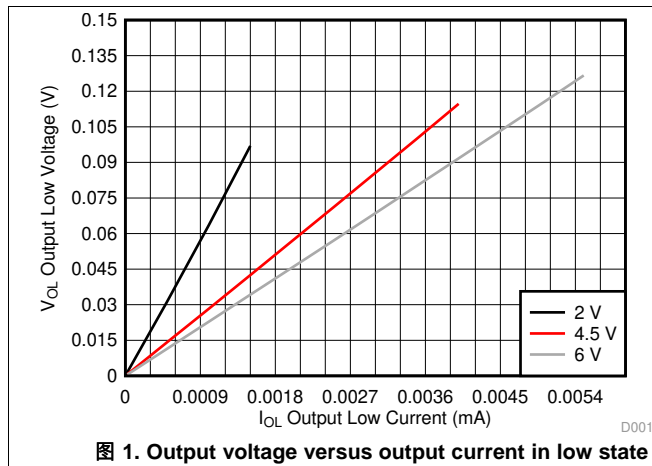


图 1. Output voltage versus output current in low state

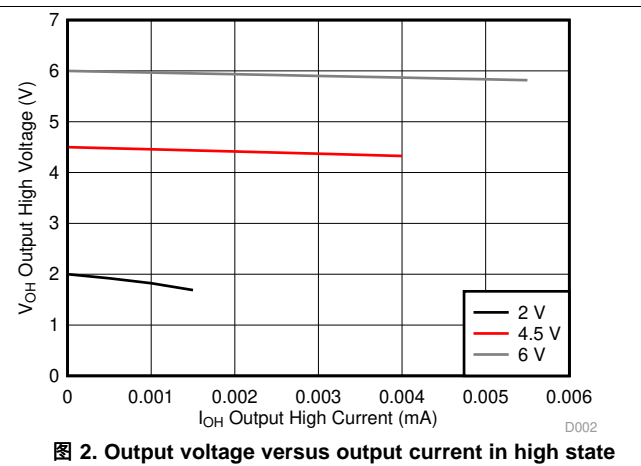
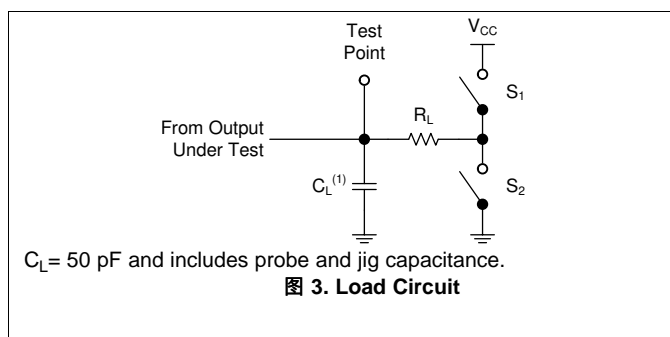


图 2. Output voltage versus output current in high state

7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_f < 6\text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.



$C_L = 50\text{ pF}$ and includes probe and jig capacitance.

图 3. Load Circuit

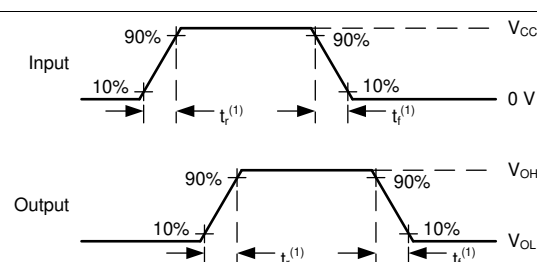
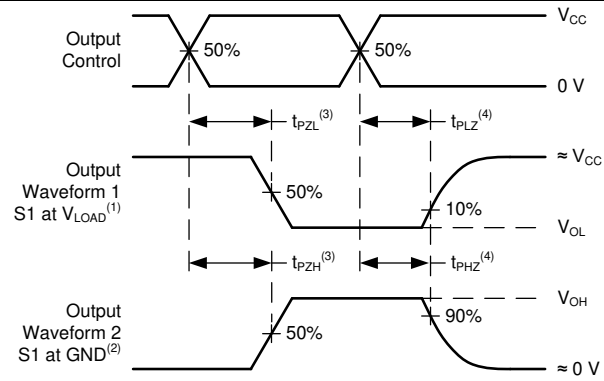


图 4. Voltage Waveforms Transition Times

Parameter Measurement Information (接下页)



The maximum between t_{PLH} and t_{PHL} is used for t_{pd} .

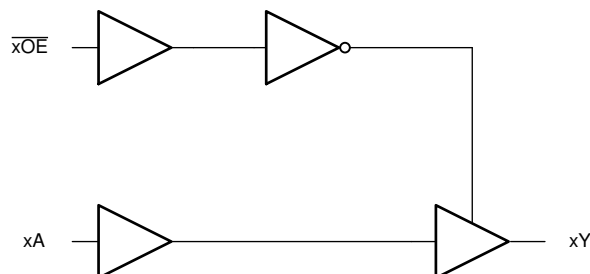
**图 5. Voltage Waveforms
Propagation Delays**

8 Detailed Description

8.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function $Y = A$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

The CD74HC125-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

3-State outputs can be placed into a high-impedance state. In this state, the output will neither source nor sink current, and leakage current is defined by the I_{OZ} specification in the [Electrical Characteristics](#). A pull-up or pull-down resistor can be used to ensure that the output remains HIGH or LOW, respectively, during the high-impedance state.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (接下页)

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 6.

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

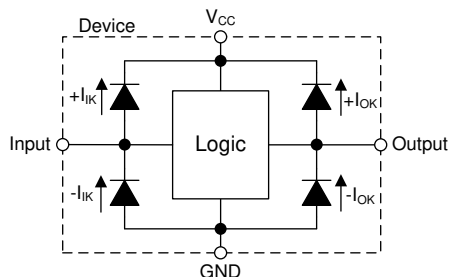


图 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 1. Function Table

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In this application, a buffer with 3-state output is used to disable a data signal as shown in [图 7](#). The remaining three buffers can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

9.2 Typical Application

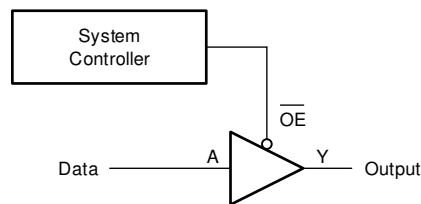


图 7. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC125-Q1 plus the maximum supply current, I_{CC} , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\text{max})$ listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HC125-Q1, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

Typical Application (接下页)

The CD74HC125-Q1 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [Recommended Operating Conditions](#).

Refer to the [Feature Description](#) for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [Electrical Characteristics](#).

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to [Feature Description](#) for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the [Layout](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HC125-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

9.2.3 Application Curves

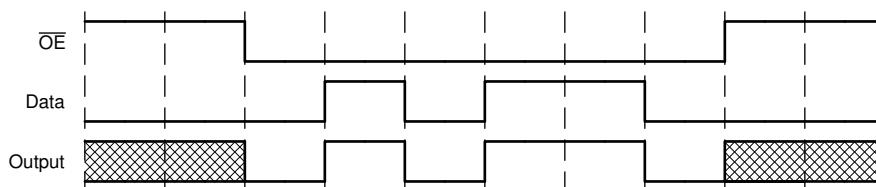


图 8. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Figure 9](#).

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

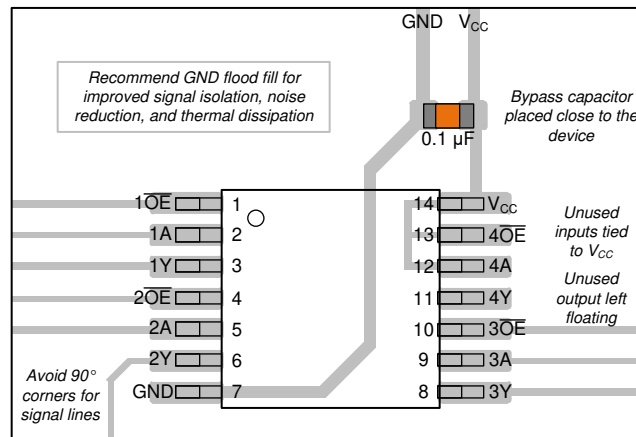


图 9. Example layout for the CD74HC125-Q1

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- [《HCMOS 设计注意事项》](#)
- [《CMOS 功耗与 CPD 计算》](#)
- [《使用逻辑器件进行设计》](#)

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

12.3 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC125QM96G4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC125Q	Samples
CD74HC125QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC125Q	Samples
CD74HC125QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC125Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD74HC125-Q1 :

- Catalog : [CD74HC125](#)
- Military : [CD54HC125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC125QM96G4Q1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC125QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC125QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC125QM96G4Q1	SOIC	D	14	2500	853.0	449.0	35.0
CD74HC125QPWRG4Q1	TSSOP	PW	14	2000	853.0	449.0	35.0
CD74HC125QPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司