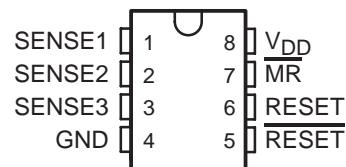


- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product Change Notification
- Qualification Pedigree†
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Triple Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator With Fixed Delay Time of 200 ms, No External Capacitor Needed
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40 μA
- Supply Voltage Range . . . 2 V to 6 V
- Defined RESET Output from $V_{\text{DD}} \geq 1.1$ V
- SO-8 and MSOP-8 Packages

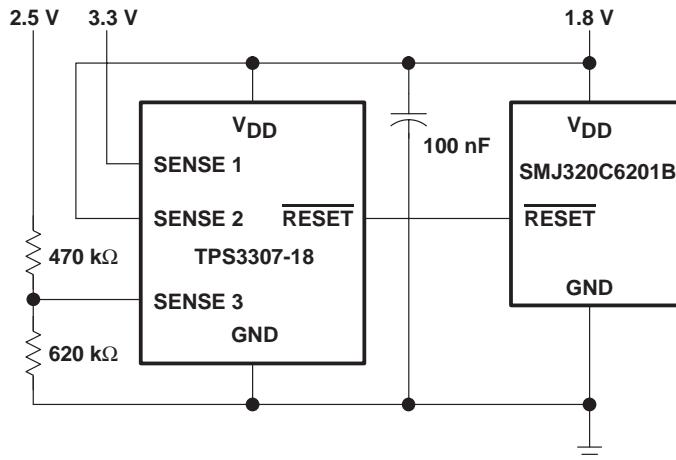
† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D or DGN PACKAGE
(TOP VIEW)



typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses Texas Instruments part numbers TPS3307-18 and SMJ320C6201B.



- Military applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Military Systems

Figure 1. Applications Using the TPS3307-18

description

The TPS3307-xx family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems which require more than one supply voltage.

The TPS3307-18 and TPS3307-33 are designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj and 5V/3.3V/adj, respectively. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPS3307-18-EP, TPS3307-33-EP TRIPLE PROCESSOR SUPERVISORS

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description (continued)

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3 V	1.8 V	User defined	2.93 V	1.68 V	1.25 V [†]
TPS3307-33	5 V	3.3 V	User defined	4.55 V	2.93 V	1.25 V [†]

[†] The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on, RESET is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps RESET active as long as SENSEn remain below the threshold voltage V_{IT+} .

An internal timer delays the return of the RESET output to the inactive state (high) to ensure proper system reset. The delay time, $t_{dtyp} = 200$ ms, starts after all SENSEn inputs have risen above the threshold voltage V_{IT+} . When the voltage at any SENSE input drops below the threshold voltage V_{IT-} , the RESET output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input, MR. A low level at MR causes RESET to become active. In addition to the active-low RESET output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or a standard 8-pin SO packages and are characterized for operation over a temperature range of -55°C to 125°C .

ORDERING INFORMATION

TA	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	Small Outline (D)	Tape and Reel	TPS3307-18MDREP	30718E
	PowerPad μ -Small Outline (DGN)	Tape and Reel	TPS3307-33MDGNREP	BNP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION/TRUTH TABLES

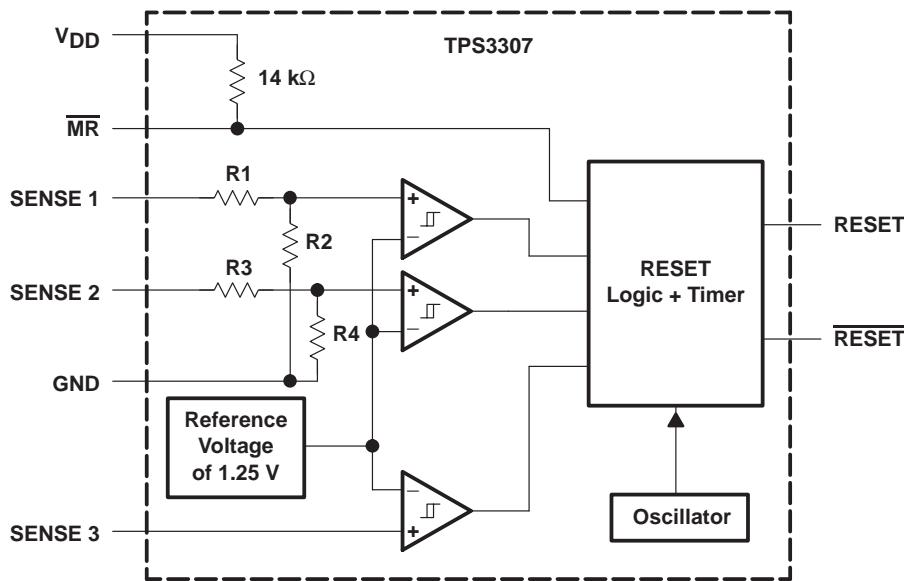
<u>MR</u>	SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	SENSE3 > V_{IT3}	<u>RESET</u>	RESET
L	X	X	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

X = Don't care

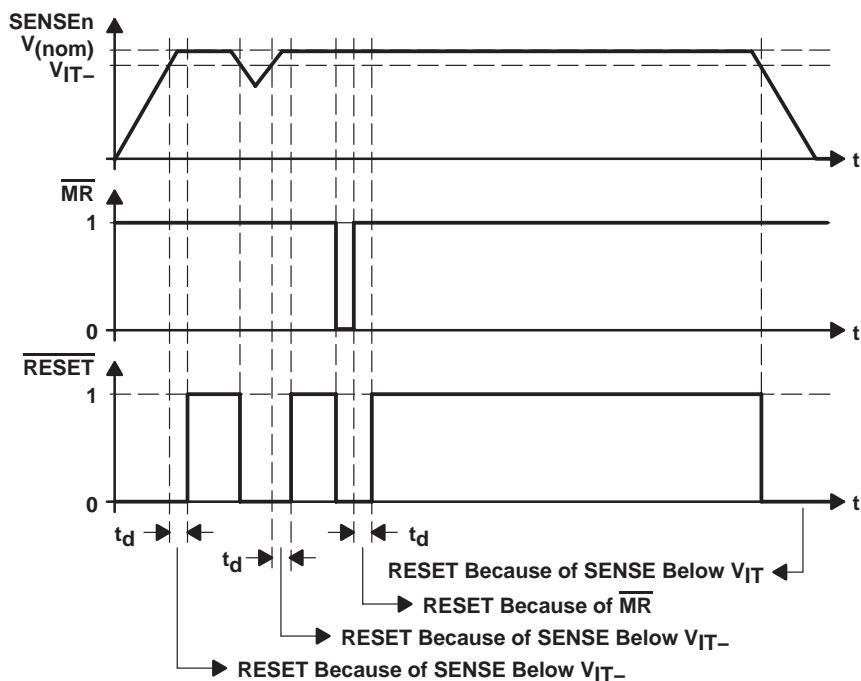


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

functional block diagram



timing diagram



TPS3307-18-EP, TPS3307-33-EP TRIPLE PROCESSOR SUPERVISORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	7 V
All other pins (see Note 1)	-0.3 V to 7 V
Maximum low output current, I_{OL}	5 mA
Maximum high output current, I_{OH}	-5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 20 mA
Maximum junction temperature, T_J	150°C
Package thermal impedance, θ_{JA} (see Note 2)	
D package	126°C/W
DGN package	58.4°C/W
Operating free-air temperature range, T_A	-55°C to 125°C
Storage temperature range, T_{stg} (see Note 3)	-65°C to 150°C
Soldering temperature	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than $t = 1000$ h continuously.

NOTE 2: The thermal impedance, θ_{JA} , for the D package is determined for JEDEC high-K PCB (JESD51-7). The thermal impedance value for the DGN package is determined for Texas Instruments recommended assembly for PowerPAD packages. See Texas Instruments technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package. Thermal impedance, θ_{JA} , values for the D and DGN packages using JEDEC low-K PCB (JESD51-3) are 215°C/W and 296°C/W, respectively.

NOTE 3: Long-term, high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See <http://www.ti.com/sc/ep> for more information.

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage at MR and SENSE3, V_I	0	$V_{DD}+0.3$	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD}+0.3)V_{IT}/1.25$ V	V
High-level input voltage at MR, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage at MR, V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at MR, $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	-55	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V_{OH}	High-level output voltage	$V_{DD} = 2 \text{ V to } 6 \text{ V}$, $I_{OH} = -20 \mu\text{A}$		$V_{DD} - 0.2 \text{ V}$			V	
		$V_{DD} = 3.3 \text{ V}$, $I_{OH} = -2 \text{ mA}$		$V_{DD} - 0.4 \text{ V}$				
		$V_{DD} = 6 \text{ V}$, $I_{OH} = -3 \text{ mA}$		$V_{DD} - 0.4 \text{ V}$				
V_{OL}	Low-level output voltage	$V_{DD} = 2 \text{ V to } 6 \text{ V}$, $I_{OL} = 20 \mu\text{A}$				0.2	V	
		$V_{DD} = 3.3 \text{ V}$, $I_{OL} = 2 \text{ mA}$				0.4		
		$V_{DD} = 6 \text{ V}$, $I_{OL} = 3 \text{ mA}$				0.4		
Power-up reset voltage (see Note 4)		$V_{DD} \geq 1.1 \text{ V}$, $I_{OL} = 20 \mu\text{A}$				0.4	V	
V_{IT-}	Negative-going input threshold voltage (see Note 5)	$SENSE3$	$V_{DD} = 2 \text{ V to } 6 \text{ V}$		1.2	1.25	1.29	V
		$SENSE1, SENSE2$		$VSENSE = 1.8 \text{ V}$	1.6	1.68	1.73	
				$VSENSE = 3.3 \text{ V}$	2.8	2.93	3.02	
				$VSENSE = 5 \text{ V}$	4.4	4.55	4.67	
V_{hys}	Hysteresis at VSENSEn input	$V_{IT-} = 1.25 \text{ V}$			2	10	30	mV
		$V_{IT-} = 1.68 \text{ V}$			2	15	40	
		$V_{IT-} = 2.93 \text{ V}$			3	30	60	
		$V_{IT-} = 4.55 \text{ V}$			3	40	80	
I_H	High-level input current	MR	$MR = 0.7 \times V_{DD}$, $V_{DD} = 6 \text{ V}$		-130	-180		μA
		$SENSE1$	$VSENSE1 = V_{DD} = 6 \text{ V}$		5	8		
		$SENSE2$	$VSENSE2 = V_{DD} = 6 \text{ V}$		6	9		
		$SENSE3$	$VSENSE3 = V_{DD}$		-1	1		
I_L	Low-level input current	MR	$MR = 0 \text{ V}$, $V_{DD} = 6 \text{ V}$		-430	-600		μA
		$SENSEn$	$VSENSE1,2,3 = 0 \text{ V}$		-1	1		
I_{DD}	Supply current					40	μA	
C_i	Input capacitance	$V_I = 0 \text{ V to } V_{DD}$				10	pF	

NOTES: 4. The lowest supply voltage at which RESET becomes active. t_r , $V_{DD} \geq 15 \mu\text{s/V}$

5. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

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timing requirements at $V_{DD} = 2 \text{ V to } 6 \text{ V}$, $R_L = 1 \text{ M}\Omega$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w Pulse width	SENSEn	$V_{SENSEnL} = V_{IT_-} - 0.2 \text{ V}$, $V_{SENSEnH} = V_{IT_+} + 0.2 \text{ V}$	6			μs
	MR	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

switching characteristics at $V_{DD} = 2 \text{ V to } 6 \text{ V}$, $R_L = 1 \text{ M}\Omega$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time	$V_{I(SENSEn)} \geq V_{IT_+} + 0.2 \text{ V}$, $MR \geq 0.7 \times V_{DD}$, See timing diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	\overline{MR} to \overline{RESET}		200	600	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	\overline{MR} to $RESET$				
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to \overline{RESET}				
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $RESET$	1	5		μs

TYPICAL CHARACTERISTICS

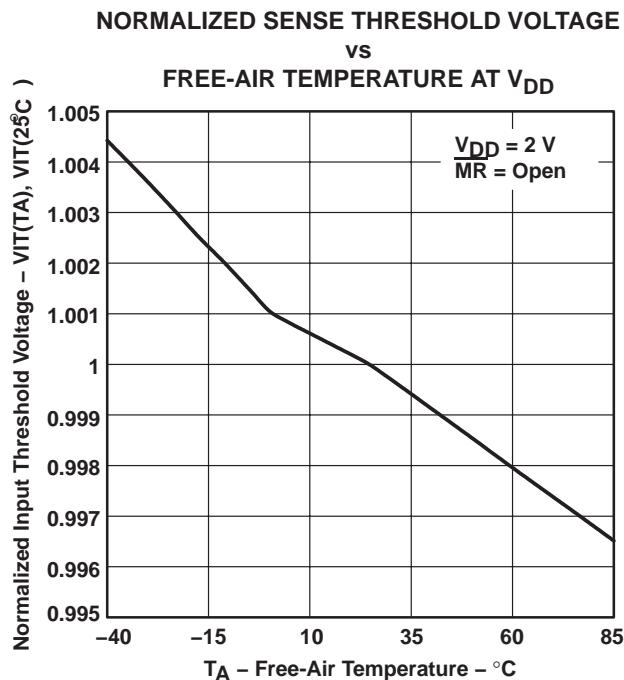


Figure 2

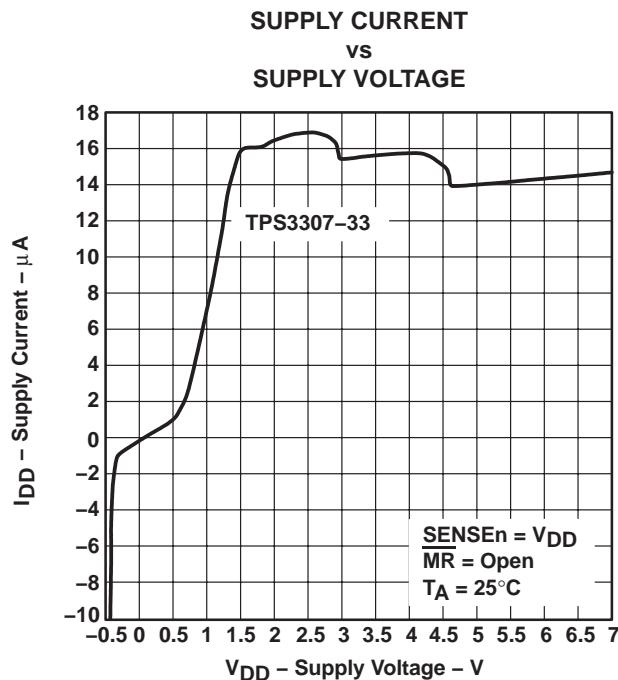


Figure 3

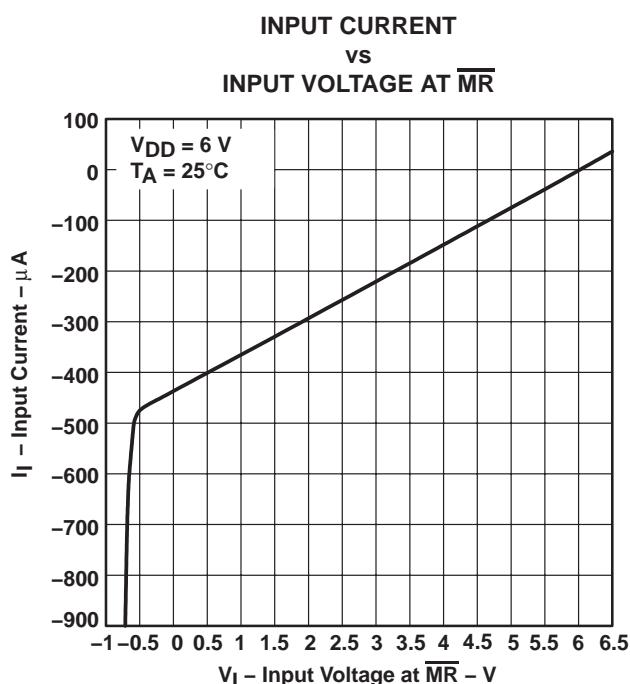


Figure 4

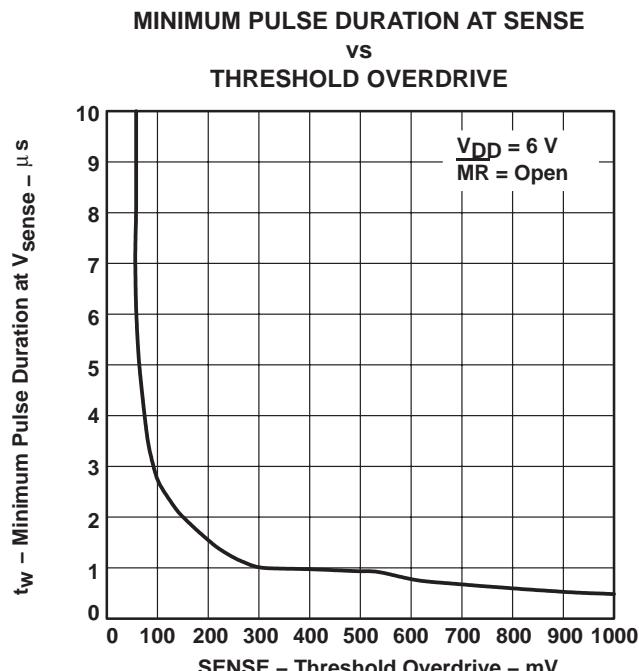


Figure 5

TPS3307-18-EP, TPS3307-33-EP TRIPLE PROCESSOR SUPERVISORS

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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

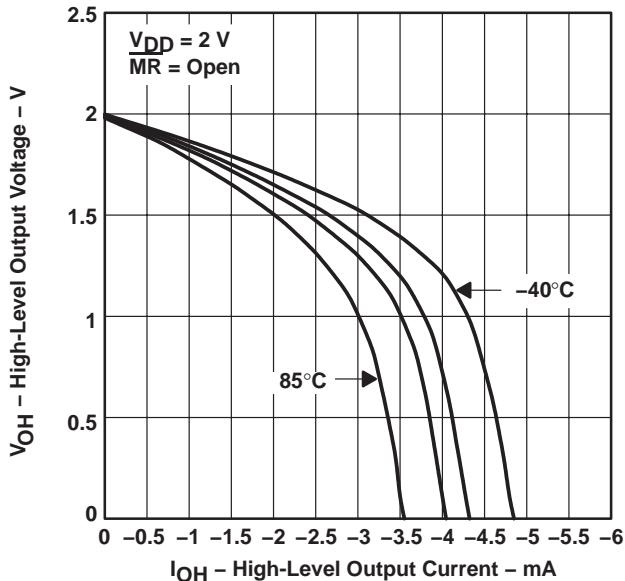


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

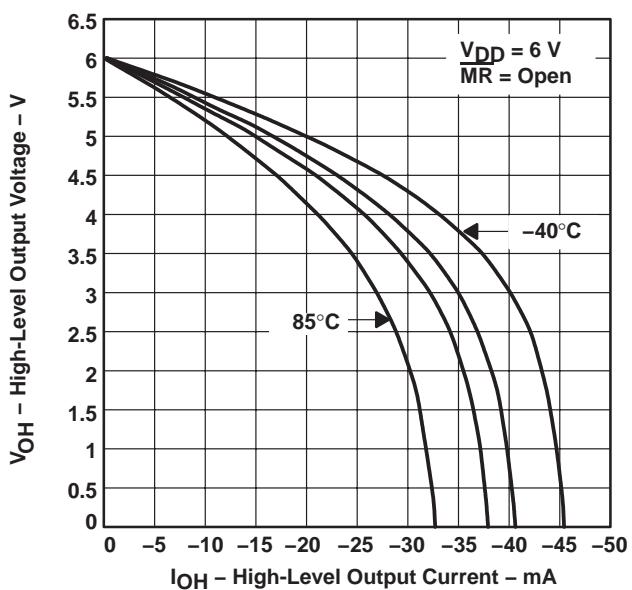


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

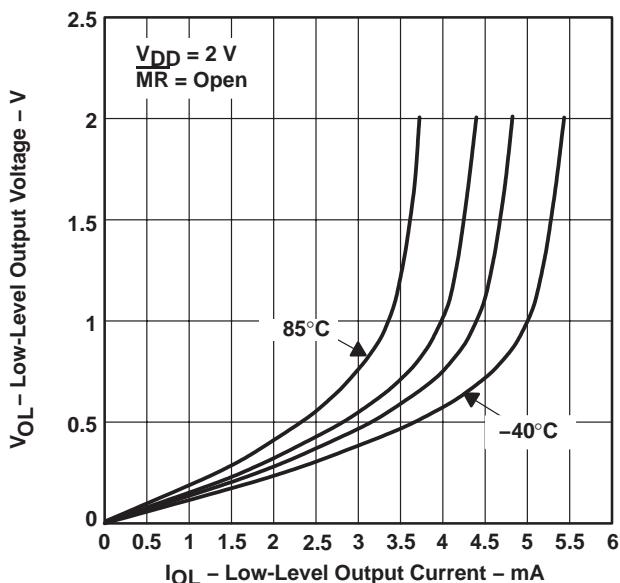


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

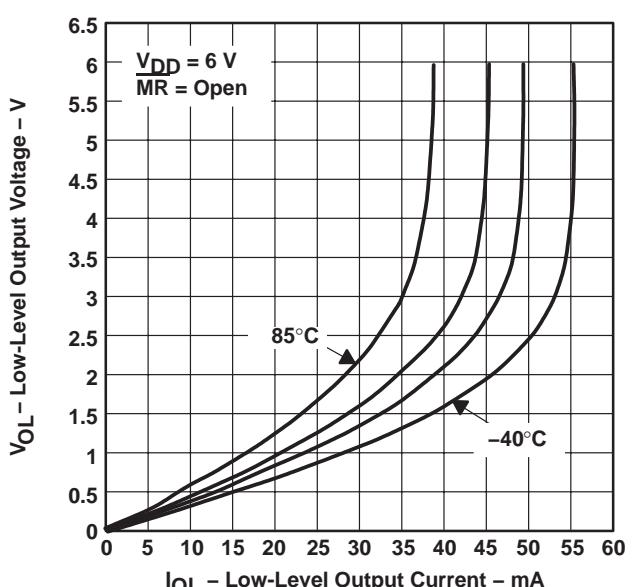


Figure 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3307-18MDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	30718E	Samples
TPS3307-18MDREPG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	30718E	Samples
TPS3307-33MDGNREP	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BNP	Samples
V62/03629-01XE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	30718E	Samples
V62/03629-02YE	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BNP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

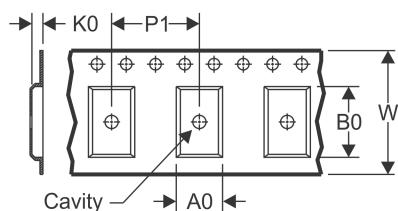
OTHER QUALIFIED VERSIONS OF TPS3307-EP :

- Catalog: [TPS3307](#)

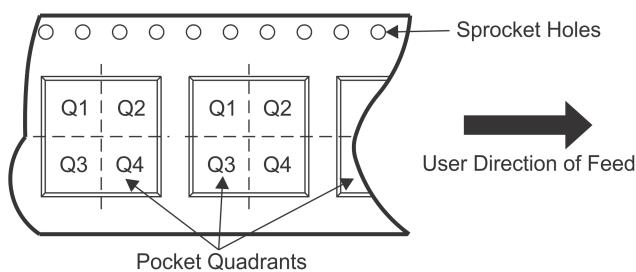
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

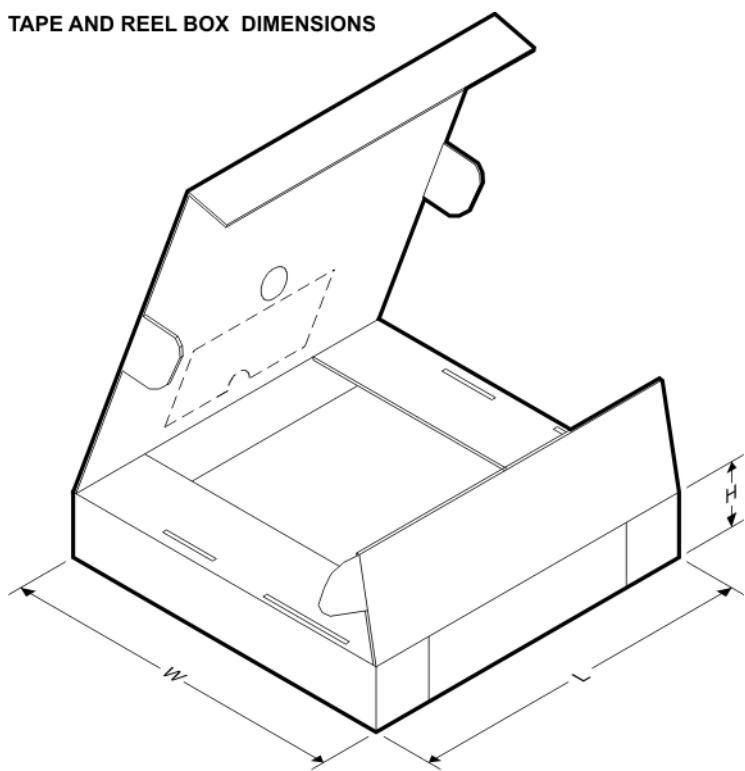
TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3307-18MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3307-33MDGNREP	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3307-18MDREP	SOIC	D	8	2500	350.0	350.0	43.0
TPS3307-33MDGNREP	HVSSOP	DGN	8	2500	358.0	335.0	35.0

GENERIC PACKAGE VIEW

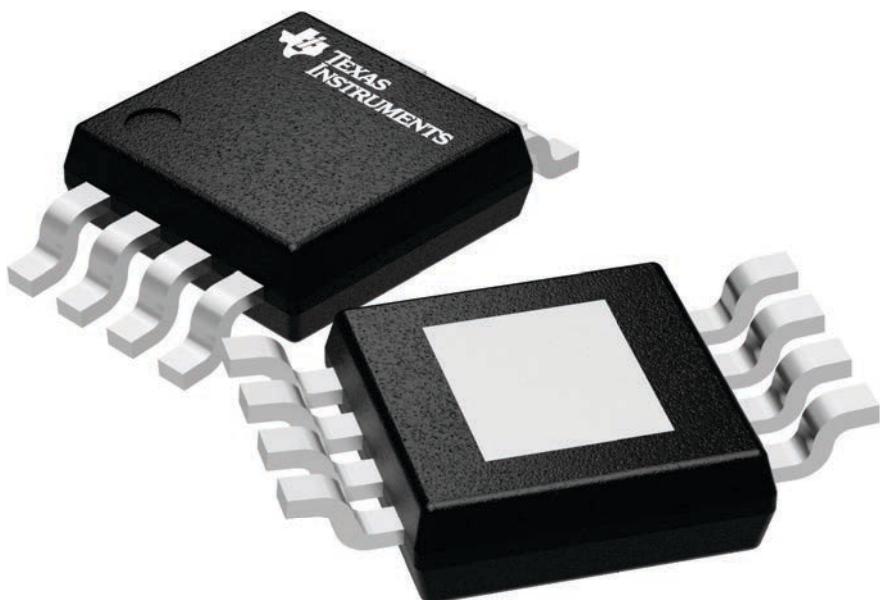
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

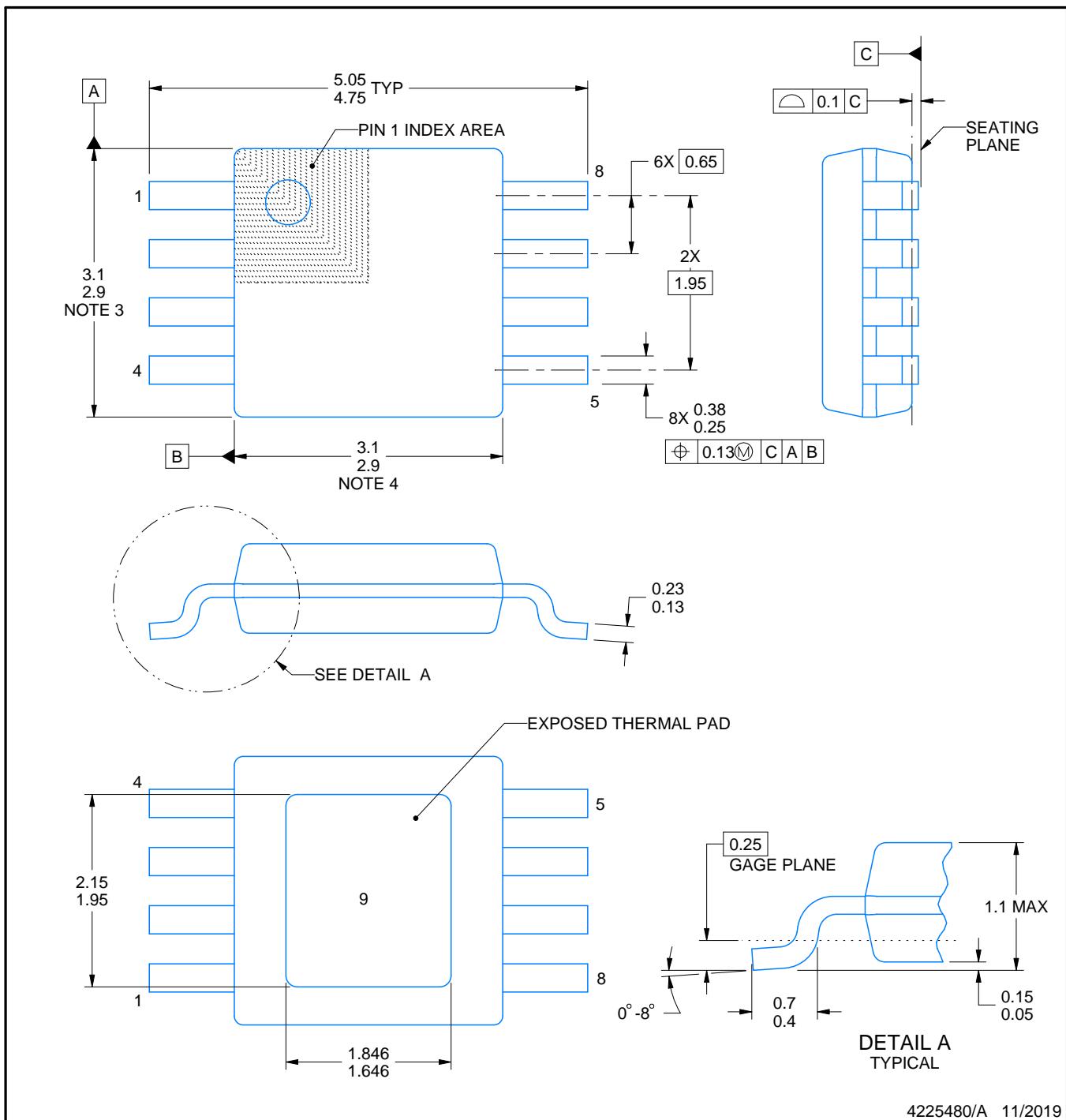
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

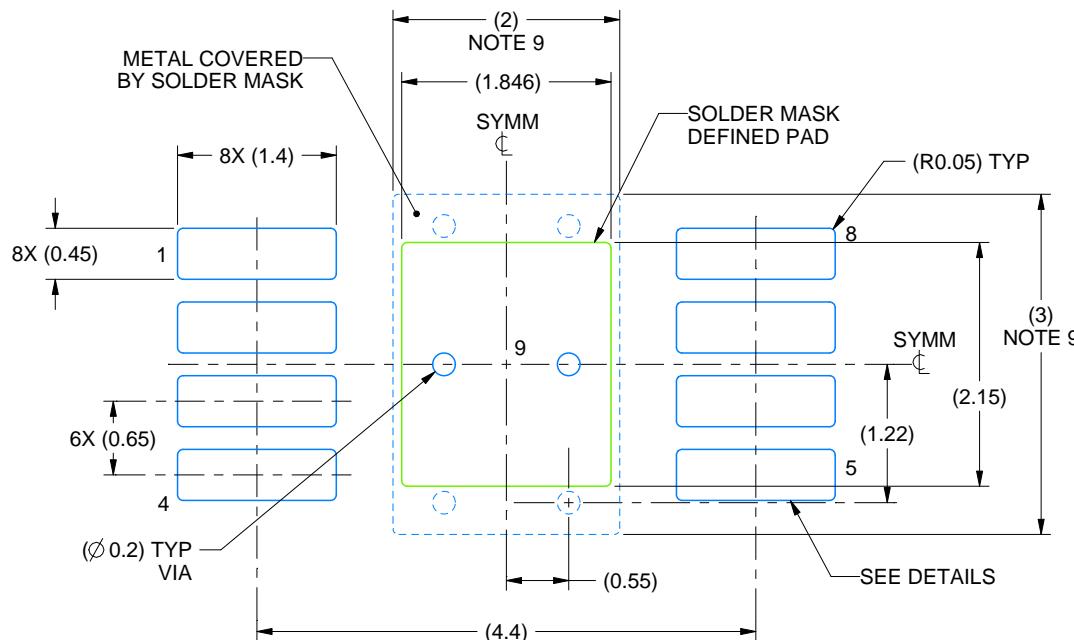
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

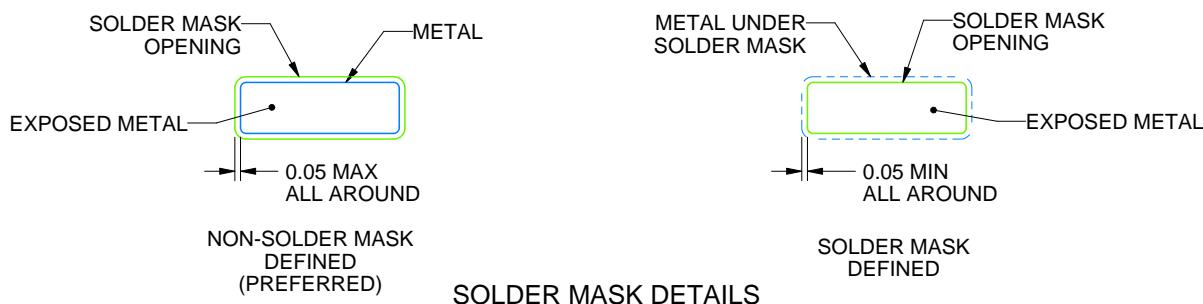
DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



4225480/A 11/2019

NOTES: (continued)

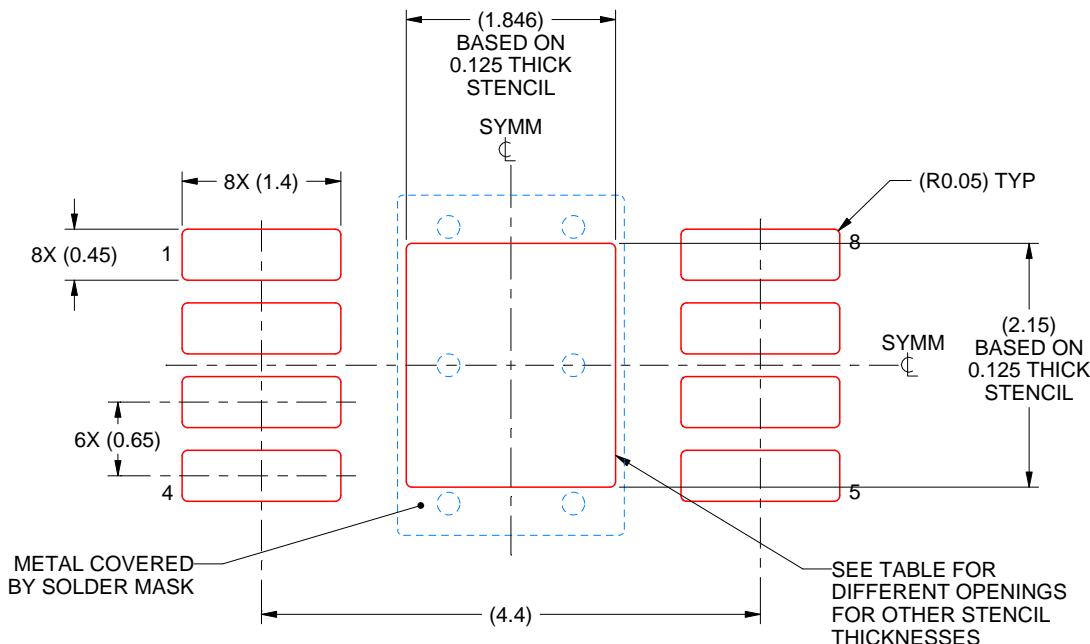
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

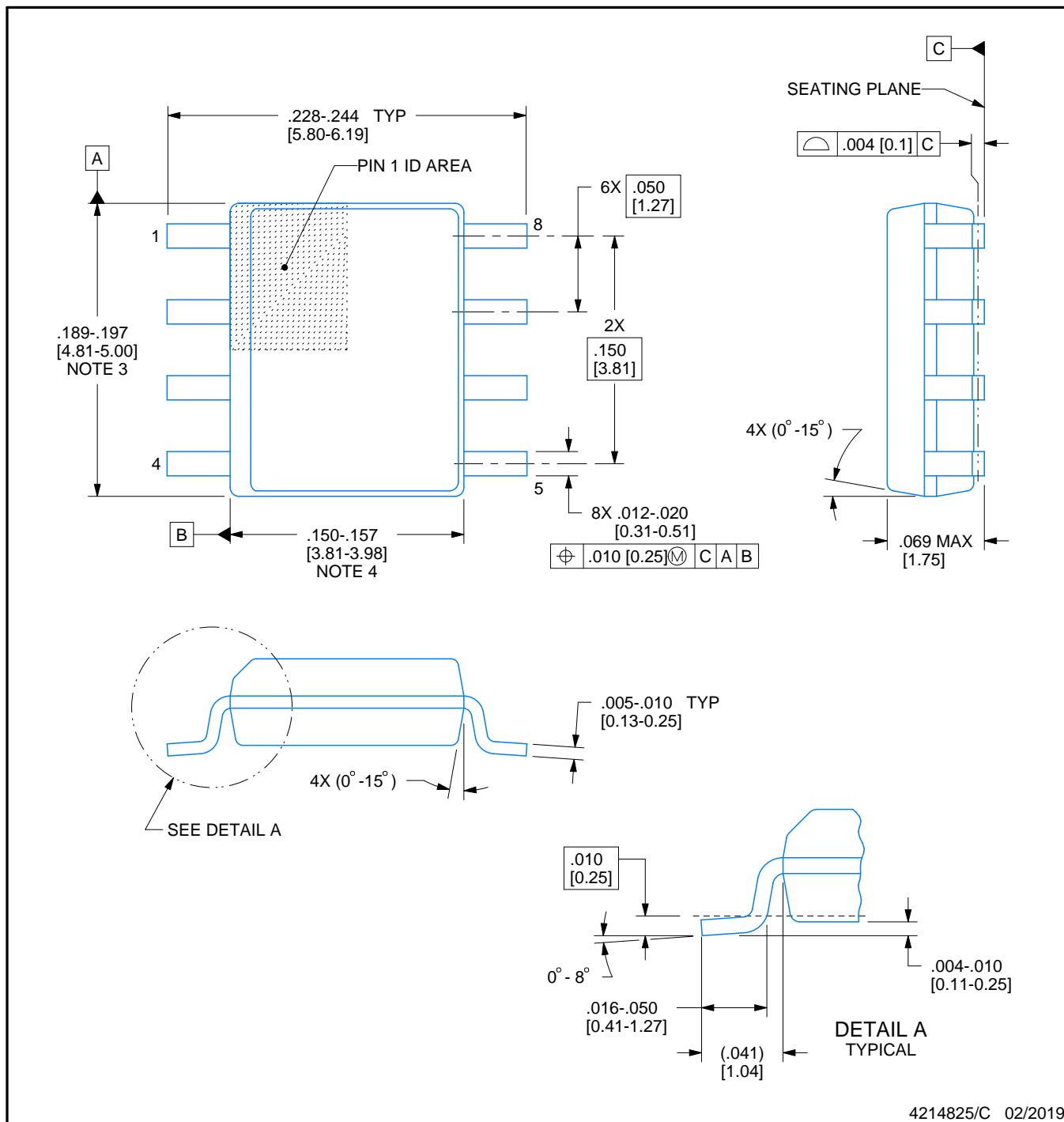


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

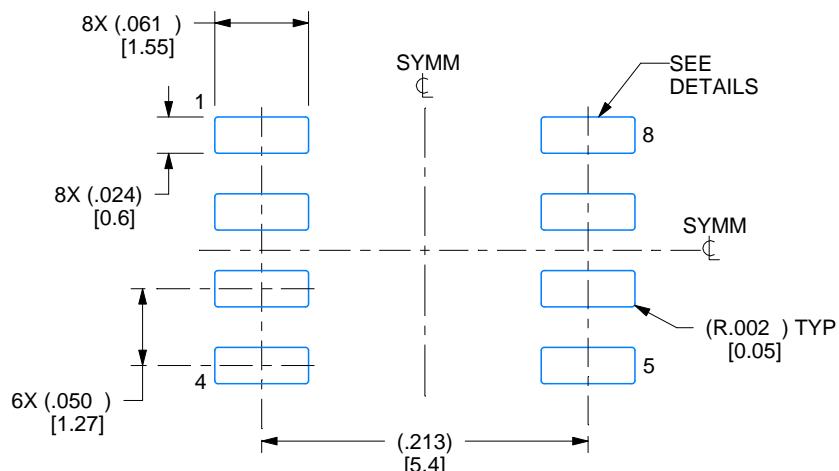
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

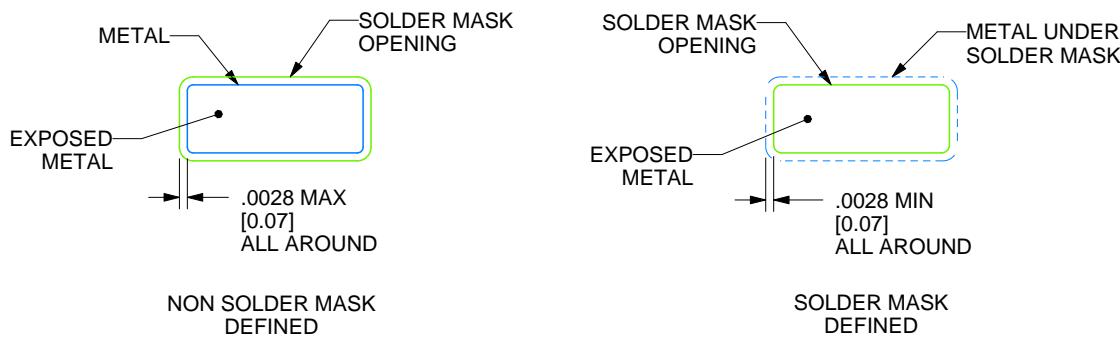
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

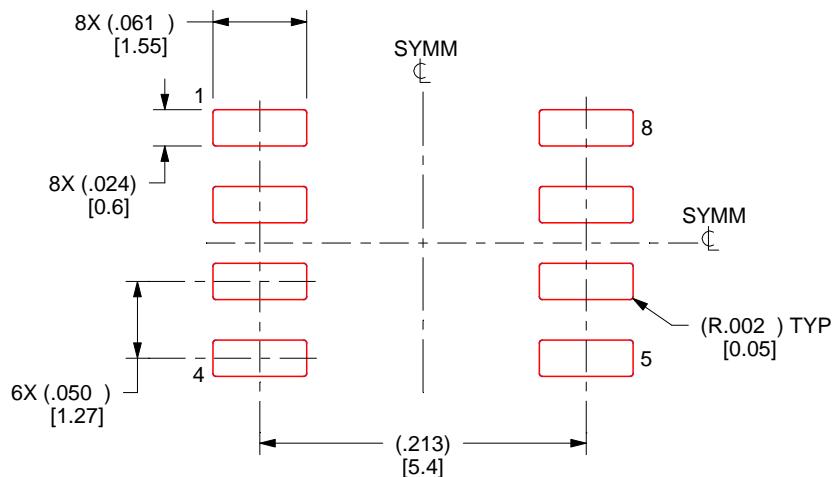
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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