OPAx365-Q1 50MHz 低失真、高 CMRR、轨到轨 I/O 单电源运算放大器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C3B
- OPA2365-Q1 提供功能安全：
  - 可帮助进行功能安全系统设计的文档
- 增益带宽：50MHz
- 零交叉失真拓扑
  - 出色的 THD+N：0.0004%
  - CMRR：100 dB（最小值）
  - 轨到轨输入和输出
  - 输入超出电源轨 100mV
- 低噪声：4.5nV/√Hz（100kHz 时）
- 压摆率：25V/μs
- 快速趋稳：0.3μs 至 0.01%
- 精密
  - 低偏移：100μV
  - 低输入偏置电流：0.2pA
- 2.2V 至 5.5V 工作电压

2 应用

- 汽车
- ADAS
- 混合动力汽车/电动汽车和动力总成
- 车身与照明
- 盲点检测
- 引擎控制单元
- 直流/直流转换器
- 短程到中程雷达
- 碰撞预警
- 工业类
- 抬头显示

3 说明

OPAx365-Q1 零交叉系列轨到轨高性能 CMOS 运算放大器针对超低电压单电源应用进行了优化。轨到轨输入/输出、低噪声 (4.5nV/√Hz) 和高速运行（50MHz 增益带宽）使得这些器件非常适合于驱动采样数据转换器（例如，ADS7822-Q1 或 ADS1115-Q1），尤其是在短程到中程雷达应用中。OPAx356-Q1 系列运算放大器也非常适合混合动力汽车/电动汽车和动力总成应用中的直流/直流转换器，以及作为发动机控制单元中的变速器控制。

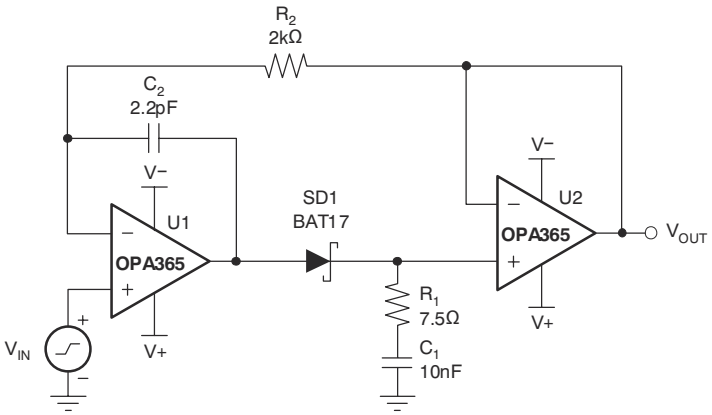
特殊功能包括出色的共模抑制比 (CMRR)、无输入级交叉失真、高输入阻抗和轨到轨输入和输出摆幅。输入共模范围同时包括正负电源。电源轨的输出电压摆幅在 10mV 以内。

OPA365-Q1（单通道版本）采用 5 引脚 SOT-23 封装。OPA2365-Q1（双通道版本）采用 8 引脚 SOIC 封装。所有版本的额定工作温度范围均为 –40°C 至 125°C。单通道和双通道版本具有完全相同的规范，可尽可能提高设计灵活性。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
OPA2365-Q1	SOIC (8)	4.90mm × 3.91mm
OPA365-Q1	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



快速趋稳峰值检测器

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (December 2015) to Revision E (November 2020)	Page
• 更新了整个文档的表、图和交叉参考的编号格式	1
• 向*特性* 部分添加了提供功能安全的文档信息	1
• Updated *Related Documentation* section	22

Changes from Revision C (April 2012) to Revision D (December 2015)	Page
• 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1

Changes from Revision B (January 2012) to Revision C (April 2012)	Page
• Added another row with V_{OS} for OPA2365-Q1 only	5
• Changed I_Q upper limit to 5.3 from 5.5	5

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5 Pin Configuration and Functions

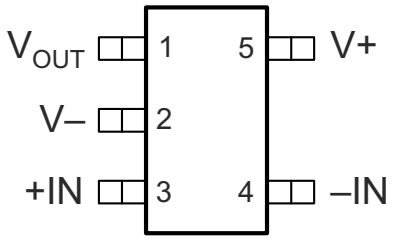


图 5-1. DBV Package 5-Pin SOT-23 Top View

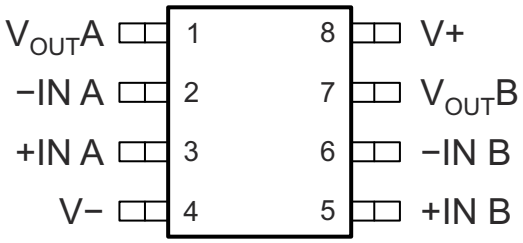


图 5-2. D Package 8-Pin SOIC Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC		
+IN	3	—	I	Noninverting input
– IN	4	—	I	Inverting input
+IN A	—	3	I	Noninverting input
– IN A	—	2	I	Inverting input
+IN B	—	5	I	Noninverting input
– IN B	—	6	I	Inverting input
V+	5	8	I	Positive (highest) supply
V –	4	4	I	Negative (lowest) supply
V_{OUT}	I	—	O	Output
V_{OUT}A	—	1	O	Output
V_{OUT}B	—	7	O	Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		5.5	V
V_I	Signal input terminals, voltage(2)	(V−) − 0.5	(V+) + 0.5	V
I_I	Signal input terminals, current(2)	−10	10	mA
t_{OSC}	Output short-circuit duration(3)	Continuous		
T_{OP}	Operating temperature	−40	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10 mA or less.

(3) Short-circuit to ground, one amplifier per package

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage V – to V+	2.2	3.3	5.5	V
T_A	Operating free-air temperature	−40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2365-Q1 D (SOIC) 8 PINS	OPA365-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.5	208.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	123.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	54.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.5	37.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.3	36.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

V_S = 2.2 V to 5.5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		25°C		100	200	µV
V_{OS} (3)	Input offset voltage		25°C		100	230	µV
dV_{OS}/ dT	Input offset voltage drift		Full range		1		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.2 V to 5.5 V	Full range		10	100	µV/V
	Channel separation, DC		25°C		0.2		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current		25°C		±0.2	±10	pA
			Full range		See 节 6.6		
I_{OS}	Input offset current		25°C		±0.2	±10	pA
NOISE							
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz	25°C		5		μV_{PP}
e_n	Input voltage noise density	f = 100 kHz	25°C		4.5		nV/√Hz
i_n	Input current noise density	f = 10 kHz	25°C		4		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage		25°C	(V-) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V-) – 0.1 V ≤ V_{CM} ≤ (V+) + 0.1 V	Full range	100	120		dB
INPUT CAPACITANCE							
	Differential		25°C		6		pF
	Common-mode		25°C		2		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ, 100 mV < V_O < (V+) – 100 mV	Full range	100	120		dB
		R_L = 600 Ω, 200 mV < V_O < (V+) – 200 mV	25°C	100	120		
		R_L = 600 Ω, 200 mV < V_O < (V+) – 200 mV	Full range	94			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		25°C		50		MHz
SR	Slew rate	V_S = 5 V, G = 1	25°C		25		V/µs
t_S	Settling time	0.1%, V_S = 5 V, 4-V Step, G = 1	25°C		200		ns
		0.01%, V_S = 5 V, 4-V Step, G = 1	25°C		300		
	Overload recovery time	V_S = 5 V, V_{IN} × Gain > V_S	25°C		< 0.1		µs
THD+N	Total harmonic distortion + noise(2)	V_S = 5 V, R_L = 600 Ω, V_O = 4 VPP, G = 1, f = 1 kHz	25°C		0.0004%		
OUTPUT							
	Voltage output swing from rail	R_L = 10 kΩ, V_S = 5.5 V	Full range		10	20	mV
I_{SC}	Short-circuit current		25°C		±65		mA
C_L	Capacitive load drive		25°C		See 节 6.6		
	Open-loop output impedance	f = 1 MHz, I_O = 0	25°C		30		Ω
POWER SUPPLY							

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V_S = 2.2 V to 5.5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_S	Specified voltage		25°C	2.2		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0	25°C		4.6	5	mA
			Full range			5.3	
TEMPERATURE RANGE							
	Specified		25°C	–40		125	°C
θ_{JA}	Thermal resistance	SOT23-5	25°C				°C/W
		SO-8	25°C		200		

(1) Full range T_A = −40°C to 125°C

(2) Third-order filter, bandwidth 80 kHz at −3 dB.

(3) For OPA2365-Q1 only

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6.6 Typical Characteristics

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

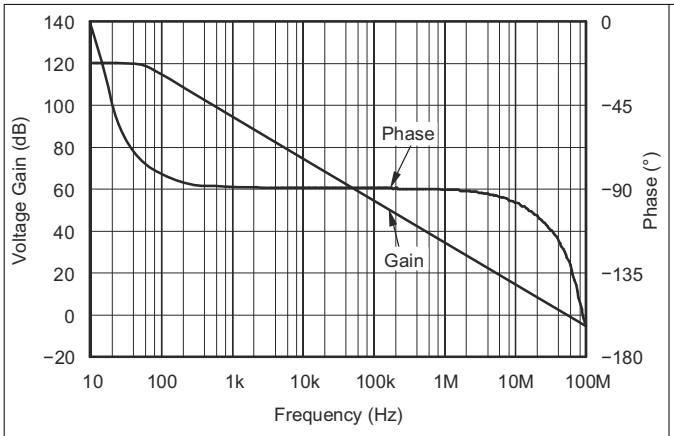


图 6-1. Open-Loop Gain and Phase vs Frequency

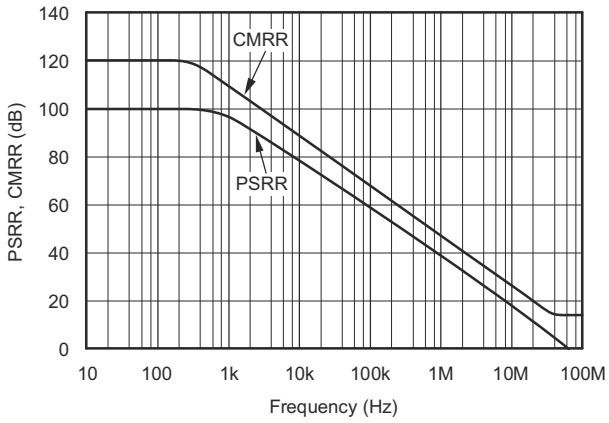


图 6-2. Power Supply and Common Mode Rejection Ratio vs Frequency

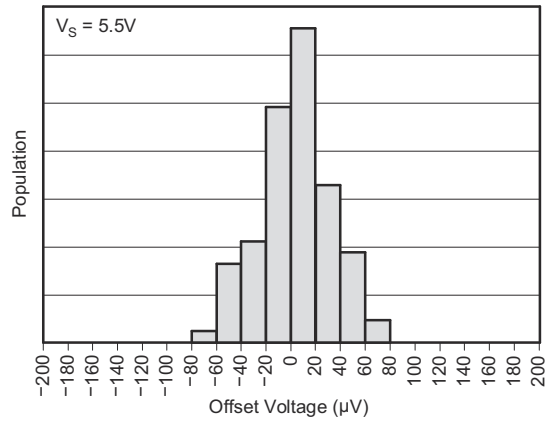


图 6-3. Offset Voltage Production Distribution

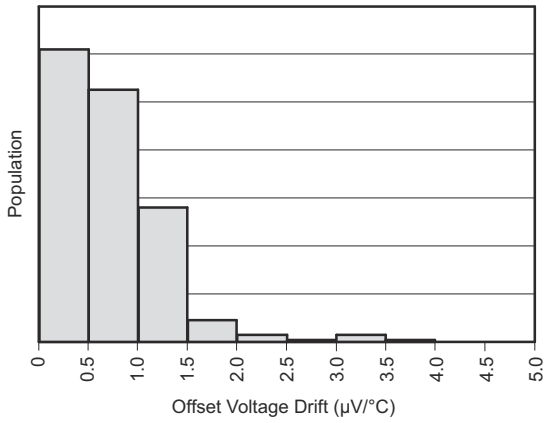


图 6-4. Offset Voltage Drift Production Distribution

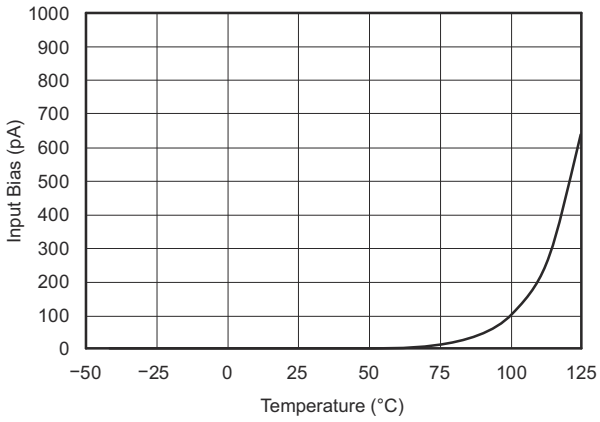


图 6-5. Input Bias Current vs Temperature

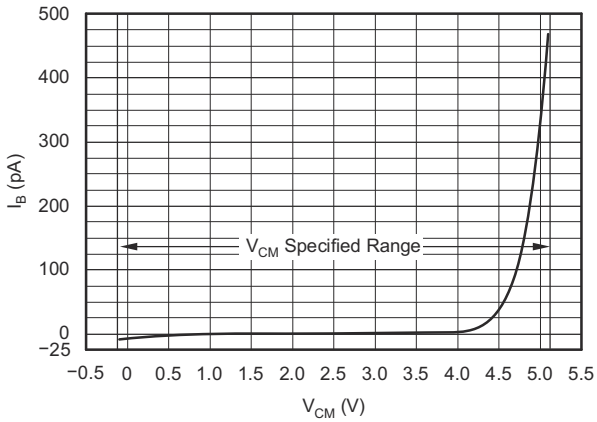


图 6-6. Input Bias Current vs Common Mode Voltage

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6.6 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

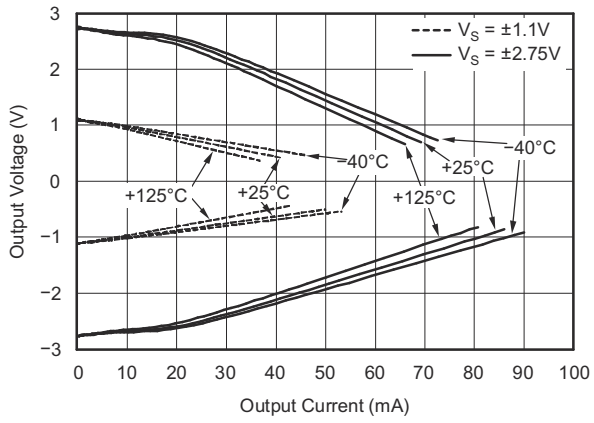


图 6-7. OPA365-Q1 Output Voltage vs Output Current

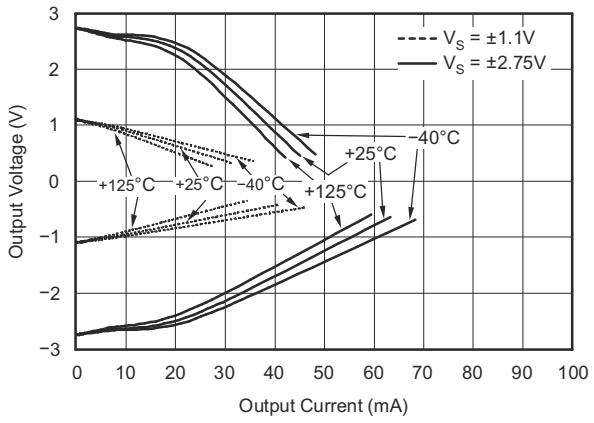


图 6-8. OPA2365-Q1 Output Voltage Swing vs Output Current

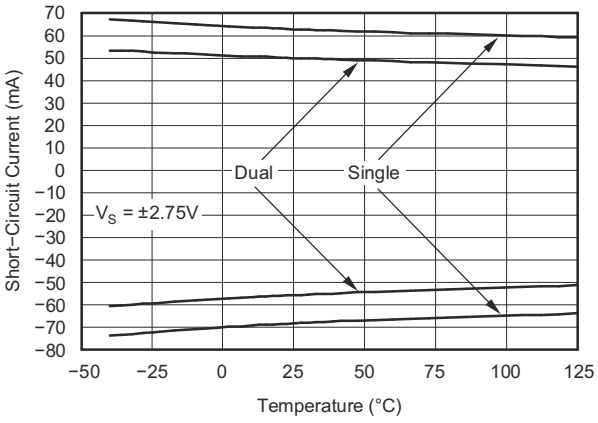


图 6-9. Short-Circuit Current vs Temperature

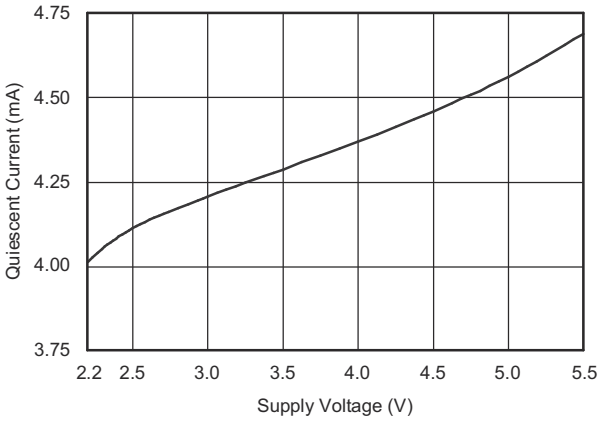


图 6-10. Quiescent Current vs Supply Voltage

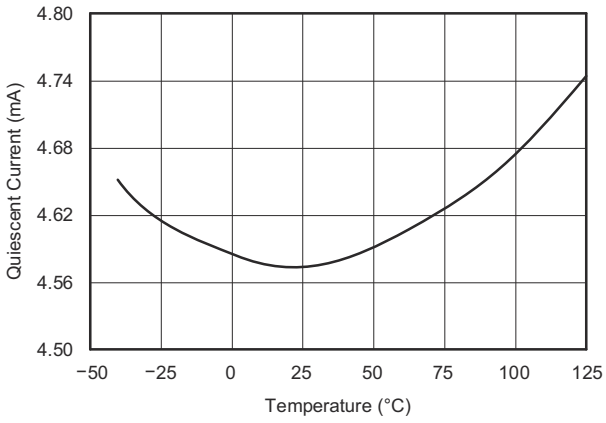


图 6-11. Quiescent Current vs Temperature

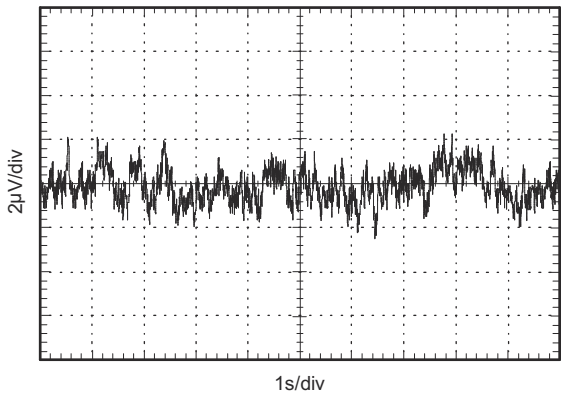


图 6-12. 0.1-Hz to 10-Hz Input Voltage Noise

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6.6 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

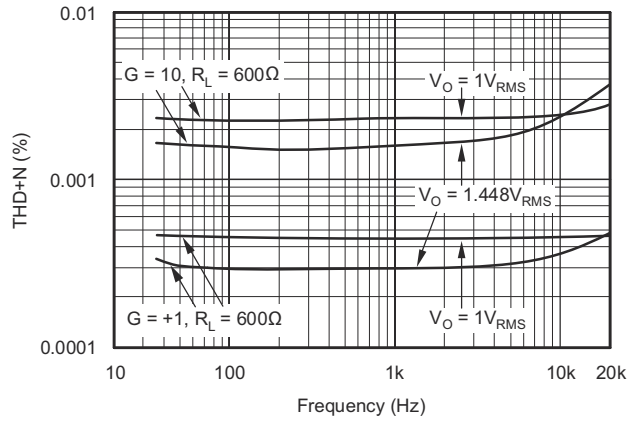


图 6-13. Total Harmonic Distortion + Noise vs Frequency

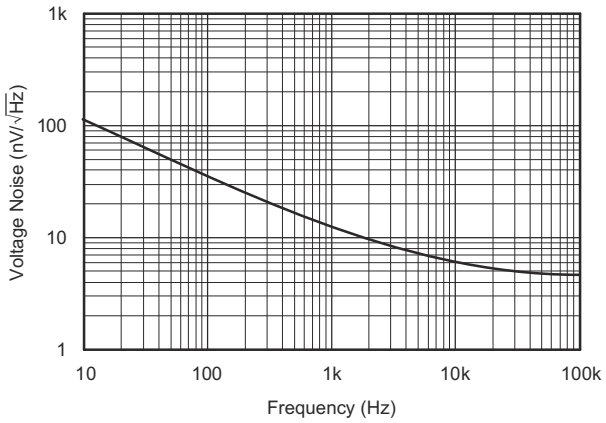


图 6-14. Input Voltage Noise Spectral Density

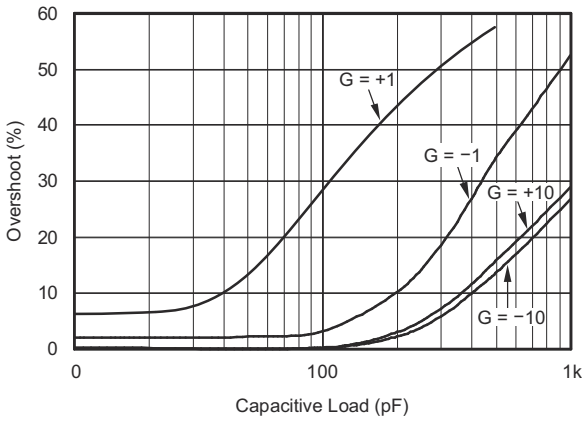


图 6-15. Overshoot vs Capacitive Load

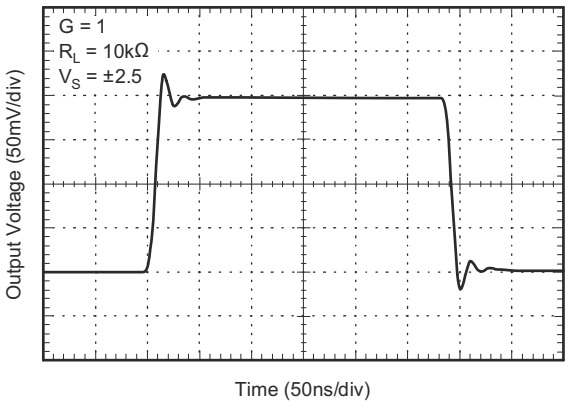


图 6-16. Small-Signal Step Response

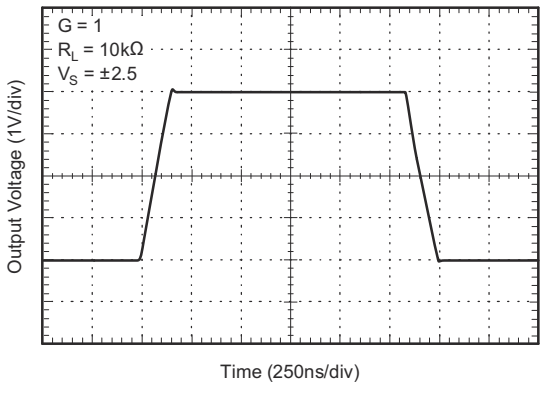


图 6-17. Large-Signal Step Response

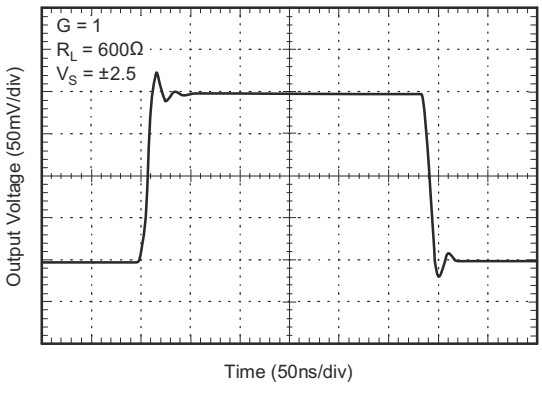


图 6-18. Small-Signal Step Response

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6.6 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, C_L = 0 pF (unless otherwise noted)

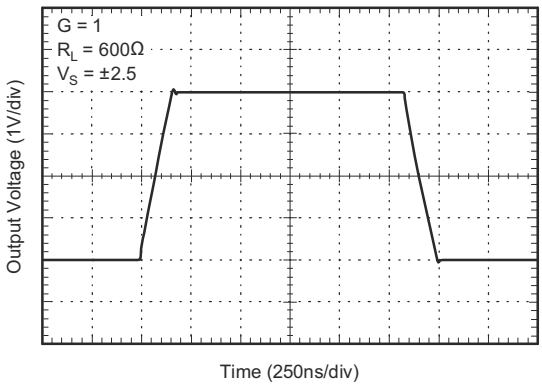


图 6-19. Large-Signal Step Response

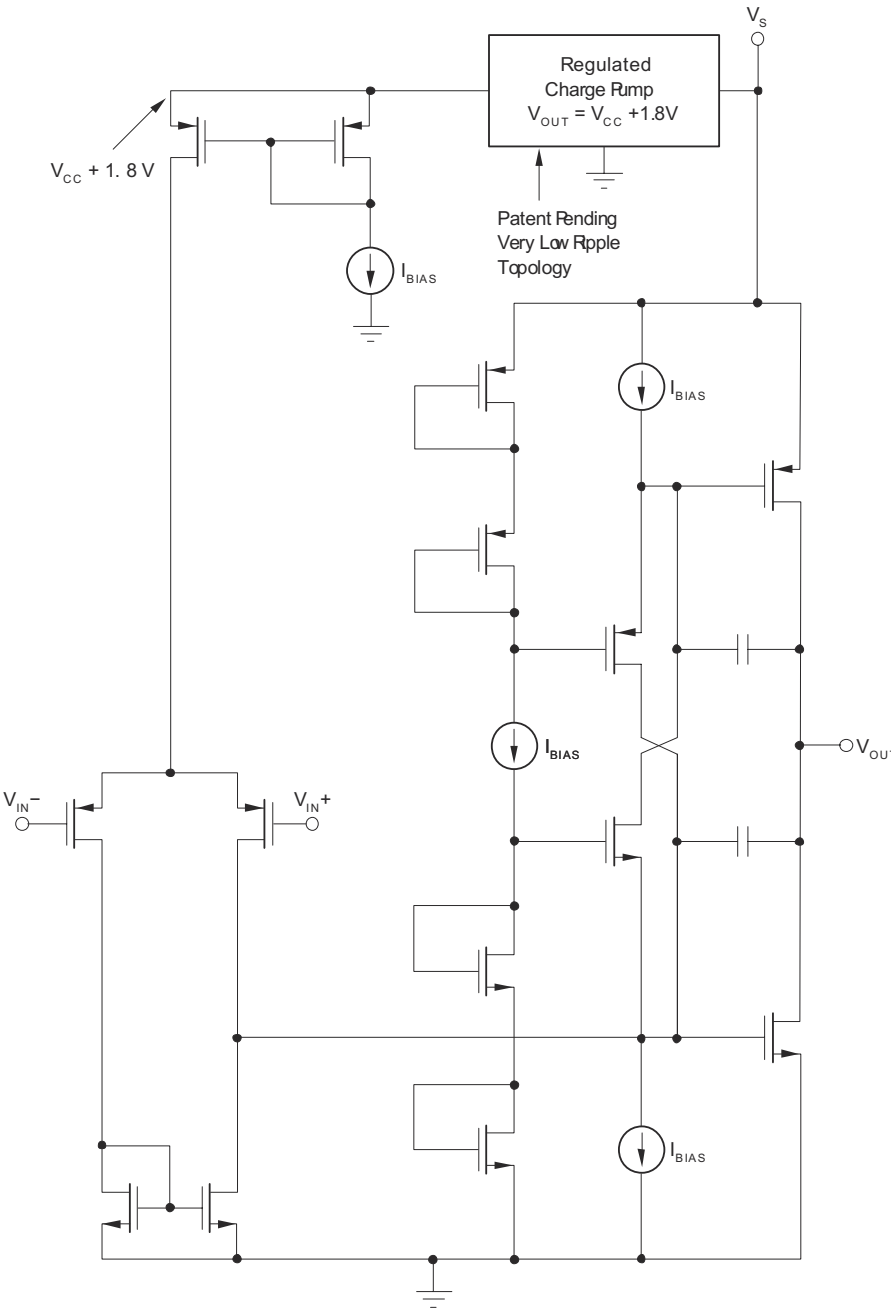
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7 Detailed Description

7.1 Overview

The OPAx365-Q1 zero-crossover family of rail-to-rail, high-performance, CMOS operational amplifiers are optimized for very low voltage, single-supply applications. Their rail-to-rail input and output, low-noise (4.5 nV/ √Hz), and high-speed operation (50-MHz gain bandwidth) make these devices ideal for driving sampling analog-to-digital converters (ADCs). Applications include audio, signal conditioning, and sensor amplification. The high-gain bandwidth of 50 MHz makes this family suited for amplifying low signal levels and high frequency such as radar signal processing .

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPA365-Q1 amplifier parameters are fully specified from 2.2 V to 5.5 V. Many of the specifications apply from −40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in 节 6.6.

7.3.2 Basic Amplifier Configurations

As with other single-supply operational amplifiers, the OPA365-Q1 may be operated with either a single supply or dual supplies (see 图 7-1). A typical dual-supply connection is shown in 图 7-1, which is accompanied by a single-supply connection. The OPA365-Q1 device is configured as a basic inverting amplifier with a gain of −10 V/V. The dual-supply connection has an output voltage centered on zero, while the single− supply connection has an output centered on the common-mode voltage V_{CM}. For the circuit shown, this voltage is 1.5 V, but may be any value within the common-mode input voltage range. The OPA365-Q1 V_{CM} range extends 100 mV beyond the power-supply rails.

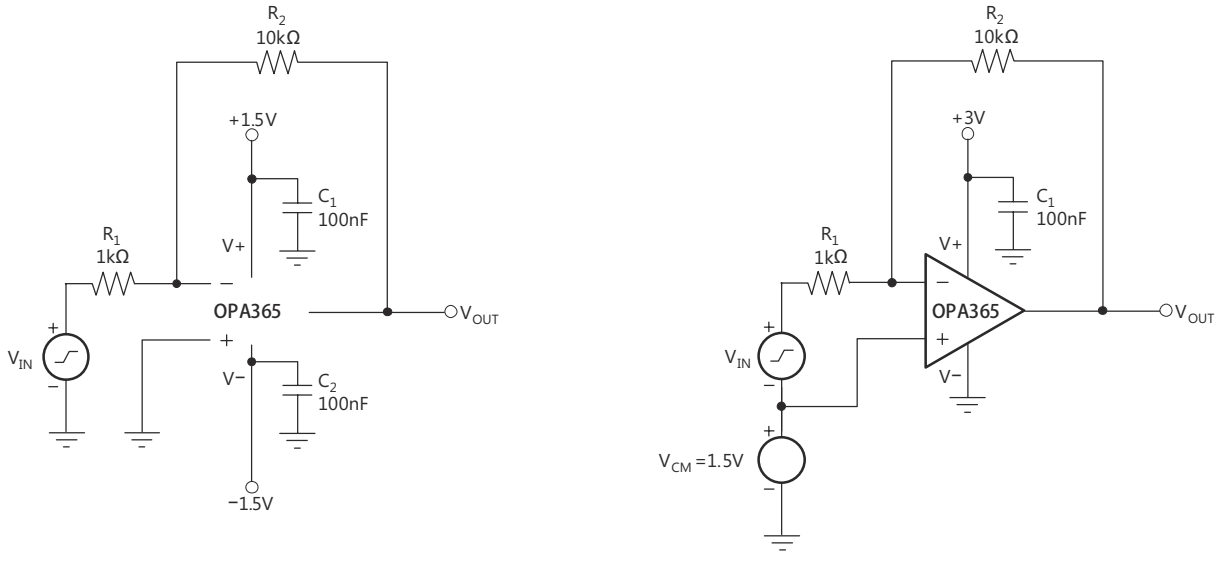


图 7-1. Basic Circuit Connections

图 7-2 shows a single-supply, electret microphone application where V_{CM} is provided by a resistive divider. The divider also provides the bias voltage for the electret element.

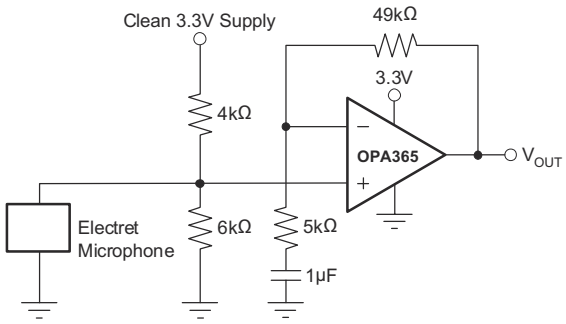


图 7-2. Microphone Preamplifier

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7.3.3 Input and ESD Protection

The OPA365-Q1 device incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, provided that the current is limited to 10 mA as stated in the *节 6.1*. 图 7-3 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to the minimum in noise-sensitive applications.

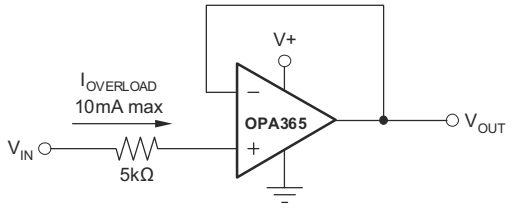


图 7-3. Input Current Protection

7.3.4 Rail-to-Rail Input

The OPA365-Q1 product family features true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary stage operational amplifiers. This topology also allows the OPA365-Q1 device to provide superior common-mode performance over the entire input range, which extends 100 mV beyond both power-supply rails, as shown in 图 7-4. When driving ADCs, the highly linear VCM range of the OPA365-Q1 device assures that the operational amplifier/ADC system linearity performance is not compromised.

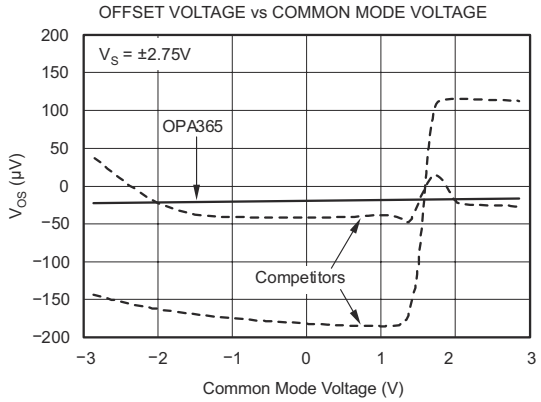


图 7-4. OPA365-Q1 Has Linear Offset Over the Entire Common-Mode Range

7.4 Device Functional Modes

The OPAx365-Q1 family of devices is powered on when the supply is connected. The device can be operated as a single-supply operational amplifier or a dual-supply amplifier depending on the application.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Capacitive Loads

The OPA365-Q1 device may be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the OPA365-Q1 device can become unstable, leading to oscillation. The particular operational amplifier circuit configuration, layout, gain and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

When operating in the unity-gain configuration, the OPA365-Q1 device remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See 图 6-15.

One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output; see 图 8-1. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, R_L = 10 kΩ, and R_S = 20 Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600 Ω, which the OPA365-Q1 device is able to drive, the error increases to 7.5%.

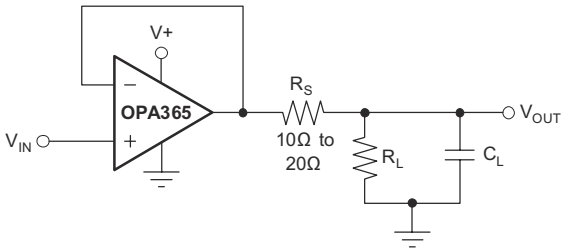


图 8-1. Improving Capacitive Load Drive

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8.1.2 Achieving an Output Level of Zero Volts (0 V)

Certain single-supply applications require the operational amplifier output to swing from 0 V to a positive full-scale voltage and have high accuracy. An example is an operational amplifier employed to drive a single-supply ADC having an input range from 0 V to 5 V. Rail-to-rail output amplifiers with very light output loading may achieve an output level within millivolts of 0 V (or $+V_S$ at the high end), but not 0 V. Furthermore, the deviation from 0 V only becomes greater as the load current required increases. This increased deviation is a result of limitations of the CMOS output stage.

When a pulldown resistor is connected from the amplifier output to a negative voltage source, the OPA365-Q1 can achieve an output level of 0 V, and even a few millivolts below 0 V. Below this limit, nonlinearity and limiting conditions become evident. 图 8-2 illustrates a circuit using this technique.

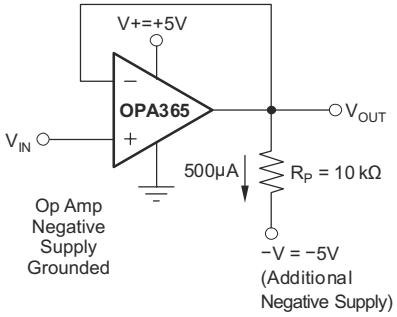


图 8-2. Swing-to-Ground

A pulldown current of approximately 500 μA is required when OPA365-Q1 is connected as a unity-gain buffer. A practical termination voltage (V_{NEG}) is −5 V, but other convenient negative voltages also may be used. The pulldown resistor R_L is calculated from $R_L = [(V_O - V_{NEG})/(500\ \mu A)]$. Using a minimum output voltage (V_O) of 0 V, $R_L = [0\ V-(-5V)]/(500\ \mu A)] = 10\ k\Omega$. Keep in mind that lower termination voltages result in smaller pulldown resistors that load the output during positive output voltage excursions.

This technique does not work with all operational amplifier, and should only be applied to operational amplifiers, such as the OPA365-Q1, that have been specifically designed to operate in this manner. Also, operating the OPA365-Q1 output at 0 V changes the output stage operating conditions, resulting in somewhat lower open-loop gain and bandwidth. Keep these precautions in mind when driving a capacitive load because these conditions can affect circuit transient response and stability.

8.1.3 Active Filtering

The OPA365-Q1 device is well-suited for active filter applications requiring a wide bandwidth, fast slew rate, low-noise, and single-supply operational amplifier. 图 8-3 shows a 500 kHz, 2nd-order, low-pass filter utilizing the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is −40 dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an ADC.

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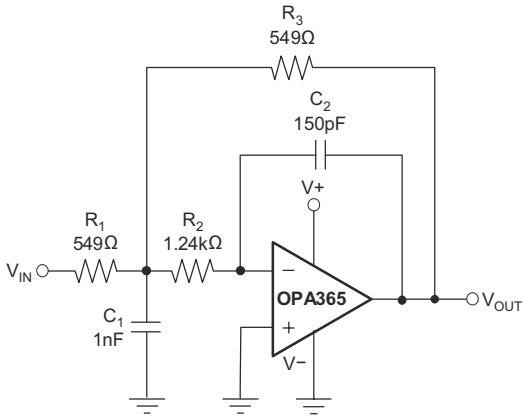


图 8-3. Second-Order Butterworth 500-kHz Low-Pass Filter

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional 2nd-order MFB stage;
3. using a noninverting filter topology such as the Sallen-Key (shown in 图 8-4).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro program. This software is available as a free download at www.ti.com.

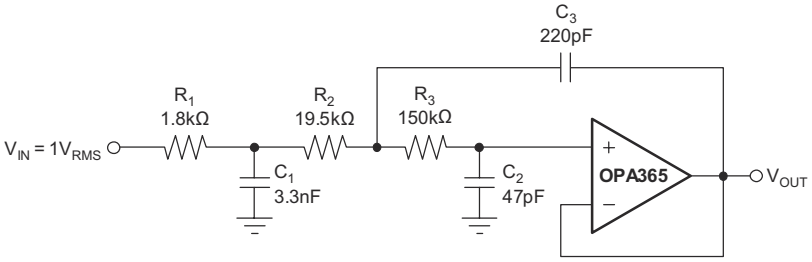


图 8-4. Configured as a 3-Pole, 20 kHz, Sallen-Key Filter

8.1.4 Driving an ADS7822-Q1 Analog-to-Digital Converter

The OPAx365-Q1 operational amplifiers are optimized for driving medium to high speed sampling A/D converters. The OPAx365-Q1 op amps buffer the A/D’s input capacitance and resulting charge injection while providing signal gain. 图 8-5 shows the OPAx365-Q1 in a basic noninverting configuration driving the ADS7822-Q1. The ADS7822-Q1 is a 12-bit, micro-power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPAx365-Q1, the combination is ideal for space-limited, low power applications. In this configuration, an RC network at the A/D’s input can be used to filter charge injection.

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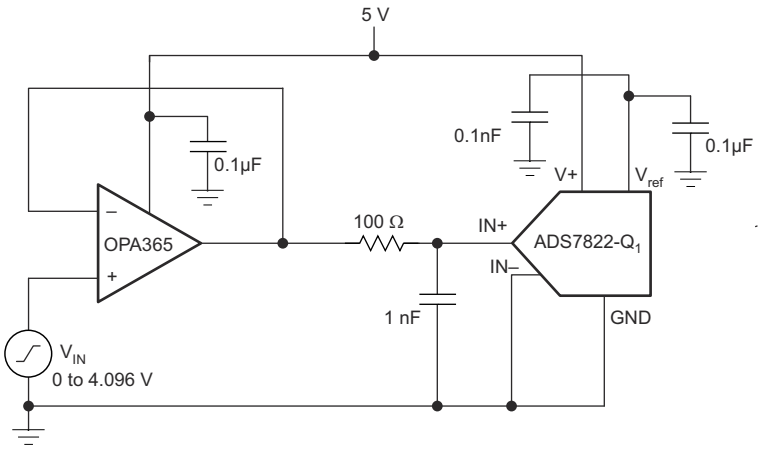


图 8-5. Driving the ADS7822-Q1

8.1.5 Driving ADS1115-Q1 Analog-to-Digital Converter

Some applications such as mutli-channels mid range radar need selection between channels. OPA2365-Q1 combined with ADS1115-Q1 fit very well for 2 channels radar selection. The circuit in 图 8-6 shows the same band pass filter but the components can be modified for different desired band pass.

The DAS1115-Q1 inputs are set as differential. the inputs accept up the ±2 V. The OPA2365-Q1 flat gain is 100 so the input signal peak is 20 mV.

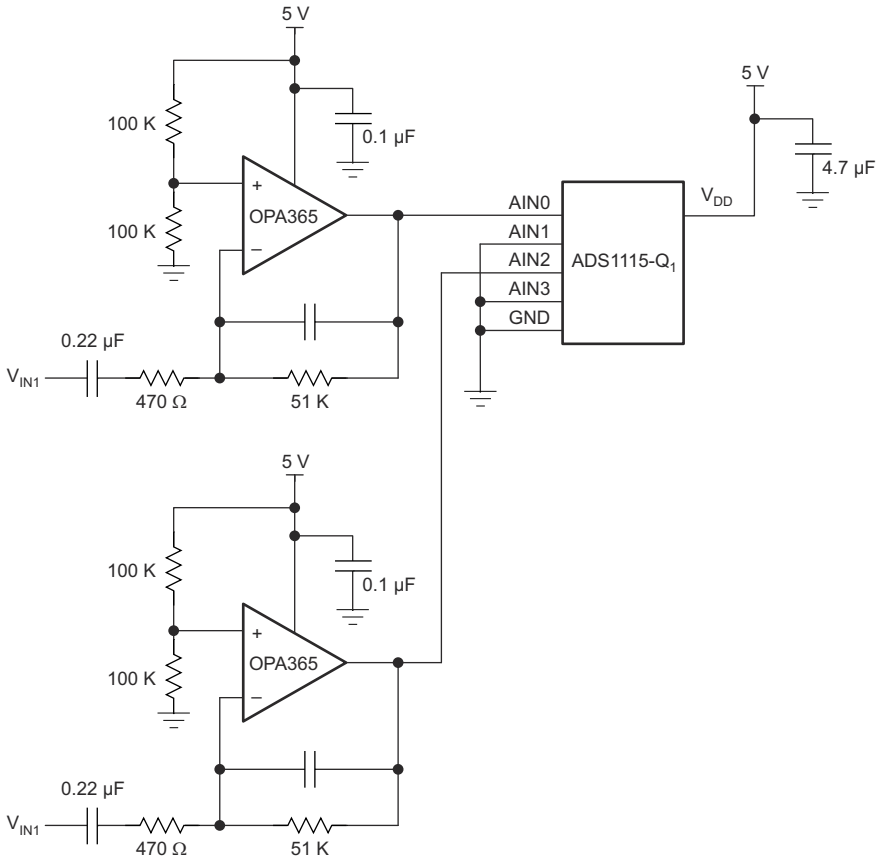


图 8-6. Driving the ADS1115-Q1

8.2 Typical Application

8.2.1 Fast Settling Peak Detector

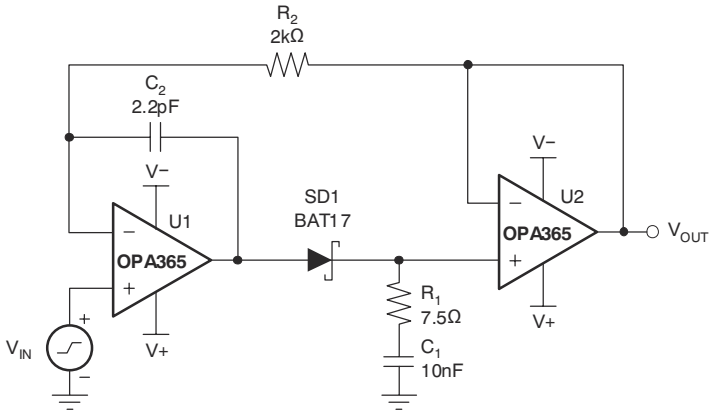


图 8-7. Fast Settling Peak Detector Schematic

Some applications require peak signal measurement. High unity gain bandwidth, wide supply voltage range, rail-to-rail input and output, and very low input bias current make the OPA2365-Q1 device very suitable for a peak detector circuit.

8.2.1.1 Design Requirements

Use the following design parameters for this application:

- Supply voltage: 2.2 V to 5 V
- Input signal: 0 V to 4.5 V
- Input signal frequency: 0 MHz to 1 MHz

8.2.1.2 Detailed Design Procedure

The circuit in 图 8-7 detects the peak of an input signal and generates a DC output equal to the peak level VOUT = VINpeak. The capacitor C1 is charged through the SD1 diode and limiting resistor R1. The only discharging path for C1 is the OPA2365-Q1 very high input impedance. This allows the peak detection of low frequency and low-duty cycle signal.

8.2.1.3 Application Curves



图 8-8. Supply Voltage 2.2 V, Peak Signal 1 V

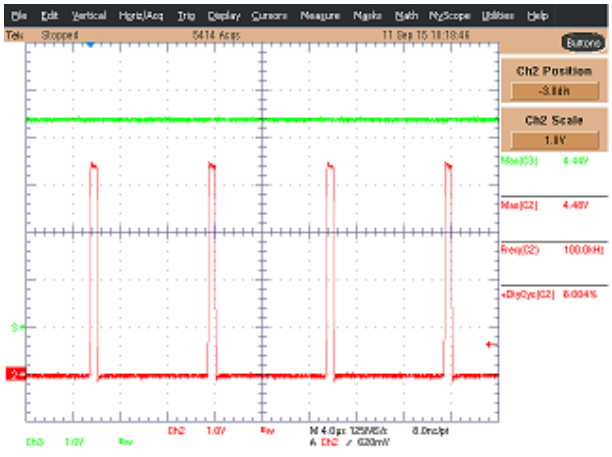


图 8-9. Supply Voltage 5 V Peak Signal 4.5 V

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8.2.2 Bandpass Filter 1.5 kHz to 160 kHz and 40-db Flat Gain

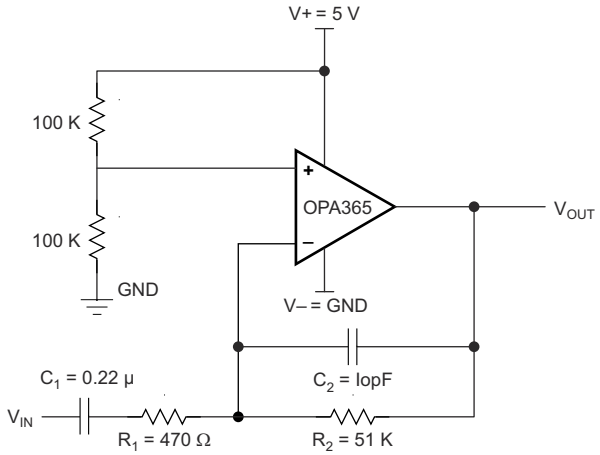


图 8-10. Bandpass Filter 1.5 kHz to 160 kHz and 40-db Flat Gain Schematic

8.2.2.1 Design Requirements

Use the following design parameters for this application:

- Supply voltage: 2.2 V to 5 V
- Input signal: 0 V to 25 mV
- Input signal frequency: 0 MHz to 1 MHz

8.2.2.2 Detailed Design Procedure

Some applications need bandpass filter – that is, radar or audio signal precessing. The cross over frequencies and flat gain can be adjusted by changing the resistors and capacitors value according to applications.

The circuit is designed for 5-V supply and 20-mV input signal. With a flat gain of 100 dB or 40 dB, the peak output signal is 2 V. The reference signal is at half way of 5 V, which is 2.5 V.

$$\text{The transfer function or gain} = \frac{V_{out}}{V_{in}} = -\frac{R_2C_1S}{(1+R_1C_1S)(1+R_2C_2S)} \quad (1)$$

$$\text{A zero at} = \frac{1}{2\pi R_2C_1} = 14.2\ \text{Hz} \quad (2)$$

$$\text{A pole at} = \frac{1}{2\pi R_1C_1} = 1.54\ \text{KHz} \quad (3)$$

$$\text{A pole at} = \frac{1}{2\pi R_2C_2} = 156\ \text{KHz} \quad (4)$$

Flat Gain of 100 or 40 dB between 1.54 kHz and 156 kHz (5)

20 db/decade below 1.54 KHz (6)

– 20 dB/decade above 156 kHz (7)

Bandpass between 1.54 kHz and 156 kHz (8)

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8.2.2.3 Application Curves

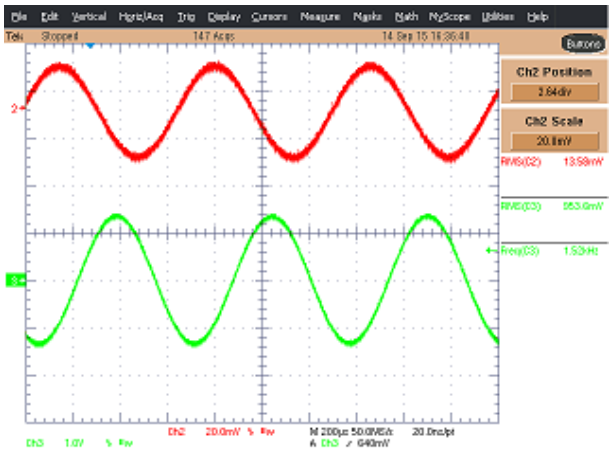


图 8-11. Gain Is –3 dB Below the Flat Gain at 1.5 kHz

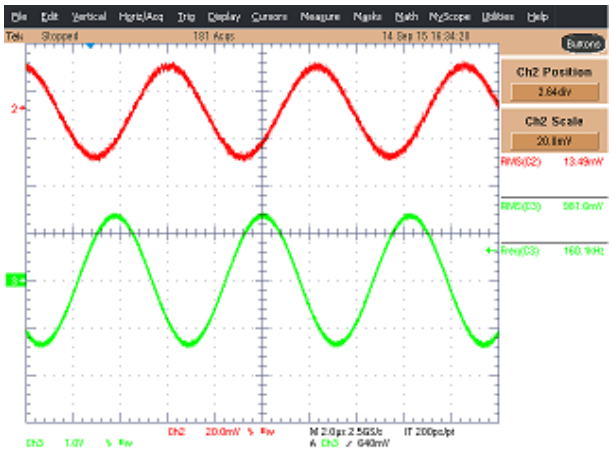


图 8-12. Gain Is –3 dB Above the Flat Gain at 160 kHz

9 Power Supply Recommendations

The OPAx365-Q1 family of devices is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to 125°C. The 节 6.6 presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see 节 6.1).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see 节 10.1.

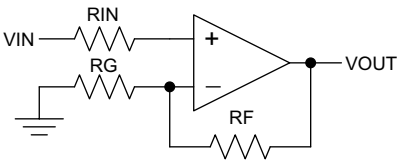
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10 Layout

10.1 Layout Guidelines

The OPA365-Q1 is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1-µF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

10.2 Layout Example



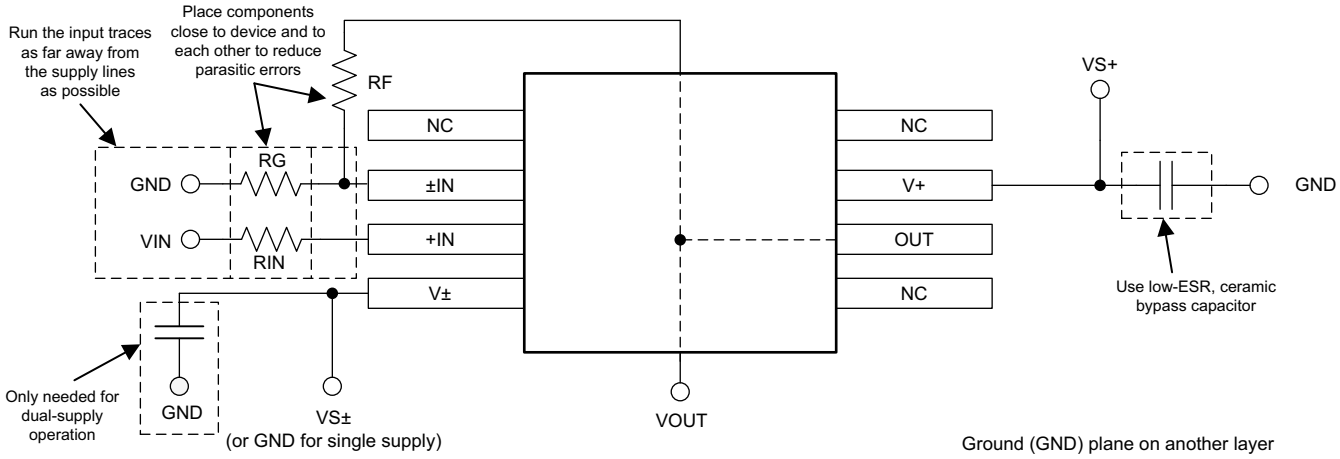


图 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Texas Instruments, ADS1258 16-Channel, 24-Bit Analog-to-Digital Converter data sheet

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2365AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	O2365Q	Samples
OPA365AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OTNQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

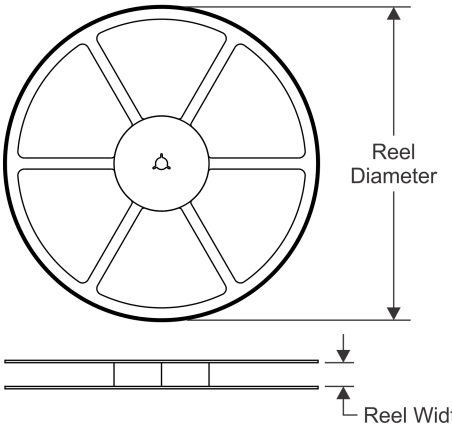
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

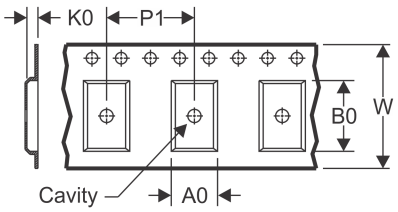
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

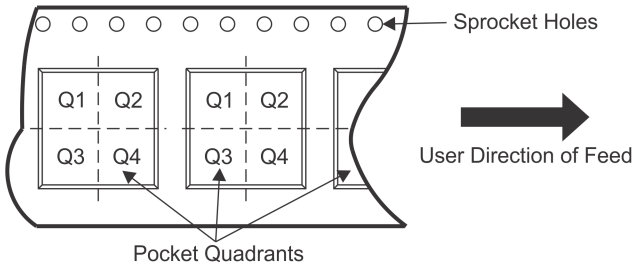


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

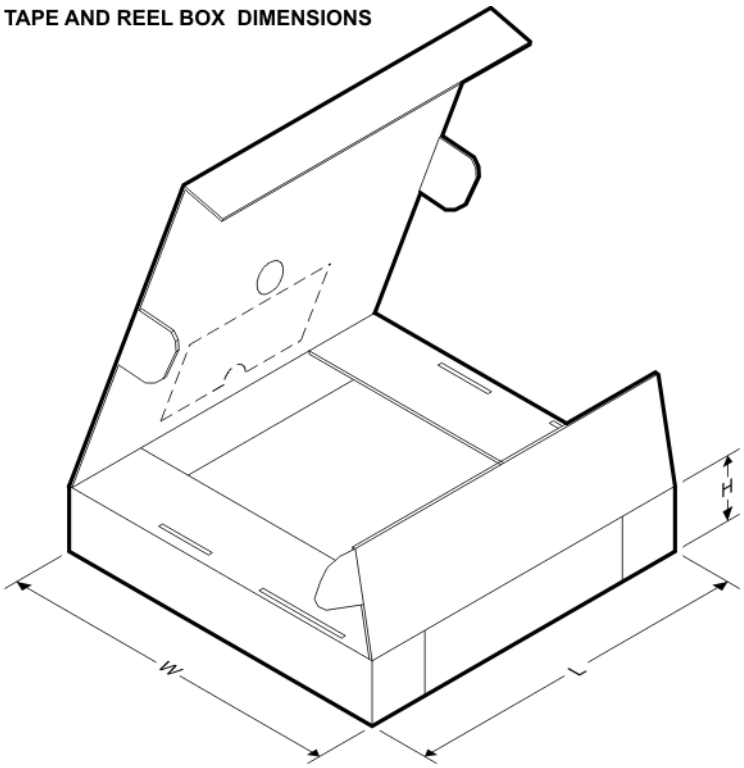
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2365AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA365AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

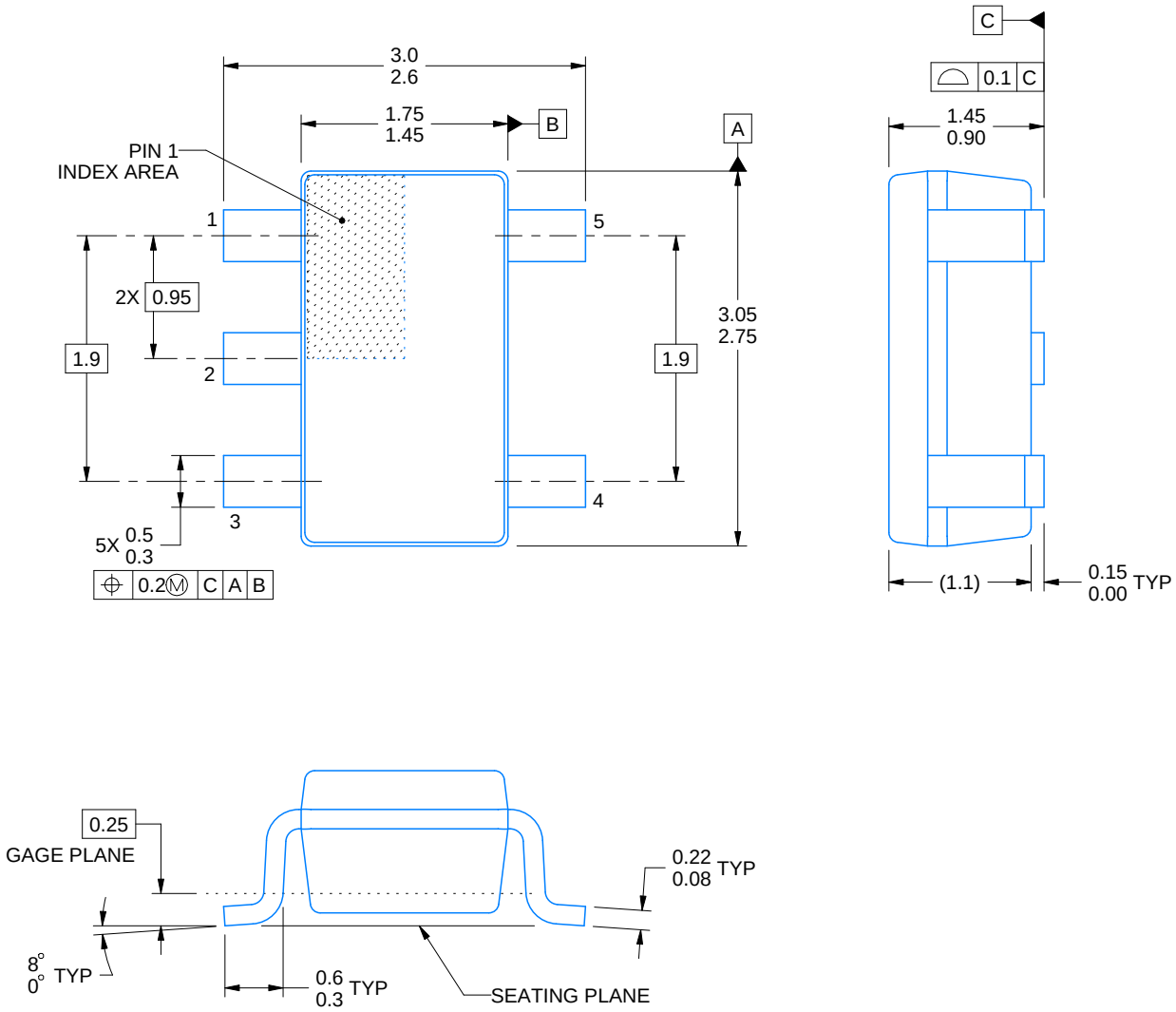
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2365AQDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
OPA365AQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

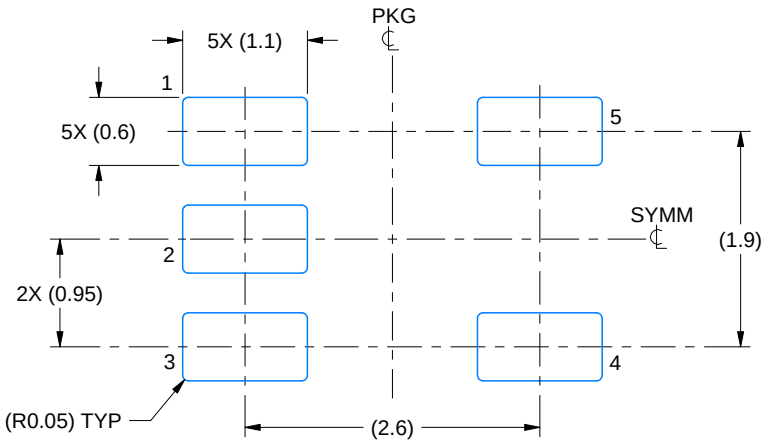
SMALL OUTLINE TRANSISTOR



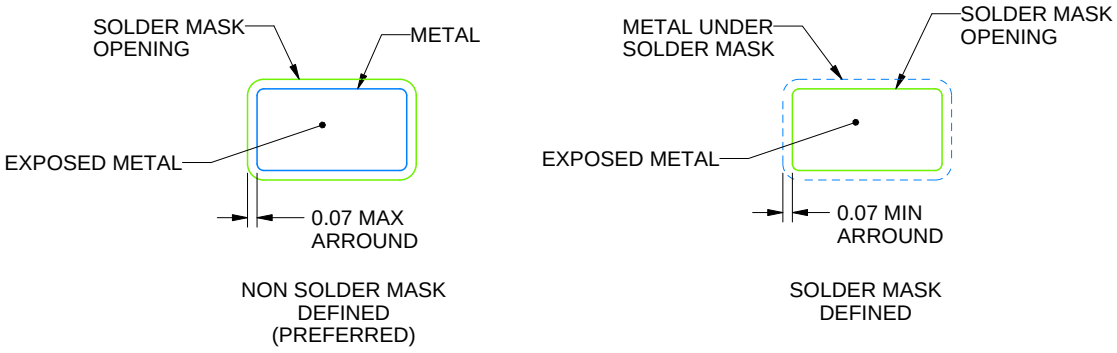
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

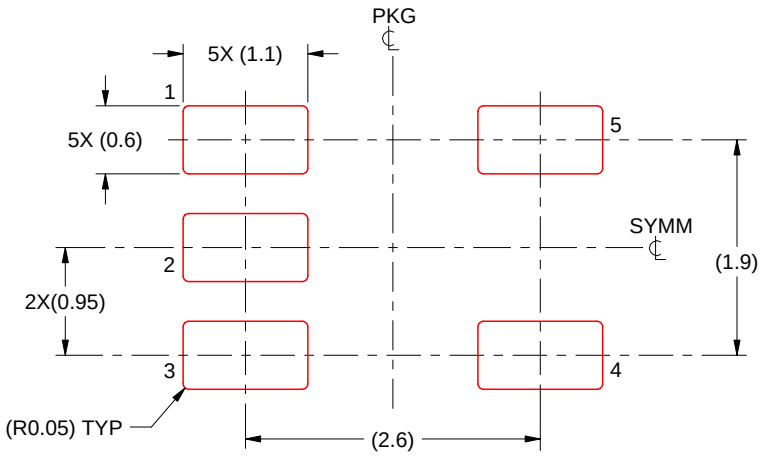


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

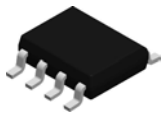


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

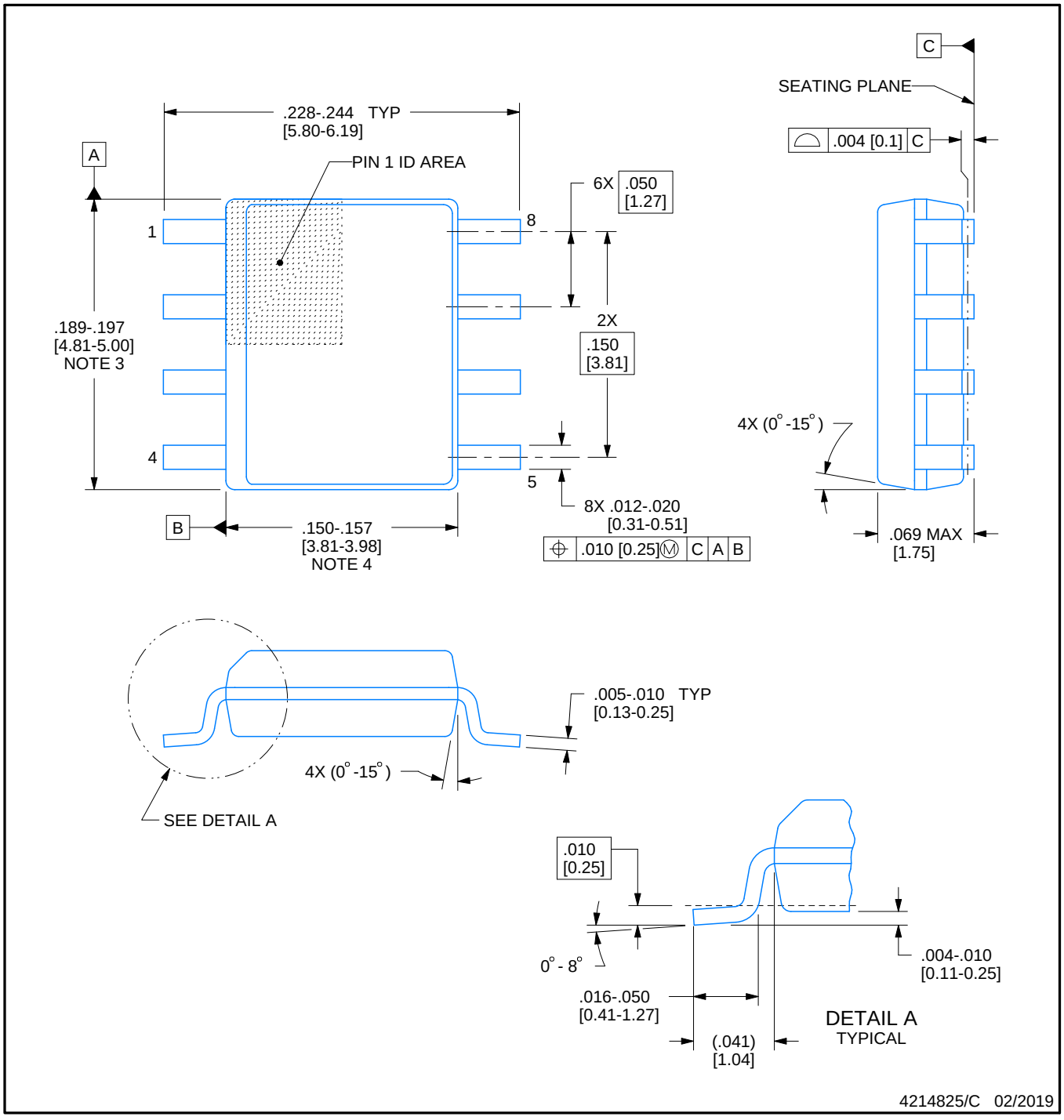


PACKAGE OUTLINE

D0008A

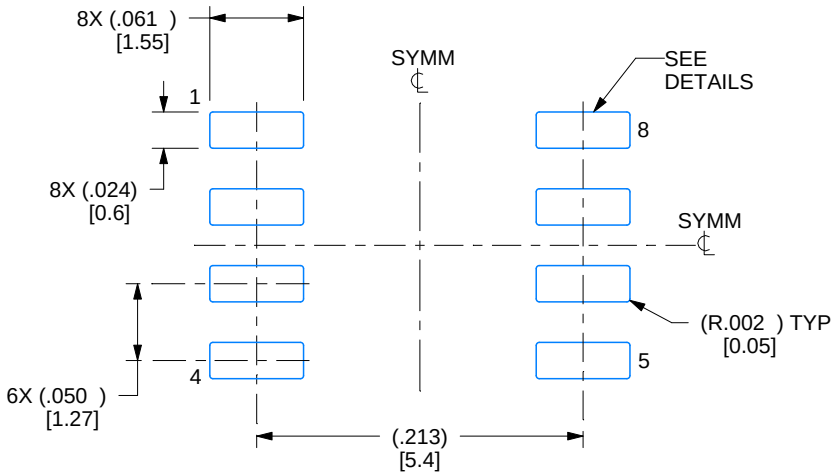
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

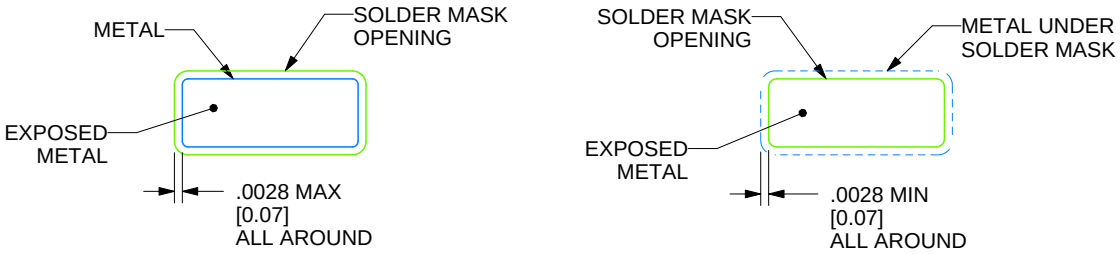


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

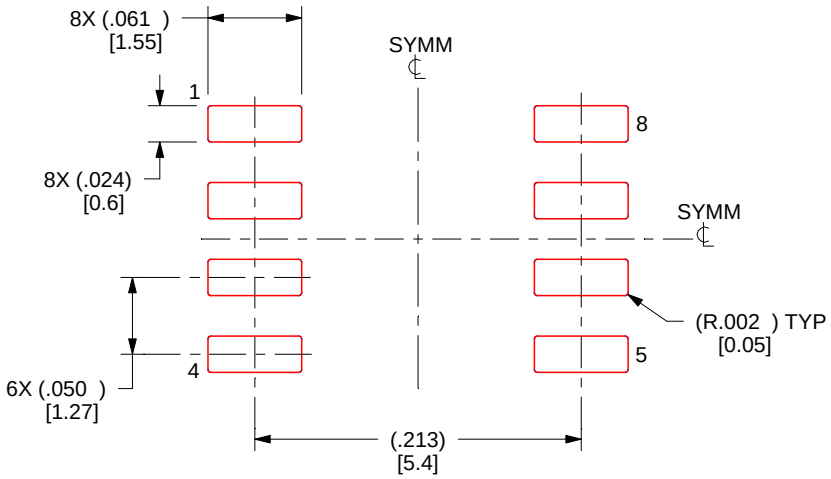
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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