

## 10.3Gbps Thunderbolt™ Port and DisplayPort™ Switch

Check for Samples: [HD3SS0001](#)

### FEATURES

- **Compatible with Thunderbolt™ Technology Electrical Standards and DisplayPort™ 1.2a**
- **Wide –3dB Differential Bandwidth of Over 10GHz on 10G Path**
- **Supports DP and DP++ Configurations**
- **Handles HPD (5V tolerant) and Cable Detect**
- **Supports AUX and DDC MUX**
- **Excellent Dynamic Characteristics (on 10G path, typical values at 5GHz):**
  - Crosstalk = –35dB
  - Off-Isolation = –24dB
  - Insertion Loss = –1.5dB
  - Return Loss = –20dB
  - Intra-pair Skew Added < 4ps
- **Single 3.3V Power Supply**
- **Small 3x3mm 24-Pin QFN Package**
- **Low Power Consumption**
  - 3.3mW Typical Active Power
  - 80  $\mu$ W Typical Detect Mode

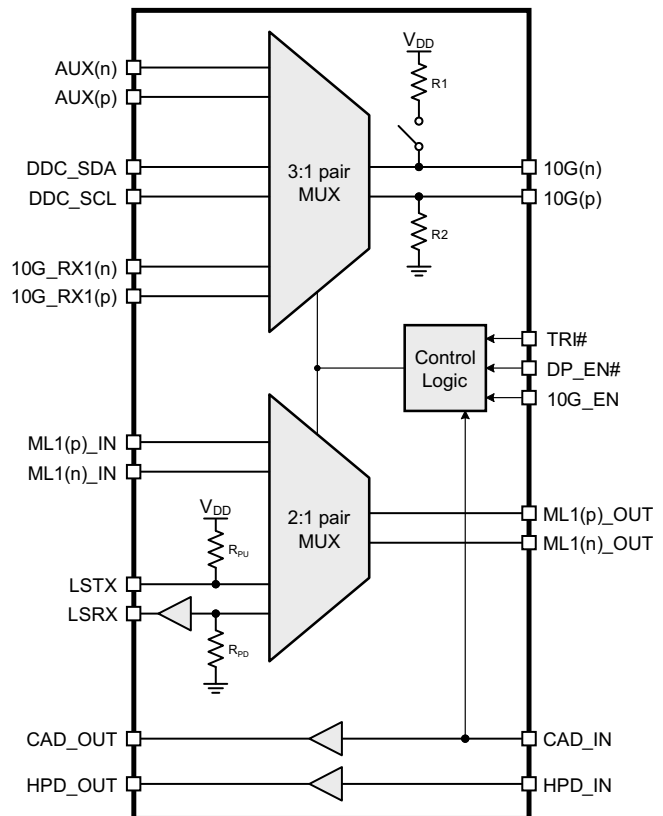
### DESCRIPTION

The HD3SS0001 is a high-speed passive-switch device with integrated buffers and resistors, designed to support Thunderbolt™ technology, DisplayPort, and Dual Mode DisplayPort. The 10G path supports a high 10GHz bandwidth and excellent loss characteristics, while the DisplayPort path supports 5.4Gbps.

The integrated 3-pairs to 1-pair multiplexer (3:1 MUX) switches between DDC, AUX, and 10.3Gbps signals. The integrated 2-pairs to 1-pair multiplexer (2:1 MUX) switches between the Thunderbolt™ technology Low Speed UART transmit/receive pair and DisplayPort Main Link 1.

The MUXs are controlled by 4 input pins: TRI#, DP\_EN#, 10G\_EN, and CAD\_IN (cable detect from the connector). The HD3SS0001 is packaged in a small 3x3mm 24-pin QFN, operates from a single 3.3V supply, and supports an ambient temperature range of –40°C to 85°C.

### FUNCTIONAL DIAGRAM



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Thunderbolt is a trademark of Intel Corp.

DisplayPort is a trademark of VESA Standards Association.

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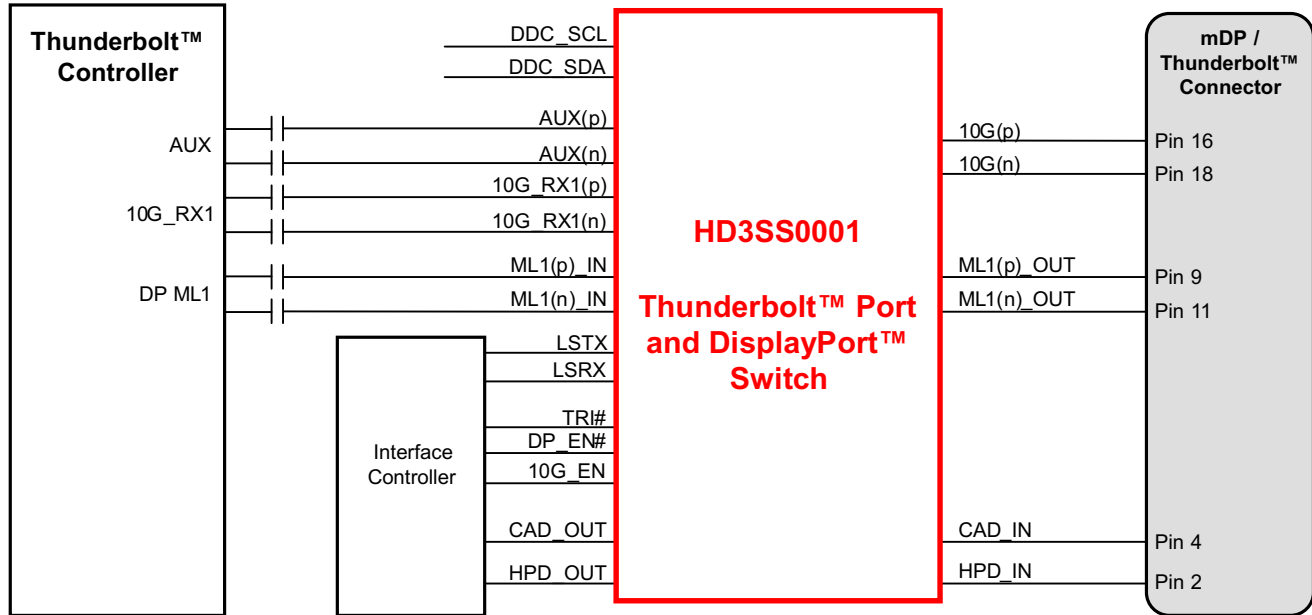
# HD3SS0001

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[www.ti.com](http://www.ti.com)


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## TYPICAL APPLICATION

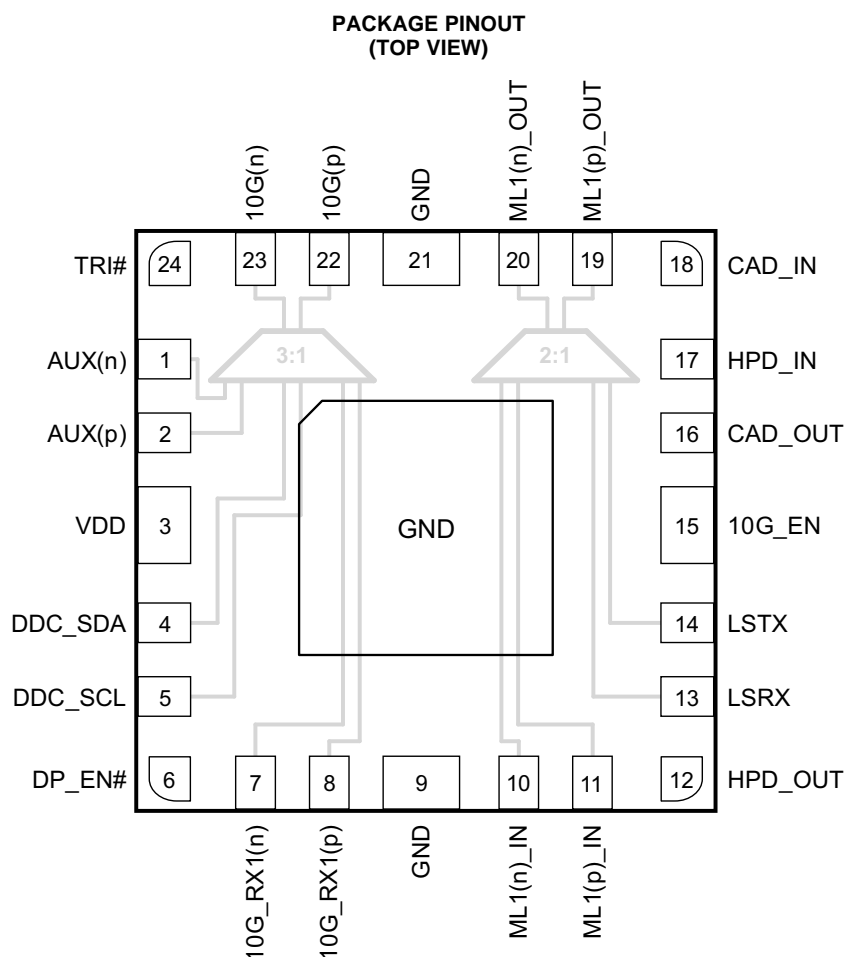


## TRUTH TABLE

| MODE                  | LOGICAL INPUT TO SET <sup>(1)</sup> |        |        |        | EFFECT                           |                                  |                            |
|-----------------------|-------------------------------------|--------|--------|--------|----------------------------------|----------------------------------|----------------------------|
|                       | TRI#                                | DP_EN# | 10G_EN | CAD_IN | 2:1 MUX SELECTION <sup>(2)</sup> | 3:1 MUX SELECTION <sup>(2)</sup> | PULL-UP RESISTOR on 10G(n) |
| Thunderbolt™ Protocol | 1                                   | 1      | 1      | X      | LS                               | 10G                              | Disconnected               |
|                       | 0                                   | 1      | 1      | X      | LS                               | Tri-stated                       | Disconnected               |
| DisplayPort           | 1                                   | 0      | 0      | 0      | ML                               | AUX                              | Connected                  |
|                       | 0                                   | 0      | 0      | 0      | Tri-Stated                       | Tri-stated                       | Connected                  |
| TMDS                  | 1                                   | 0      | 0      | 1      | ML                               | DDC                              | Connected                  |
|                       | 0                                   | 0      | 0      | 1      | Tri-Stated                       | Tri-stated                       | Connected                  |
| Detect Mode           | X                                   | 1      | 0      | X      | LS                               | Tri-Stated                       | Connected                  |
| [Invalid]             | X                                   | 0      | 1      | X      | Tri-Stated                       | Tri-Stated                       | Disconnected               |

(1) "X" = Don't Care.

(2) MUX Selection names are abbreviated.



**MUX PIN MAPPING<sup>(1)</sup>**

| CONTROLLER-SIDE PIN | Connector-Side Pin |
|---------------------|--------------------|
| AUX(n)              | 10G(n)             |
| DDC_SDA             |                    |
| 10G_RX1(n)          |                    |
| AUX(p)              | 10G(p)             |
| DDC_SCL             |                    |
| 10G_RX1(p)          |                    |
| ML1(p)_IN           | ML1(p)_OUT         |
| LSTX                |                    |
| ML1(n)_IN           | ML1(n)_OUT         |
| LSRX                |                    |

(1) NOTE: The HD3SS0001 can tolerate polarity inversions for the differential signals denoted by the (p) and (n) terminology, to ease potential board routing issues. LSTX/LSRX cannot be swapped, since LSRX is buffered and therefore unidirectional. Also, note that the integrated pullup on 10G(n) and the integrated pulldown on 10G(p) cannot be swapped.

**PIN FUNCTIONS**

| PIN               |                 | I/O          | SYSTEM SIDE | DESCRIPTION   |
|-------------------|-----------------|--------------|-------------|---|
| NO.               | NAME            |              |             |   |
| 11                | ML1(p)_IN       | I            | Controller  | DisplayPort MainLink1(p) input                                    |
| 10                | ML1(n)_IN       |              |             | DisplayPort MainLink1(n) input                                    |
| 24                | TRI#            |              |             | Tri-State control (see <a href="#">TRUTH TABLE</a> )              |
| 6                 | DP_EN#          |              |             | DisplayPort Enable, active-low (see <a href="#">TRUTH TABLE</a> ) |
| 15                | 10G_EN          |              |             | 10.3Gbps Mode Enable (see <a href="#">TRUTH TABLE</a> )           |
| 18                | CAD_IN          |              | Connector   | Cable Detect  |
| 17                | HPD_IN          |              |             | Hot Plug Detect   |
| 2                 | AUX(p)          | I/O          | Controller  | AUX Positive Signal   |
| 1                 | AUX(n)          |              |             | AUX Negative Signal   |
| 5                 | DDC_SCL         |              |             | DDC Clock   |
| 4                 | DDC_SDA         |              |             | DDC Data  |
| 14                | LSTX            |              |             | UART TX Signal  |
| 13                | LSRX            |              |             | UART RX Signal  |
| 22                | 10G(p)          |              | Connector   | 10G_RX1(p) or AUX(p) or DDC_SCL, with pull-down                   |
| 23                | 10G(n)          |              |             | 10G_RX1(n) or AUX(n) or DDC_SDA, with pull-up                     |
| 19                | ML1(p)_OUT      |              |             | DisplayPort MainLink1(p) output or LSTX                           |
| 20                | ML1(n)_OUT      |              |             | DisplayPort MainLink1(n) output or LSRX                           |
| 8                 | 10G_RX1(p)      |              | Controller  | 10.3Gbps Positive Signal  |
| 7                 | 10G_RX1(n)      |              |             | 10.3Gbps Negative Signal  |
| 16                | CAD_OUT         |              |             | Cable Detect  |
| 12                | HPD_OUT         |              |             | Hot Plug Detect   |
| 3                 | V <sub>DD</sub> | Power Supply |             | Power supply  |
| 9, 21, Center Pad | GND             |              |             | Reference ground  |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range (unless otherwise noted)

|                                     |                                     | VALUE                     |                      | UNIT |
|-------------------------------------|-------------------------------------|---------------------------|----------------------|------|
|                                     |                                     | MIN                       | MAX                  |      |
| Supply voltage range <sup>(2)</sup> | V <sub>DD</sub>                     | −0.5                      | 4                    | V    |
| Voltage range                       | Differential I/O                    | −0.5                      | 4                    | V    |
|                                     | Control pin/buffers                 | −0.5                      | V <sub>DD</sub> +0.5 |      |
| Electrostatic discharge             | Human body model <sup>(3)</sup>     |                           | ±1,500               | V    |
|                                     | Charged-device model <sup>(4)</sup> |                           | ±500                 |      |
| Continuous power dissipation        |                                     | See Power Characteristics |                      |      |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC/ESDA JS-001-2011
- (4) Tested in accordance with JEDEC JESD22 C101-E

## THERMAL INFORMATION

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC <sup>(1)</sup> |  | HD3SS0001         | UNITS |
|-------------------------------|--|-------------------|-------|
|                               |  | 24-PIN VQFN (RLL) |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 41.5              | °C/W  |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance    | 43.1              |       |
| $\theta_{JCbot}$              | Junction-to-case (bottom) thermal resistance | 6.3               |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 11.2              |       |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 1.2               |       |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 11.2              |       |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## POWER CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER    |                                  | TEST CONDITIONS        | MIN | TYP | MAX <sup>(1)</sup> | UNIT |
|--------------|----------------------------------|------------------------|-----|-----|--------------------|------|
| $I_{DD}$     | Supply Current in Active Mode    | Outputs Floating       |     | 1.0 | 1.3                | mA   |
| $I_{DETECT}$ | Supply Current in Detect Mode    | DP_EN# = 1, 10G_EN = 0 |     | 26  | 50                 | μA   |
| $P_D$        | Power Dissipation in Active Mode |                        |     | 3.3 | 4.7                | mW   |
| $P_{Detect}$ | Power Dissipation in Detect Mode |                        |     | 80  | 150                | μW   |

(1) The maximum ratings are simulated for  $V_{DD} = 3.6V$ .

## RECOMMENDED OPERATING CONDITIONS

Typical values for all parameters are at  $V_{DD} = 3.3V$  and  $T_A = 25^{\circ}C$ . (Temperature limits are specified by design)

| PARAMETER       | NOTES/CONDITIONS   | MIN  | TYP | MAX                     | UNIT |
|-----------------|--|------|-----|-------------------------|------|
| $V_{DD}$        | Supply voltage   | 3.0  | 3.3 | 3.6 <sup>(1)</sup>      | V    |
| $T_A$           | Operating free-air temperature   | –40  |     | 85                      | °C   |
| $V_{IH}$        | Input high voltage<br>CAD_IN, HPD_IN <sup>(2)</sup> , TRI#, DP_EN#, and 10G_EN<br>ML1(n)_OUT (when 2:1 MUX selects LS)   | 2.0  |     | $V_{DD}$                | V    |
|                 |  | 2.0  |     | $V_{DD}$                |      |
| $V_{IL}$        | Input low voltage<br>CAD_IN, HPD_IN <sup>(2)</sup> , TRI#, DP_EN#, and 10G_EN<br>ML1(n)_OUT (when 2:1 MUX selects LS)  | –0.1 |     | 0.8                     | V    |
|                 |  | –0.1 |     | 0.8                     |      |
| $V_{OH}$        | Output high voltage<br>CAD_OUT, HPD_OUT<br>LSRX (when 2:1 MUX selects LS)  | 2.7  |     | $V_{DD}$                | V    |
|                 |  | 2.7  |     | $V_{DD}$ <sup>(1)</sup> |      |
| $V_{OL}$        | Output low voltage<br>CAD_OUT, HPD_OUT<br>LSRX (when 2:1 MUX selects LS)   | 0.0  |     | 0.1                     | V    |
|                 |  | 0.0  |     | 0.1                     |      |
| $I_{IH}$        | High-level input current<br>TRI#, DP_EN#, 10G_EN, CAD_IN, and HPD_IN;<br>$V_{DD} = 3.6V$ , $V_{IN} = V_{DD}$<br>ML1(n)_OUT; $V_{DD} = 3.6V$ ; $V_{IN} = V_{DD}$ (when 2:1 MUX selects LS)  |      |     | 5                       | μA   |
|                 |  |      |     | 3.75                    |      |
| $I_{IL}$        | Low-level input current<br>TRI#, DP_EN#, 10G_EN, CAD_IN, and HPD_IN;<br>$V_{DD} = 3.6V$ , $V_{IN} = GND$<br>ML1(n)_OUT; $V_{DD} = 3.6V$ , $V_{IN} = GND$ (when 2:1 MUX selects LS)         |      |     | 100                     | nA   |
|                 |  |      |     | 100                     |      |
| $V_{I/O\_Diff}$ | Differential I/O voltage<br>AUX(p)/AUX(n), 10G_RX1(p)/10G_RX1(n),<br>ML1(p)_IN/ML1(n)_IN, 10G(p)/10G(n), and<br>ML1(p)_OUT/ML1(n)_OUT when MUX's are connected to<br>Differential Signals. | 0    |     | 1.8                     | Vpp  |
| $V_{I/O\_CM}$   | Common mode I/O voltage<br>AUX(p)/AUX(n), 10G_RX1(p)/10G_RX1(n),<br>ML1(p)_IN/ML1(n)_IN, 10G(p)/10G(n), and<br>ML1(p)_OUT/ML1(n)_OUT when MUX's are connected to<br>Differential Signals.  | 0    |     | 2.0                     | V    |

(1)  $V_{DD}$  range supports 3.0V to 3.6V, but for Thunderbolt products it is anticipated that the  $V_{DD}$  must be maintained at less than or equal to 3.4V to ensure that the  $V_{OH}$  on the LSRx do not exceed 3.4V.

(2) HPD\_IN is 5V tolerant.

## ELECTRICAL CHARACTERISTICS

(under recommended operation conditions)

| PARAMETER   | CONDITIONS  | MIN   | TYP  | MAX | UNIT     |
|---|---|-------|------|-----|----------|
| <b>Thunderbolt™ Technology 10.3Gbps Link: 10G_RX1(p), 10G_RX1(n) <sup>(1)</sup></b> |   |       |      |     |          |
| $R_L$   | Differential Return Loss<br>$f = 5.0$ GHz   |       | –20  |     | dB       |
| $I_L$   | Differential Insertion Loss<br>$f = 5.0$ GHz  |       | –1.5 |     | dB       |
| $O_{IRR}$   | Differential Off Isolation<br>$f = 5.0$ GHz (see <a href="#">Figure 3</a> )                               |       | –24  |     | dB       |
| $X_{TALK}$  | Differential Crosstalk<br>$f = 5.0$ GHz   |       | –35  |     | dB       |
| BW  | Bandwidth   | –3 dB | 10   |     | GHz      |
| $t_{PD}$  | Propagation Delay(from input to output)<br>$R_{sc}$ and $R_L = 50 \Omega$ (see <a href="#">Figure 2</a> ) |       |      | 200 | ps       |
| $T_{SKEW}$  | Intra-Pair Skew Added<br>$R_{sc}$ and $R_L = 50 \Omega$ (see <a href="#">Figure 2</a> )                   |       |      | 4   | ps       |
| $C_{ON}$  | Outputs ON Capacitance<br>$V_I = 0$ V, Outputs Open, Switch ON  |       | 1.5  |     | pF       |
| $C_{OFF}$   | Outputs OFF Capacitance<br>$V_I = 0$ V, Outputs Open Switch OFF   |       | 1    |     | pF       |
| $R_{ON}$  | Output ON resistance<br>$V_{DD} = 3.3$ V, $I_O = -15 \mu A$   |       | 7.5  |     | $\Omega$ |
| $\Delta R_{ON}$   | On resistance match between pairs of the same channel<br>$V_{DD} = 3.3V$ ; $I_O = -15 \mu A$              |       |      | 1   | $\Omega$ |
| $T_{ON}$  | Control Line Change to MUX Output Switched<br>See <a href="#">Figure 1</a>                                |       |      | 400 | μs       |
| $T_{OFF}$   |   |       |      | 10  |          |

(1) These values apply for CAD\_IN tri-stated, unless otherwise noted.

## ELECTRICAL CHARACTERISTICS (continued)

(under recommended operation conditions)

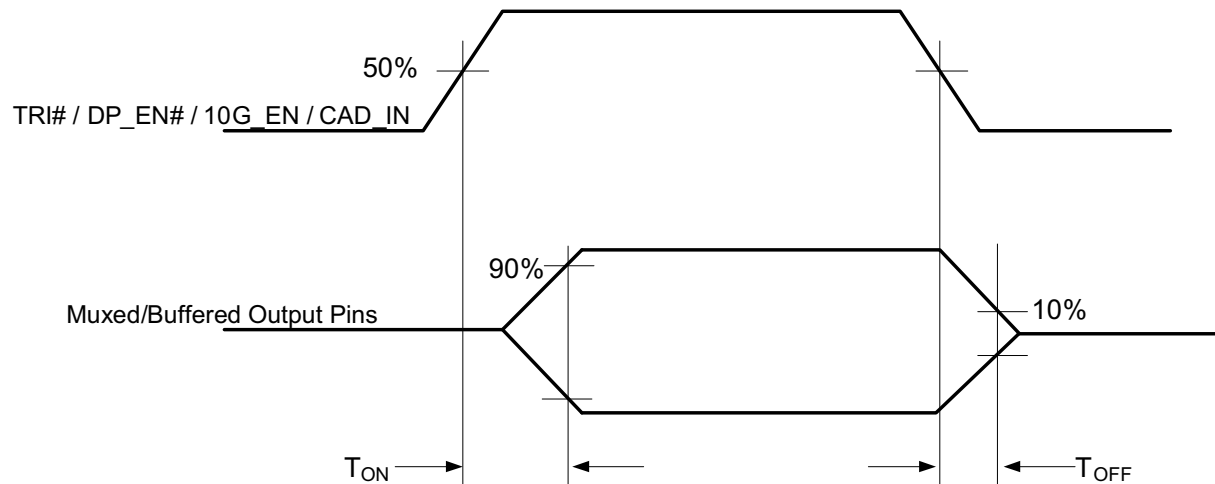
| PARAMETER                                     |   | CONDITIONS   | MIN | TYP  | MAX | UNIT |
|---|---|--|-----|------|-----|------|
| DisplayPort Link: ML1(p)_IN, ML1(n)_IN        |   |  |     |      |     |      |
| R <sub>L</sub>                                | Differential Return Loss                              | f = 2.7 GHz  |     | −16  |     | dB   |
| I <sub>L</sub>                                | Differential Insertion Loss                           | f = 2.7 GHz; V <sub>CM</sub> = 0 V   |     | −0.8 |     | dB   |
| O <sub>IRR</sub>                              | Differential Off-Isolation                            | f = 2.7 GHz (see Figure 3)   |     | −20  |     | dB   |
| X <sub>TALK</sub>                             | Differential Crosstalk                                | f = 2.7 GHz  |     | −35  |     | dB   |
| BW  | Differential Bandwidth                                | −3 dB  |     | 7    |     | GHz  |
| t <sub>PD</sub>                               | Propagation Delay(from input to output)               | R <sub>SC</sub> and R <sub>L</sub> = 50 Ω (see Figure 2)   |     |      | 200 | ps   |
| T <sub>SKEW</sub>                             | Intra-pair Skew Added                                 | R <sub>SC</sub> and R <sub>L</sub> = 50 Ω (see Figure 2)   |     |      | 4   | ps   |
| C <sub>ON</sub>                               | Outputs ON Capacitance                                | V <sub>I</sub> = 0 V; Outputs Open; Switch ON  |     | 1.5  |     | pF   |
| C <sub>OFF</sub>                              | Outputs OFF Capacitance                               | V <sub>I</sub> = 0 V; Outputs Open; Switch OFF   |     | 1    |     | pF   |
| R <sub>ON</sub>                               | Output ON resistance                                  | V <sub>DD</sub> = 3.3 V; I <sub>O</sub> = −15 mA; V <sub>CM</sub> = 0.5 V to 1.5 V; CAD_IN = 0 V |     | 6    | 8   | Ω    |
| ΔR <sub>ON</sub>                              | On resistance match between pairs of the same channel | V <sub>DD</sub> = 3.3 V; I <sub>O</sub> = -15 mA; V <sub>CM</sub> = 0.5 V to 1.5 V               |     |      | 1   | Ω    |
| T <sub>ON</sub>                               | Control Line Change to MUX Output Switched            | See Figure 1   |     |      | 400 | μs   |
| T <sub>OFF</sub>                              |   |  |     |      | 10  |      |
| Thunderbolt™ Technology Low Speed UART : LSTX |   |  |     |      |     |      |
| C <sub>ON</sub>                               | Outputs ON capacitance                                | V <sub>I</sub> = 0 V , Outputs Open, Switch ON   |     | 8    |     | pF   |
| C <sub>OFF</sub>                              | Outputs OFF capacitance                               | V <sub>I</sub> = 0 V, Outputs Open, Switch OFF   |     | 3    |     | pF   |
| R <sub>ON</sub>                               | Output ON resistance                                  | V <sub>DD</sub> = 3 V, V <sub>CM</sub> = 0 V to 3 V, I <sub>O</sub> = −1 mA<br>CAD_IN = 0 V      |     | 12   | 19  | Ω    |
| t <sub>PD</sub>                               | Propagation Delay                                     | LSTX to ML1(p)_OUT   |     | 200  |     | ps   |
| DisplayPort: AUX(p), AUX(n)                   |   |  |     |      |     |      |
| C <sub>ON</sub>                               | Outputs ON Capacitance                                | V <sub>I</sub> = 0 V; Outputs Open; Switch ON  |     | 6    |     | pF   |
| C <sub>OFF</sub>                              | Outputs OFF Capacitance                               | V <sub>I</sub> = 0 V; Outputs Open; Switch OFF   |     | 3    |     | pF   |
| R <sub>ON</sub>                               | Output ON resistance                                  | V <sub>DD</sub> = 3.3V; I <sub>O</sub> = −10 mA; AUX(p) = 0.3 V;<br>AUX(n) = 3.0 V; CAD_IN = 0 V |     | 12   |     | Ω    |
| ΔR <sub>ON</sub>                              | On resistance match between pairs of the same channel | V <sub>DD</sub> = 3.3 V; I <sub>O</sub> = −10 mA;<br>V <sub>CM</sub> = 0.5 V to 1.5 V            |     |      | 1   | Ω    |
| T <sub>ON</sub>                               | Control line change to Mux output switched            | See Figure 2   |     |      | 40  | ms   |
| T <sub>OFF</sub>                              |   |  |     |      | 10  | μs   |
| Thunderbolt Technology Low Speed UART : LSRX  |   |  |     |      |     |      |
| C <sub>ON</sub>                               | Outputs capacitance                                   |  |     | 3    |     | pF   |
| Z <sub>O</sub>                                | Output impedance                                      | V <sub>DD</sub> = 3.3 V  |     | 60   |     | Ω    |
| t <sub>PD</sub>                               | Propagation delay                                     | ML1(n)_OUT to LSRX   |     | 3.2  |     | ns   |
| t <sub>r</sub>                                | Rise Time   | V <sub>DD</sub> = 3 V  |     | 3    |     | ns   |
| t <sub>f</sub>                                | Fall Time   | V <sub>DD</sub> = 3 V  |     | 3    |     | ns   |
| T <sub>ON</sub>                               | Control line change to MUX Output Switched            | See Figure 1   |     |      | 400 | μs   |
| T <sub>OFF</sub>                              |   |  |     |      | 10  | μs   |

## ELECTRICAL CHARACTERISTICS (continued)

(under recommended operation conditions)

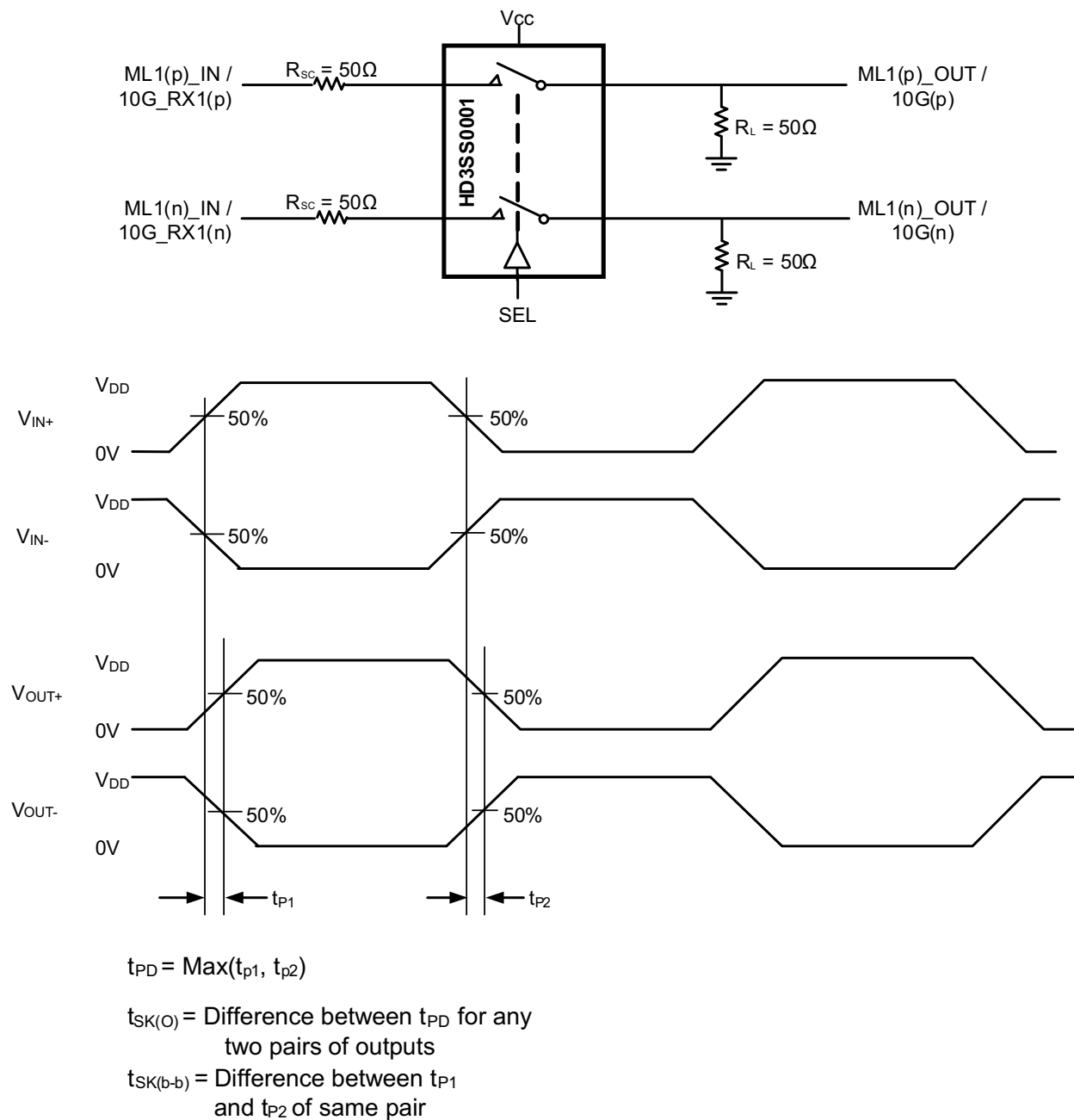
| PARAMETER  |  | CONDITIONS  | MIN | TYP | MAX | UNIT |
|--|--|---|-----|-----|-----|------|
| DisplayPort : DDC_SCL, DDC_SDA                     |  |   |     |     |     |      |
| C <sub>ON</sub>                                    | Outputs ON capacitance                     | V <sub>I</sub> = 0 V, Outputs Open, Switch ON   |     | 9   |     | pF   |
| C <sub>OFF</sub>                                   | Outputs OFF capacitance                    | V <sub>I</sub> = 0 V, Outputs Open, Switch OFF  |     | 3   |     | pF   |
| R <sub>ON</sub>                                    | Output ON resistance                       | V <sub>DD</sub> = 3.3 V, I <sub>O</sub> = −10 mA, V <sub>CM</sub> = 0.4 V, CAD_IN = 3.3 V |     | 80  | 150 | Ω    |
| T <sub>ON</sub>                                    | Control line change to MUX output switched | See <a href="#">Figure 1</a>  |     | 400 | μs  |      |
| T <sub>OFF</sub>                                   |  |   |     | 10  |     |      |
| UART and 10G MUX Outputs : LSTX/LSRX/10G(p)/10G(n) |  |   |     |     |     |      |
| R1   | Integrated Pullup Resistance               | 10G(n) pin when in DP, TMDS, or Detect Mode   |     | 87  | 105 | kΩ   |
| R2   | Integrated Pulldown Resistance             | 10G(p) pin when in DP, TMDS, or Detect Mode, or VDD = 0V                                  |     | 87  | 105 | kΩ   |
| R <sub>PU</sub>                                    | Integrated pullup resistance               | LSTX  |     | 8.7 |     | kΩ   |
| R <sub>PD</sub>                                    | Integrated pulldown resistance             | LSRX  |     | 1.2 |     | MΩ   |

## TEST DIAGRAMS

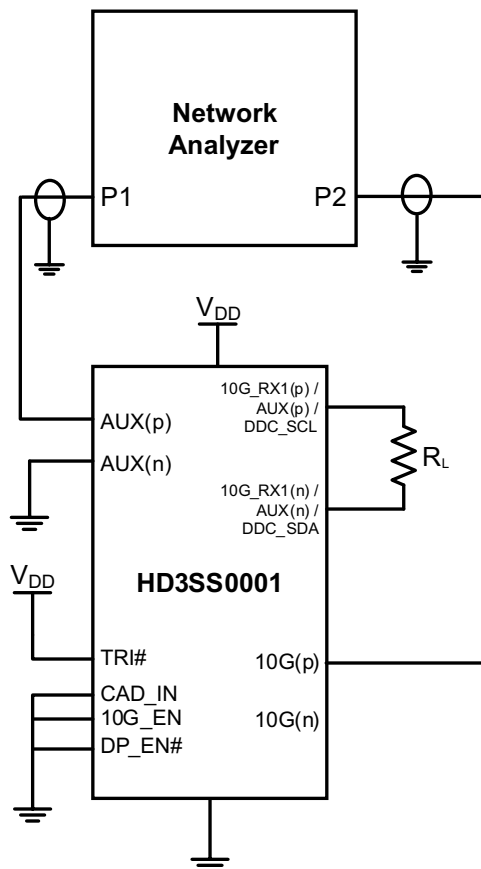


**Figure 1. Control Line Change to Switched Signals**





**Figure 2. Propagation Delay and Skew**



**Figure 3. Off-Isolation Measurement Setup**

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| HD3SS0001RLLR    | ACTIVE        | VQFN         | RLL                | 24   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 3SS001                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| HD3SS0001RLLR | VQFN         | RLL             | 24   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

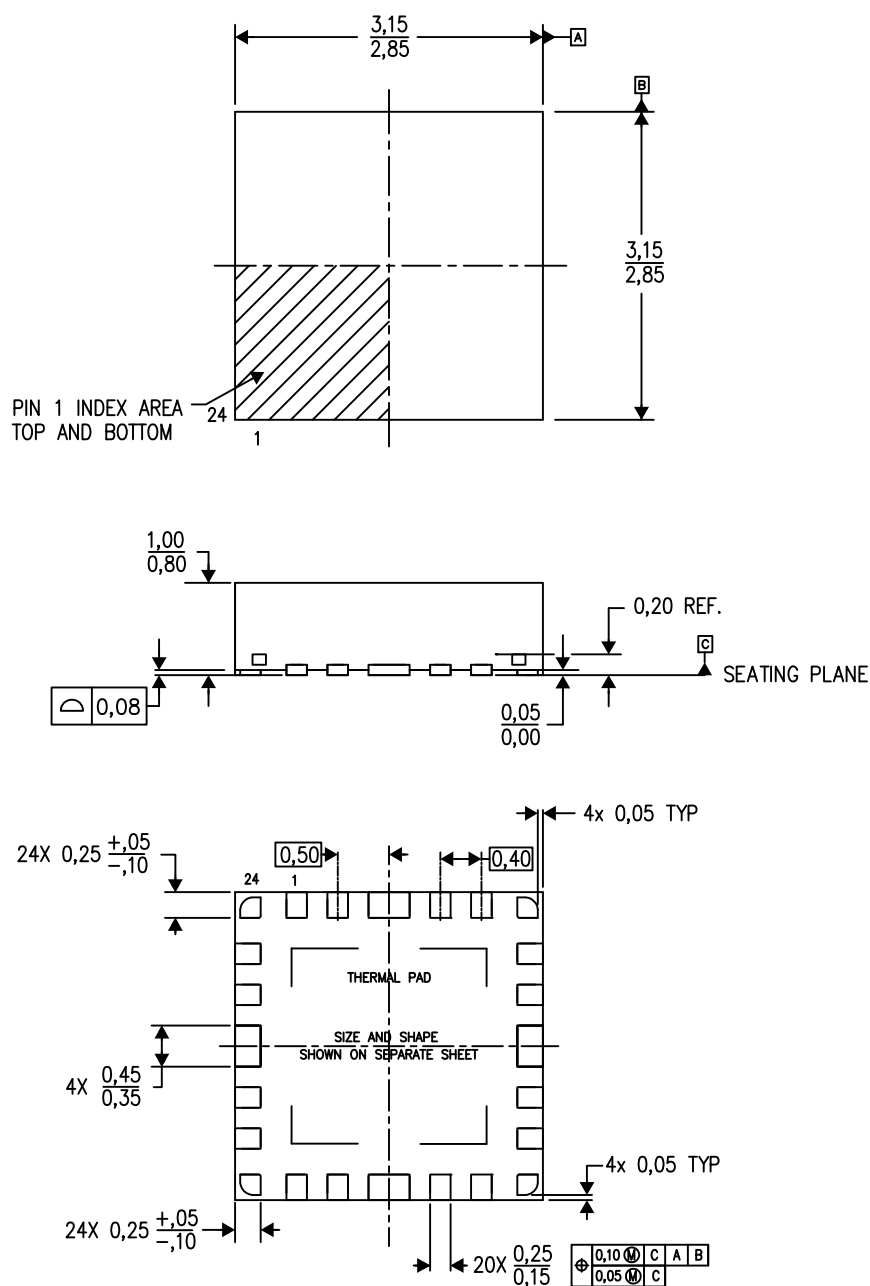


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| HD3SS0001RLLR | VQFN         | RLL             | 24   | 3000 | 367.0       | 367.0      | 35.0        |

RLL (S-PVQFN-N24)

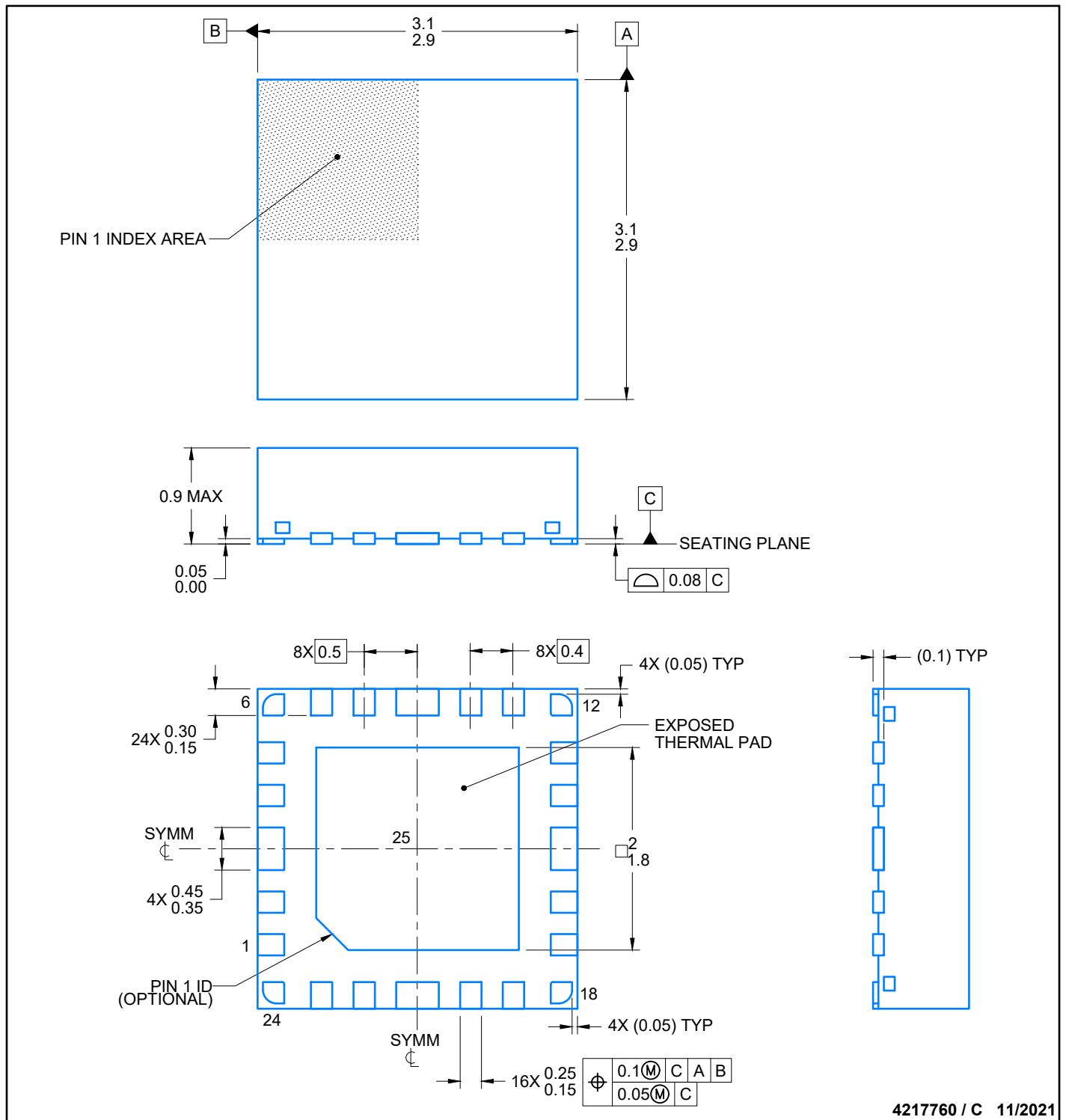
PLASTIC QUAD FLATPACK NO-LEAD



4214704/C 08/13

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

# RLL0024A

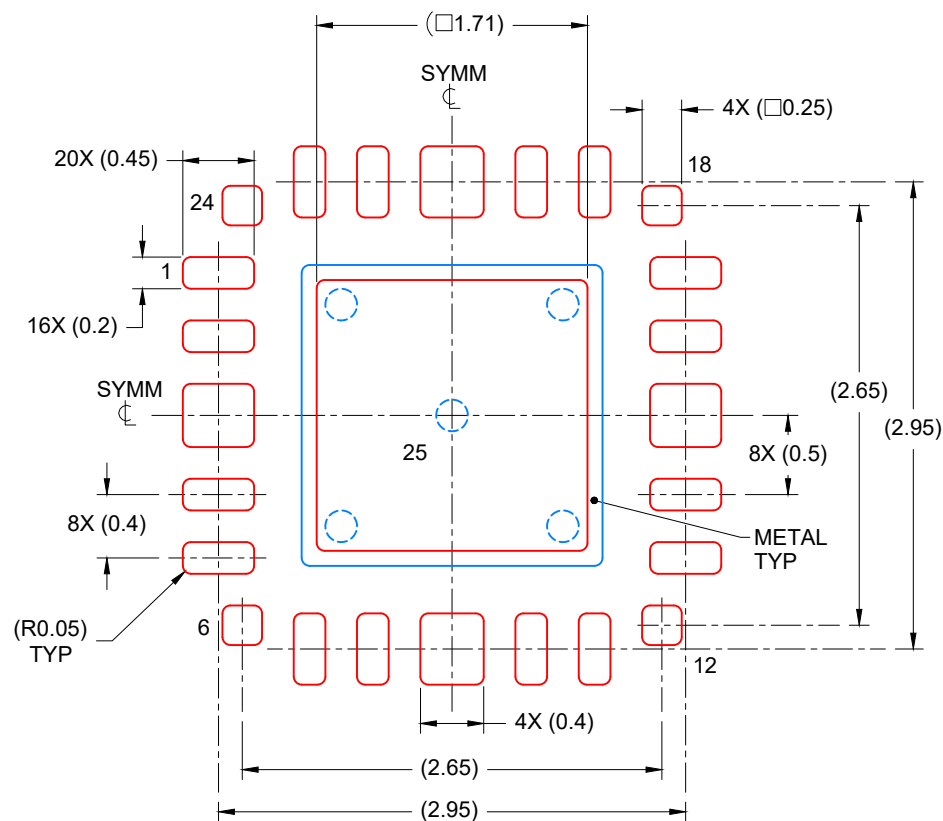


#### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.





## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD  
81% PRINTED COVERAGE BY AREA  
SCALE: 20X

4217760 / C 10/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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