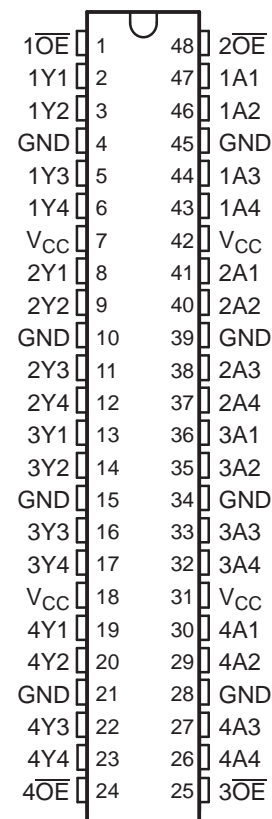


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54LVT162244A . . . WD PACKAGE  
SN74LVT162244A . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The 'LVT162244A devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When V<sub>CC</sub> is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I<sub>off</sub> and power-up 3-state. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN54LVT162244A, SN74LVT162244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

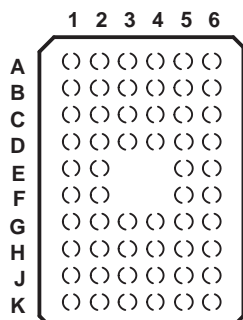
### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVT162244AGRDR	LZ244A
	FBGA – ZRD (Pb-free)		SN74LVT162244AZRDR	
	SSOP – DL	Tube of 25	SN74LVT162244ADL	LVT162244A
			SN74LVT162244ADLG4	
		Reel of 1000	SN74LVT162244ADLR	
			74LVT162244ADLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVT162244ADGGR 74LVT162244ADGGRE4	LVT162244A
	TVSOP – DGV	Reel of 2000	SN74LVT162244ADGVR	LZ244A
			74LVT162244ADGVRE4	
	VFBGA – GQL	Reel of 1000	SN74LVT162244AGQLR	LZ244A
SN74LVT162244AZQLR				
–55°C to 125°C	CFP – WD	Tube	SNJ544LVT162244AWD <sup>(2)</sup>	SNJ54LVT162244AWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) Product preview

#### GQL OR ZQL PACKAGE (TOP VIEW)

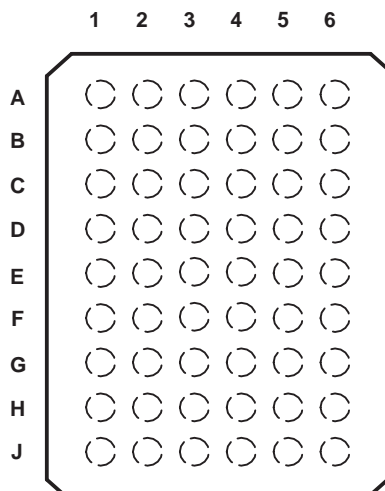


#### TERMINAL ASSIGNMENTS<sup>(1)</sup> (56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
<b>A</b>	1 $\overline{OE}$	NC	NC	NC	NC	2 $\overline{OE}$
<b>B</b>	1Y2	1Y1	GND	GND	1A1	1A2
<b>C</b>	1Y4	1Y3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4
<b>D</b>	2Y2	2Y1	GND	GND	2A1	2A2
<b>E</b>	2Y4	2Y3			2A3	2A4
<b>F</b>	3Y1	3Y2			3A2	3A1
<b>G</b>	3Y3	3Y4	GND	GND	3A4	3A3
<b>H</b>	4Y1	4Y2	V <sub>CC</sub>	V <sub>CC</sub>	4A2	4A1
<b>J</b>	4Y3	4Y4	GND	GND	4A4	4A3
<b>K</b>	4 $\overline{OE}$	NC	NC	NC	NC	3 $\overline{OE}$

(1) NC – No internal connection

GRD OR ZRD PACKAGE  
(TOP VIEW)



TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
<b>A</b>	1Y1	NC	1 $\overline{OE}$	2 $\overline{OE}$	NC	1A1
<b>B</b>	1Y3	1Y2	NC	NC	1A2	1A3
<b>C</b>	2Y1	1Y4	V <sub>CC</sub>	V <sub>CC</sub>	1A4	2A1
<b>D</b>	2Y3	2Y2	GND	GND	2A2	2A3
<b>E</b>	3Y1	2Y4	GND	GND	2A4	3A1
<b>F</b>	3Y3	3Y2	GND	GND	3A2	3A3
<b>G</b>	4Y1	3Y4	V <sub>CC</sub>	V <sub>CC</sub>	3A4	4A1
<b>H</b>	4Y3	4Y2	NC	NC	4A2	4A3
<b>J</b>	4Y4	NC	4 $\overline{OE}$	3 $\overline{OE}$	NC	4A4

(1) NC – No internal connection

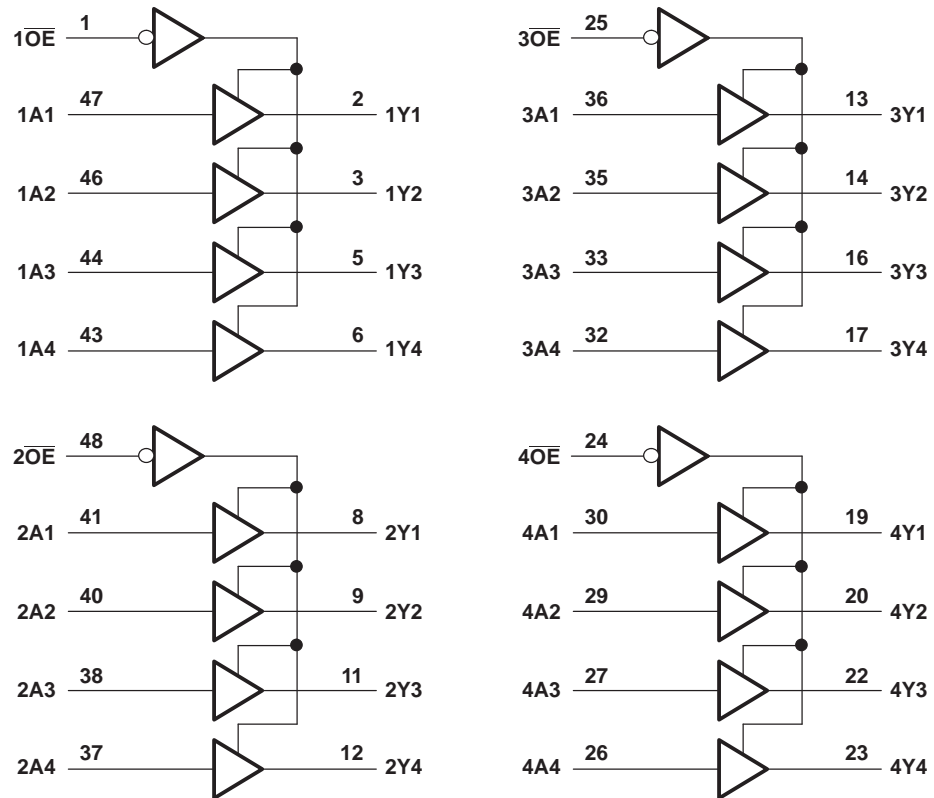
FUNCTION TABLE  
(each 4-bit buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

**SN54LVT162244A, SN74LVT162244A**  
**3.3-V ABT 16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state		30	mA
$I_O$	Current into any output in the high state <sup>(3)</sup>		30	mA
$I_{IK}$	Input clamp current	$V_I < 0$	–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		SN54LVT162244A <sup>(2)</sup>		SN74LVT162244A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–12		–12	mA
$I_{OL}$	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Product preview

# SN54LVT162244A, SN74LVT162244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT162244A <sup>(1)</sup>			SN74LVT162244A			UNIT
			MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ ,	$I_I = -18\text{ mA}$	-1.2			-1.2			V
$V_{OH}$	$V_{CC} = 3\text{ V}$ ,	$I_{OH} = -12\text{ mA}$	2						V
$V_{OL}$	$V_{CC} = 3\text{ V}$ ,	$I_{OL} = 12\text{ mA}$	0.8			0.8			V
$I_I$	Control inputs	$V_{CC} = 0\text{ or }3.6\text{ V}$ ,	$V_I = 5.5\text{ V}$		10		10		$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}\text{ or GND}$		$\pm 1$		$\pm 1$		
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$	1		1			
			$V_I = 0$	-5		-5			
$I_{off}$	$V_{CC} = 0$ ,	$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				$\pm 100$			$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ ,	$V_O = 3\text{ V}$	5			5			$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ ,	$V_O = 0.5\text{ V}$	-5			-5			$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$		$\pm 100$ <sup>(3)</sup>			$\pm 100$			$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$		$\pm 100$ <sup>(3)</sup>			$\pm 100$			$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high	0.19		0.19				mA
		Outputs low	5		5				
		Outputs disabled	0.19		0.19				
$\Delta I_{CC}$ <sup>(4)</sup>	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA
$C_i$	$V_I = 3\text{ V or }0$		4			4			pF
$C_o$	$V_O = 3\text{ V or }0$		9			9			pF

(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

## Switching Characteristics

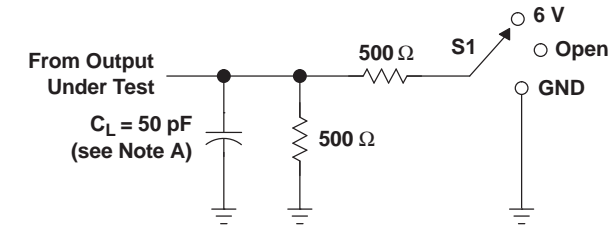
over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT162244A <sup>(1)</sup>				SN74LVT162244A				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(2)</sup>	MAX	MIN		MAX
$t_{PLH}$	A	Y	1.1	4.6	5.1		1.4	3.4	4	4.8		ns
$t_{PHL}$			1.1	3.9	4.5		1.2	2.9	3.6	4.1		
$t_{PZH}$	$\overline{OE}$	Y	1.1	5.4	6.7		1.2	3.9	5.1	6.5		ns
$t_{PZL}$			1.3	4.9	6.1		1.4	3.8	4.5	5.8		
$t_{PHZ}$	$\overline{OE}$	Y	1.6	5.9	6.5		2.2	4.4	5	5.4		ns
$t_{PLZ}$			1	5.9	5.8		2	4.2	5	5.4		
$t_{sk(LH)}$								0.5			ns	
$t_{sk(HL)}$								0.5				

(1) Product preview

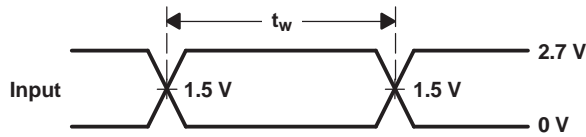
(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION

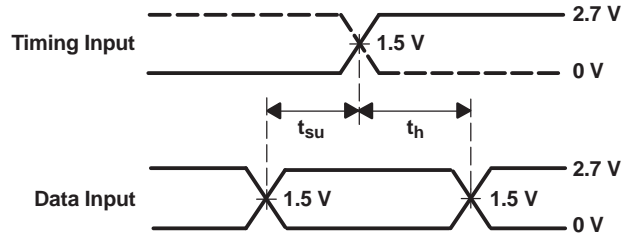


LOAD CIRCUIT

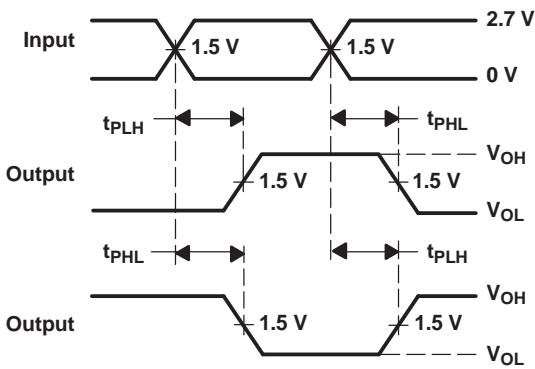
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



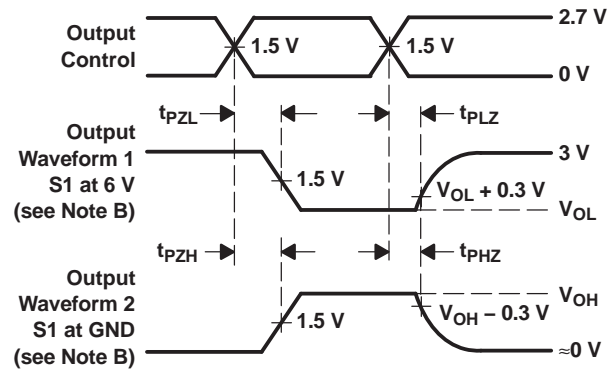
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVT162244ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162244A	<a href="#">Samples</a>
SN74LVT162244ADGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162244A	<a href="#">Samples</a>
SN74LVT162244ADGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LZ244A	<a href="#">Samples</a>
SN74LVT162244ADL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162244A	<a href="#">Samples</a>
SN74LVT162244ADLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT162244A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT162244ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVT162244ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVT162244ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT162244ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVT162244ADGVR	TVSOP	DGV	48	2000	853.0	449.0	35.0
SN74LVT162244ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVT162244ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

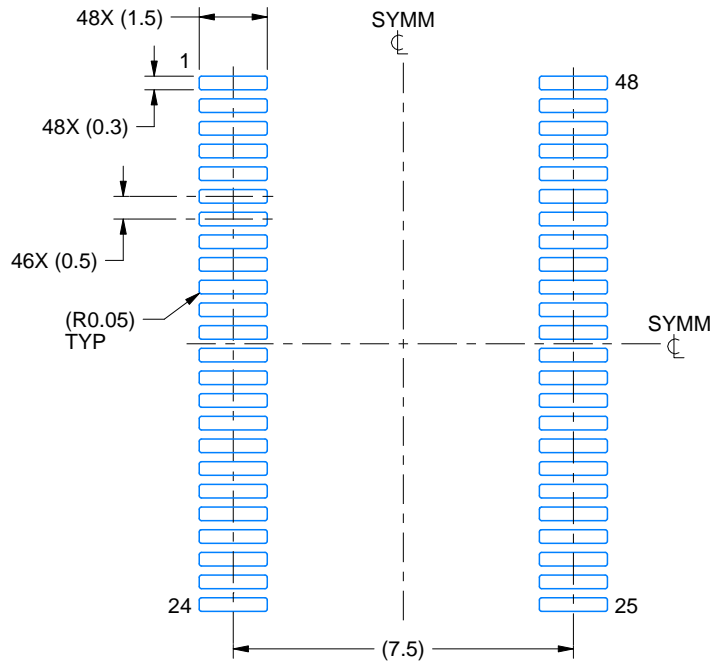


# EXAMPLE BOARD LAYOUT

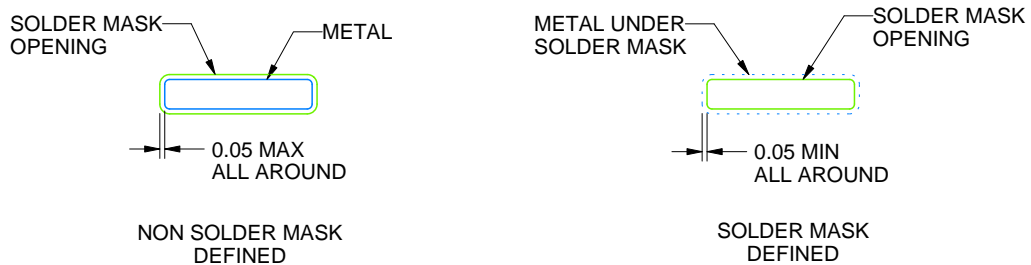
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

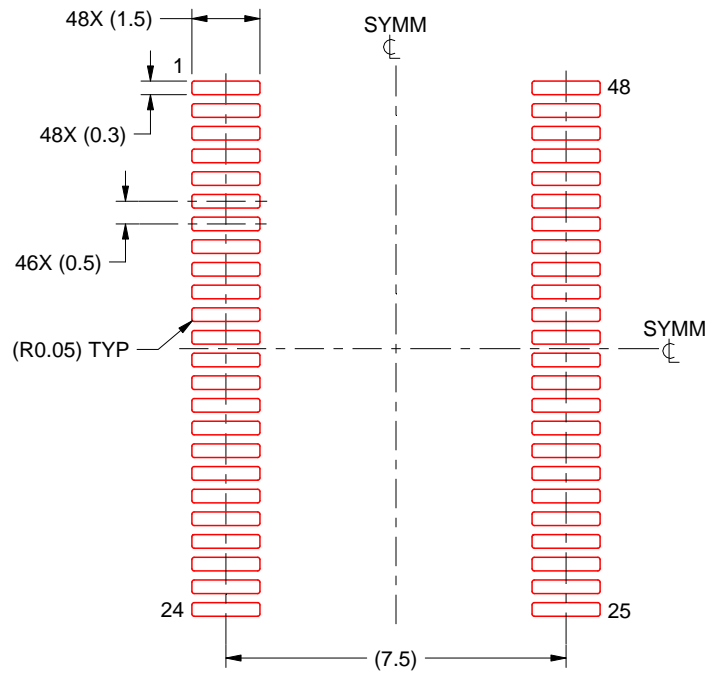
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

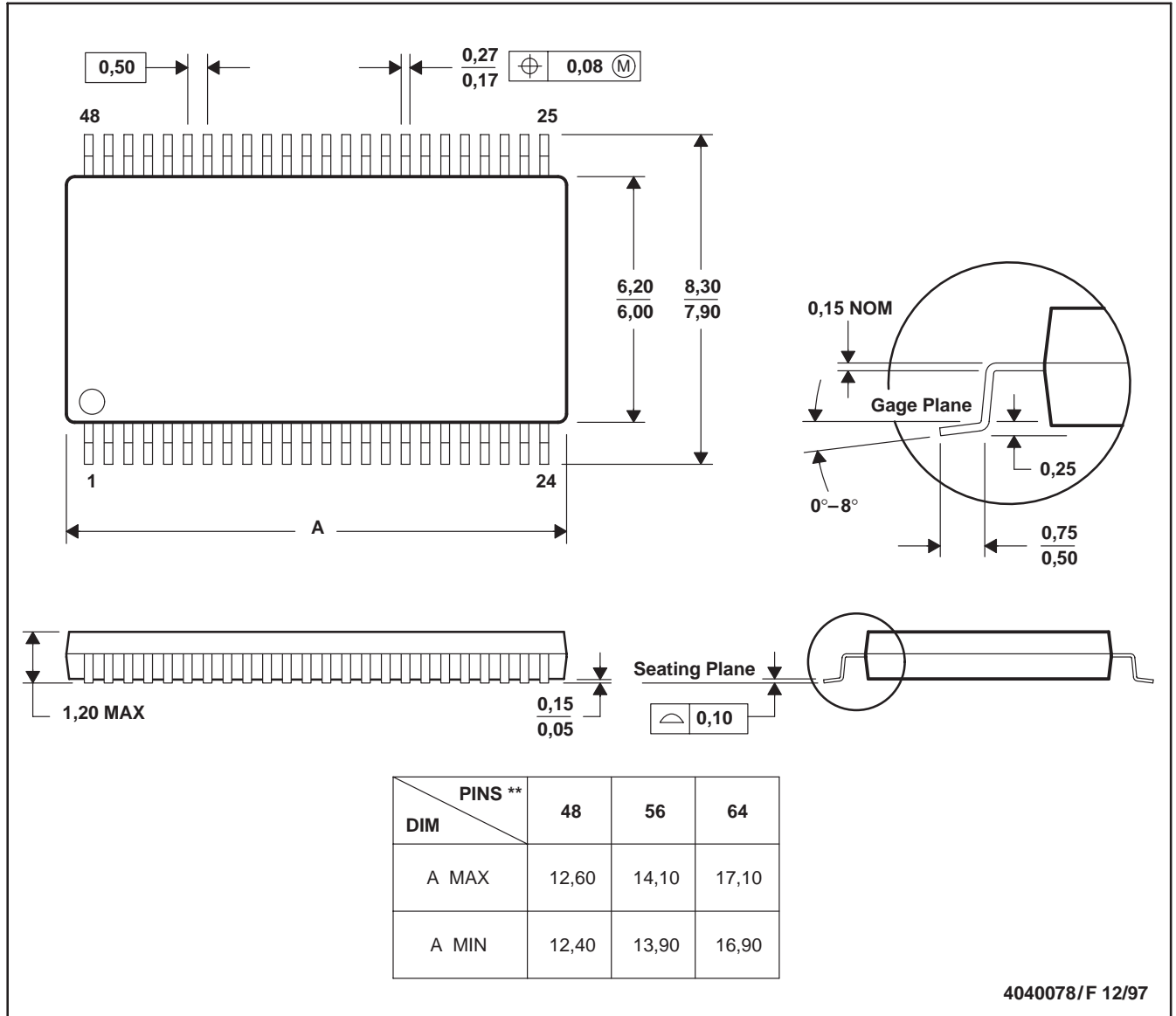
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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