# SN74AUP1G00 Low-Power Single 2-Input Positive-NAND Gate

## 1 Features

- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Available in the Ultra Small 0.64 $mm^2$ Package (DPW) with 0.5-mm Pitch
- Low Static-Power Consumption ($I_{CC}$ = 0.9 µA Max)
- Low Dynamic-Power Consumption ($C_{pd}$ = 4 pF Typical at 3.3 V)
- Low Input Capacitance ($C_i$ = 1.5 pF Typical)
- Low Noise Overshoot and Undershoot <10% of $V_{CC}$
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input ($V_{hys}$ = 250 mV Typical at 3.3 V)
- Wide Operating $V_{CC}$ Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd}$ = 4.8 ns Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## 2 Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3D Machine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital
- Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card
- X-ray: Baggage Scanner, Medical, and Dental

## 3 Description

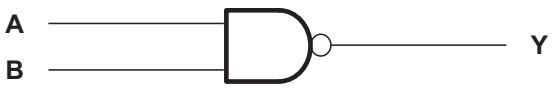
This single 2-input positive-NAND gate performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74AUP1G00DBV | SOT-23 (5) | 2.90 mm × 1.60 mm |
| SN74AUP1G00DCK | SC70 (5) | 2.00 mm × 1.25 mm |
| SN74AUP1G00DRL | SOT (5) | 1.60 mm × 1.20 mm |
| SN74AUP1G00DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74AUP1G00DSF | SON (6) | 1.00 mm × 1.00 mm |
| SN74AUP1G00YFP | DSBGA (6) | 1.00 mm × 1.40 mm |
| SN74AUP1G00YZP | DSBGA (5) | 1.37 mm × 0.87 mm |
| SN74AUP1G00DPW | X2SON (5) | 0.80 mm × 0.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision I (June 2014) to Revision J** — **Page**

- Changed X2SON package pin count from: "(4)" to: "(5)" ... 1
- Added DSF (SON) (6), YFP (DSBGA) (6), and YZP (DSBGA) (5) packages to *Device Information* ... 1
- Changed pinout images with new diagrams ... 4
- Changed *Pin Functions* table to *Pin Functions — DBV, DCK, DRL, DPW, DRY, and DSF* and *Pin Functions — YZP and YFP* tables ... 4
- Added missing pinout information to *Pin Functions* table ... 4
- Added Junction temperature, $T_J$ ... 6
- Changed *Handling Ratings* table to a *ESD Ratings* table ... 6
- Changed unit from: "A" to:"µA" for $I_{OL}$ at $V_{CC}$ = 0.8 V ... 7
- Added *Receiving Notification of Documentation Updates* section and *Community Resources* section ... 17

**Changes from Revision H (April 2012) to Revision I** — **Page**

- Updated document to new TI data sheet format. ... 1
- Removed Ordering Information table. ... 1
- Updated $I_{off}$ in *Features*. ... 1
- Added *Applications*. ... 1
- Added *Device Information* table. ... 1
- Added DPW Package ... 4
- Added *Handling Ratings* table. ... 6
- Added *Thermal Information* table. ... 7
- Added *Typical Characteristics*. ... 10


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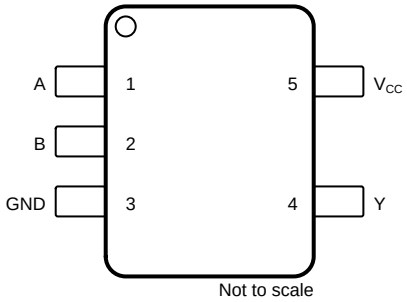
**Changes from Revision G (March 2010) to Revision H** **Page**

- Corrected the MIN Value for 1.2 V per available characterization data. ..... 9

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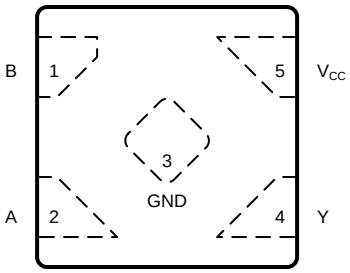
# 5 Pin Configuration and Functions

**DBV, DCK, or DRL Package**
**5-Pin SOT-23, SC70, or SOT**
**Top View**



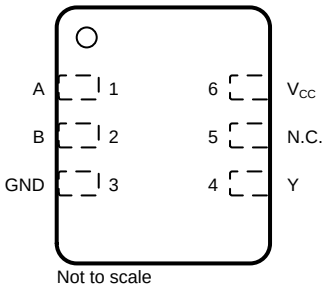

Not to scale

**DPW Package**
**5-Pin X2SON**
**Top View**




Not to scale

**DRY or DSF Package**
**6-Pin SON**
**Top View**




Not to scale

N.C. – No internal connection

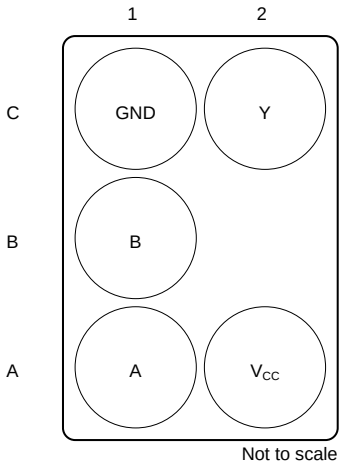
**Pin Functions — DBV, DCK, DRL, DPW, DRY, and DSF(1)**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DBV, DCK, DRL | DPW | DRY, DSF | | |
| A | 1 | 2 | 1 | I | Input A |
| B | 2 | 1 | 2 | I | Input B |
| GND | 3 | 3 | 3 | — | Ground |
| N.C. | – | – | 5 | — | No internal connection |
| $V_{CC}$ | 5 | 5 | 6 | — | Power Pin |
| Y | 4 | 4 | 4 | O | Output Y |

(1) See mechanical drawings for dimensions.

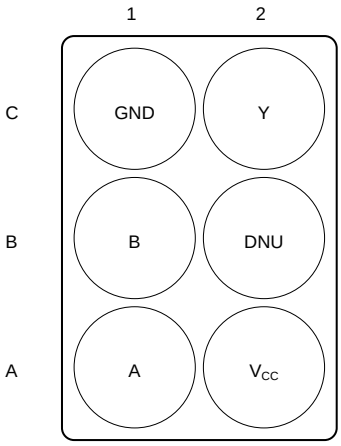

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**YZP Package**
**5-Pin DSBGA**
**Bottom View**




Not to scale

**YFP Package**
**6-Pin DSBGA**
**Bottom View**




Not to scale

DNU – Do not use

## Pin Functions — YZP and YFP(1)

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| YZP | YFP | NAME | | |
| A1 | A1 | A | I | Input A |
| A2 | A2 | $V_{CC}$ | — | Power Pin |
| B1 | B1 | B | I | Input B |
| – | B2 | DNU | — | Do not use |
| C1 | C1 | GND | — | Ground |
| C2 | C2 | Y | O | Output Y |

(1) See mechanical drawings for dimensions.

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 4.6 | V |
| $V_I$ | Input voltage (2) | | –0.5 | 4.6 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state (2) | | –0.5 | 4.6 | V |
| $V_O$ | Output voltage range in the high or low state (2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | 50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | 50 | mA |
| $I_O$ | Continuous output current | | | 20 | mA |
| | Continuous current through $V_{CC}$ or GND | | | 50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 (2) | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.8 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 0.8 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | 0.65 × $V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 0.8 V | | 0 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | | 0.35 × $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.9 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 0.8 V | | –20 | μA |
| | | $V_{CC}$ = 1.1 V | | –1.1 | mA |
| | | $V_{CC}$ = 1.4 V | | –1.7 | |
| | | $V_{CC}$ = 1.65 | | –1.9 | |
| | | $V_{CC}$ = 2.3 V | | –3.1 | |
| | | $V_{CC}$ = 3 V | | –4 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 0.8 V | | 20 | μA |
| | | $V_{CC}$ = 1.1 V | | 1.1 | mA |
| | | $V_{CC}$ = 1.4 V | | 1.7 | |
| | | $V_{CC}$ = 1.65 V | | 1.9 | |
| | | $V_{CC}$ = 2.3 V | | 3.1 | |
| | | $V_{CC}$ = 3 V | | 4 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 0.8 V to 3.6 V | | 200 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74AUP1G00 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DPW (X2SON) | DRL (SOT) | DRY (SON) | DSF (SON) | |
| | | 5 PINS | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 298.6 | 314.4 | 291.8 | 349.7 | 554.9 | 407.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 240.2 | 128.7 | 224.2 | 120.5 | 385.4 | 232.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 134.6 | 100.6 | 245.8 | 171.4 | 388.2 | 306.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 114.5 | 7.1 | 31.4 | 10.8 | 159.0 | 40.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 133.9 | 99.8 | 245.6 | 169.4 | 384.1 | 306.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | 195.4 | n/a | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to +85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –20 µA | 0.8 V to 3.6 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | V |
| | | $I_{OH}$ = –1.1 mA | 1.1 V | 0.75 × $V_{CC}$ | | | 0.7 × $V_{CC}$ | | |
| | | $I_{OH}$ = –1.7 mA | 1.4 V | 1.11 | | | 1.03 | | |
| | | $I_{OH}$ = –1.9 mA | 1.65 V | 1.32 | | | 1.3 | | |
| | | $I_{OH}$ = –2.3 mA | 2.3 V | 2.05 | | | 1.97 | | |
| | | $I_{OH}$ = –3.1 mA | | 1.9 | | | 1.85 | | |
| | | $I_{OH}$ = –2.7 mA | 3 V | 2.72 | | | 2.67 | | |
| | | $I_{OH}$ = –4 mA | | 2.6 | | | 2.55 | | |
| $V_{OL}$ | | $I_{OL}$ = 20 µA | 0.8 V to 3.6 V | | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 1.1 mA | 1.1 V | | | 0.3 × $V_{CC}$ | | 0.3 × $V_{CC}$ | |
| | | $I_{OL}$ = 1.7 mA | 1.4 V | | | 0.31 | | 0.37 | |
| | | $I_{OL}$ = 1.9 mA | 1.65 V | | | 0.31 | | 0.35 | |
| | | $I_{OL}$ = 2.3 mA | 2.3 V | | | 0.31 | | 0.33 | |
| | | $I_{OL}$ = 3.1 mA | | | | 0.44 | | 0.45 | |
| | | $I_{OL}$ = 2.7 mA | 3 V | | | 0.31 | | 0.33 | |
| | | $I_{OL}$ = 4 mA | | | | 0.44 | | 0.45 | |
| $I_I$ | A or B input | $V_I$ = GND to 3.6 V | 0 V to 3.6 V | | | 0.1 | | 0.5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V | | | 0.2 | | 0.6 | µA |
| $\Delta I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V to 0.2 V | | | 0.2 | | 0.6 | µA |
| $I_{CC}$ | | $V_I$ = GND or ($V_{CC}$ to 3.6 V), $I_O$ = 0 | 0.8 V to 3.6 V | | | 0.5 | | 0.9 | µA |
| $\Delta I_{CC}$ | | $V_I$ = $V_{CC}$ – 0.6 V(1), $I_O$ = 0 | 3.3 V | | | 40 | | 50 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 0 V | | 1.5 | | | | pF |
| | | | 3.6 V | | 1.5 | | | | |
| $C_o$ | | $V_O$ = GND | 0 V | | 3 | | | | pF |

(1) One input at $V_{CC}$ – 0.6 V, other input at $V_{CC}$ or GND.

## 6.6 Switching Characteristics, $C_L$ = 5 pF

over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to +85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 0.8 V | | 16.6 | | | | ns |
| | | | 1.2 V ± 0.1 V | 2.6 | 7 | 13.8 | 2.1 | 17.1 | |
| | | | 1.5 V ± 0.1 V | 2.9 | 5 | 9.2 | 2.9 | 11.1 | |
| | | | 1.8 V ± 0.15 V | 2 | 4 | 7.1 | 2 | 9 | |
| | | | 2.5 V ± 0.2 V | 1.3 | 2.9 | 4.9 | 1.3 | 6.2 | |
| | | | 3.3 V ± 0.3 V | 1 | 2.4 | 3.8 | 1 | 4.8 | |


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## 6.7 Switching Characteristics, $C_L$ = 10 pF

over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to +85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 0.8 V | | 18.9 | | | | ns |
| | | | 1.2 V ± 0.1 V | 3.2 | 8 | 15.7 | 3.1 | 18.8 | |
| | | | 1.5 V ± 0.1 V | 2.9 | 5.8 | 10.5 | 2.9 | 12.1 | |
| | | | 1.8 V ± 0.15 V | 2 | 4.7 | 8.2 | 2 | 9.8 | |
| | | | 2.5 V ± 0.2 V | 1.3 | 3.4 | 5.7 | 1.3 | 6.8 | |
| | | | 3.3 V ± 0.3 V | 1 | 2.9 | 4.5 | 1 | 5.2 | |

## 6.8 Switching Characteristics, $C_L$ = 15 pF

over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to +85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 0.8 V | | 21.3 | | | | ns |
| | | | 1.2 V ± 0.1 V | 3.6 | 9 | 17.3 | 3.1 | 21.5 | |
| | | | 1.5 V ± 0.1 V | 2.9 | 6.5 | 11.6 | 2.9 | 14 | |
| | | | 1.8 V ± 0.15 V | 2 | 5.3 | 9.2 | 2 | 11.4 | |
| | | | 2.5 V ± 0.2 V | 1.3 | 3.9 | 6.4 | 1.3 | 8 | |
| | | | 3.3 V ± 0.3 V | 1 | 3.3 | 5.1 | 1 | 6.4 | |

## 6.9 Switching Characteristics, $C_L$ = 30 pF

over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to +85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 0.8 V | | 28.4 | | | | ns |
| | | | 1.2 V ± 0.1 V | 4.9 | 11.9 | 21.9 | 4.4 | 27.1 | |
| | | | 1.5 V ± 0.1 V | 2.9 | 8.6 | 14.7 | 2.9 | 17.7 | |
| | | | 1.8 V ± 0.15 V | 2 | 7.1 | 11.5 | 2 | 14.2 | |
| | | | 2.5 V ± 0.2 V | 1.3 | 5.3 | 8.1 | 1.3 | 10 | |
| | | | 3.3 V ± 0.3 V | 1 | 4.5 | 6.5 | 1 | 8 | |

## 6.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 0.8 V | 4 | pF |
| | | | 1.2 V ± 0.1 V | 4 | |
| | | | 1.5 V ± 0.1 V | 4 | |
| | | | 1.8 V ± 0.15 V | 4 | |
| | | | 2.5 V ± 0.2 V | 4 | |
| | | | 3.3 V ± 0.3 V | 4 | |

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## 6.11 Typical Characteristics

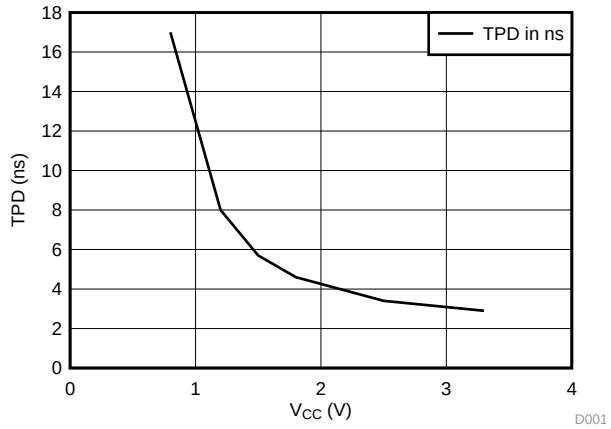



**Figure 1. TDP vs $V_{CC}$**

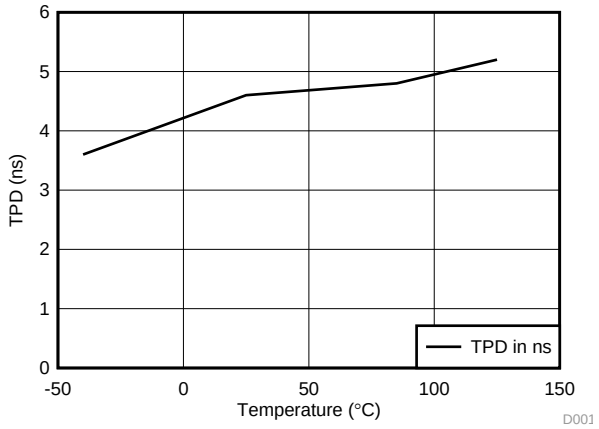
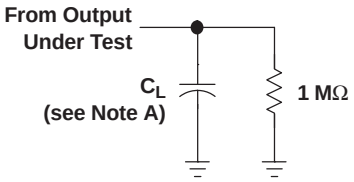



**Figure 2. TPD vs Temperature**


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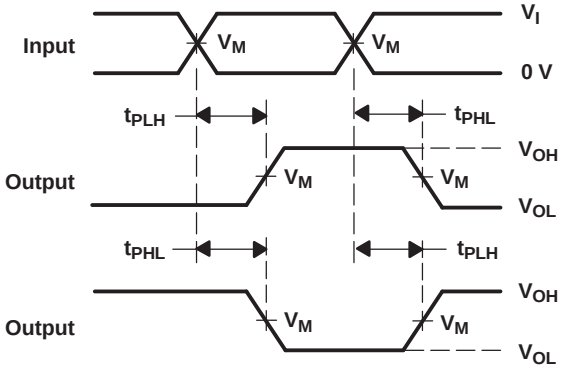
# 7 Parameter Measurement Information

## 7.1 Propagation Delays, Setup and Hold Times, and Pulse Width

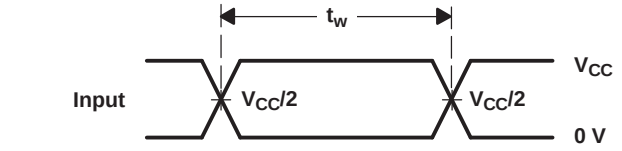



LOAD CIRCUIT

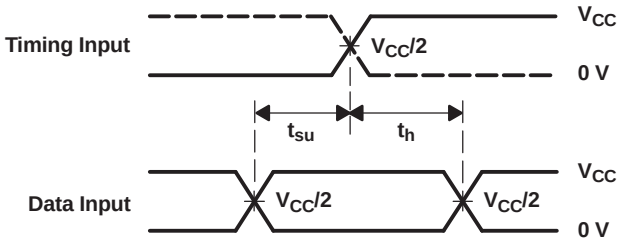
| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
PULSE DURATION



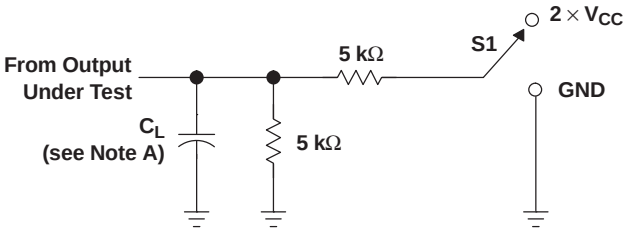

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
E. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

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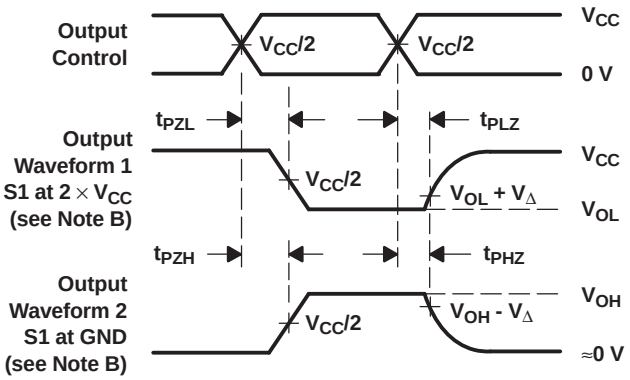
## 7.2 Enable and Disable Times




| TEST | S1 |
|---|---|
| $t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | 2 × $V_{CC}$<br>GND |

LOAD CIRCUIT

| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $V_\Delta$ | 0.1 V | 0.1 V | 0.1 V | 0.15 V | 0.15 V | 0.3 V |




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**


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# 8 Detailed Description

## 8.1 Overview

This is a single 2-input positive-NAND gate that is designed in Texas Instrument's ultra-low power technology. It performs the Boolean function $Y = \overline{A} \times \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The AUP family of devices has quiescent power consumption less than 1 µA and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered. The $I_{off}$ feature also allows for live insertion.

## 8.2 Functional Block Diagram

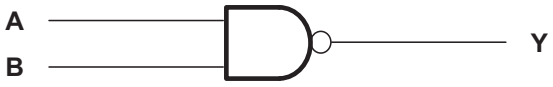



**Figure 5. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

- Wide operating $V_{CC}$ range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- $I_{off}$ feature allows voltages on the inputs and outputs when $V_{CC}$ is 0 V
- Low noise due to slower edge rates

## 8.4 Device Functional Modes

Table 1 shows the functional modes of the SN74AUP1G00 device.

**Table 1. Function Table**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

# 9 Application and Implementation

## 9.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire $V_{CC}$ range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

## 9.2 Typical Application

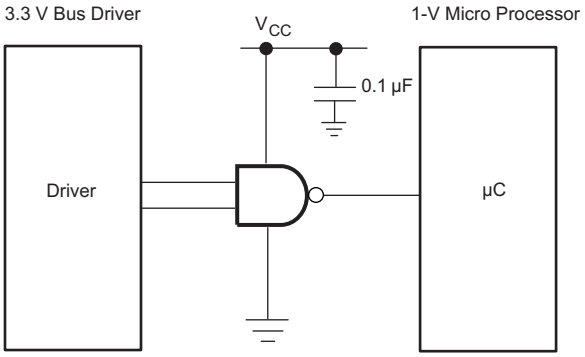



**Figure 6. Typical Application Diagram**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

### 9.2.2 Detailed Design Procedure

1. Recommended Input conditions:
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in *Recommended Operating Conditions*
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in *Recommended Operating Conditions*
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid $V_{CC}$
2. Recommended output conditions:
   - Load currents should not exceed 20 mA on the output and 50 mA total for the part
   - Outputs should not be pulled above $V_{CC}$


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## Typical Application (continued)

### 9.2.3 Application Curves

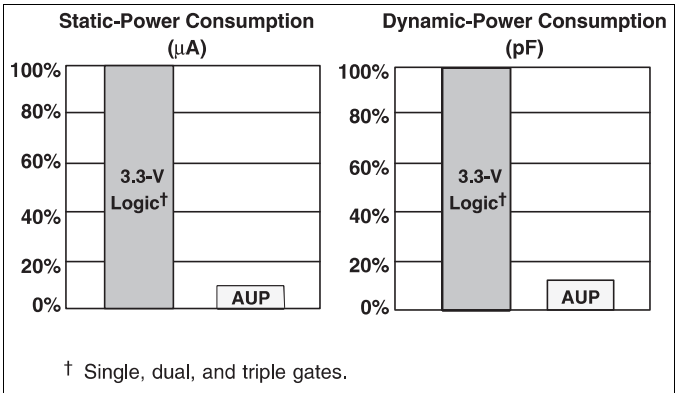



**Figure 7. AUP – The Lowest-Power Family**

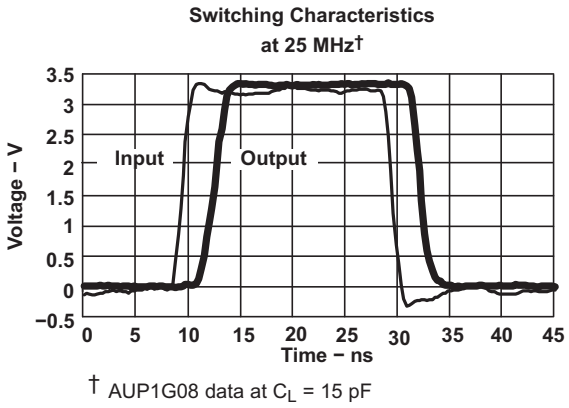



**Figure 8. Excellent Signal Integrity**

The AUP family of single gate logic makes excellent translators for the new lower voltage microprocessors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

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# 10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple $V_{CC}$ pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 9 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

## 11.2 Layout Example

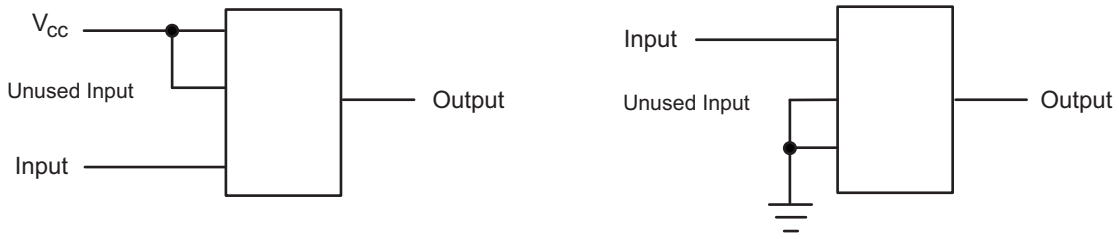



**Figure 9. Layout Diagram**


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# 12 Device and Documentation Support

## 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G00DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H00R | Samples |
| SN74AUP1G00DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H00R | Samples |
| SN74AUP1G00DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HAF, HAK, HAR) | Samples |
| SN74AUP1G00DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HAF, HAK, HAR) | Samples |
| SN74AUP1G00DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HAR | Samples |
| SN74AUP1G00DPWR | ACTIVE | X2SON | DPW | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | A4 | Samples |
| SN74AUP1G00DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (HA7, HAR) | Samples |
| SN74AUP1G00DRY2 | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HA | Samples |
| SN74AUP1G00DRYR | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HA | Samples |
| SN74AUP1G00DSF2 | ACTIVE | SON | DSF | 6 | 5000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HA | Samples |
| SN74AUP1G00DSFR | ACTIVE | SON | DSF | 6 | 5000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HA | Samples |
| SN74AUP1G00YFPR | ACTIVE | DSBGA | YFP | 6 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | | HAN | Samples |
| SN74AUP1G00YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HAN | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

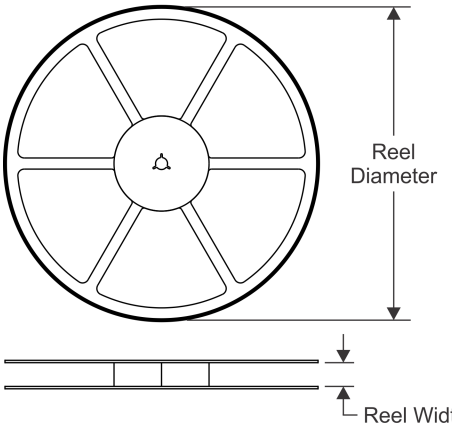
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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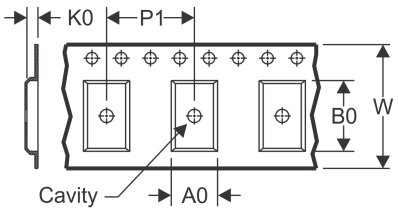
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

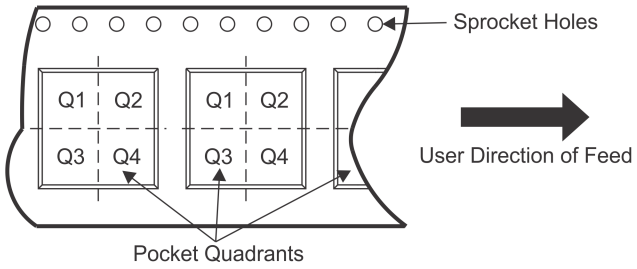



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

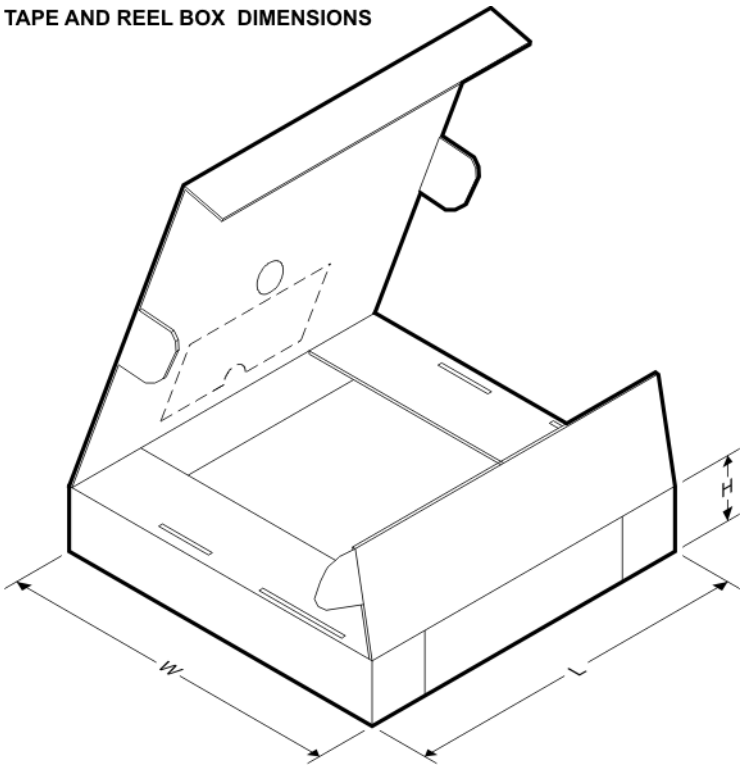
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G00DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74AUP1G00DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DRY2 | SON | DRY | 6 | 5000 | 180.0 | 8.4 | 1.65 | 1.2 | 0.7 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DRY2 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.6 | 1.15 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1G00DSF2 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.63 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DSF2 | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| SN74AUP1G00DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.63 | 4.0 | 8.0 | Q2 |
| SN74AUP1G00DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G00YFPR | DSBGA | YFP | 6 | 3000 | 178.0 | 9.2 | 0.89 | 1.29 | 0.62 | 4.0 | 8.0 | Q1 |
| SN74AUP1G00YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUP1G00DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DCKR | SC70 | DCK | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AUP1G00DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AUP1G00DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DRY2 | SON | DRY | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DRY2 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G00DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G00DSF2 | SON | DSF | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DSF2 | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G00DSFR | SON | DSF | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G00DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G00YFPR | DSBGA | YFP | 6 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74AUP1G00YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

# GENERIC PACKAGE VIEW

## DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

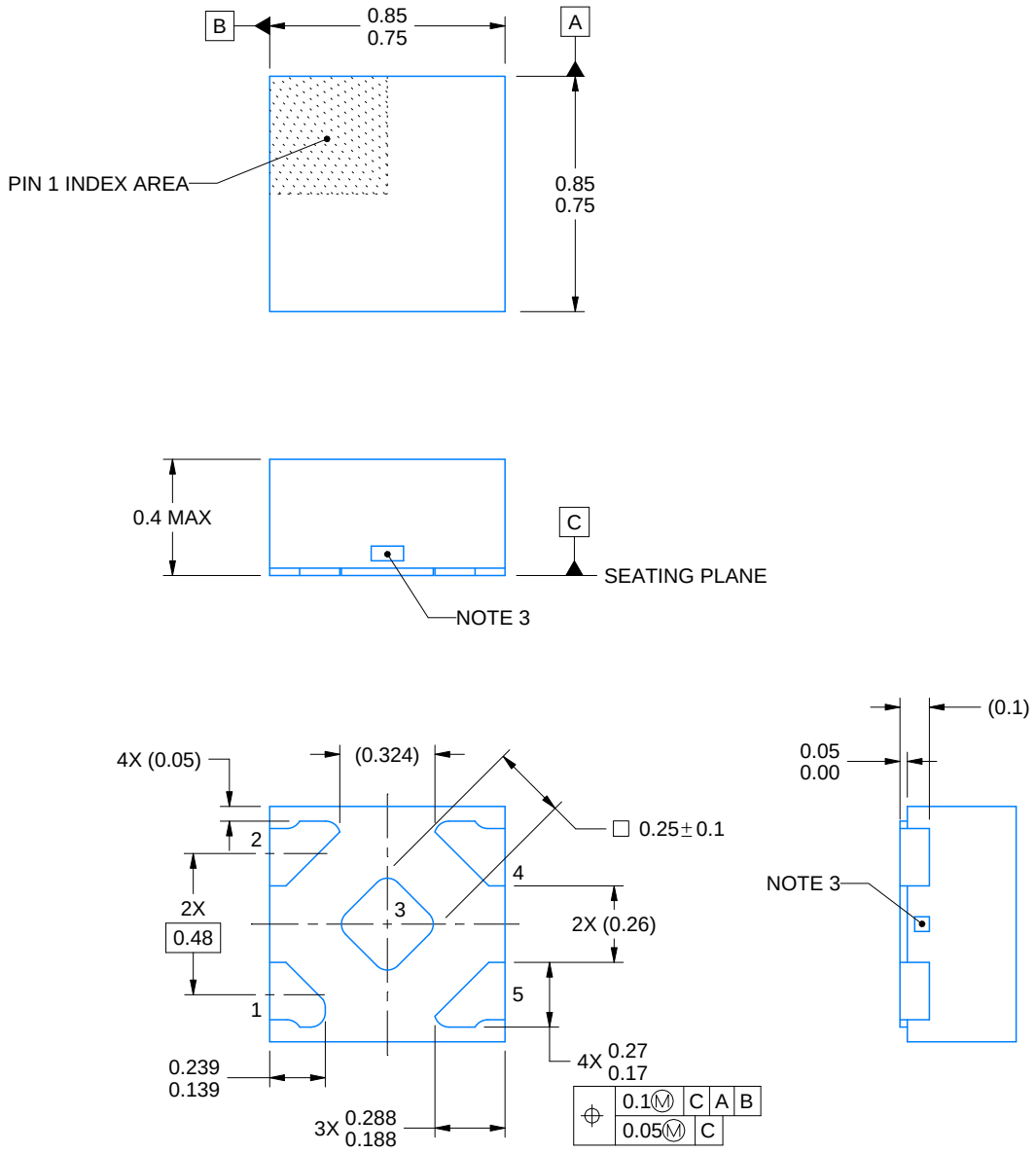
4211218-3/D

# PACKAGE OUTLINE

## DPW0005A

## X2SON - 0.4 mm max height

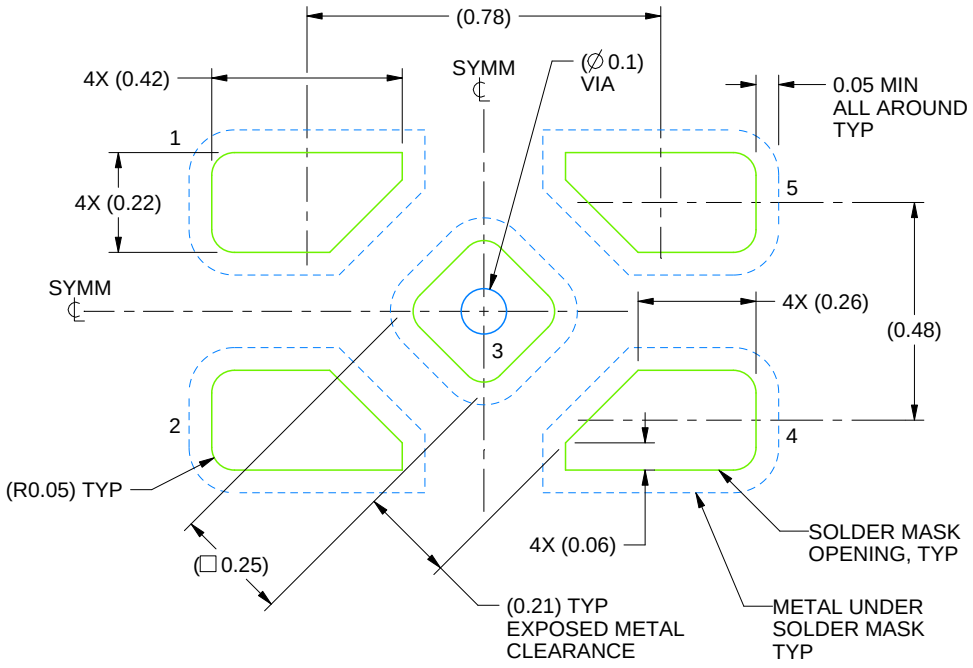
PLASTIC SMALL OUTLINE - NO LEAD




4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

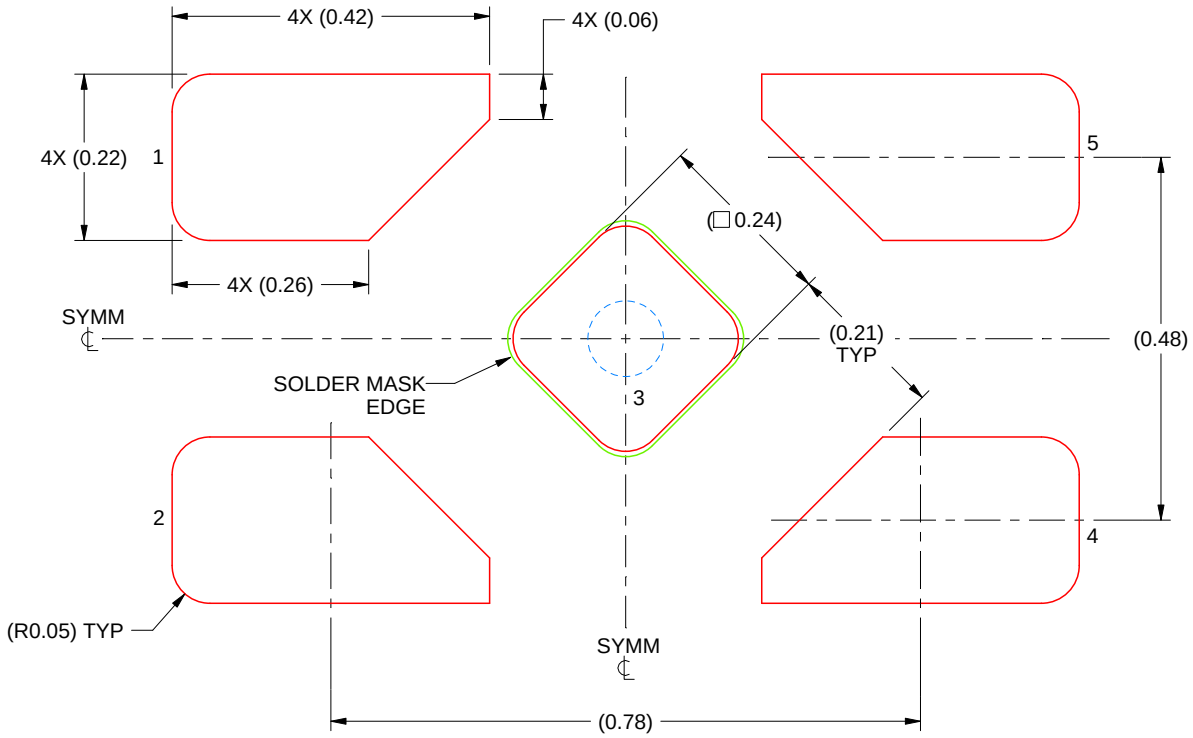
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DPW0005A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

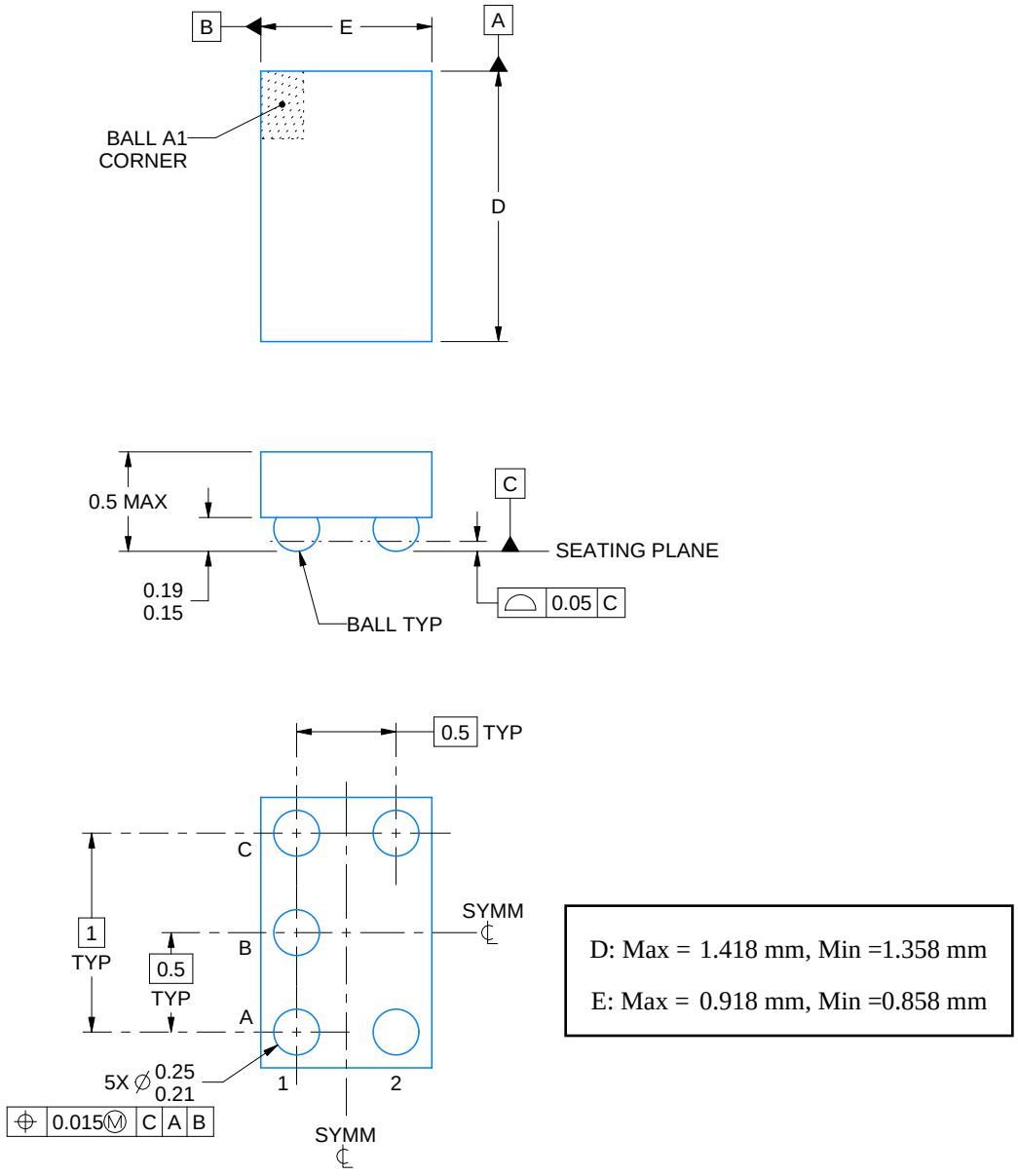
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## YZP0005

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



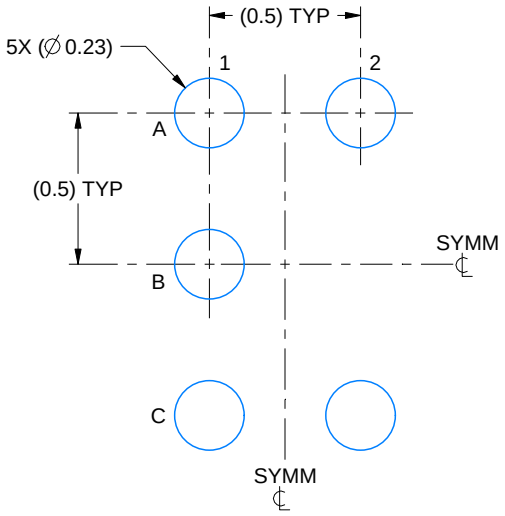

D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

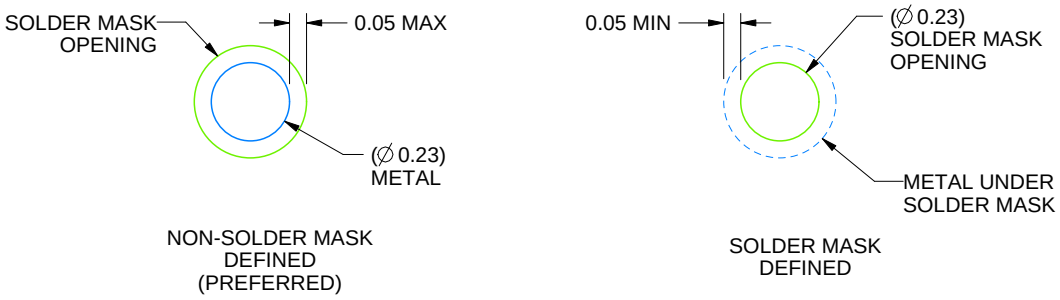
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X

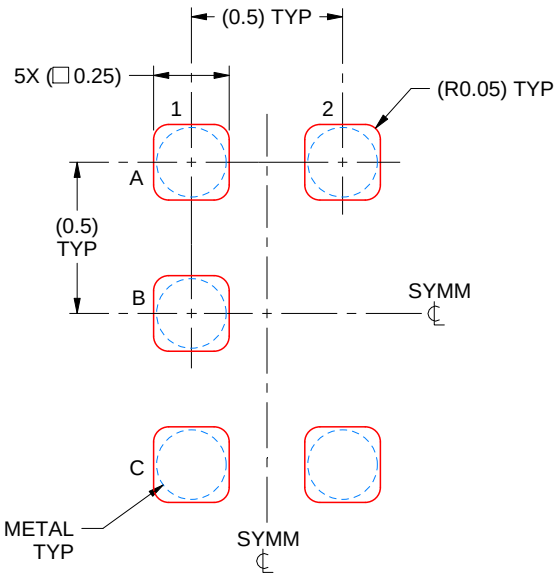



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

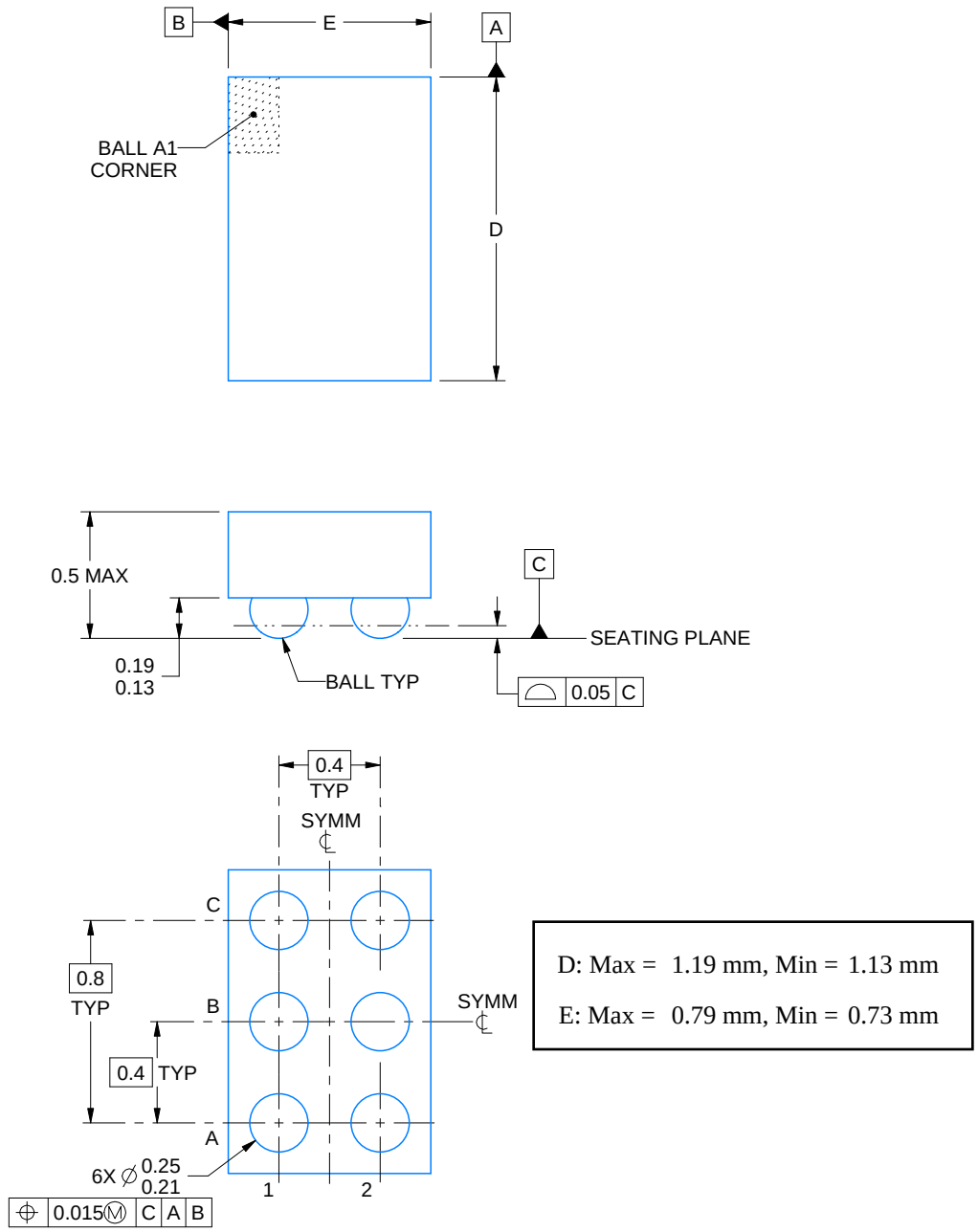
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## YFP0006

## DSBGA - 0.5 mm max height

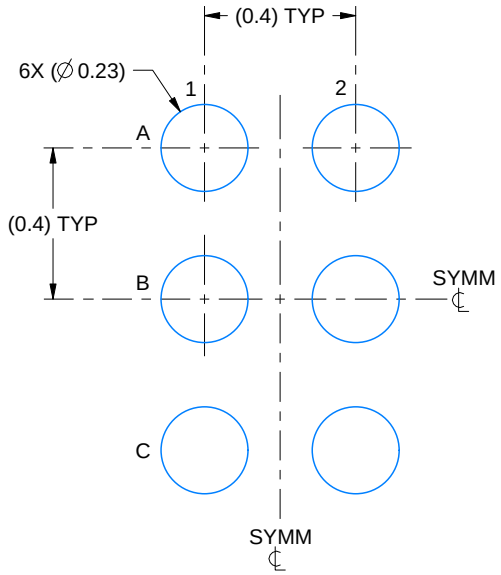
DIE SIZE BALL GRID ARRAY



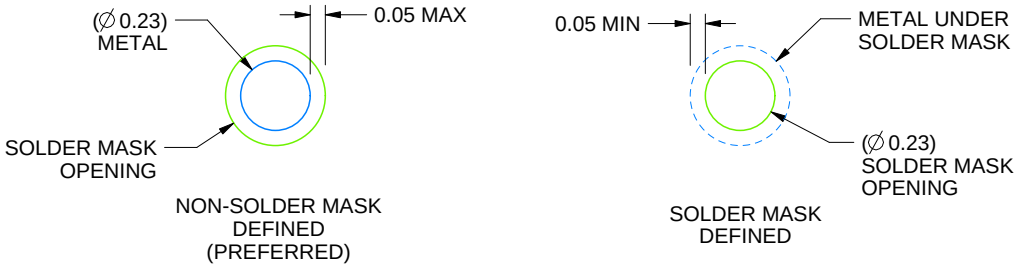

4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:50X

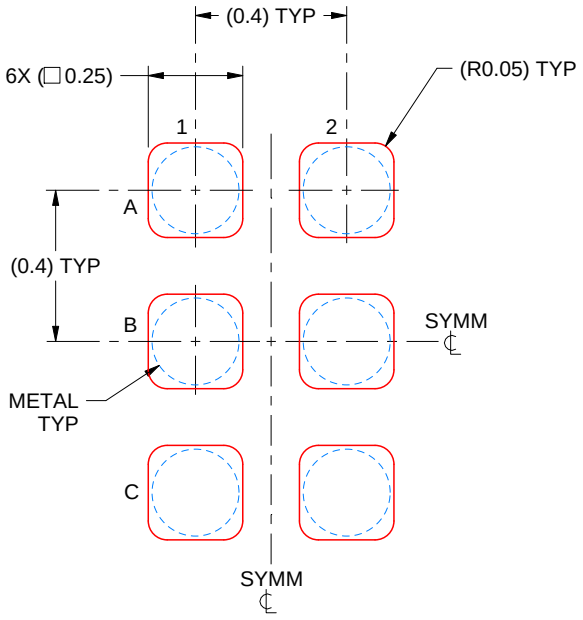



SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

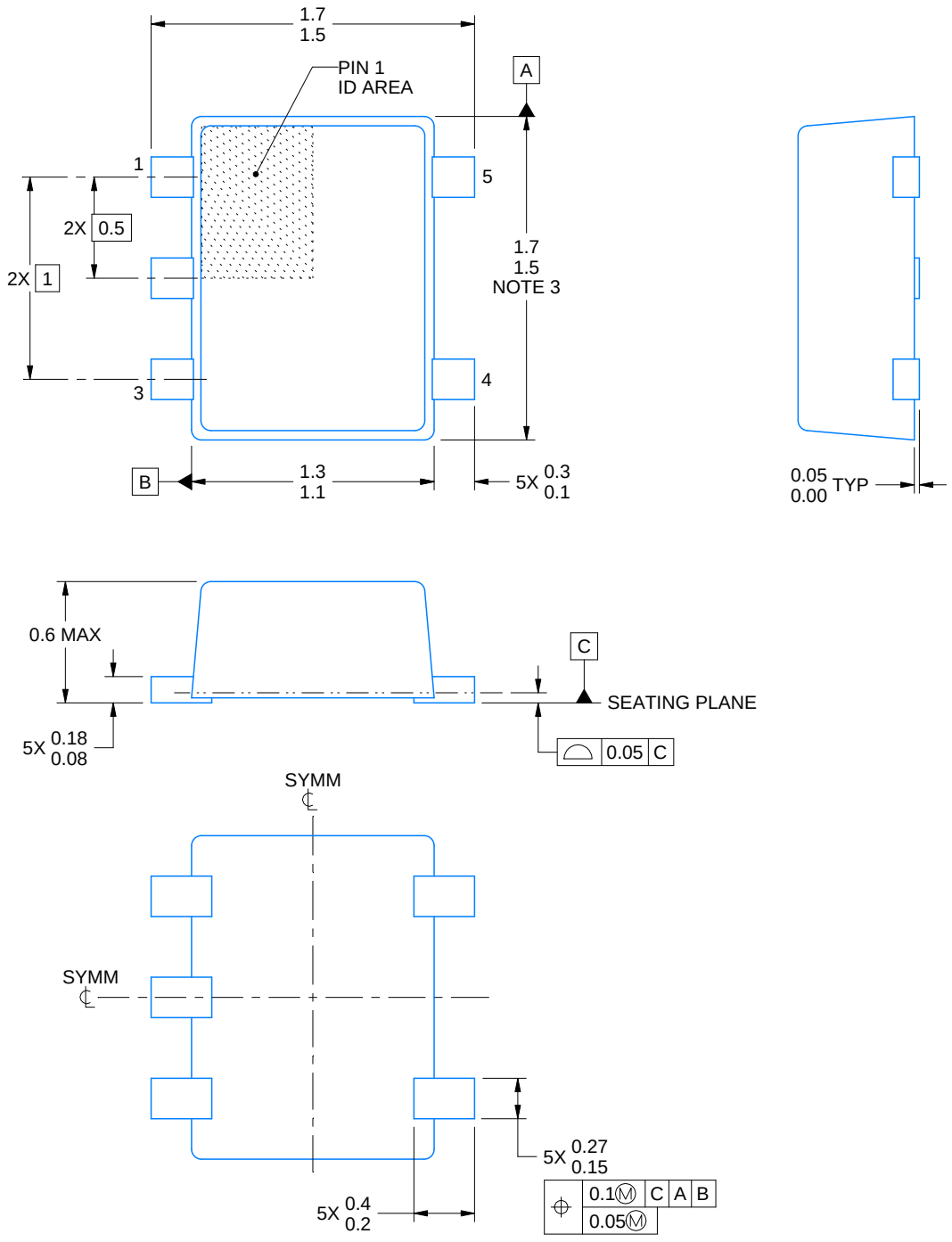
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DRL0005A

## SOT - 0.6 mm max height

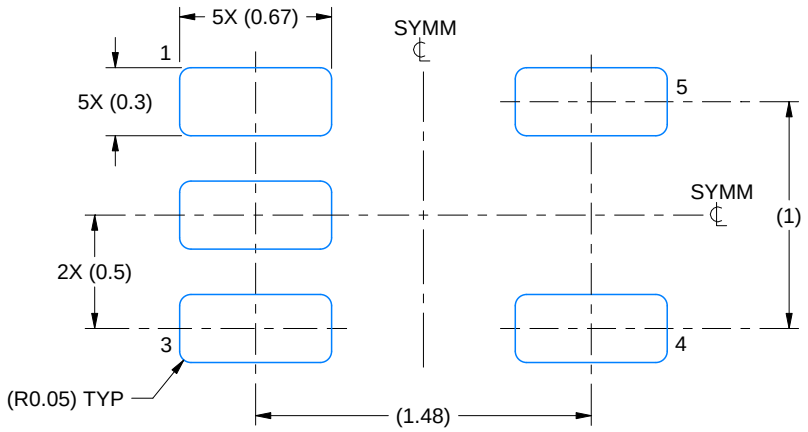
PLASTIC SMALL OUTLINE



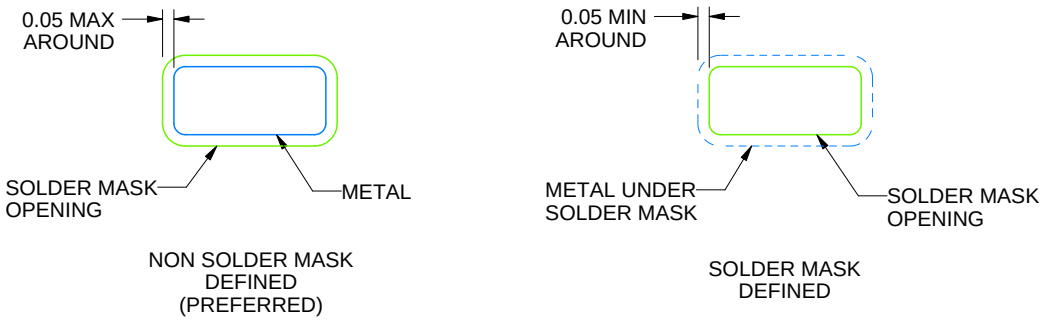

4220753/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1




LAND PATTERN EXAMPLE
SCALE:30X

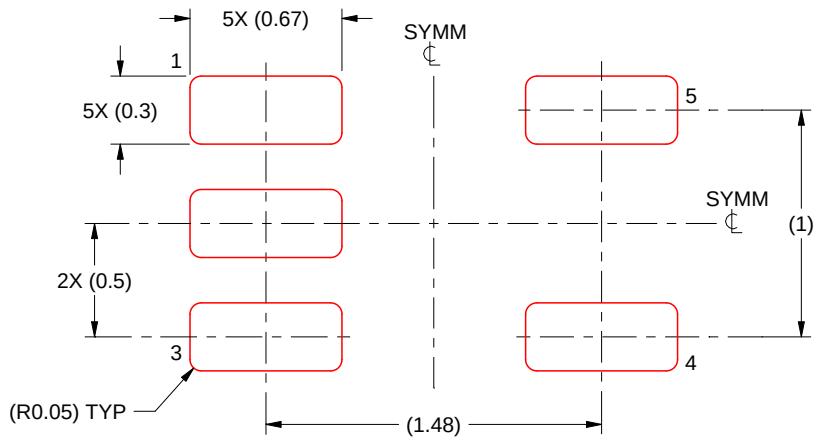



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

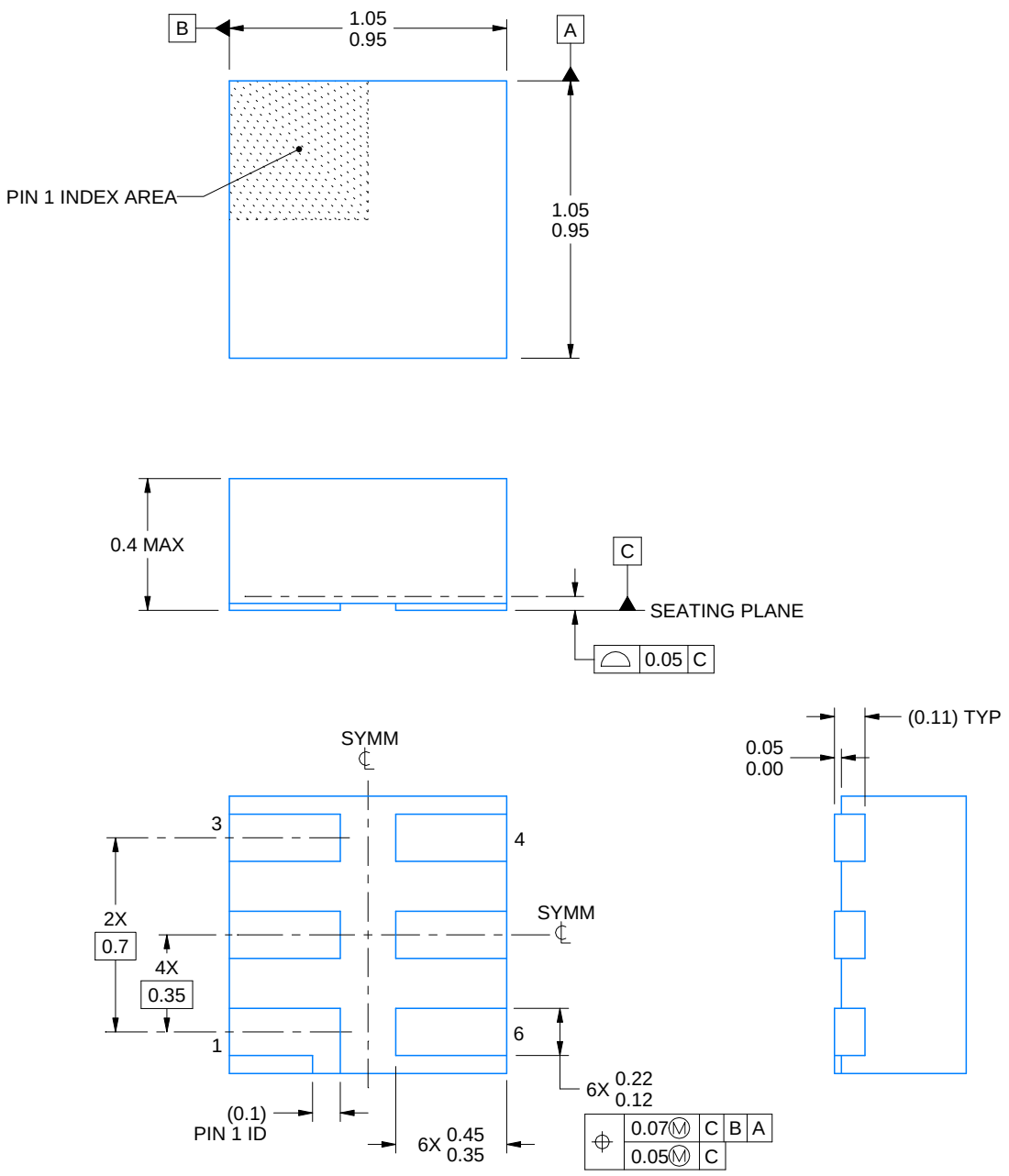
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DSF0006A

## X2SON - 0.4 mm max height

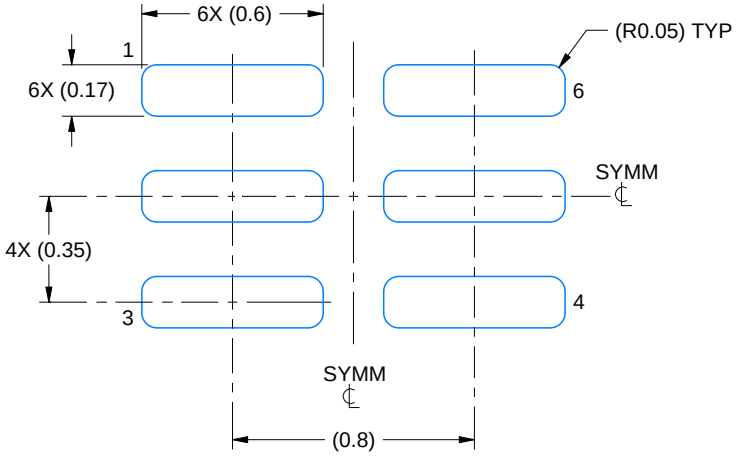
PLASTIC SMALL OUTLINE - NO LEAD



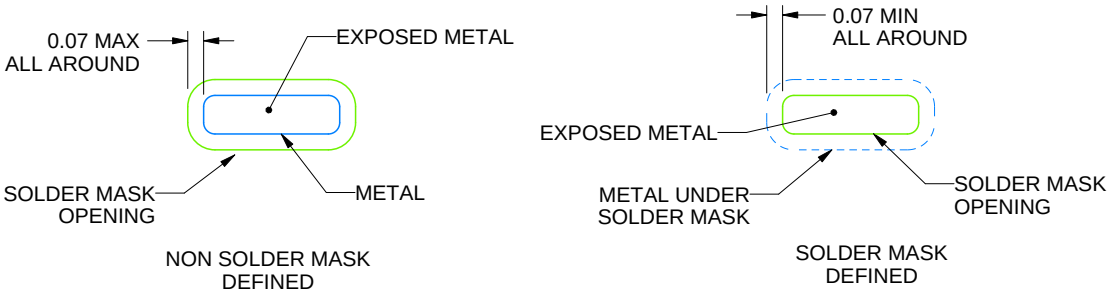

4220597/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

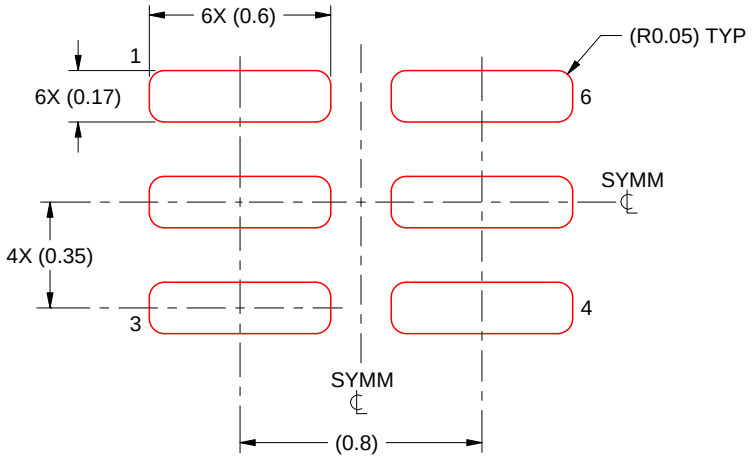
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



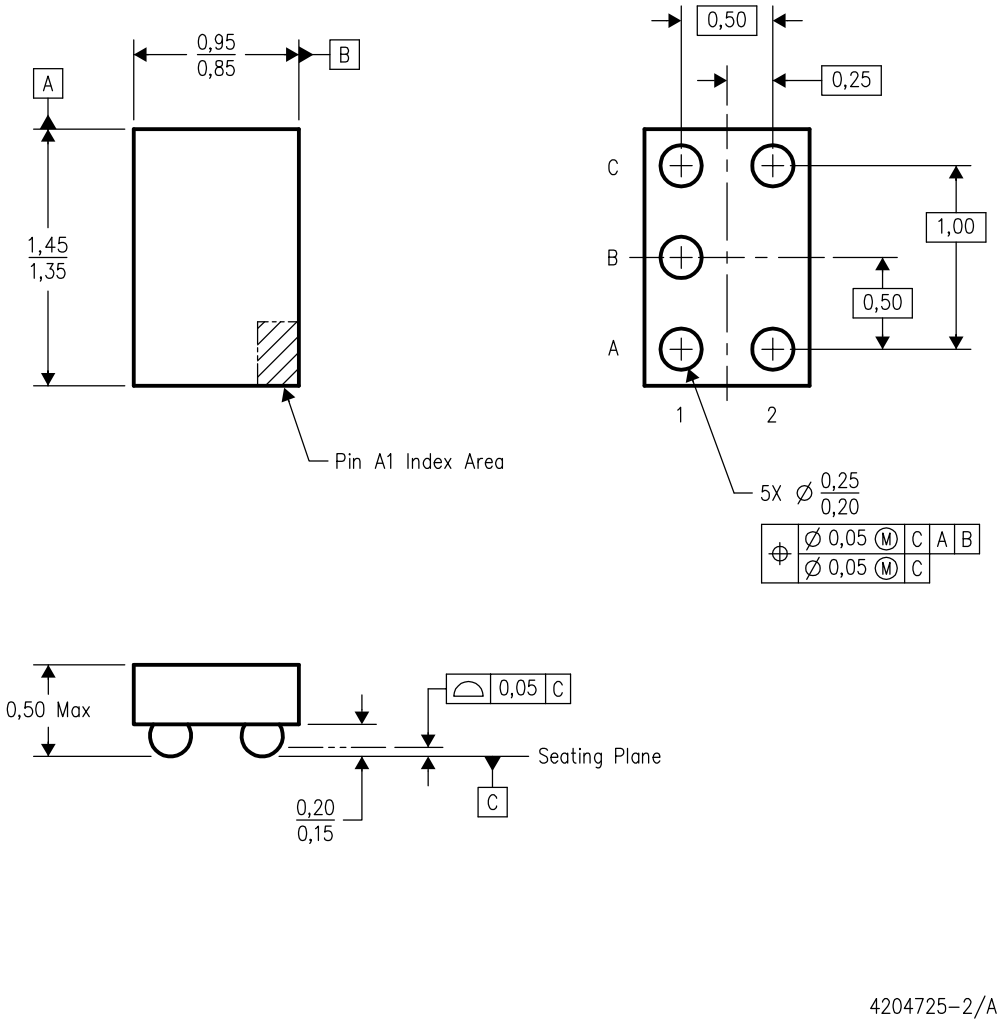

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

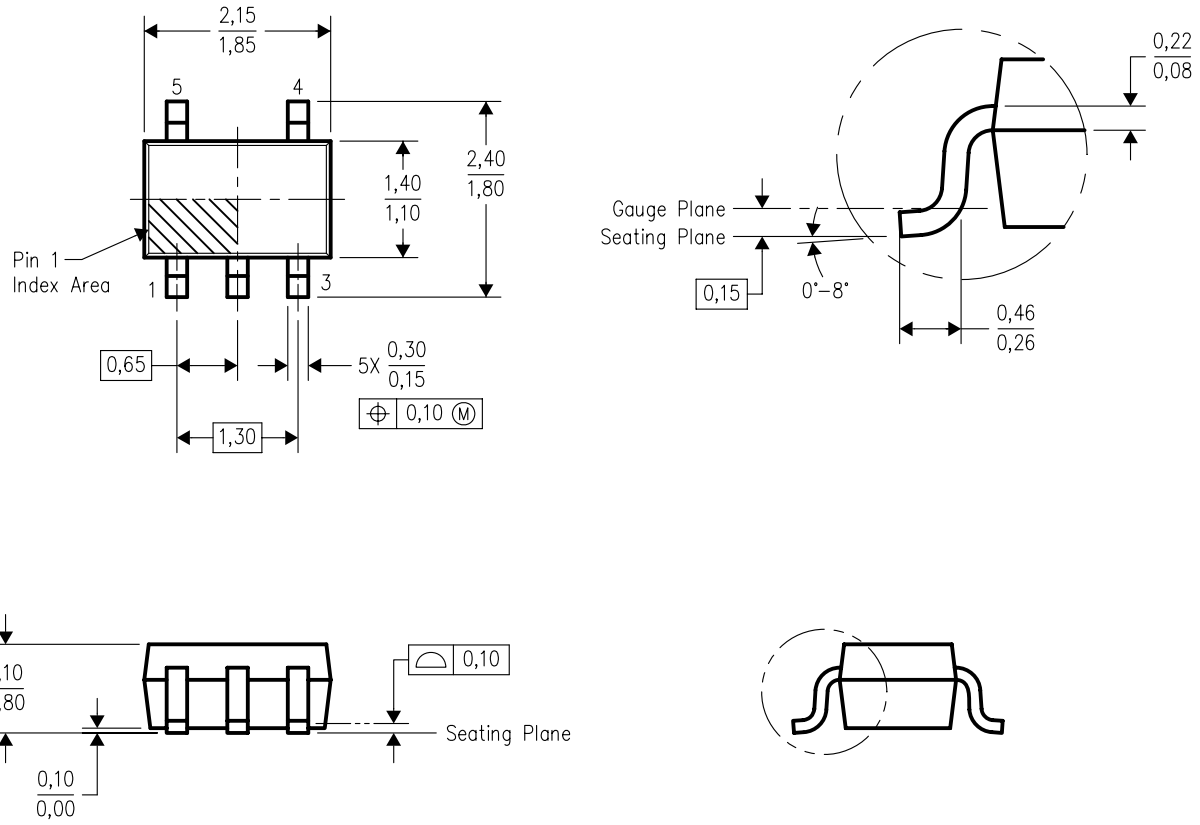
YEP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead–free.

**NanoStar is a trademark of Texas Instruments.**

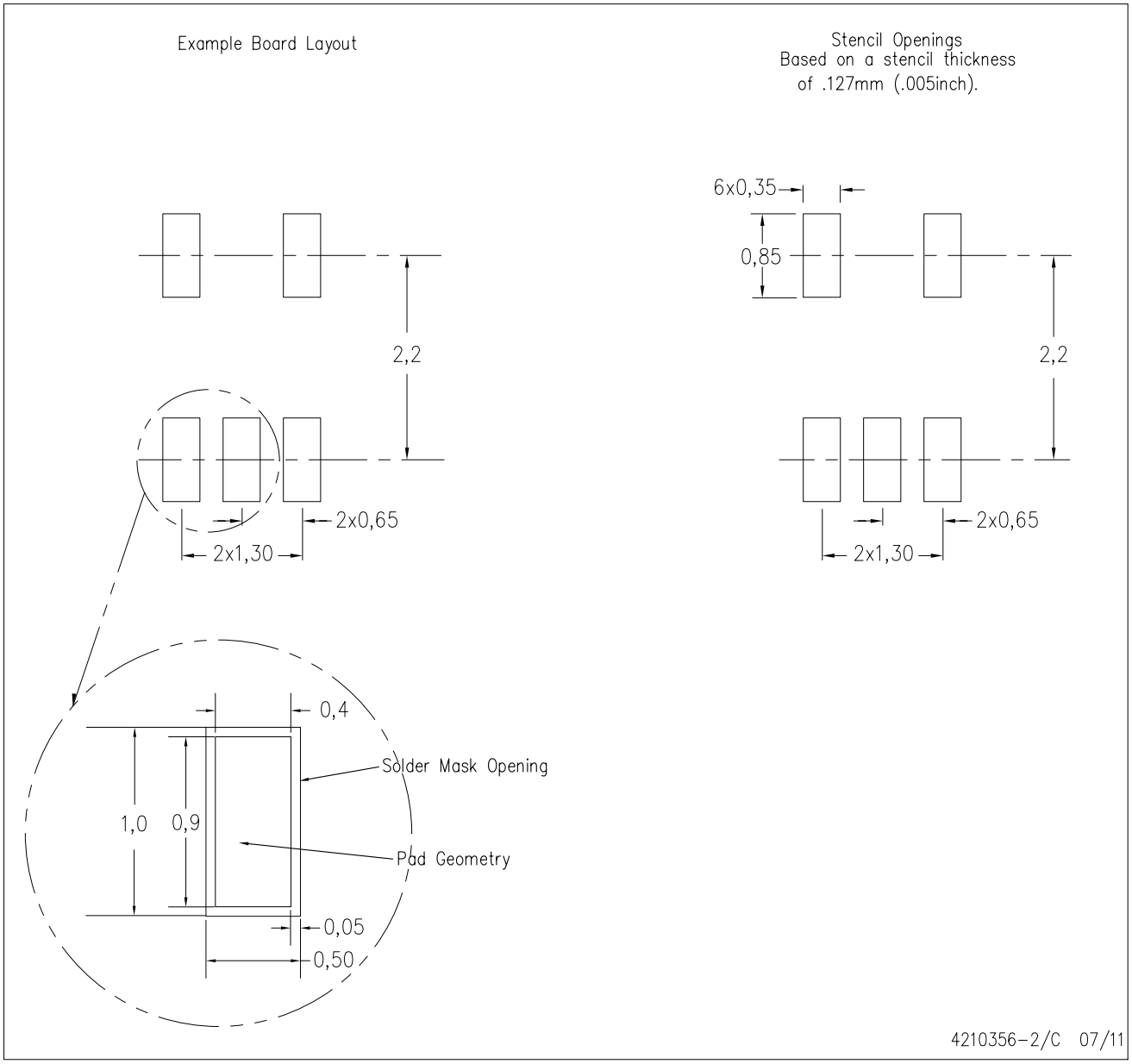
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

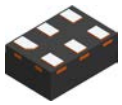
# DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

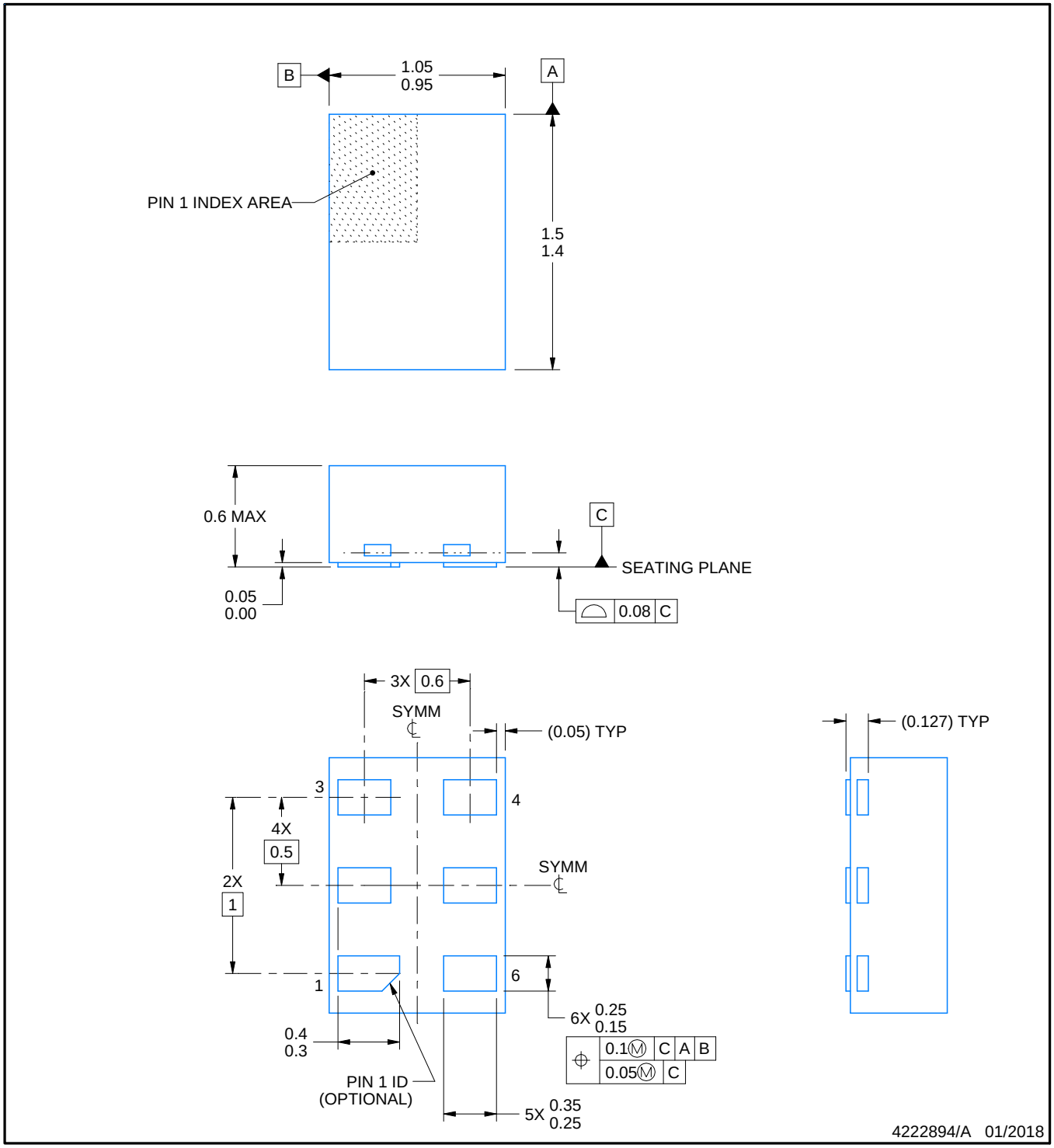
# DRY0006A



# PACKAGE OUTLINE

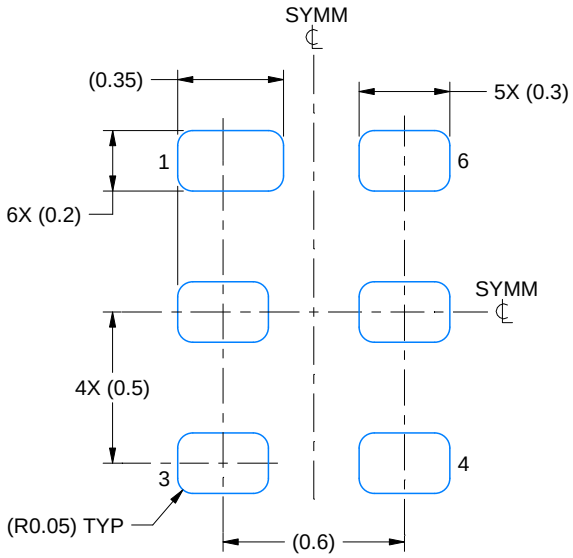
## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

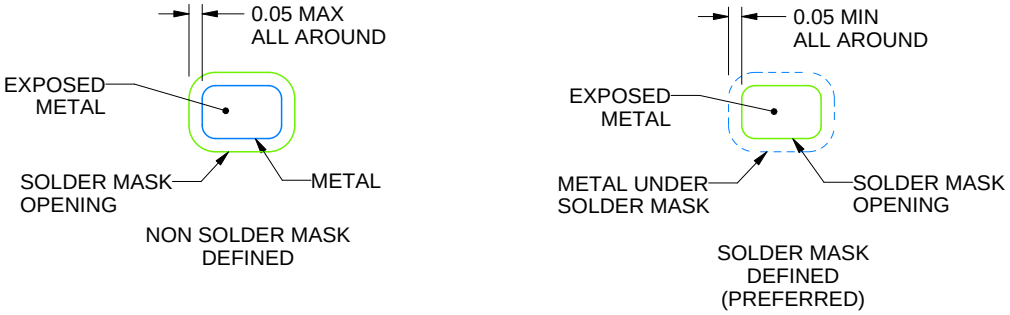



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

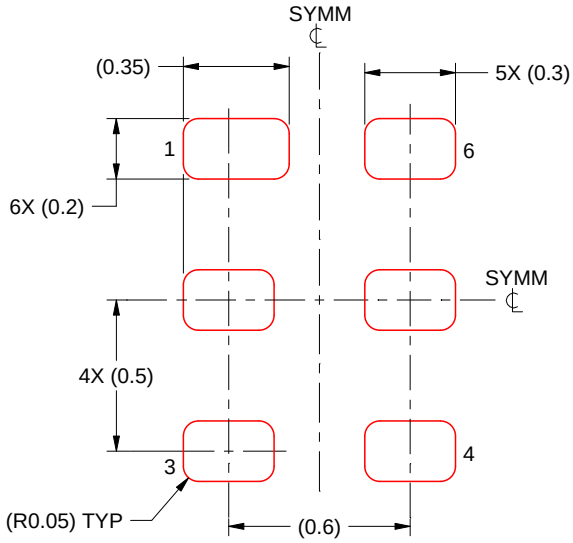
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

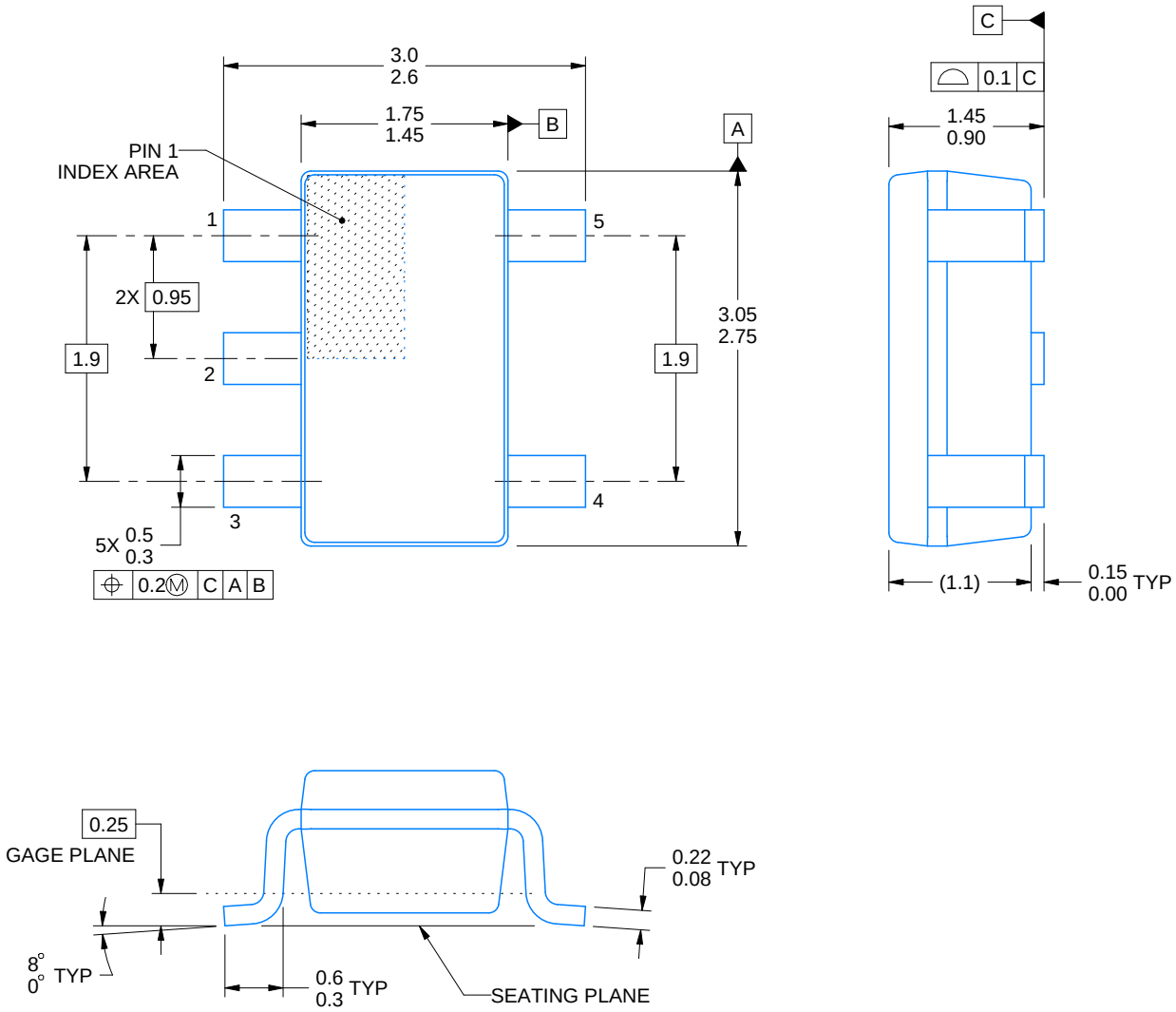
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

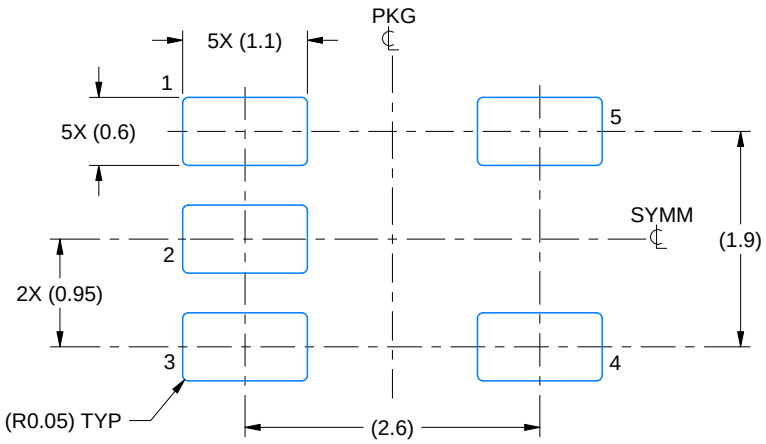
SMALL OUTLINE TRANSISTOR



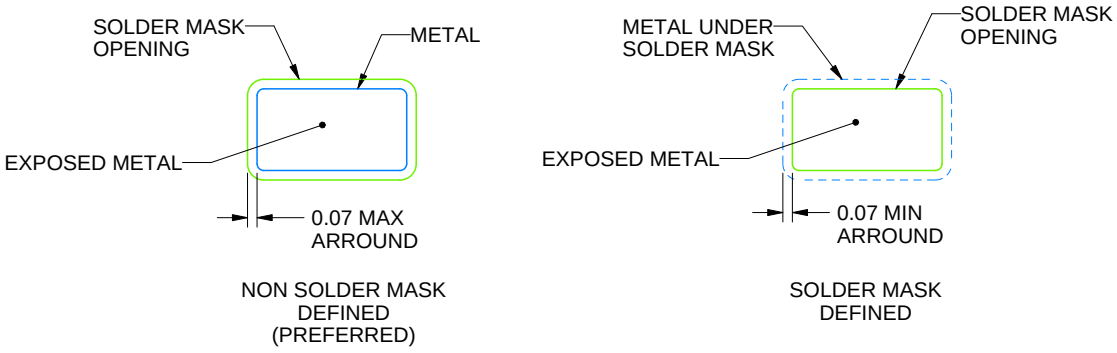

4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

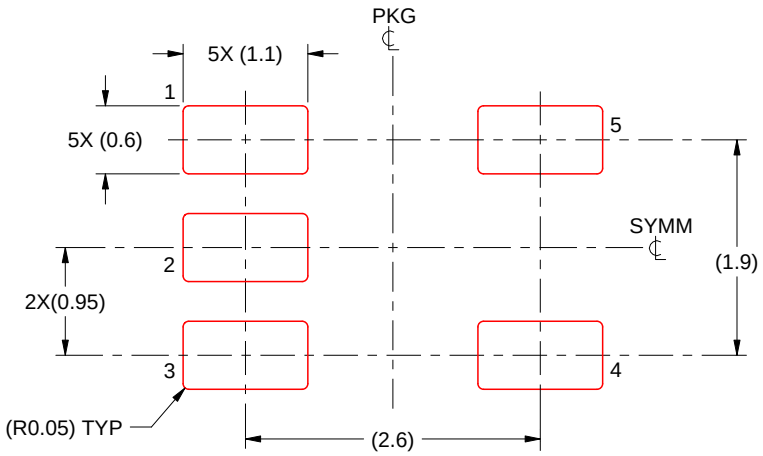



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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