

## TPL0401x-10-Q1 具有 I<sup>2</sup>C 接口的 128 抽头单通道数字电位计

### 1 特性

- 单通道 128 位置分辨率
- 10kΩ 端到端电阻选项
- 低温度系数: 22ppm/°C
- I<sup>2</sup>C 串行接口
- 2.7V 至 5.5V 单电源运行
- ±20% 电阻容差
- A 和 B 版本具有不同的 I<sup>2</sup>C 地址
- L 端子内部连接至 GND
- 工作温度: -40°C 至 +125°C
- 采用行业标准 SC70 封装
- 根据 JESD 22 测试得出的静电放电 (ESD) 性能
  - 2000V 人体放电模型 (A114-B, II 类)

### 2 应用

- 机械电位计的替代产品
- 可调电源
- 可调增益放大器和偏移修剪
- 设定点阈值精密校准
- 传感器微调和校准

### 3 说明

TPL0401x-10-Q1 器件是一款具有 128 个抽头位置的单通道线性抽头数字电位计。TPL0401x-10-Q1 的低电平端子内部连接至 GND。可使用 I<sup>2</sup>C 接口来调节抽头位置。TPL0401x-10-Q1 采用 6 引脚 SC70 封装, 额定温度范围为 -40°C 至 +125°C。此部件有一个 10kΩ 端到端电阻, 工作电源电压范围为 2.7V 至 5.5V。这类产品广泛用于为低功耗 DDR3 存储器设定电压基准。

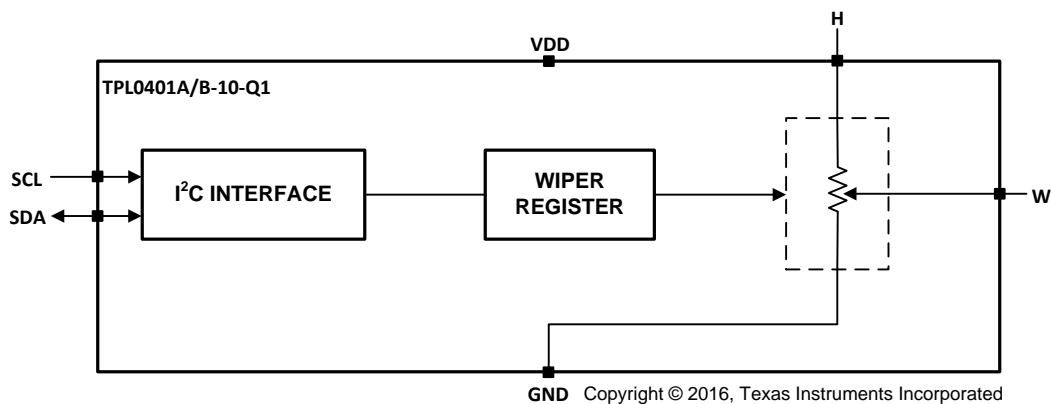
TPL0401x-10-Q1 的低电平端子内部连接至 GND。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TPL0401A-10-Q1 TPL0401B-10-Q1	SC70 (6)	2.00mm × 1.25mm

(1) 要了解所有可用封装, 请参见数据表末尾的可订购产品附录。

简化电路原理图



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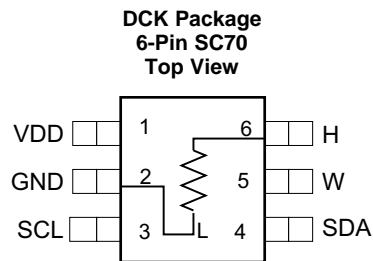
## 4 修订历史记录

日期	修订版本	注释
2016 年 11 月	*	首次发布。

## 5 Device Comparison Table

PART NUMBER	END-TO-END RESISTANCE	I <sup>2</sup> C ADDRESS
TPL0401A-10-Q1	10 kΩ	010 1110 (0x2E)
TPL0401B-10-Q1	10 kΩ	011 1110 (0x3E)

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD	Power	Positive supply voltage
2	GND	—	Ground
3	SCL	I	I <sup>2</sup> C Clock
4	SDA	I/O	I <sup>2</sup> C Data
5	W	I/O	Wiper terminal
6	H	I/O	High terminal
—	L	I/O	Low terminal (Internally connected to GND)

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage   V <sub>DD</sub> to GND	-0.3	7	V
I <sub>H</sub> , I <sub>L</sub> , I <sub>W</sub>	Continuous current		±5	mA
V <sub>I</sub>	Digital input pins (SDA, SCL)	-0.3	V <sub>DD</sub> + 0.3	V
	Potentiometer pins (H, W)	-0.3	V <sub>DD</sub> + 0.3	
T <sub>J(MAX)</sub>	Maximum junction temperature		130	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2500
		Charged-device model (CDM), per AEC Q100-011	±1000

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage	2.7	5.5	V
V <sub>W</sub> , V <sub>H</sub> , SDA, SCL	Terminal voltage	0	V <sub>DD</sub>	V
V <sub>IH</sub>	Voltage input high ( SCL, SDA )	0.7 × V <sub>DD</sub>	V <sub>DD</sub>	V
V <sub>IL</sub>	Voltage input low ( SCL, SDA )	0	0.3 × V <sub>DD</sub>	V
I <sub>W</sub>	Wiper current	-2	2	mA
T <sub>A</sub>	Ambient operating temperature	-40	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPL0401x-10-Q1	UNIT
		DCK (SC70)	
		6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	234	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	110.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	79	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	77	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.5 Electrical Characteristics

Typical values are specified at 25°C and V<sub>DD</sub> = 3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>TOTAL</sub>	End-to-end resistance	8	10	12	kΩ
R <sub>H</sub>	Terminal resistance		100	200	Ω
R <sub>W</sub>	Wiper resistance		35	100	Ω

## Electrical Characteristics (continued)

Typical values are specified at 25°C and  $V_{DD} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_H$	Terminal capacitance			10		pF
$C_W$	Wiper capacitance			11		pF
$TC_R$	Resistance temperature coefficient			22		ppm/°C
$I_{DD(STBY)}$	$V_{DD}$ standby current	–40°C to +105°C			0.5	μA
		–40°C to +125°C			1.5	
$I_{IN-DIG}$	Digital pins leakage current (SCL, SDA Inputs)		–2.5		2.5	μA
<b>SERIAL INTERFACE SPECS (SDA, SCL)</b>						
$V_{IH}$	Input high voltage		$0.7 \times V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input low voltage		0		$0.3 \times V_{DD}$	V
$V_{OL}$	Output low voltage	SDA Pin, $I_{OL} = 4\text{ mA}$			0.4	V
$C_{IN}$	Pin capacitance	SCL, SDA Inputs		7		pF
<b>VOLTAGE DIVIDER MODE (<math>V_H = V_{DD}</math>, <math>V_W = \text{Not Loaded}</math>)</b>						
$INL^{(1)(2)}$	Integral non-linearity		–0.5		0.5	LSB
$DNL^{(3)(2)}$	Differential non-linearity		–0.25		0.25	LSB
$ZS_{ERROR}^{(4)(5)}$	Zero-scale error		0	0.75	1.5	LSB
$FS_{ERROR}^{(6)(5)}$	Full-scale error		–1.5	–0.75	0	LSB
$TC_V$	Ratiometric temperature coefficient	Wiper set at mid-scale		4		ppm/°C
BW	Bandwidth	Wiper set at mid-scale, $C_{LOAD} = 10\text{ pF}$		2862		kHz
$T_{SW}$	Wiper settling time	See <a href="#">Figure 10</a>		0.152		μs
THD+N	Total harmonic distortion	$V_H = 1\text{ V}_{RMS}$ at 1 kHz, measurement at W		0.03		%
<b>RHEOSTAT MODE (<math>V_H = V_{DD}</math>, <math>V_W = \text{Not Loaded}</math>)</b>						
$RINL^{(7)(8)}$	Rheostat mode integral non-linearity		–1		1	LSB
$RDNL^{(9)(8)}$	Rheostat mode differential non-linearity		0.5		0.5	LSB
$R_{OFFSET}^{(10)(11)}$	Rheostat-mode zero-scale error		0	0.75	2	LSB

(1)  $INL = ((V_{MEAS[code\ x]} - V_{MEAS[code\ 0]}) / LSB) - [code\ x]$

(2)  $LSB = (V_{MEAS[code\ 127]} - V_{MEAS[code\ 0]}) / 127$

(3)  $DNL = ((V_{MEAS[code\ x]} - V_{MEAS[code\ x-1]}) / LSB) - 1$

(4)  $ZS_{ERROR} = V_{MEAS[code\ 0]} / IDEAL\_LSB$

(5)  $IDEAL\_LSB = V_H / 128$

(6)  $FS_{ERROR} = ((V_{MEAS[code\ 127]} - V_H) / IDEAL\_LSB) + 1$

(7)  $RINL = ((R_{MEAS[code\ x]} - R_{MEAS[code\ 0]}) / RLSB) - [code\ x]$

(8)  $RLSB = (R_{MEAS[code\ 127]} - R_{MEAS[code\ 0]}) / 127$

(9)  $RDNL = ((R_{MEAS[code\ x]} - R_{MEAS[code\ x-1]}) / RLSB) - 1$

(10)  $R_{OFFSET} = R_{MEAS[code\ 0]} / IDEAL\_RLSB$

(11)  $IDEAL\_RLSB = R_{TOT} / 128$

## 7.6 Timing Requirements

		MIN	MAX	UNIT
<b>STANDARD MODE</b>				
$f_{SCL}$	I <sup>2</sup> C Clock frequency	0	100	kHz
$t_{SCH}$	I <sup>2</sup> C Clock high time	4		μs
$t_{SCL}$	I <sup>2</sup> C Clock low time	4.7		μs
$t_{sp}$	I <sup>2</sup> C Spike time	0	50	ns
$t_{SDS}$	I <sup>2</sup> C Serial data setup time	250		ns

### Timing Requirements (continued)

		MIN	MAX	UNIT
$t_{SDH}$	I <sup>2</sup> C Serial data hold time	0		ns
$t_{ICR}$	I <sup>2</sup> C Input rise time		1000	ns
$t_{ICF}$	I <sup>2</sup> C Input fall time		300	ns
$t_{OCF}$	I <sup>2</sup> C Output fall time, 10 pF to 400 pF bus		300	ns
$t_{BUF}$	I <sup>2</sup> C Bus free time between stop and start	4.7		μs
$t_{STS}$	I <sup>2</sup> C Start or repeater start condition setup time	4.7		μs
$t_{STH}$	I <sup>2</sup> C Start or repeater start condition hold time	4		μs
$t_{SPS}$	I <sup>2</sup> C Stop condition setup time	4		μs
$t_{VD(DATA)}$	Valid data time, SCL low to SDA output valid		1	μs
$t_{VD(ACK)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1	μs
<b>FAST MODE</b>				
$f_{SCL}$	I <sup>2</sup> C Clock frequency	0	400	kHz
$t_{SCH}$	I <sup>2</sup> C Clock high time	0.6		μs
$t_{SCL}$	I <sup>2</sup> C Clock low time	1.3		μs
$t_{sp}$	I <sup>2</sup> C Spike time	0	50	ns
$t_{SDS}$	I <sup>2</sup> C Serial data setup time	100		ns
$t_{SDH}$	I <sup>2</sup> C Serial data hold time	0		ns
$t_{ICR}$	I <sup>2</sup> C Input rise time	20	300	ns
$t_{ICF}$	I <sup>2</sup> C Input fall time	$20 \times (V_{DD} / 5.5)$	300	ns
$t_{OCF}$	I <sup>2</sup> C Output fall time, 10 pF to 400 pF bus	$(V_{DD} / 5.5) \times 20$	300	ns
$t_{BUF}$	I <sup>2</sup> C Bus free time between stop and start	1.3		μs
$t_{STS}$	I <sup>2</sup> C Start or repeater start condition setup time	1.3		μs
$t_{STH}$	I <sup>2</sup> C Start or repeater start condition hold time	0.6		μs
$t_{SPS}$	I <sup>2</sup> C Stop condition setup time	0.6		μs
$t_{VD(DATA)}$	Valid data time, SCL low to SDA output valid		1	μs
$t_{VD(ACK)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1	μs

### 7.7 Typical Characteristics

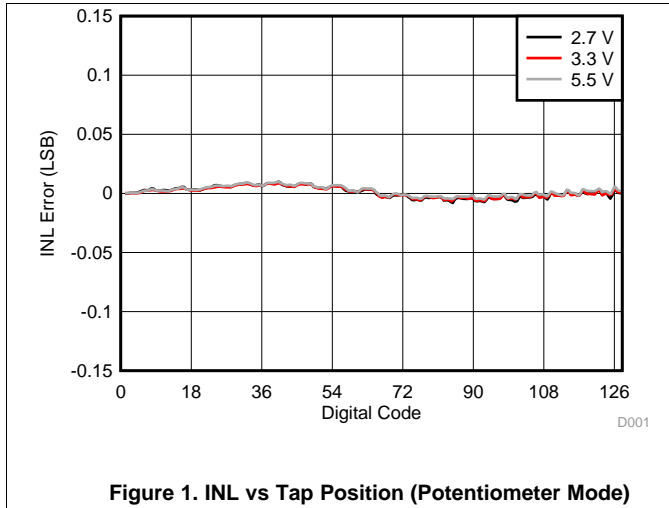


Figure 1. INL vs Tap Position (Potentiometer Mode)

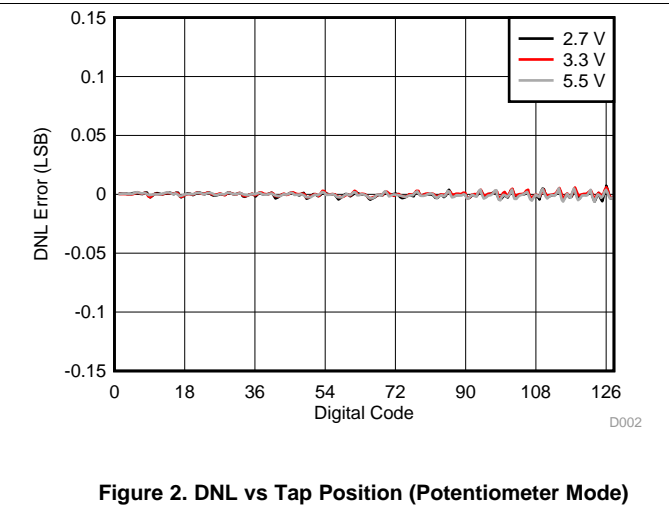


Figure 2. DNL vs Tap Position (Potentiometer Mode)

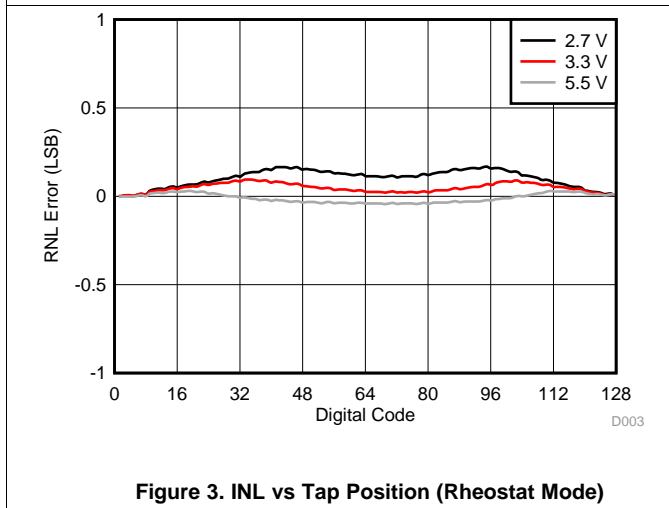


Figure 3. INL vs Tap Position (Rheostat Mode)

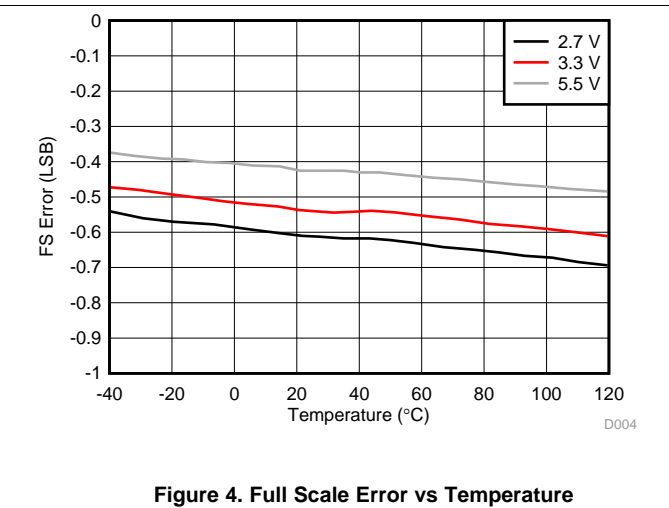


Figure 4. Full Scale Error vs Temperature

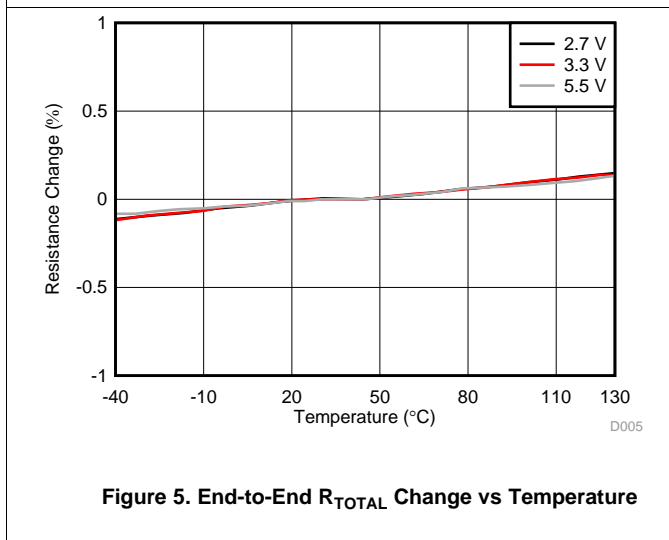


Figure 5. End-to-End  $R_{TOTAL}$  Change vs Temperature

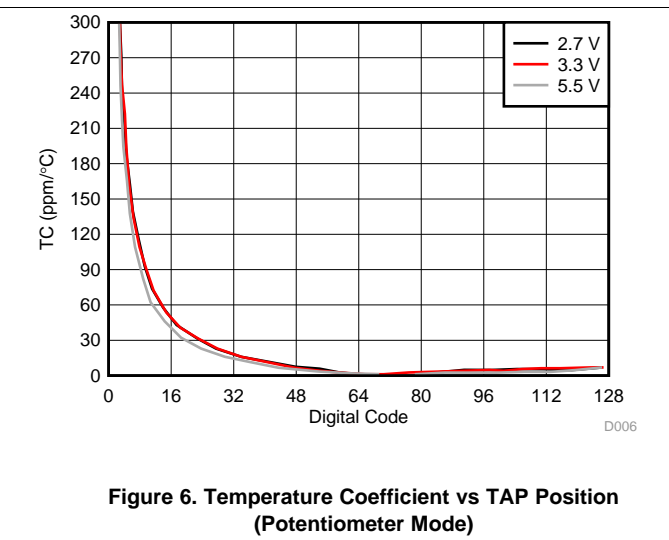
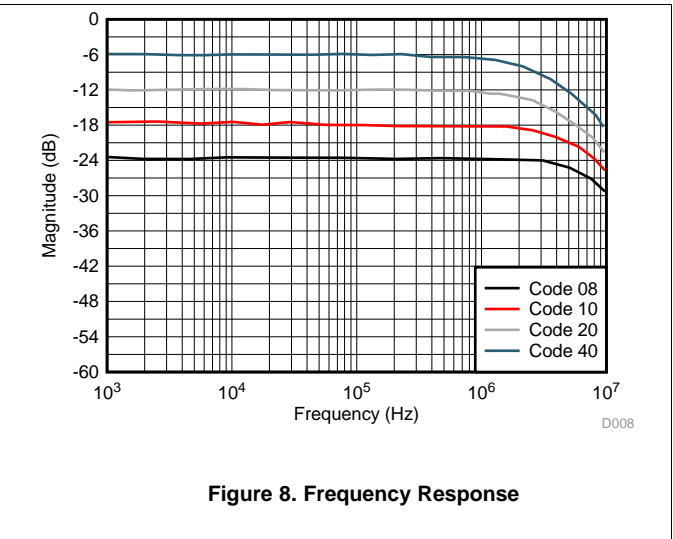
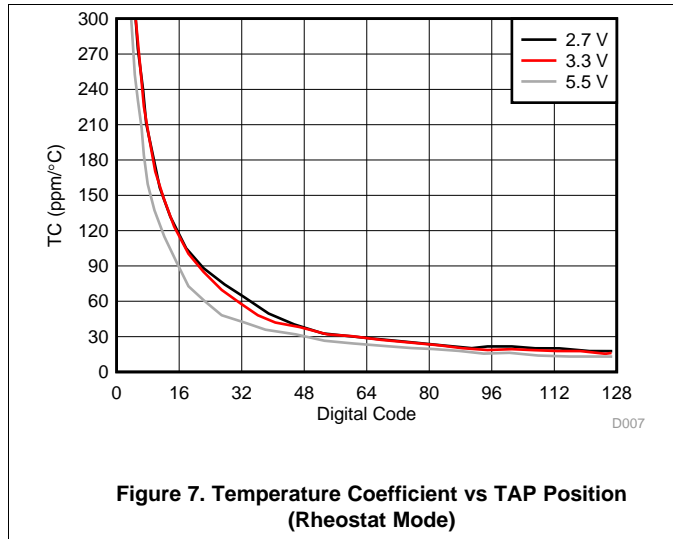
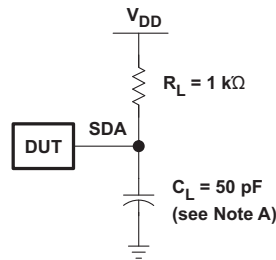


Figure 6. Temperature Coefficient vs TAP Position (Potentiometer Mode)

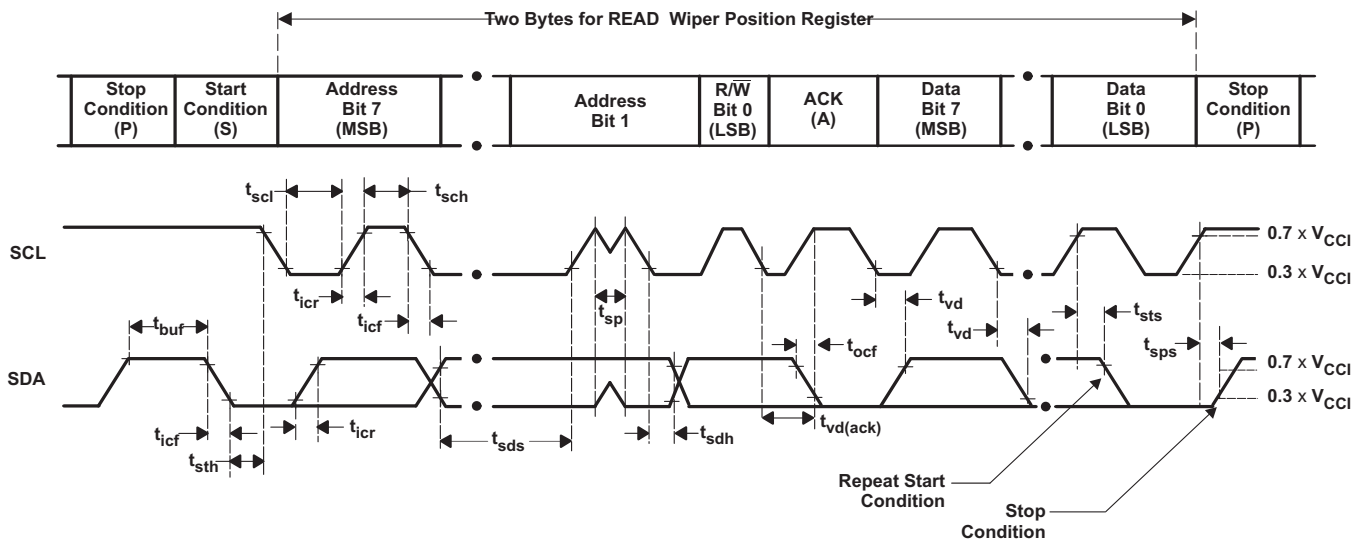
Typical Characteristics (continued)



## 8 Parameter Measurement Information



SDA LOAD CONFIGURATION



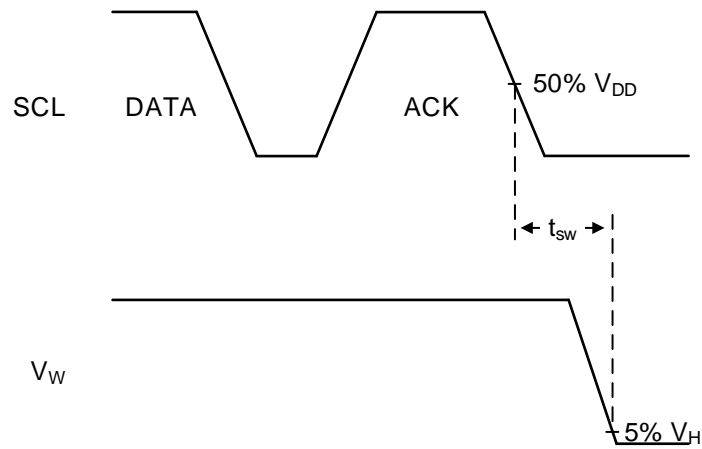
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2	Wiper Position Data

- A.  $C_L$  includes probe and jig capacitance.  $t_{ocf}$  is measured with  $C_L$  of 10 pF or 400 pF.
- B. All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 9. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms

### Parameter Measurement Information (continued)



- A. Code change is from 0x40 to 0x00
- B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.

**Figure 10. Switch Time Waveform (t<sub>sw</sub>)**

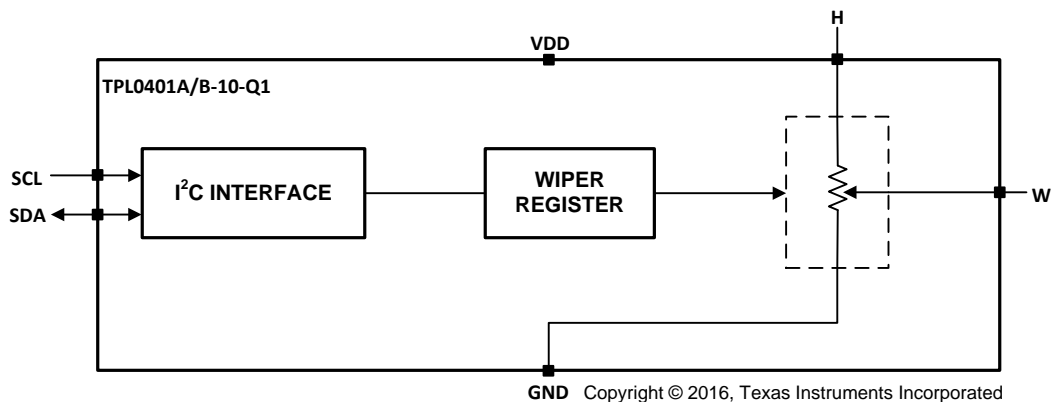
## 9 Detailed Description

### 9.1 Overview

The TPL0401x-10-Q1 has a single linear-taper digital potentiometer with 128 wiper positions and an end-to-end resistance of 10 k $\Omega$ . The potentiometer can be used as a three-terminal potentiometer. The main operation of TPL0401x-10-Q1 is in voltage divider mode.

The low (L) terminal of the TPL0401x-10-Q1 is tied directly to GND. The high (H) and low (GND) terminals of TPL0401-10-Q1 are equivalent to the fixed terminals of a mechanical potentiometer. The H terminal must have a higher voltage than the low terminal (GND). The position of the wiper (W) terminal is controlled by the value in the Wiper Resistance (WR) 8-bit register. When the WR register contains all zeroes (zero-scale), the wiper terminal is closest to its L terminal. As the value of the WR register increases from all zeroes to all ones (full-scale), the wiper moves from the position closest to the GND terminal to the position closest to the H terminal. At the same time, the resistance between W and GND increases, whereas the resistance between W and H decreases.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

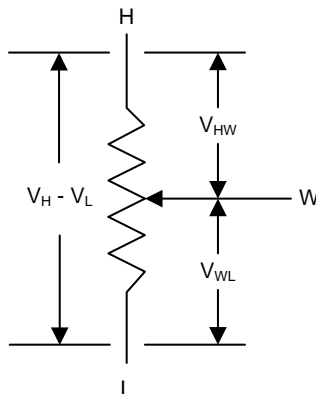
The TPL0401x-10-Q1 device is a single-channel, linear taper digital potentiometer with 128 wiper positions. Default power up state for the TPL0401x-10-Q1 is mid code (0x40). The TPL0401x-10-Q1 has the low terminal connected to GND internally. The position of the wiper can be adjusted using an I<sup>2</sup>C interface. The TPL0401x-10-Q1 is available in a 6-pin SOT package with a specified temperature range of –40°C to +125°C. The part has a 10-k $\Omega$  end-to-end resistance and can operate with a supply voltage range of 2.7 V to 5.5 V. This kind of product is widely used in setting the voltage reference for low power DDR3 memory. The TPL0401x-10-Q1 has the low terminal internal and connected to GND.

### 9.4 Device Functional Modes

#### 9.4.1 Voltage Divider Mode

The digital potentiometer generates a voltage divider when all three terminals are used. The voltage divider at wiper-to-H and wiper-to-GND is proportional to the input voltage at H to L (see [Figure 11](#)).

## Device Functional Modes (continued)



**Figure 11. Equivalent Circuit for Voltage Divider Mode**

For example, connecting terminal H to 5 V, the output voltage at terminal W can range from 0 V to 5 V. [Equation 1](#) is the general equation defining the output voltage at terminal W for any valid input voltage applied to terminal H and terminal L (GND).

$$V_W = V_{WL} = (V_H - V_L) \times \frac{D}{128} \quad (1)$$

The voltage difference between terminal H and terminal W can also be calculated in [Equation 2](#).

$$V_{HW} = (V_H - V_L) \times \left( 1 - \left( \frac{D}{128} \right) \right)$$

where

- D is the decimal value of the wiper code (2)

[Table 1](#) shows the ideal values for DPOT with end-to end resistance of 10 kΩ. The absolute values of resistance can vary significantly but the Ratio ( $R_{WL}/R_{TOT}$ ) is extremely accurate.

The linearity values are *relative* linearity values (that is, linearity after zero-scale and full-scale offset errors are removed). Consider this when expecting a certain absolute accuracy because some error is introduced when the device gets close in magnitude to the offset errors.

Note that the MSB is always discarded during a write to the wiper position register. For example, if 0x80 is written to the wiper position register, a read returns 0x00. Another similar example is if 0xFF is written, then 0x7F is read.

**Table 1. Resistance Values Table**

STEP	HEX	R <sub>WL</sub> (KΩ)	R <sub>HW</sub> (KΩ)	R <sub>WL</sub> /R <sub>TOT</sub>
0	0x00	0.00	10.00	0.0%
1	0x01	0.08	9.92	0.8%
2	0x02	0.16	9.84	1.6%
3	0x03	0.23	9.77	2.3%
4	0x04	0.31	9.69	3.1%
5	0x05	0.39	9.61	3.9%
6	0x06	0.47	9.53	4.7%
7	0x07	0.55	9.45	5.5%
8	0x08	0.63	9.38	6.3%
9	0x09	0.70	9.30	7.0%
10	0x0A	0.78	9.22	7.8%

**Table 1. Resistance Values Table (continued)**

STEP	HEX	R <sub>WL</sub> (KΩ)	R <sub>HW</sub> (KΩ)	R <sub>WL</sub> /R <sub>TOT</sub>
11	0x0B	0.86	9.14	8.6%
12	0x0C	0.94	9.06	9.4%
13	0x0D	1.02	8.98	10.2%
14	0x0E	1.09	8.91	10.9%
15	0x0F	1.17	8.83	11.7%
16	0x10	1.25	8.75	12.5%
17	0x11	1.33	8.67	13.3%
18	0x12	1.41	8.59	14.1%
19	0x13	1.48	8.52	14.8%
20	0x14	1.56	8.44	15.6%
21	0x15	1.64	8.36	16.4%
22	0x16	1.72	8.28	17.2%
23	0x17	1.80	8.20	18.0%
24	0x18	1.88	8.13	18.8%
25	0x19	1.95	8.05	19.5%
26	0x1A	2.03	7.97	20.3%
27	0x1B	2.11	7.89	21.1%
28	0x1C	2.19	7.81	21.9%
29	0x1D	2.27	7.73	22.7%
30	0x1E	2.34	7.66	23.4%
31	0x1F	2.42	7.58	24.2%
32	0x20	2.50	7.50	25.0%
33	0x21	2.58	7.42	25.8%
34	0x22	2.66	7.34	26.6%
35	0x23	2.73	7.27	27.3%
36	0x24	2.81	7.19	28.1%
37	0x25	2.89	7.11	28.9%
38	0x26	2.97	7.03	29.7%
39	0x27	3.05	6.95	30.5%
40	0x28	3.13	6.88	31.3%
41	0x29	3.20	6.80	32.0%
42	0x2A	3.28	6.72	32.8%
43	0x2B	3.36	6.64	33.6%
44	0x2C	3.44	6.56	34.4%
45	0x2D	3.52	6.48	35.2%
46	0x2E	3.59	6.41	35.9%
47	0x2F	3.67	6.33	36.7%
48	0x30	3.75	6.25	37.5%
49	0x31	3.83	6.17	38.3%
50	0x32	3.91	6.09	39.1%
51	0x33	3.98	6.02	39.8%
52	0x34	4.06	5.94	40.6%
53	0x35	4.14	5.86	41.4%
54	0x36	4.22	5.78	42.2%
55	0x37	4.30	5.70	43.0%
56	0x38	4.38	5.63	43.8%
57	0x39	4.45	5.55	44.5%

**Table 1. Resistance Values Table (continued)**

STEP	HEX	R <sub>WL</sub> (KΩ)	R <sub>HW</sub> (KΩ)	R <sub>WL</sub> /R <sub>TOT</sub>
58	0x3A	4.53	5.47	45.3%
59	0x3B	4.61	5.39	46.1%
60	0x3C	4.69	5.31	46.9%
61	0x3D	4.77	5.23	47.7%
62	0x3E	4.84	5.16	48.4%
63	0x3F	4.92	5.08	49.2%
64 (POR Default)	0x40	5.00	5.00	50.0%
65	0x41	5.08	4.92	50.8%
66	0x42	5.16	4.84	51.6%
67	0x43	5.23	4.77	52.3%
68	0x44	5.31	4.69	53.1%
69	0x45	5.39	4.61	53.9%
70	0x46	5.47	4.53	54.7%
71	0x47	5.55	4.45	55.5%
72	0x48	5.63	4.38	56.3%
73	0x49	5.70	4.30	57.0%
74	0x4A	5.78	4.22	57.8%
75	0x4B	5.86	4.14	58.6%
76	0x4C	5.94	4.06	59.4%
77	0x4D	6.02	3.98	60.2%
78	0x4E	6.09	3.91	60.9%
79	0x4F	6.17	3.83	61.7%
80	0x50	6.25	3.75	62.5%
81	0x51	6.33	3.67	63.3%
82	0x52	6.41	3.59	64.1%
83	0x53	6.48	3.52	64.8%
84	0x54	6.56	3.44	65.6%
85	0x55	6.64	3.36	66.4%
86	0x56	6.72	3.28	67.2%
87	0x57	6.80	3.20	68.0%
88	0x58	6.88	3.13	68.8%
89	0x59	6.95	3.05	69.5%
90	0x5A	7.03	2.97	70.3%
91	0x5B	7.11	2.89	71.1%
92	0x5C	7.19	2.81	71.9%
93	0x5D	7.27	2.73	72.7%
94	0x5E	7.34	2.66	73.4%
95	0x5F	7.42	2.58	74.2%
96	0x60	7.50	2.50	75.0%
97	0x61	7.58	2.42	75.8%
98	0x62	7.66	2.34	76.6%
99	0x63	7.73	2.27	77.3%
100	0x64	7.81	2.19	78.1%
101	0x65	7.89	2.11	78.9%
102	0x66	7.97	2.03	79.7%
103	0x67	8.05	1.95	80.5%
104	0x68	8.13	1.88	81.3%

**Table 1. Resistance Values Table (continued)**

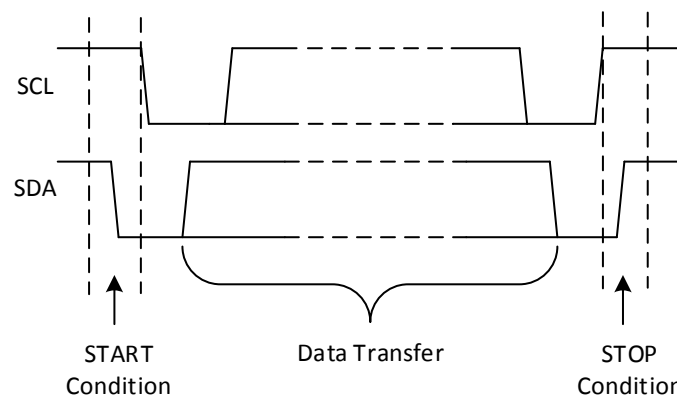
STEP	HEX	R <sub>WL</sub> (KΩ)	R <sub>HW</sub> (KΩ)	R <sub>WL</sub> /R <sub>TOT</sub>
105	0x69	8.20	1.80	82.0%
106	0x6A	8.28	1.72	82.8%
107	0x6B	8.36	1.64	83.6%
108	0x6C	8.44	1.56	84.4%
109	0x6D	8.52	1.48	85.2%
110	0x6E	8.59	1.41	85.9%
111	0x6F	8.67	1.33	86.7%
112	0x70	8.75	1.25	87.5%
113	0x71	8.83	1.17	88.3%
114	0x72	8.91	1.09	89.1%
115	0x73	8.98	1.02	89.8%
116	0x74	9.06	0.94	90.6%
117	0x75	9.14	0.86	91.4%
118	0x76	9.22	0.78	92.2%
119	0x77	9.30	0.70	93.0%
120	0x78	9.38	0.63	93.8%
121	0x79	9.45	0.55	94.5%
122	0x7A	9.53	0.47	95.3%
123	0x7B	9.61	0.39	96.1%
124	0x7C	9.69	0.31	96.9%
125	0x7D	9.77	0.23	97.7%
126	0x7E	9.84	0.16	98.4%
127	0x7F	9.92	0.08	99.2%

## 9.5 Programming

### 9.5.1 I<sup>2</sup>C General Operation and Overview

#### 9.5.1.1 START and STOP Conditions

I<sup>2</sup>C communication with this device is initiated by the master sending a START condition and terminated by the master sending a STOP condition. A high-to-low transition on the SDA line while the SCL is high defines a START condition. A low-to-high transition on the SDA line while the SCL is high defines a STOP condition. See [Figure 12](#).



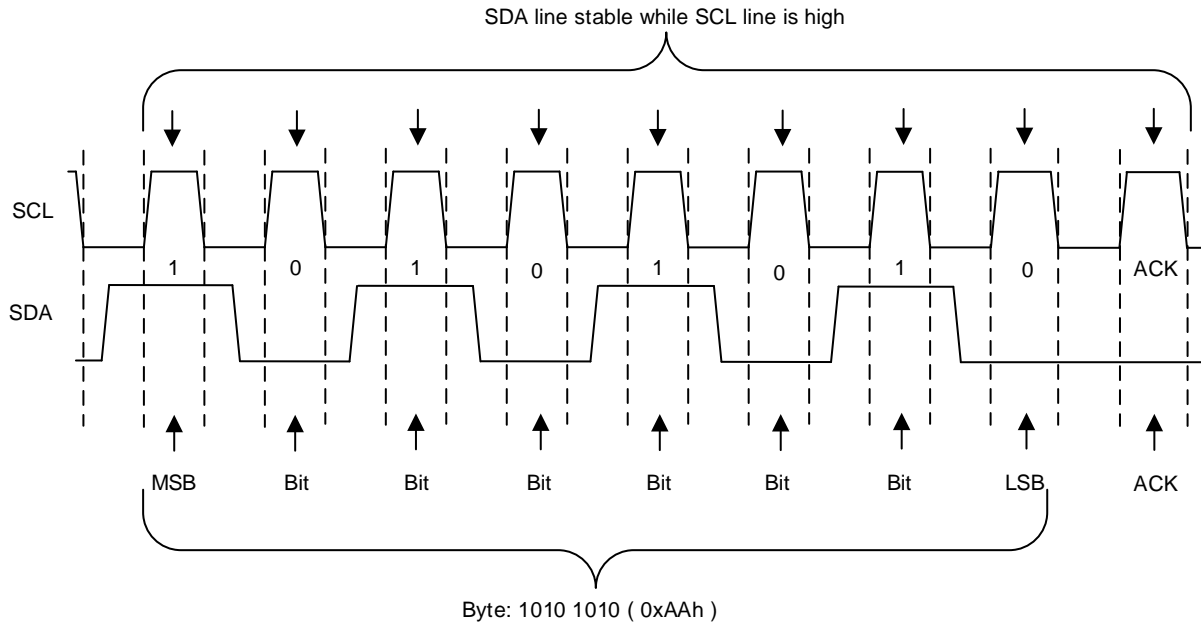
**Figure 12. Definition of START and STOP Conditions**

## Programming (continued)

### 9.5.1.2 Data Validity and Byte Formation

One data bit is transferred during each clock pulse of the SCL. One byte is comprised of eight bits on the SDA line. See [Figure 13](#). A byte may either be a device address, register address, or data written to or read from a slave.

Data is transferred Most Significant Bit (MSB) first. Any number of data bytes can be transferred from the master to slave between the START and STOP conditions. Data on the SDA line must remain stable during the high phase of the clock period, as changes in the data line when the SCL is high are interpreted as control commands (START or STOP).



**Figure 13. Definition of Byte Formation**

### 9.5.1.3 Acknowledge (ACK) and Not Acknowledge (NACK)

Each byte is followed by one ACK bit from the receiver. The ACK bit allows the receiver to communicate to the transmitter that the byte was successfully received and another byte may be sent.

The transmitter must release the SDA line before the receiver can send the ACK bit. To send an ACK bit, the receiver shall pull down the SDA line during the low phase of the ACK/NACK-related clock period (period 9), so that the SDA line is stable low during the high phase of the ACK/NACK-related clock period. Consider setup and hold times. [Figure 14](#) shows an example use of ACK.

Programming (continued)

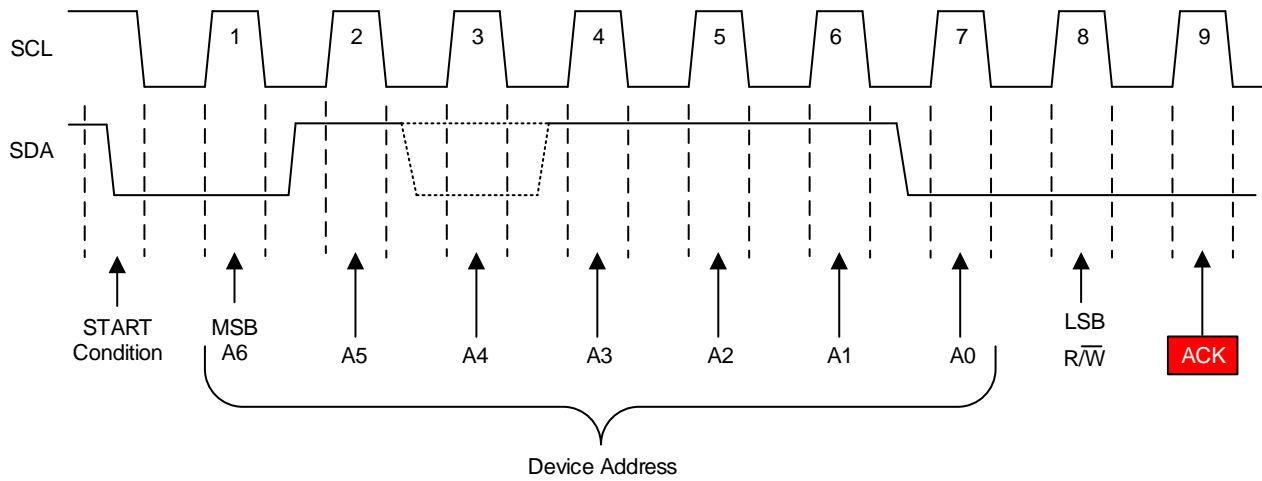


Figure 14. Example Use of ACK

When the SDA line remains high during the ACK/NACK-related clock period, this is a NACK signal. There are several conditions that lead to the generation of a NACK:

- The receiver is unable to receive or transmit because it is performing some real-time function and is not ready to start communication with the master.
- During the transfer, the receiver gets data or commands that it does not understand.
- During the transfer, the receiver cannot receive any more data bytes.
- A master-receiver is done reading data and indicates this to the slave through a NACK.

Figure 15 shows an example use of NACK.

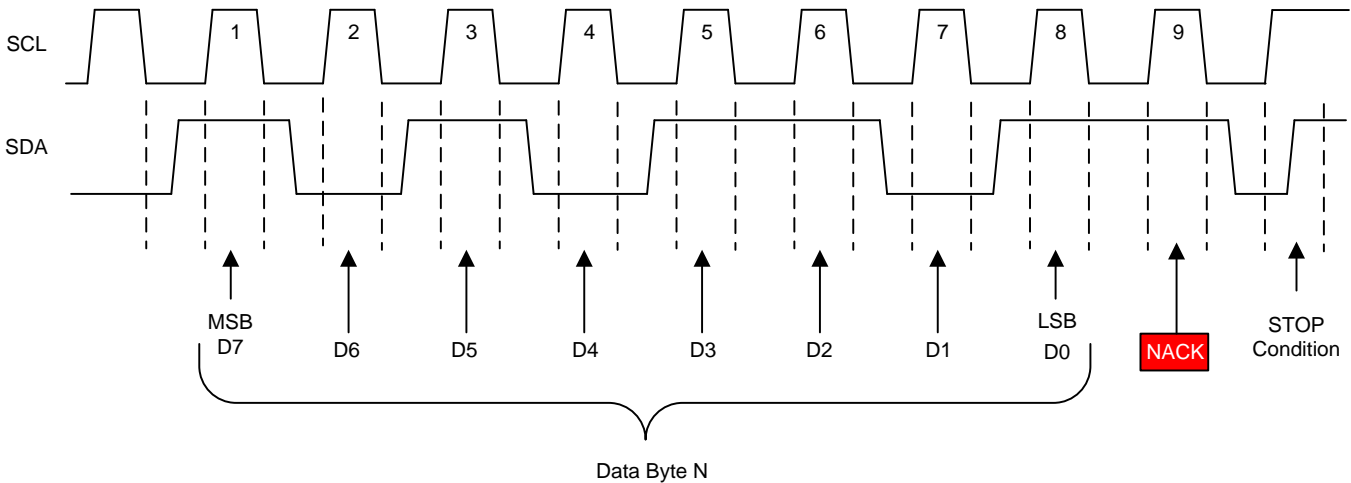


Figure 15. Example Use of NACK

9.5.1.4 Repeated Start

A repeated START condition may be used in place of a complete STOP condition followed by another START condition when performing a read function. The advantage of this is that the I<sup>2</sup>C bus does not become available after the stop and therefore prevents other devices from grabbing the bus between transfers.

## Programming (continued)

### 9.5.2 Programming With I<sup>2</sup>C

#### 9.5.2.1 Write Operation

To write on the I<sup>2</sup>C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. After the slave responds with an acknowledge, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know that it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition. See [Figure 16](#).

Master controls SDA line

Slave controls SDA line

#### Write to one register in a device

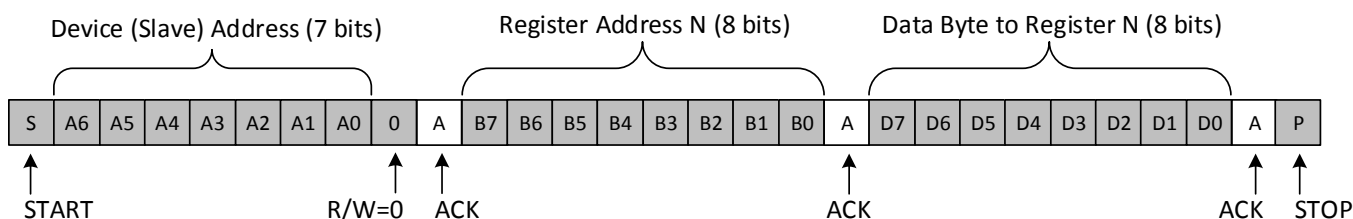


Figure 16. Write Operation

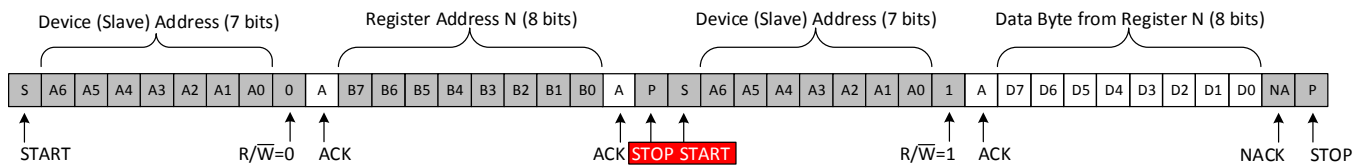
#### 9.5.2.2 Read Operation

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/W bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmission.

The master continues to send out the clock pulses, for each byte of data that it wishes to receive. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it was expecting (or needs to stop communication), it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition. [Figure 17](#) shows the read operation from one register.

## Programming (continued)

### Read from one register in a device



### Read from one register in a device (Repeated Start)

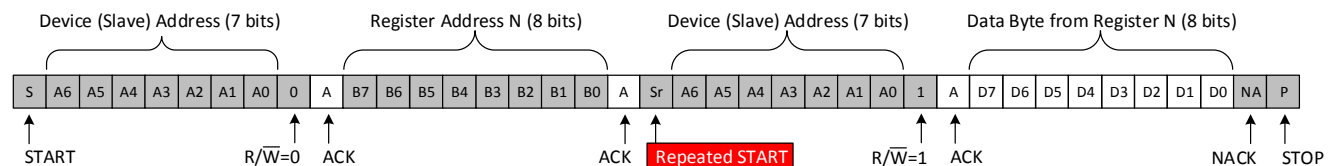


Figure 17. Read Operation from One Register

### Read from one register in a device with single register

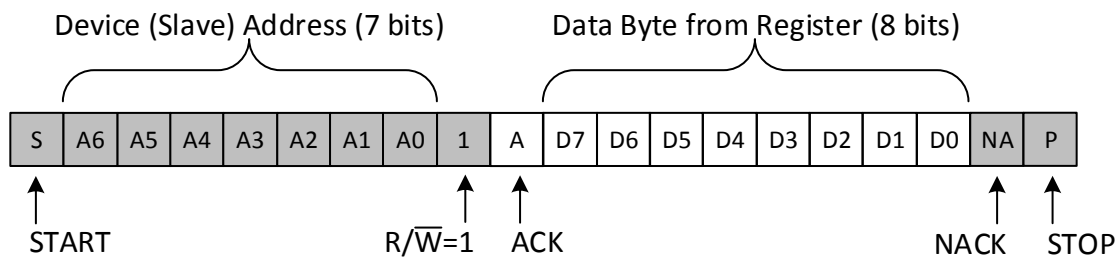


Figure 18. Short Read Operation

The TPL0401x-10-Q1 has 1 register, and it is not a requirement that the register address be sent before a read. A shorter read allows the user to simply send a read request to the device address as shown in [Figure 18](#).

## 9.6 Register Maps

### 9.6.1 Slave Address

[Table 2](#) and [Table 3](#) show the TPL0401A-10-Q1 and TPL0401B-10-Q1 bit address respectively.

Table 2. TPL0401A-10-Q1 Bit Address

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
0	1	0	1	1	1	0	R/W

Table 3. TPL0401B-10-Q1 Bit Address

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
0	1	1	1	1	1	0	R/W

### 9.6.2 Register Address

Following the successful acknowledgment of the address byte, the bus master sends a command byte as shown in [Figure 19](#), which is stored in the Control Register in the TPL0401x-10-Q1. The TPL0401x-10-Q1 has only 1 register, but requires the command byte be sent during communication.



**Figure 19. Register Address Byte**

[Table 4](#) shows the TPL0401x-10-Q1 register address byte.

**Table 4. Register Address Byte**

REGISTER ADDRESS BITS								REGISTER ADDRESS (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	0x00	Wiper Position	Read/Write byte	0100 0000 (0x40)

See [Table 1](#) for more information on the wiper position register values. Note that the MSB is always discarded during a write to the wiper position register. For example, if 0x80 is written to the wiper position register, a read returns 0x00. Another similar example is if 0xFF is written, then 0x7F is read.

## 10 Application and Implementation

### 10.1 Application Information

There are many applications in which voltage division is needed through the use of a digital potentiometer such as the TPL0401x-10-Q1; this is one example of the many. In conjunction with many amplifiers, the TPL0401x-10-Q1 can effectively be used in voltage divider mode to create a buffer to adjust the reference voltage for DDR3 DIMM1 Memory.

### 10.2 Typical Application

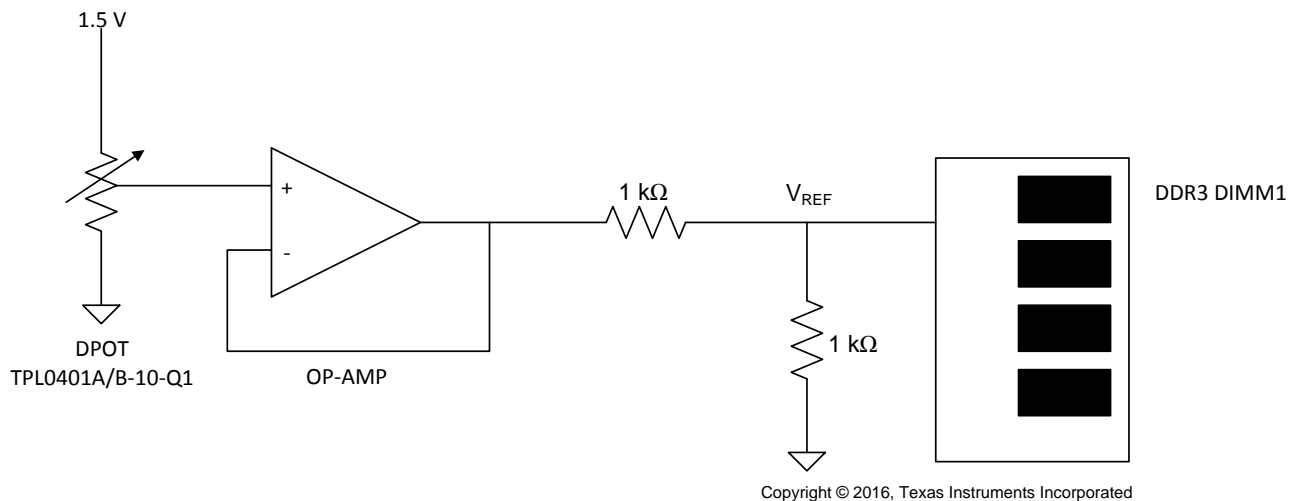


Figure 20. DDR3 Voltage Reference Adjustment

#### 10.2.1 Design Requirements

Table 5 lists the design parameters for this example.

Table 5. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	1.5 V
$V_{REF}$	0 V to 0.75 V

#### 10.2.2 Detailed Design Procedure

The TPL0401x-10-Q1 can be used in voltage divider mode with a unity-gain op amp buffer to provide a clean voltage reference for DDR3 DIMM1 Memory. The analog output voltage,  $V_{REF1}$  is determined by the wiper setting programmed through the I<sup>2</sup>C bus.

The op amp is required to buffer the high-impedance output of the TPL0401x-10-Q1 or else loading placed on the output of the voltage divider affects the output voltage.

### 10.2.3 Application Curve

The voltage, 1.5 V, applied to terminal H of TPL0401x-10-Q1 determines the voltage that is buffered by the unity-gain op amp and divided as the DDR3 DIMM1 voltage reference. By using the TPL0401x-10-Q1, and dividing the 1.5 V, a maximum of 0.75 V is applied to the buffer and passed to the voltage divider. The output voltage then ranges from 0 V to 0.75 V.

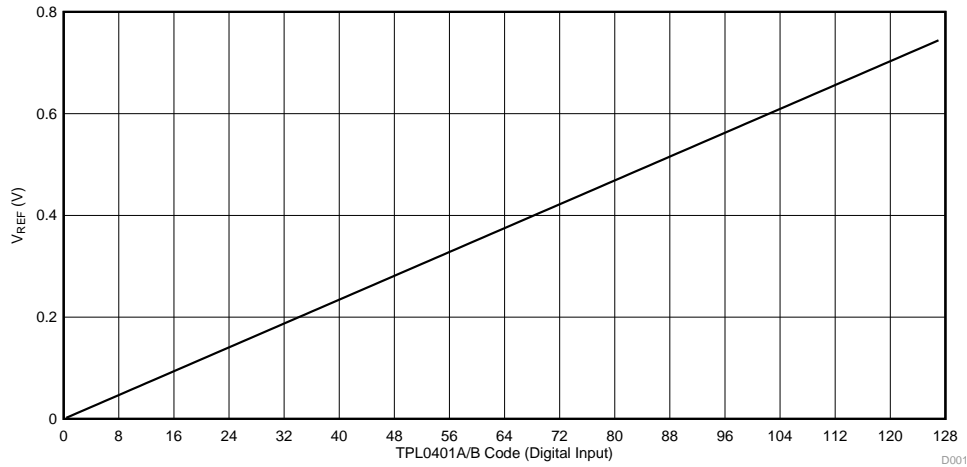


Figure 21. TPL0401-10-Q1 Digital Input vs Reference Voltage for DDR3 DIMM Memory

## 11 Power Supply Recommendations

### 11.1 Power Sequence

Protection diodes limit the voltage compliance at SDA, SCL, terminal H, and terminal W, making it important to power up  $V_{DD}$  first before applying any voltage to SDA, SCL, terminal H, and terminal W. The diodes are forward-biasing, meaning  $V_{DD}$  can be powered unintentionally if  $V_{DD}$  is not powered first. The ideal power-up sequence is  $V_{DD}$ , digital inputs, and  $V_W$  and  $V_H$ . The order of powering digital inputs,  $V_H$  and  $V_W$  does not matter as long as they are powered after  $V_{DD}$ .

### 11.2 Power-On Reset Requirements

In the event of a glitch or data corruption, the TPL0401-10-Q1 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

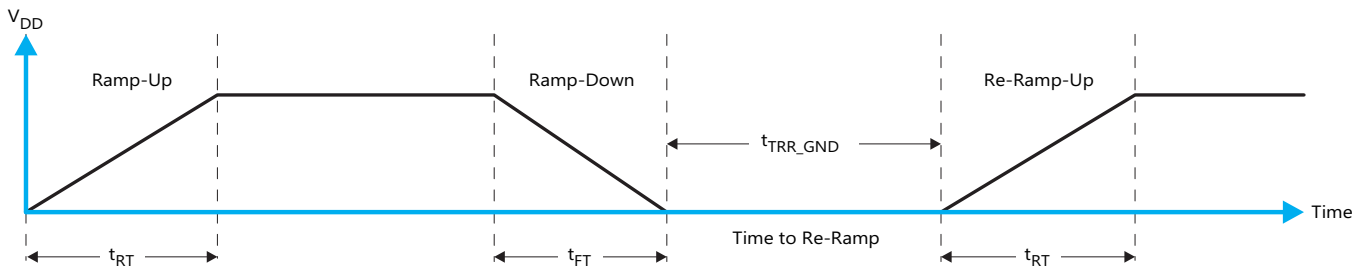


Figure 22.  $V_{DD}$  is Lowered to 0 V and then Ramped Up to  $V_{DD}$

Table 6 specifies the performance of the power-on reset feature for TCA6408A for both types of power-on reset.

Table 6. Recommended Supply Sequencing and Ramp Rates at  $T_A = 25^\circ\text{C}$  <sup>(1)</sup>

PARAMETER			MIN	MAX	UNIT
$t_{FT}$	Fall rate	See Figure 22	0.0001	1000	ms
$t_{RT}$	Rise rate	See Figure 22	0.0001	1000	ms
$t_{RR\_GND}$	Time to re-ramp (when $V_{DD}$ drops to GND)	See Figure 22	1		$\mu\text{s}$

(1) Not tested. Specified by design.

### 11.3 I<sup>2</sup>C Communication After Power Up

In order to ensure a complete device reset after a power up condition, the user must wait 120  $\mu\text{s}$  after power up before initiating communication with the TPL0401x-10-Q1. See Figure 23 for an example waveform.

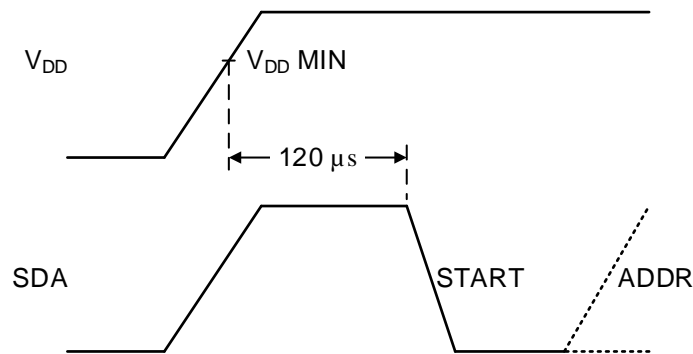


Figure 23. Recommended Start Up Sequence

#### **11.4 Wiper Position While Unpowered and After Power Up**

When DPOT is powered off, the impedance of the device is undefined and not known.

Upon power-up, the device returns to 0x40h code because this device does not contain non-volatile memory.

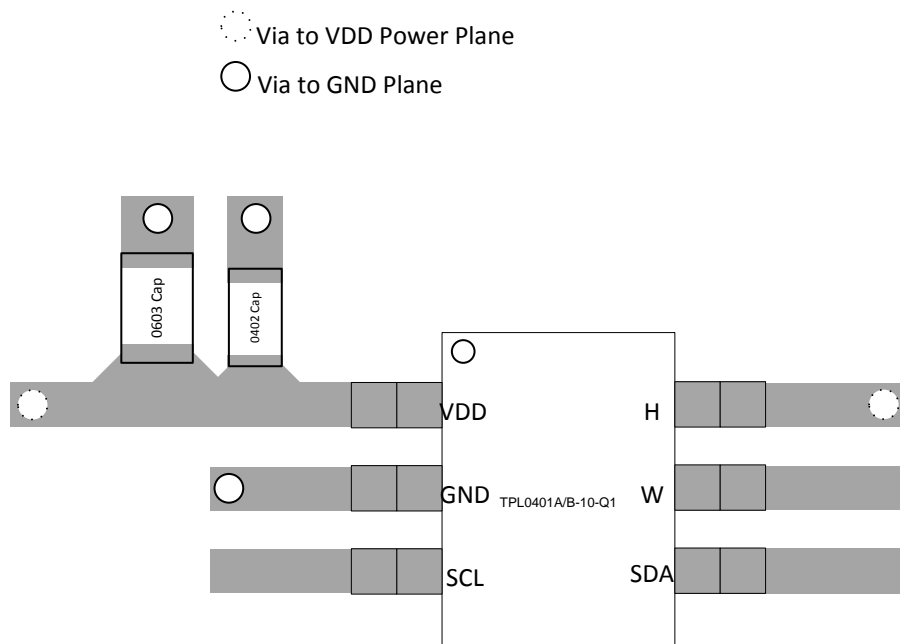
## 12 Layout

### 12.1 Layout Guidelines

To ensure reliability of the device, follow common printed-circuit board (PCB) layout guidelines:

- Leads to the input must be as direct as possible with a minimum conductor length.
- The ground path must have low resistance and low inductance.
- Use short trace-lengths to avoid excessive loading.
- It is common to have a dedicated ground plane on an inner layer of the board.
- Terminals that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias.
- Use bypass capacitors on power supplies and placed them as close as possible to the  $V_{DD}$  pin.
- Apply low equivalent series resistance (0.1- $\mu$ F to 10- $\mu$ F tantalum or electrolytic capacitors) at the supplies to minimize transient disturbances and to filter low-frequency ripple.
- To reduce the total I<sup>2</sup>C bus capacitance added by PCB parasitics, data lines (SCL and SDA) must be as short as possible and the widths of the traces must also be minimized (for example, 5 to 10 mils depending on copper weight).

### 12.2 Layout Example



**Figure 24. Layout Recommendation**

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

相关文档如下:

- 《[PC 总线上拉电阻计算](#)》
- 《[理解 I2C 总线](#)》
- 《[TPL0401 评估模块用户指南](#)》

### 13.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 7. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPL0401A-Q1	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TPL0401B-Q1	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 13.3 接收文档更新通知

如需接收文档更新通知，请访问 [ti.com](#) 上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 13.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 商标

E2E is a trademark of Texas Instruments.  
 All other trademarks are the property of their respective owners.

### 13.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL0401A-10QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15N	<a href="#">Samples</a>
TPL0401B-10QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	15O	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

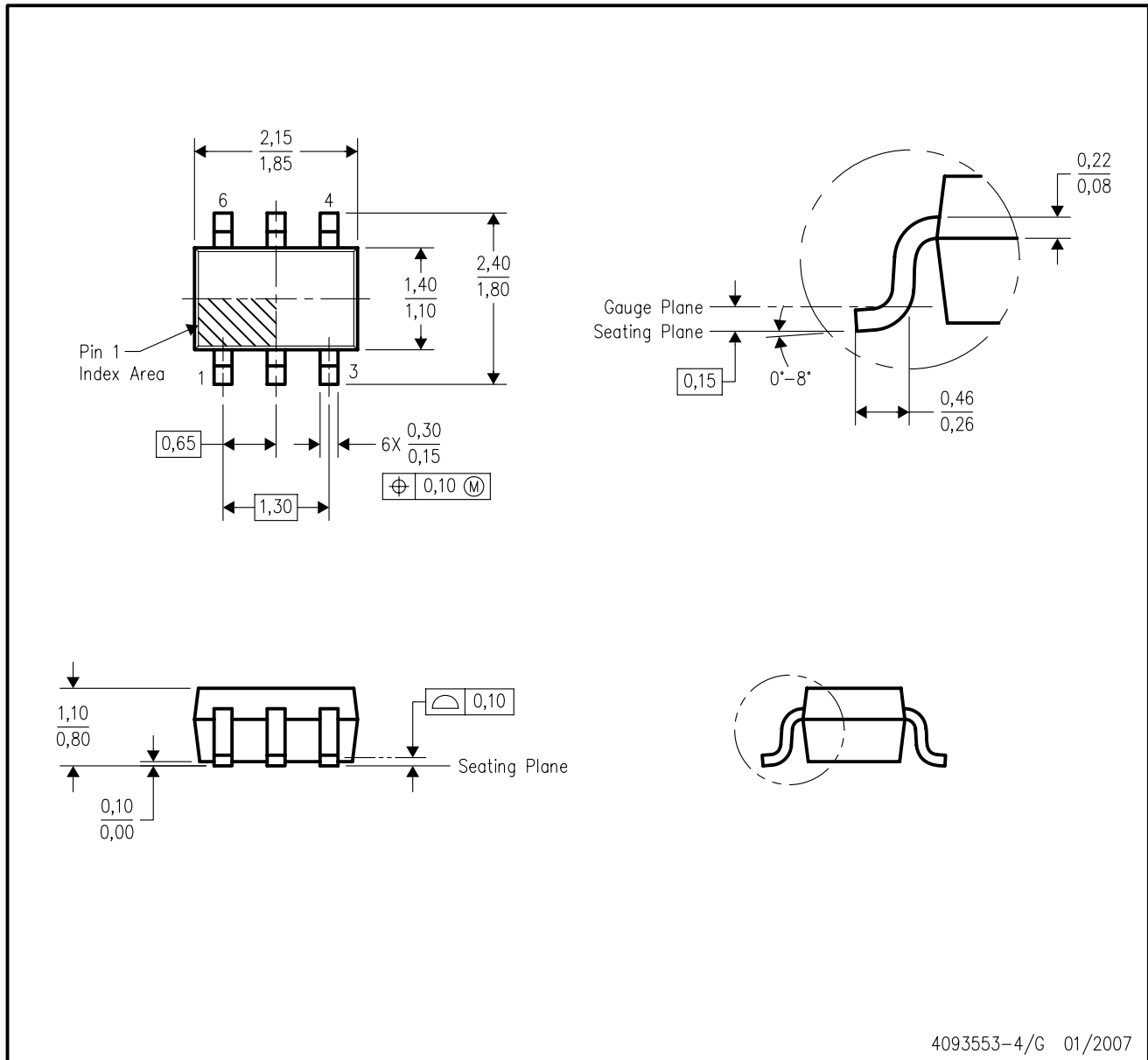
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DCK (R-PDSO-G6)

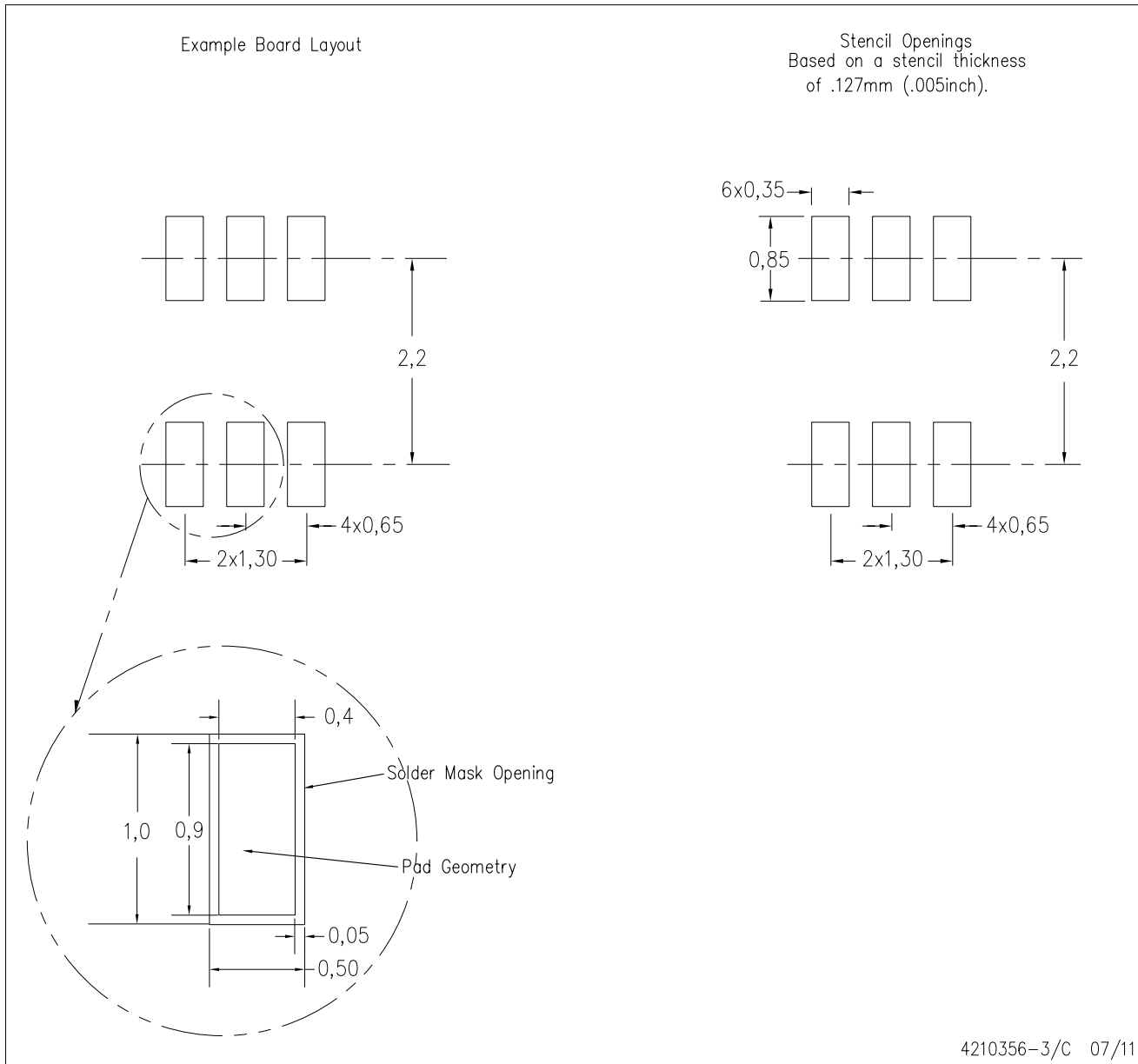
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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