

TLV2361, TLV2362

HIGH-PERFORMANCE LOW-VOLTAGE OPERATIONAL AMPLIFIERS

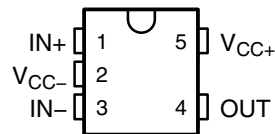
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- **Low Supply-Voltage Operation . . . $V_{CC} = \pm 1$ V Min**
- **Wide Bandwidth . . . 7 MHz Typ at $V_{CC\pm} = \pm 2.5$ V**
- **High Slew Rate . . . 3 V/ μ s Typ at $V_{CC\pm} = \pm 2.5$ V**
- **Wide Output Voltage Swing . . . ± 2.4 V Typ at $V_{CC\pm} = \pm 2.5$ V, $R_L = 10$ k Ω**
- **Low Noise . . . 8 nV/ $\sqrt{\text{Hz}}$ Typ at $f = 1$ kHz**

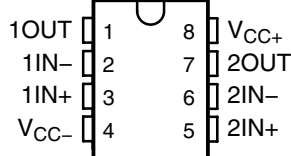
description/ordering information

The TLV236x devices are high-performance dual operational amplifiers built using an original Texas Instruments bipolar process. These devices can be operated at a very low supply voltage (± 1 V), while maintaining a wide output swing. The TLV236x devices offer a dramatically improved dynamic range of signal conditioning in low-voltage systems. The TLV236x devices also provide higher performance than other general-purpose operational amplifiers by combining higher unity-gain bandwidth and faster slew rate. With their low distortion and low-noise performance, these devices are well suited for audio applications.

TLV2361 . . . DBV PACKAGE (TOP VIEW)



TLV2362 . . . D, DGK, P, PS, OR PW PACKAGE (TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING [‡]
-0°C to 70°C	SOT-23-5 (DBV)	Reel of 3000	TLV2361CDBVR	YC3_
		Reel of 250	TLV2361CDBVT	
-40°C to 85°C	SOT-23-5 (DBV)	Reel of 3000	TLV2361IDBVR	YC4_
		Reel of 250	TLV2361IDBVT	
	MSOP/VSSOP (DGK)	Reel of 2500	TLV2362IDGKR	YBS
	PDIP (P)	Tube of 50	TLV2362IP	TLV2362IP
	SOIC (D)	Tube of 75	TLV2362ID	2362I
		Reel of 2500	TLV2362IDR	
	SOP (PS)	Reel of 2000	TLV2362IPSR	TY2362
	TSSOP (PW)	Tube of 150	TLV2362IPW	TY2362
Reel of 2000		TLV2362IPWR		

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] DBV: The actual top-side marking has one additional character that designates the wafer fab/assembly site.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



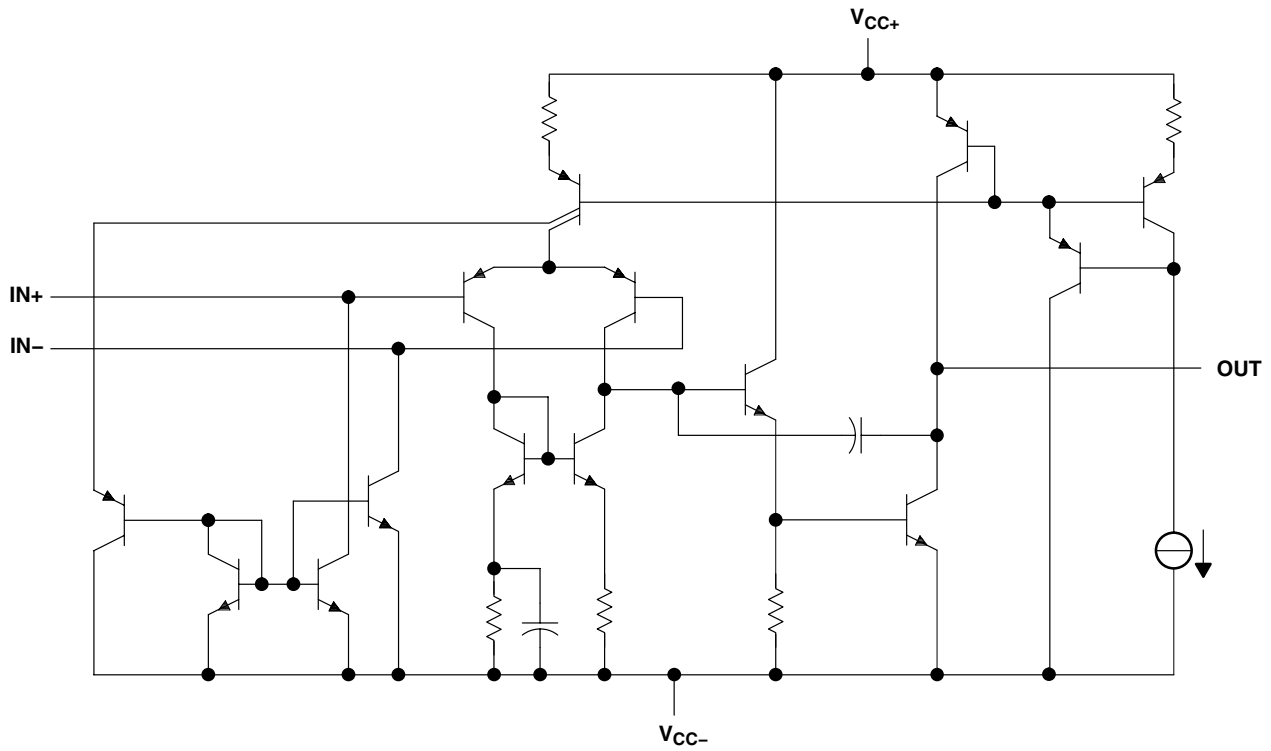
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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	TLV2361	TLV2362
Transistors	30	46
Resistors	6	11
Diodes	1	1
Capacitors	2	4
JFET	1	1

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	3.5 V
Supply voltage, V_{CC-} (see Note 1)	–3.5 V
Differential input voltage, V_{ID} (see Note 2)	± 3.5 V
Input voltage, V_I (any input) (see Notes 1 and 3)	$V_{CC\pm}$
Output voltage, V_O	± 3.5 V
Output current, I_O	20 mA
Duration of short-circuit current at (or below) 25°C (output shorted to GND)	Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5):	
D package	97°C/W
DBV package	206°C/W
DGK package	172°C/W
P package	85°C/W
PS package	95°C/W
PW package	149°C/W
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. All input voltage values must not exceed V_{CC} .
 4. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	± 1	± 2.5	V
T_A	Operating free-air temperature	0	70	°C
		–40	85	



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TLV2361 and TLV2362 electrical characteristics, $V_{CC\pm} = \pm 1.5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0,$	$V_{IC} = 0$	25°C	1	6		mV
				Full range		7.5		
I_{IO}	Input offset current	$V_O = 0,$	$V_{IC} = 0$	25°C	5	100		nA
				Full range		150		
I_{IB}	Input bias current	$V_O = 0,$	$V_{IC} = 0$	25°C	20	150		nA
				Full range		250		
V_{IC}	Common-mode input voltage	$ V_{IO} \leq 7.5\text{ mV}$		25°C	± 0.5			V
				Full range	± 0.5			
V_{OM+}	Maximum positive-peak output voltage	$R_L = 10\text{ k}\Omega$		25°C	1.2	1.4		V
		$R_L \geq 10\text{ k}\Omega$		Full range	1.2			
V_{OM-}	Maximum negative-peak output voltage	$R_L = 10\text{ k}\Omega$		25°C	-1.2	-1.4		V
		$R_L \geq 10\text{ k}\Omega$		Full range	-1.2			
I_{CC}	Supply current (per amplifier)	$V_O = 0,$	No load	25°C	1.4	2.25		mA
				Full range		2.75		mA
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 1\text{ V},$	$R_L = 10\text{ k}\Omega$	TLV2361	25°C	60	80	dB
				TLV2362		55		
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 0.5\text{ V}$		25°C	75		dB	
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm} = \pm 1.5\text{ V to } \pm 2.5\text{ V}$		25°C	80		dB	

TLV2361 and TLV2362 operating characteristics, $V_{CC\pm} = \pm 1.5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS			TYP	UNIT
SR	Slew rate	$A_V = 1,$	$V_I = \pm 0.5\text{ V}$		2.5	V/ μs
B_1	Unity-gain bandwidth	$A_V = 40,$	$R_L = 10\text{ k}\Omega,$	$C_L = 100\text{ pF}$	6	MHz
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega,$	$R_F = 10\text{ k}\Omega,$	$f = 1\text{ kHz}$	9	nV/ $\sqrt{\text{Hz}}$



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TLV2361 and TLV2362 electrical characteristics, $V_{CC\pm} = \pm 2.5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0,$	$V_{IC} = 0$	25°C		1	6	mV
				Full range			7.5	
I_{IO}	Input offset current	$V_O = 0,$	$V_{IC} = 0$	25°C		5	100	nA
				Full range			150	
I_{IB}	Input bias current	$V_O = 0,$	$V_{IC} = 0$	25°C		20	150	nA
				Full range			250	
V_{IC}	Common-mode input voltage	$ V_{IO} \leq 7.5$ mV		25°C	± 1.5			V
				Full range	± 1.4			
V_{OM+}	Maximum positive-peak output voltage	$R_L = 10$ k Ω		25°C	2	2.4		V
		$R_L \geq 10$ k Ω		Full range	2			
V_{OM-}	Maximum negative-peak output voltage	$R_L = 10$ k Ω		25°C	-2	-2.4		V
		$R_L \geq 10$ k Ω		Full range	-2			
I_{CC}	Supply current (per amplifier)	$V_O = 0,$	No load	25°C		1.75	2.5	mA
				Full range			3	
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 1$ V,	$R_L = 10$ k Ω	TLV2361	25°C	60	80	dB
				TLV2362				
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 0.5$ V		25°C		85		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm} = \pm 1.5$ V to ± 2.5 V		25°C		80		dB

TLV2361 and TLV2362 operating characteristics, $V_{CC\pm} = \pm 2.5$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
SR	Slew rate	$A_V = 1,$	$V_I = \pm 0.5$ V	3	V/ μ s
B_1	Unity-gain bandwidth	$A_V = 40,$	$R_L = 10$ k $\Omega,$ $C_L = 100$ pF	7	MHz
V_n	Equivalent input noise voltage	$R_S = 100$ $\Omega,$	$R_F = 10$ k $\Omega,$ $f = 1$ kHz	8	nV/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion, plus noise	$A_V = 1,$	$V_O = \pm 1.2$ V, $R_L = 10$ k $\Omega,$ $f = 3$ kHz	0.004	%



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TYPICAL CHARACTERISTICS

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Supply current vs Supply voltage	2
Maximum positive output voltage vs Output current	3
Maximum negative output voltage vs Output current	4
Maximum peak-to-peak output voltage vs Frequency	5
Equivalent input noise voltage vs Frequency	6
Total harmonic distortion vs Frequency	7
Total harmonic distortion vs Output voltage	8



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TYPICAL CHARACTERISTICS

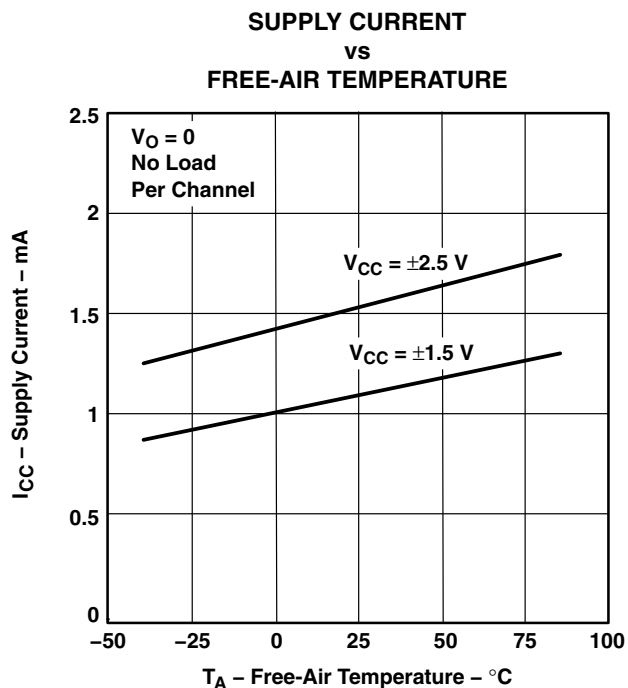


Figure 1

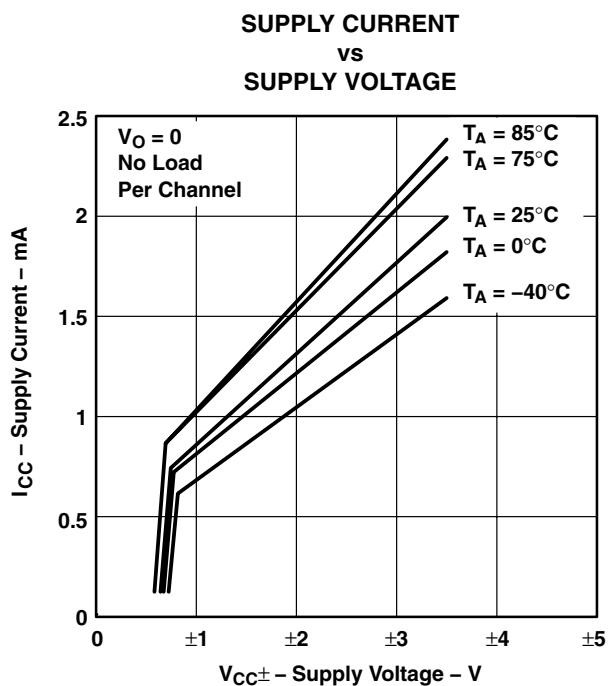


Figure 2

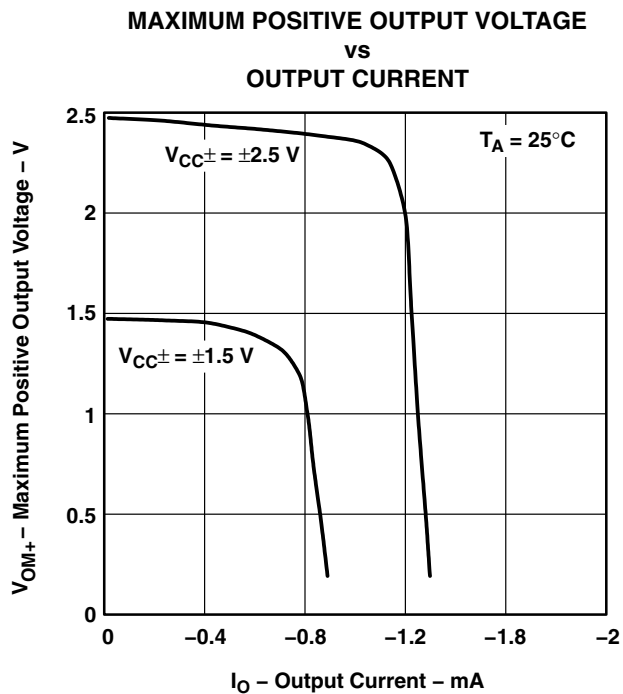


Figure 3

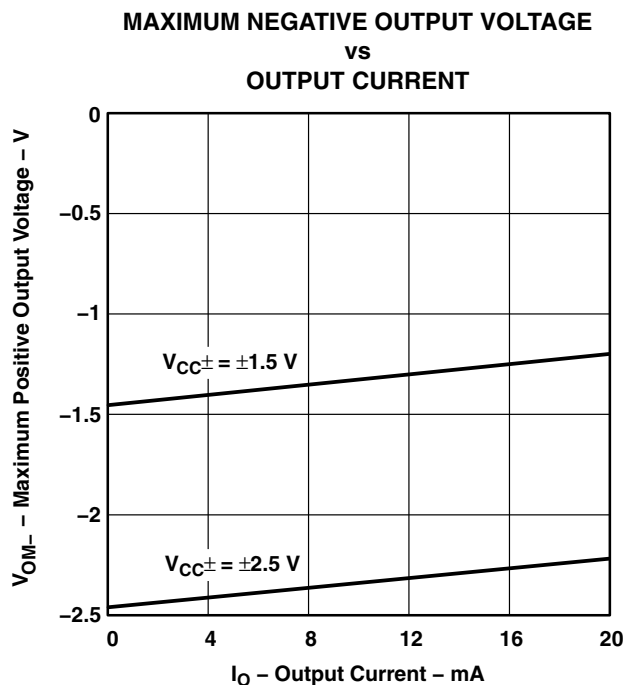


Figure 4

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

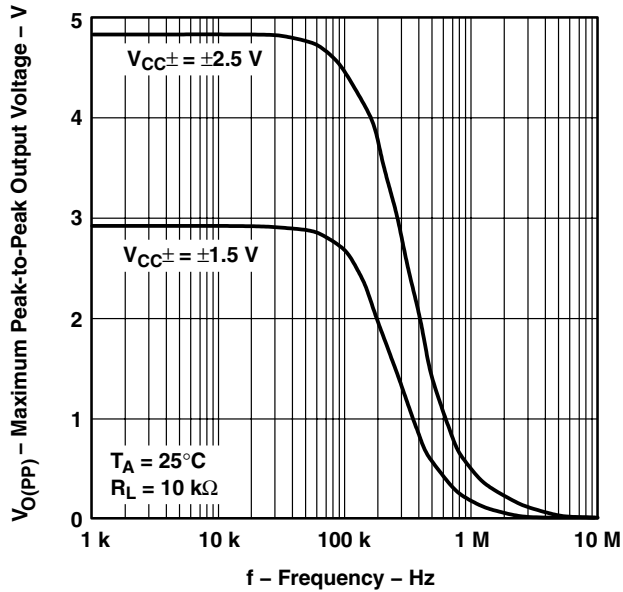


Figure 5

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

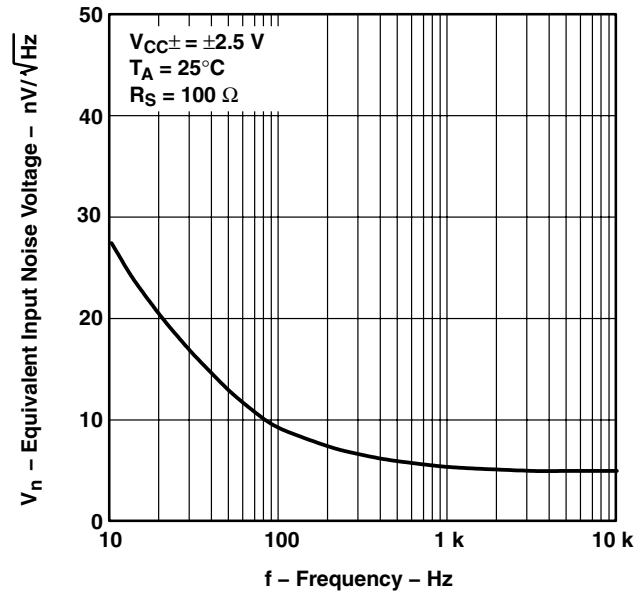


Figure 6

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

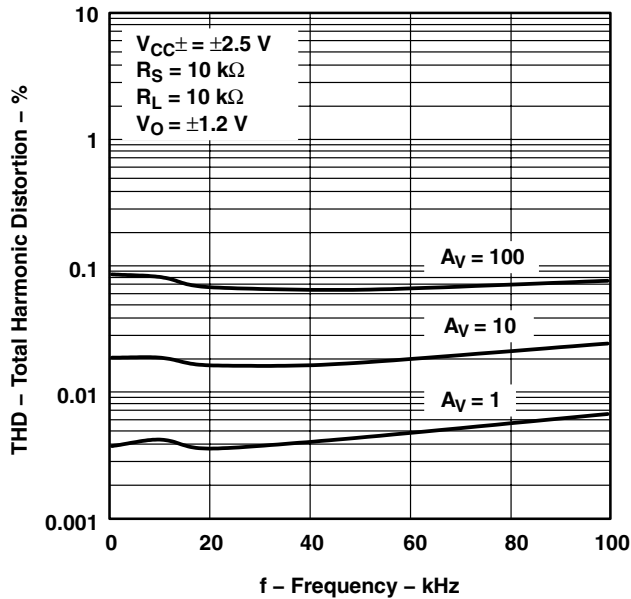


Figure 7

TOTAL HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

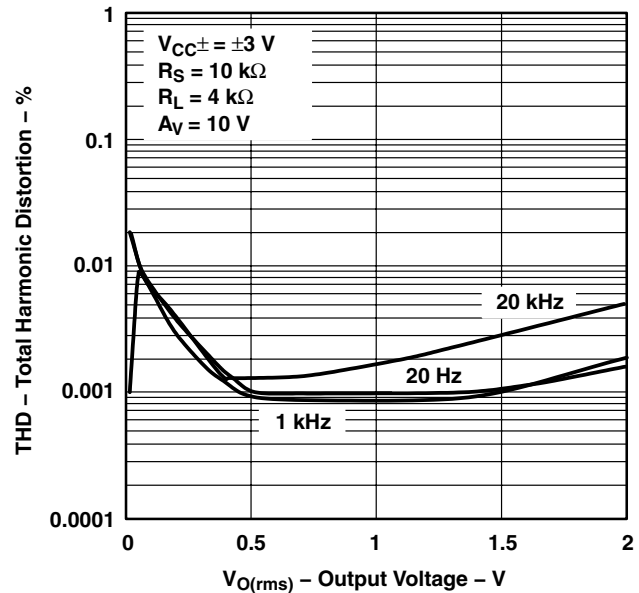


Figure 8



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2361CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	(YC3B, YC3G, YC3J, YC3L)	Samples
TLV2361CDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	(YC3B, YC3G, YC3J, YC3L)	Samples
TLV2361IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(YC4B, YC4G, YC4J, YC4L)	Samples
TLV2361IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(YC4B, YC4G, YC4J, YC4L)	Samples
TLV2362ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2362I	Samples
TLV2362IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YBL, YBS, YBU)	Samples
TLV2362IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YBL, YBS, YBU)	Samples
TLV2362IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2362I	Samples
TLV2362IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLV2362IP	Samples
TLV2362IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2362	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

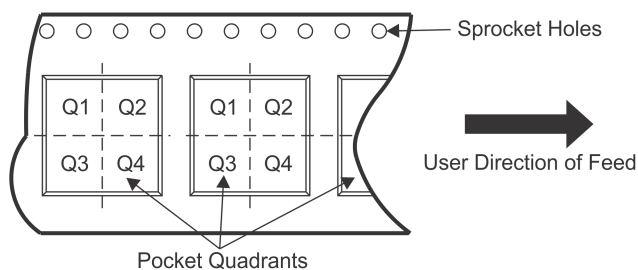
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



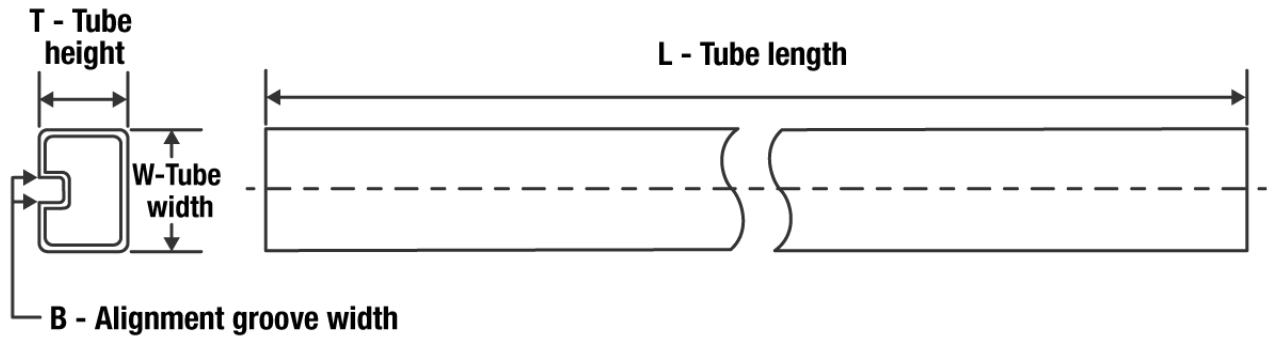
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2361CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2361CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2361CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2361CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2361IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2361IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2361IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2361IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2362IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TLV2362IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2362IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2361CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2361CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2361CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2361CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2361IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2361IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2361IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2361IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2362IDGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
TLV2362IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2362IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2362ID	D	SOIC	8	75	507	8	3940	4.32
TLV2362IP	P	PDIP	8	50	506	13.97	11230	4.32

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



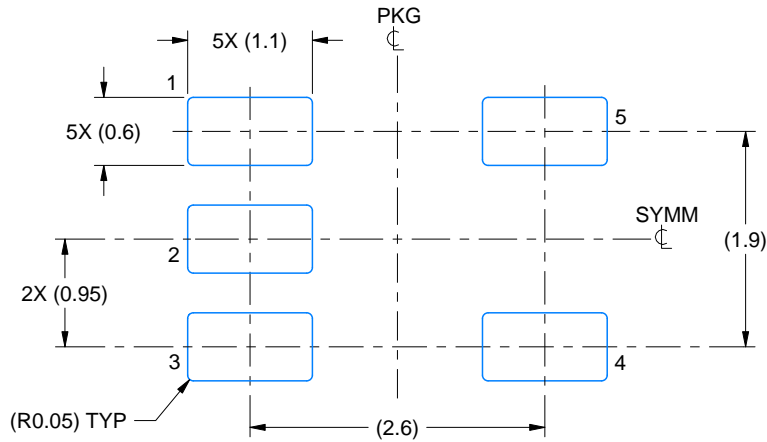
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

EXAMPLE BOARD LAYOUT

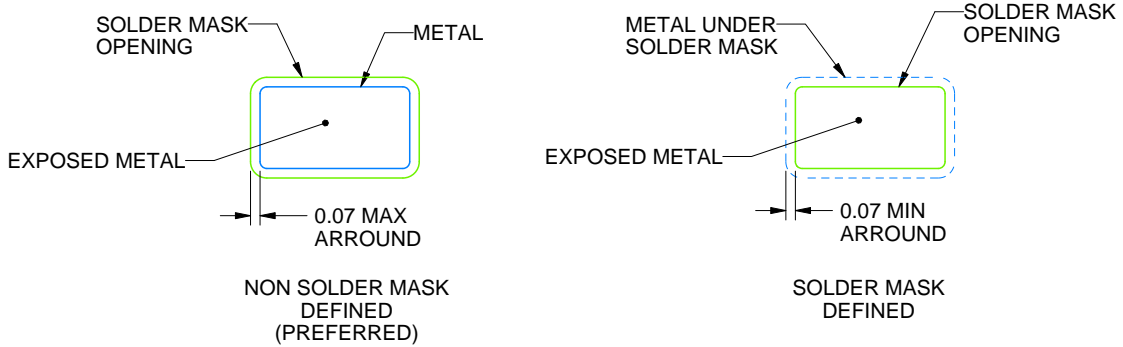
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

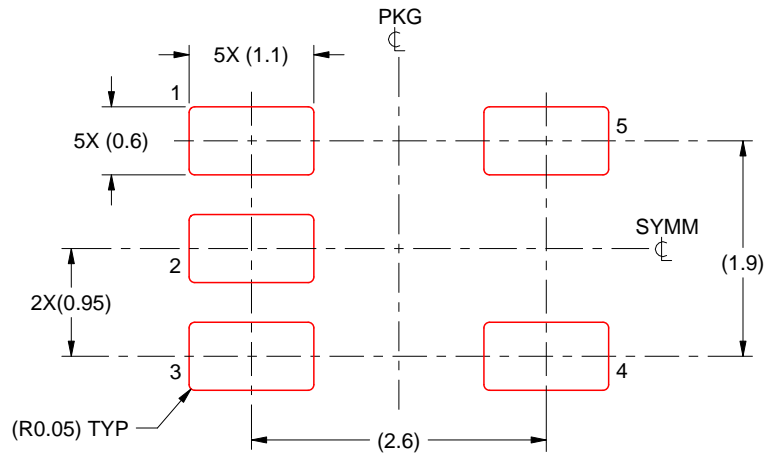
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

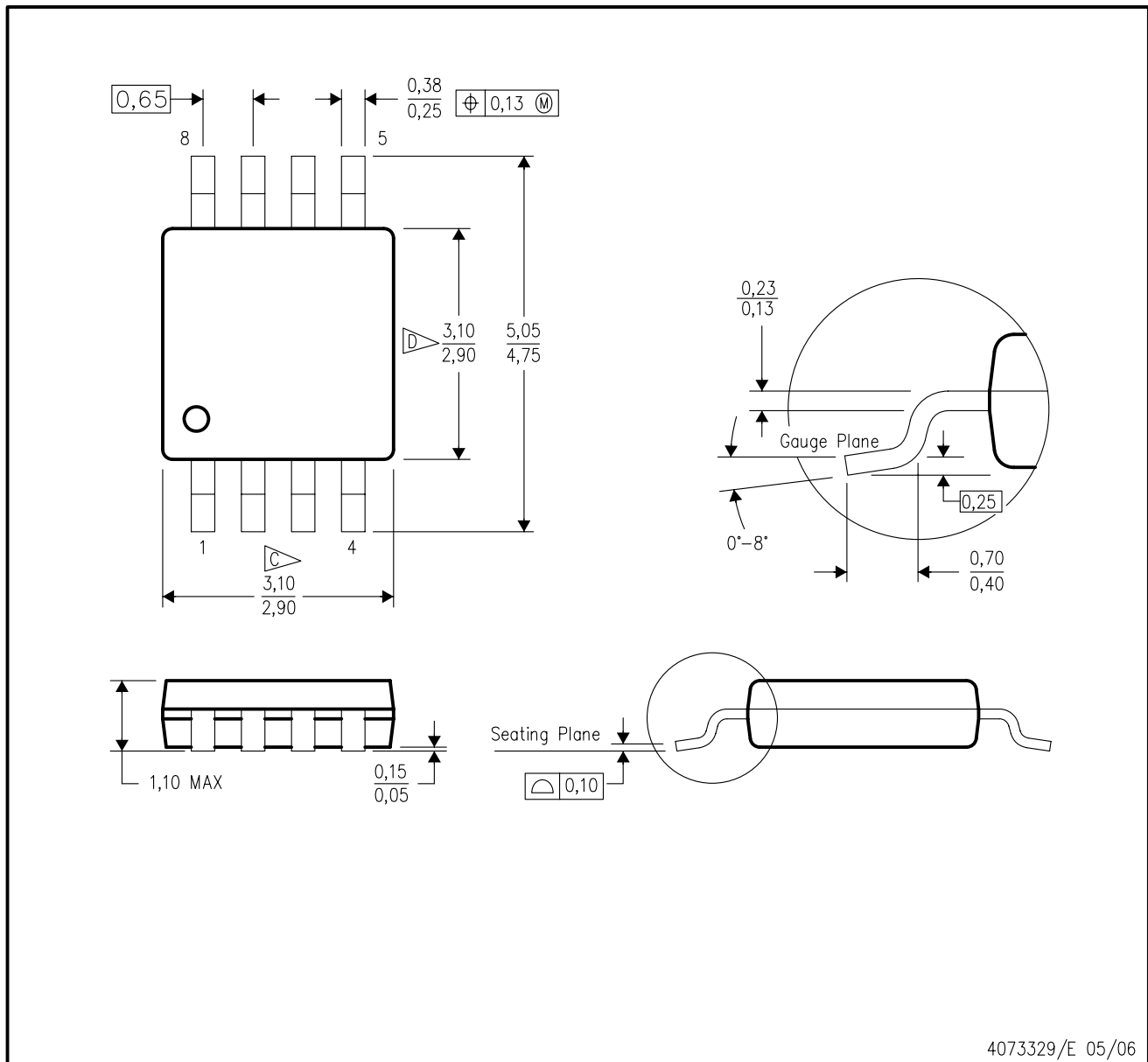
4214839/F 06/2021

NOTES: (continued)

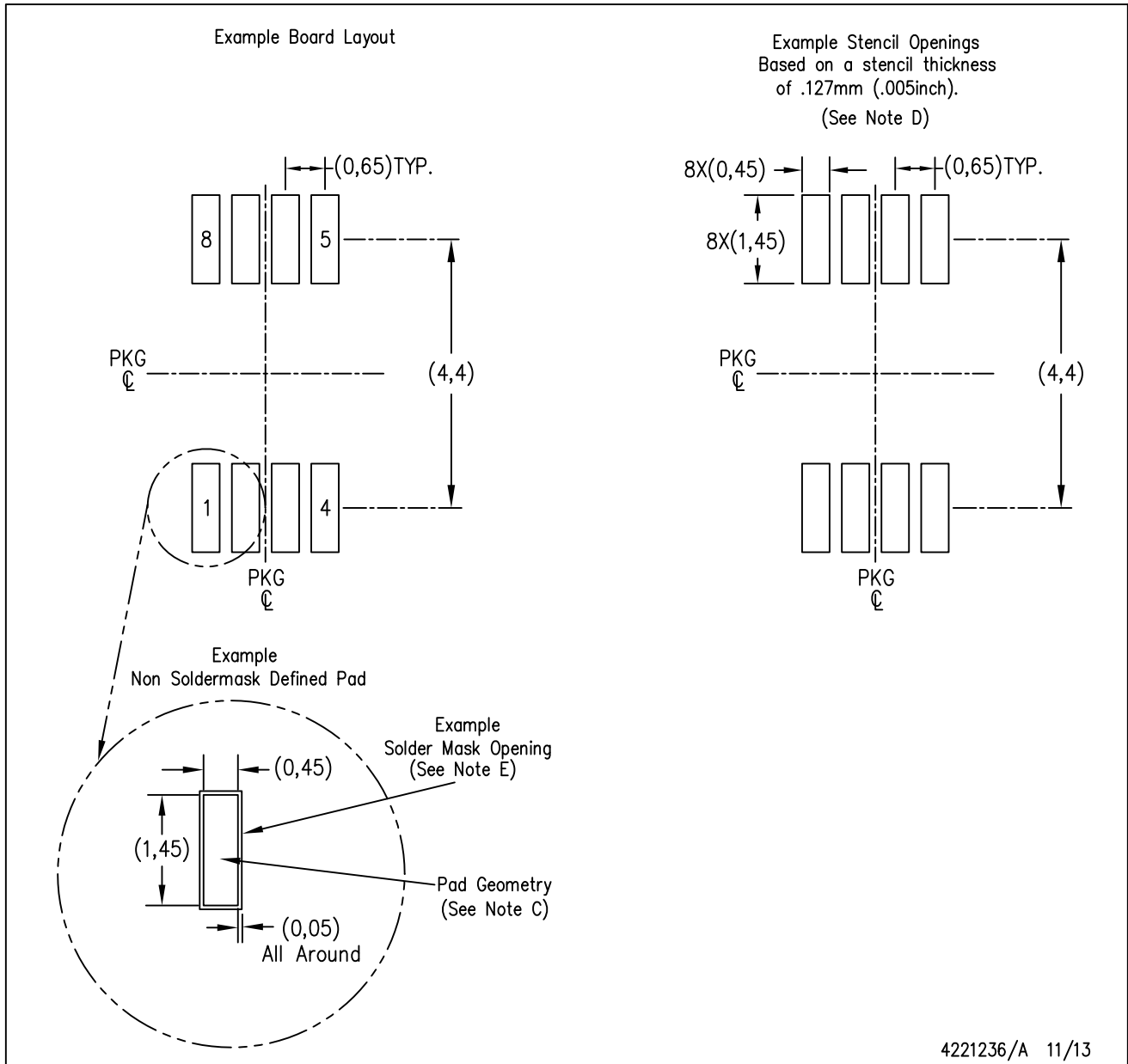
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

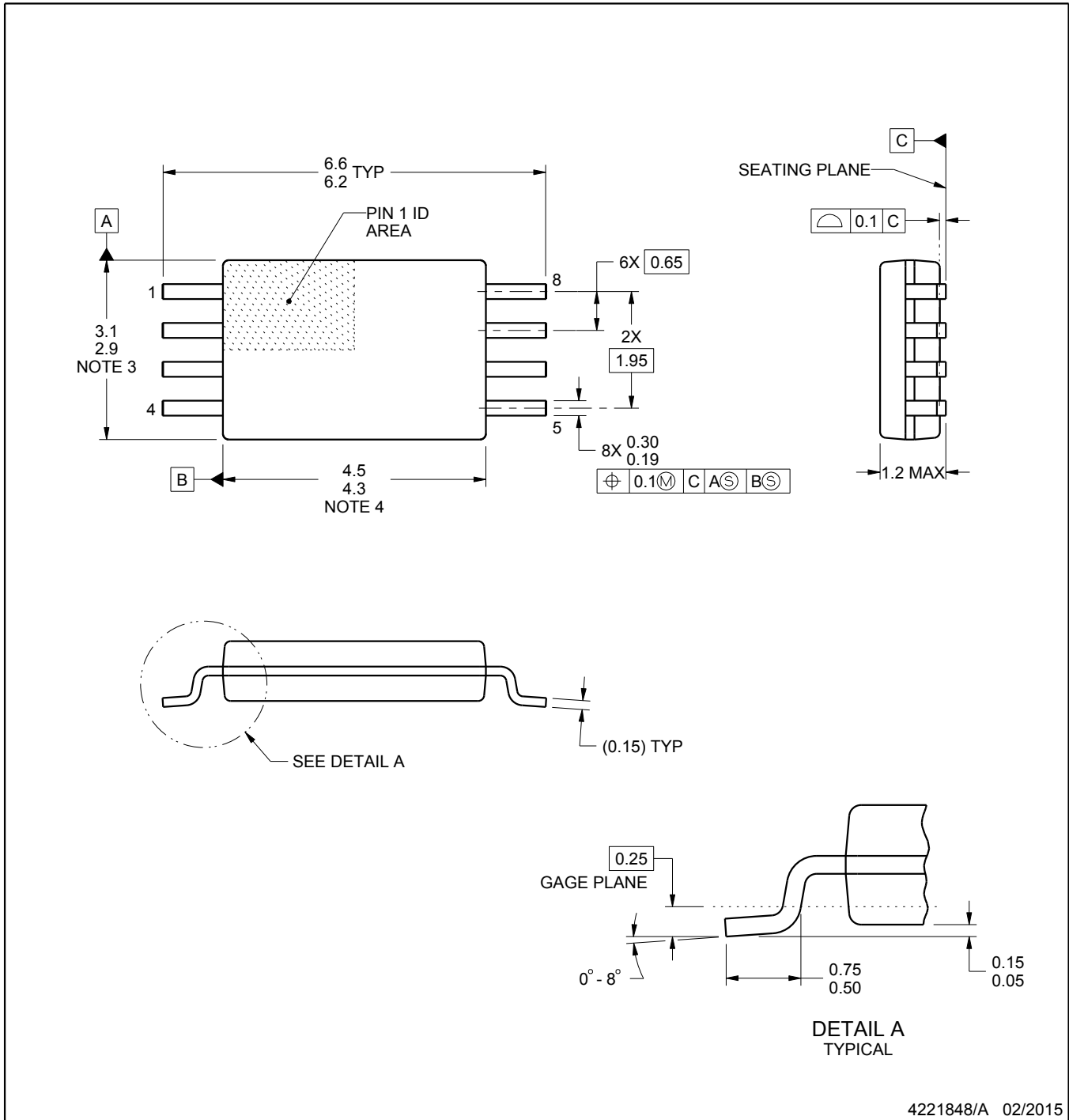
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

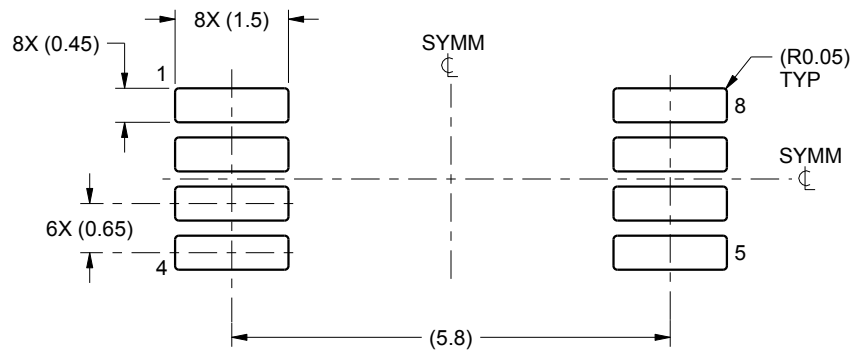
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

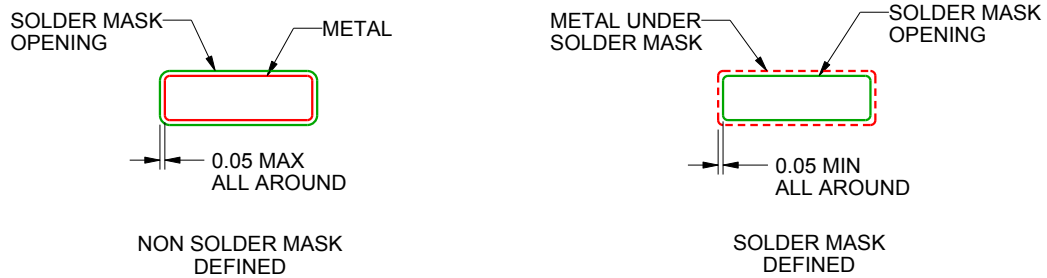
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

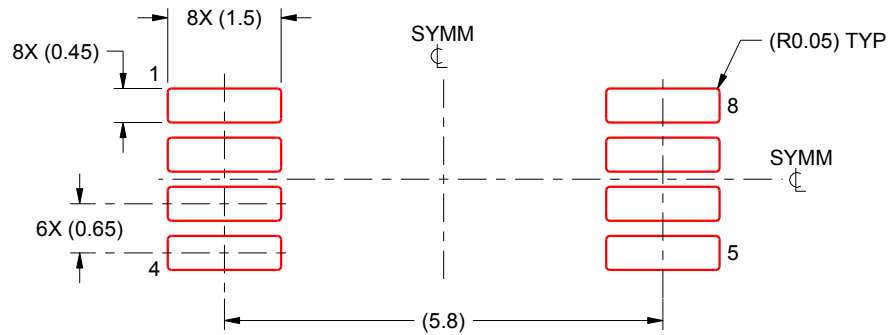
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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