

SN54ABT16952, SN74ABT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS082C – FEBRUARY 1991 – REVISED JANUARY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5 V$, $T_A = 25^\circ C$**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

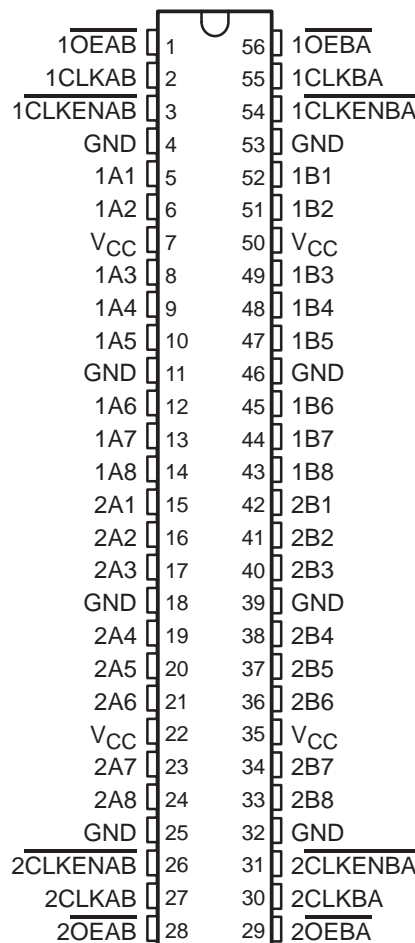
description

The 'ABT16952 are 16-bit registered transceivers that contain two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16952 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{CLKENAB}$ or $\overline{CLKENBA}$) input is low. Taking the output-enable (\overline{OEAB} or \overline{OEBA}) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16952 is characterized for operation over the full military temperature range of $-55^\circ C$ to $125^\circ C$. The SN74ABT16952 is characterized for operation from $-40^\circ C$ to $85^\circ C$.

SN54ABT16952 . . . WD PACKAGE
SN74ABT16952 . . . DGG OR DL PACKAGE
(TOP VIEW)



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 **TEXAS
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FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	
H	X	L	X	B_0^\ddagger
X	L	L	X	B_0^\ddagger
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar, but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

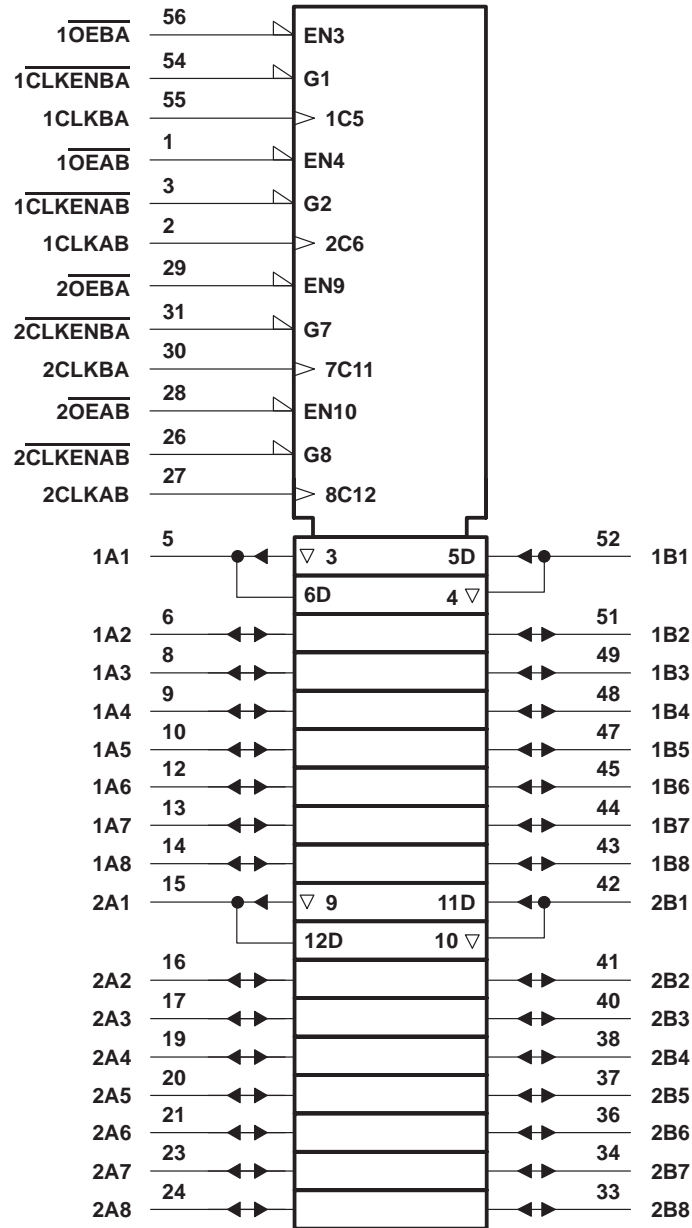
‡ Level of B before the indicated steady-state input conditions were established



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logic symbol†

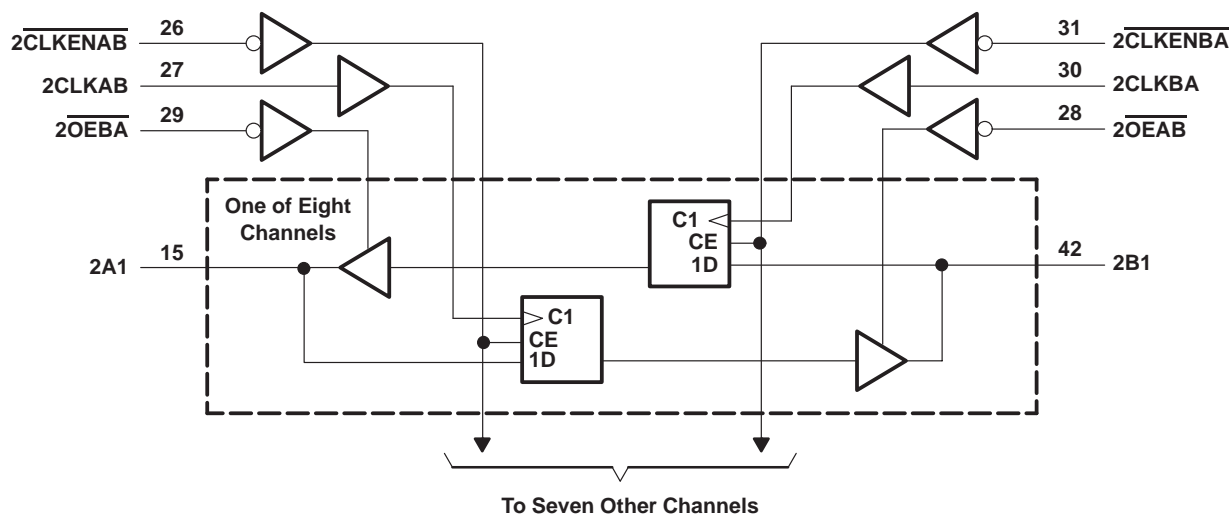
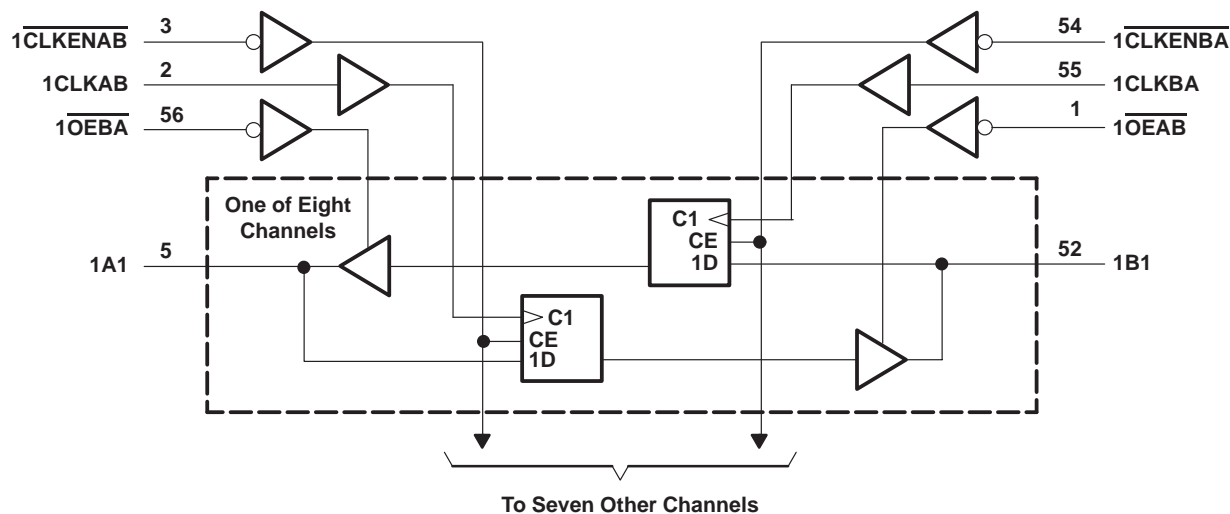


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16952	96 mA
SN74ABT16952	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16952		SN74ABT16952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT16952		SN74ABT16952		UNIT		
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA			2.5		2.5		2.5	V		
	V _{CC} = 5 V, I _{OH} = -3 mA			3		3		3			
	V _{CC} = 4.5 V	I _{OH} = -24 mA			2		2			2	
I _{OH} = -32 mA				2*				2			
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA				0.55		0.55	V		
		I _{OL} = 64 mA				0.55*		0.55			
V _{hys}				100					mV		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA	
	A or B ports				±100		±100		±100		
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V			50		50		50	μA		
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V			-50		-50		-50	μA		
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA		
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high				50		50	μA		
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V			-50	-100	-200		-50	-200	mA	
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			2		2		mA	
			Outputs low			35		35			35
			Outputs disabled			2		2			2
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			0.5		0.5		0.5	mA		
C _i	Control inputs	V _I = 2.5 V or 0.5 V			3				pF		
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V			8.5				pF		

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C		SN54ABT16952		SN74ABT16952		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	150	0	150	0	150	MHz
t _w †	Pulse duration, CLKAB or CLKBA high or low	3.3		3.3		3.3		ns
t _{su}	Setup time, before CLKAB↑ or CLKBA↑	A or B		3.5		3.5		ns
		CLKENAB or CLKENBA		3		3		
t _h	Hold time, after CLKAB↑ or CLKBA↑	A or B		1		1		ns
		CLKENAB or CLKENBA		1		1		

† This parameter is warranted, but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT16952		SN74ABT16952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			150			150		150		MHz
t _{PLH}	CLK	A or B	1	2.6	3.9	1	4.4	1	4.3	ns
t _{PHL}			1	2.6	4.2	1	4.6	1	4.5	
t _{PZH}	\overline{OE}	A or B	1	2.5	3.8	1	4.7	1	4.6	ns
t _{PZL}			1	2.8	5.1	1	6.1	1	6	
t _{PHZ}	\overline{OE}	A or B	1.7	3.4	4.7	1.7	6.1	1.7	5.5	ns
t _{PLZ}			1.3	3	3.9	1.3	4.8	1.3	4.2	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

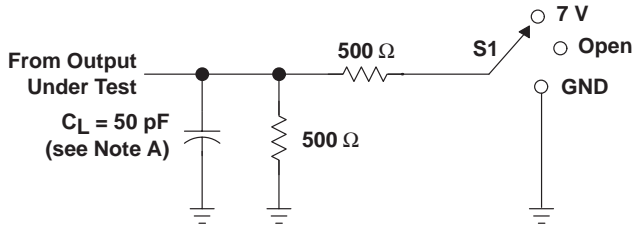


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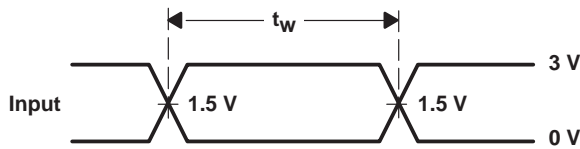
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PARAMETER MEASUREMENT INFORMATION

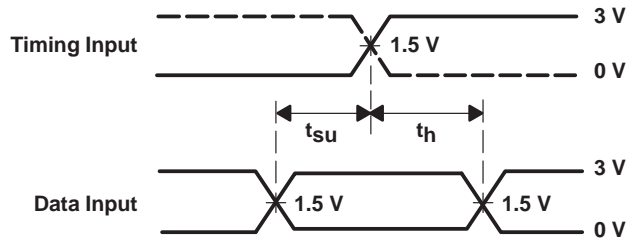


LOAD CIRCUIT

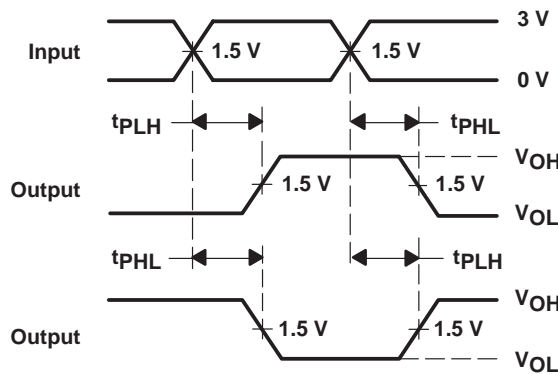
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



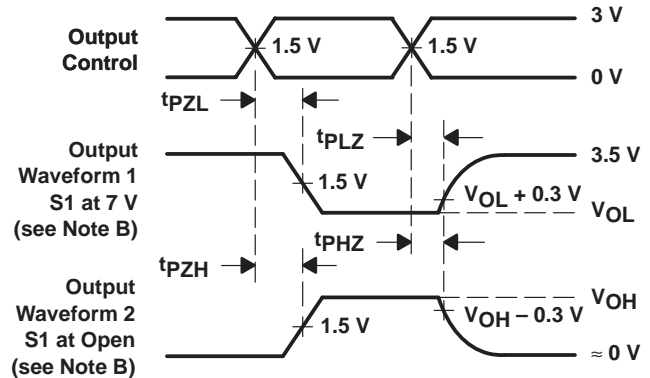
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT16952DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952	Samples
SN74ABT16952DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952	Samples
SN74ABT16952DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952	Samples
SN74ABT16952DLRG4	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16952DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT16952DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16952DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ABT16952DLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16952DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

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