TMUX1104 5V 低泄漏电流 4:1 精密多路复用器

1 特性

- 宽电源电压范围：1.08V 至 5.5V
- 低泄漏电流：3pA
- 低电荷注入：1.5pC
- 低导通电阻：2Ω
- 工作温度范围：-40°C 至 +125°C
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 轨至轨运行
- 双向信号路径
- 先断后合开关
- ESD 保护 HBM：2000V

2 应用

- 超声波扫描仪
- 患者监护和诊断
- 血糖监测仪
- 光纤网络
- 光学测试设备
- 远程无线电单元
- 有线网络
- 数据采集系统
- ATE 测试设备
- 工厂自动化和工业控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 声纳接收器
- 电池监控系统

3 说明

TMUX1104 是精密互补金属氧化物半导体 (CMOS) 多路复用器 (MUX)。TMUX1104 提供单通道 4:1 配置。1.08V 至 5.5V 的宽电源电压工作范围 可支持 医疗设备到工业系统的大量应用。该器件可在源极 (Sx) 和漏极 (D) 引脚上支持从 GND 到 V_{DD} 范围的双向模拟和数字信号。所有逻辑输入均具有兼容 1.8V 逻辑电平的阈值，当器件在有效电源电压范围内运行时，这些阈值可确保 TTL 和 CMOS 逻辑兼容性。失效防护逻辑 电路允许在电源引脚之前的控制引脚上施加电压，从而保护器件免受潜在的损害。

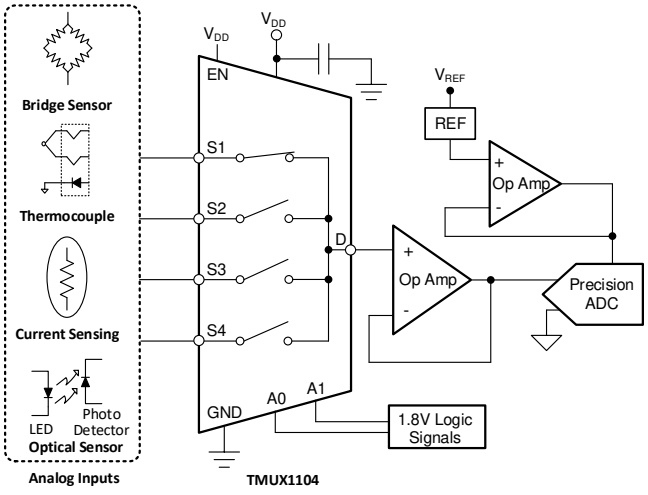
TMUX1104 是精密开关和多路复用器器件系列的一部分。这些器件具有非常低的导通和关断泄漏电流以及较低的电荷注入，因此可用于高精度测量 应用。5nA 的低电源电流和小型封装选项使其可用于便携式 应用。

器件信息(1)

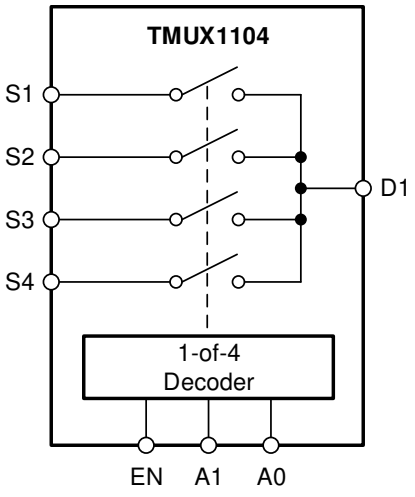
器件型号	封装	封装尺寸（标称值）
TMUX1104	VSSOP (10) (DGS)	3.00mm × 3.00mm
	USON (10) (DQA)	2.50mm x 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

简化电路原理图



方框图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2018) to Revision B **Page**

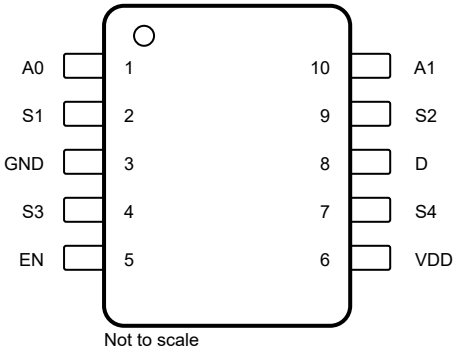
- 删除了*器件信息* 表中 DQA 封装的*产品预览* 说明 ... 1
- Deleted the *Product Preview* note from the DQA package in the *Pin Configuration and Functions* section ... 3
- Added DQA (USON) thermal values to *Thermal Information* ... 4

Changes from Original (November 2018) to Revision A **Page**

- 将文件状态从*预告信息* 更改为*生产组合* 数据 ... 1

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



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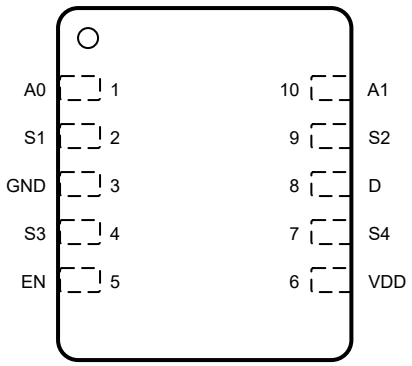
DQA Package
10-Pin USON
Top View



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Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DGS, DQA		
A0	1	I	Address line 0. Controls the switch configuration as shown in 表 1.
S1	2	I/O	Source pin 1. Can be an input or output.
GND	3	P	Ground (0 V) reference
S3	4	I/O	Source pin 3. Can be an input or output.
EN	5	I	Active high logic enable. When this pin is low, all switches are turned off. When this pin is high, the A[1:0] logic inputs determine which switch is turned on.
VDD	6	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
S4	7	I/O	Source pin 4. Can be an input or output.
D	8	I/O	Drain pin. Can be an input or output.
S2	9	I/O	Source pin 2. Can be an input or output.
A1	10	I	Address line 1. Controls the switch configuration as shown in 表 1.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	6	V
V_{SEL} or V_{EN}	Logic control input pin voltage (EN, A0, A1)	–0.5	6	V
I_{SEL} or I_{EN}	Logic control input pin current (EN, A0, A1)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–30	30	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive power supply voltage	1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V_{DD}	V
V_{SEL} or V_{EN}	Logic control input pin voltage	0		5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMUX1104		UNIT
		DGS (VSSOP)	DQA (USON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.9	173.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.1	99.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	116.5	73.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.0	8.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	114.6	73.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (V_{DD} = 5 V ±10 %)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		2	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.85		Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-Leakage Current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-Leakage Current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.75		0.75	nA
			–40°C to +125°C	–3.5		3.5	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 2.5 V Refer to On-Leakage Current	25°C	–0.025	±0.003	0.025	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.95		0.95	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 4.5 V / 1.5 V Refer to On-Leakage Current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.75		0.75	nA
			–40°C to +125°C	–3.5		3.5	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.005		µA
			–40°C to +125°C			1	µA

(1) When V_S is 4.5 V, V_D is 1.5 V, and vice versa.

Electrical Characteristics (V_{DD} = 5 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		14		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		12		ns
			–40°C to +85°C			17	ns
			–40°C to +125°C			18	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		5		ns
			–40°C to +85°C			8	ns
			–40°C to +125°C			9	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		155		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		28		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		35		pF

6.6 Electrical Characteristics (V_{DD} = 3.3 V ±10 %)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		3.7	8.8	Ω
			–40°C to +85°C			9.5	Ω
			–40°C to +125°C			9.8	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		1.9		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		2.2		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-Leakage Current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3 V Switch On V_D = V_S = 3 V / 1 V Refer to On-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.005		µA
			–40°C to +125°C			1	µA

(1) When V_S is 3 V, V_D is 1 V, and vice versa.

Electrical Characteristics (V_{DD} = 3.3 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		15		ns
			–40°C to +85°C			21	ns
			–40°C to +125°C			22	ns
t_{OPEN} (BBM)	Break before make time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		9		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		14		ns
			–40°C to +85°C			21	ns
			–40°C to +125°C			21	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		7		ns
			–40°C to +85°C			9	ns
			–40°C to +125°C			10	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		155		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		28		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		35		pF

6.7 Electrical Characteristics (V_{DD} = 1.8 V ±10 %)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.98 V Switch Off V_D = 1.62 V / 1 V V_S = 1 V / 1.62 V Refer to Off-Leakage Current	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.98 V Switch Off V_D = 1.62 V / 1 V V_S = 1 V / 1.62 V Refer to Off-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98 V Switch On V_D = V_S = 1.62 V / 1 V Refer to On-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.001		µA
			–40°C to +125°C			0.85	µA

(1) When V_S is 1.62 V, V_D is 1 V, and vice versa.

Electrical Characteristics (V_{DD} = 1.8 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		28		ns
			–40°C to +85°C			44	ns
			–40°C to +125°C			44	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		16		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		25		ns
			–40°C to +85°C			41	ns
			–40°C to +125°C			41	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		13		ns
			–40°C to +85°C			23	ns
			–40°C to +125°C			23	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		140		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		28		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		35		pF

6.8 Electrical Characteristics (V_{DD} = 1.2 V ±10 %)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1 V / 0.8 V V_S = 0.8 V / 1 V Refer to Off-Leakage Current	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1 V / 0.8 V V_S = 0.8 V / 1 V Refer to Off-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32 V Switch On V_D = V_S = 1 V / 0.8 V Refer to On-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.001		µA
			–40°C to +125°C			0.7	µA

(1) When V_S is 1 V, V_D is 0.8 V, and vice versa.

Electrical Characteristics (V_{DD} = 1.2 V ±10 %) (continued)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		55		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		28		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		50		ns
			–40°C to +85°C			175	ns
			–40°C to +125°C			175	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		35		ns
			–40°C to +85°C			135	ns
			–40°C to +125°C			135	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		125		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		32		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		40		pF

6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

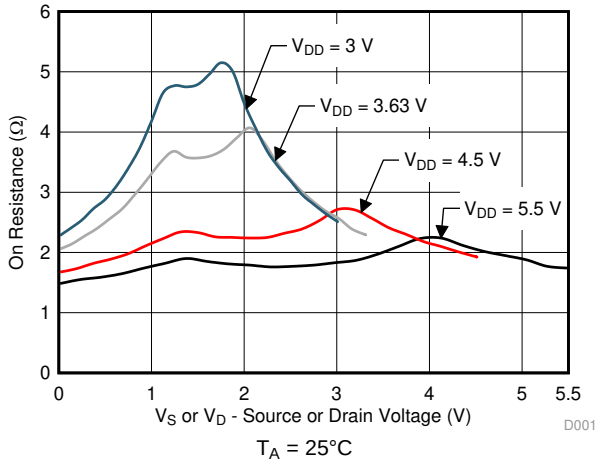


图 1. On-Resistance vs Source or Drain Voltage

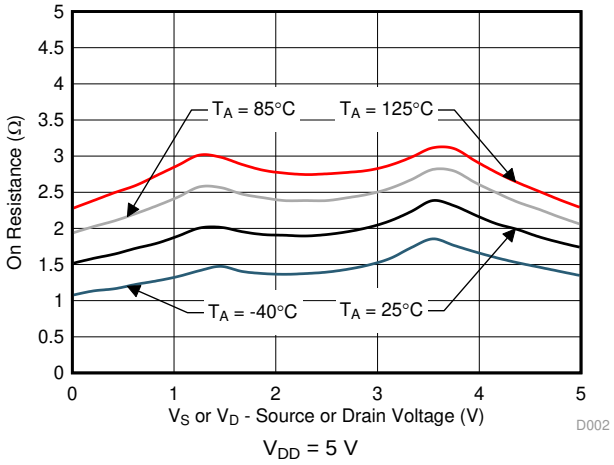


图 2. On-Resistance vs Temperature

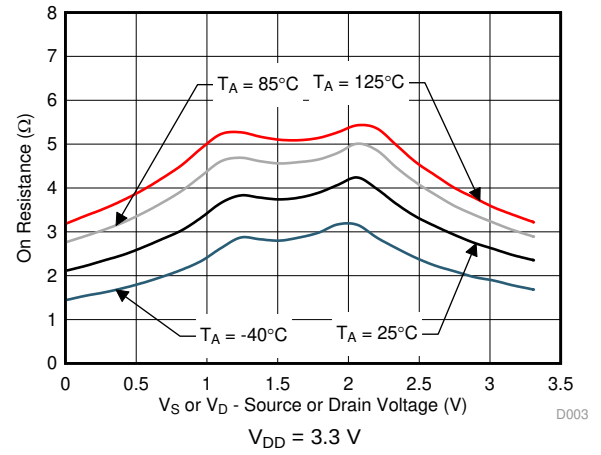


图 3. On-Resistance vs Temperature

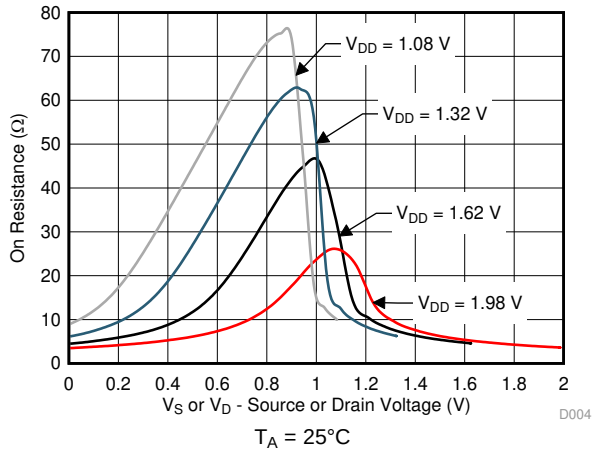


图 4. On-Resistance vs Source or Drain Voltage

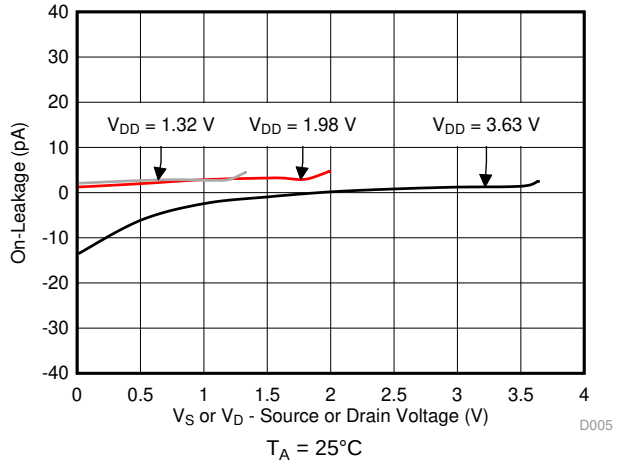


图 5. On-Leakage vs Source or Drain Voltage

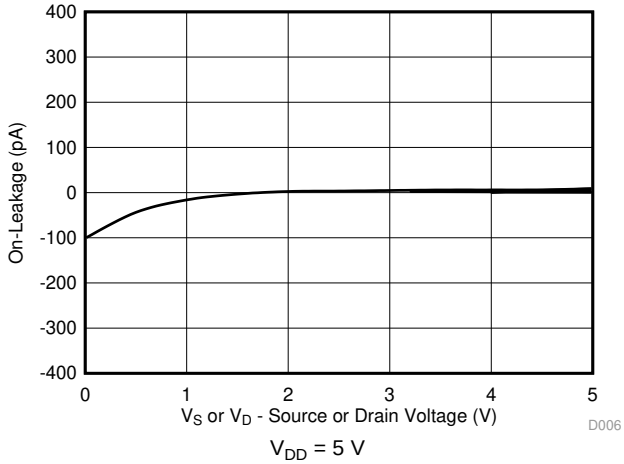
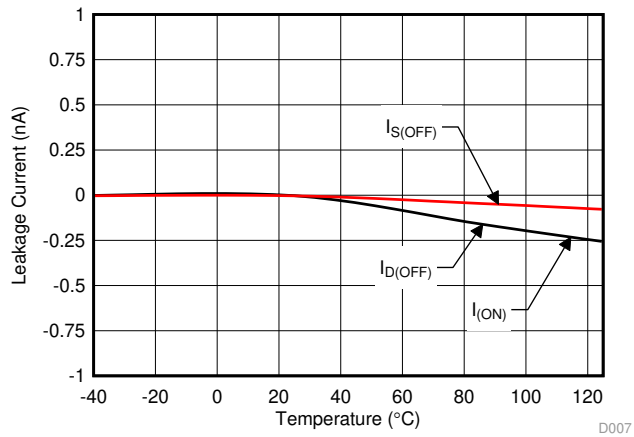


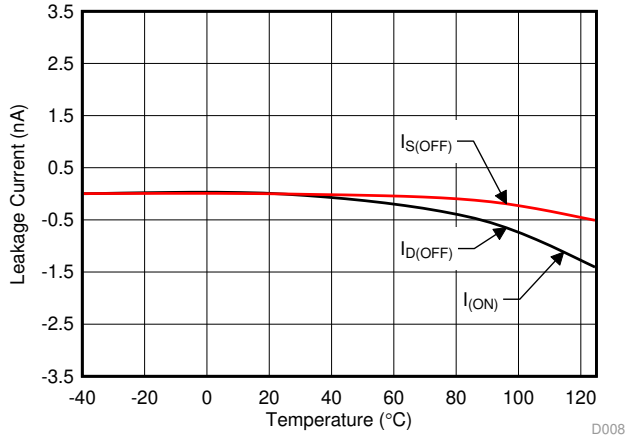
图 6. On-Leakage vs Source or Drain Voltage

Typical Characteristics (接下页)



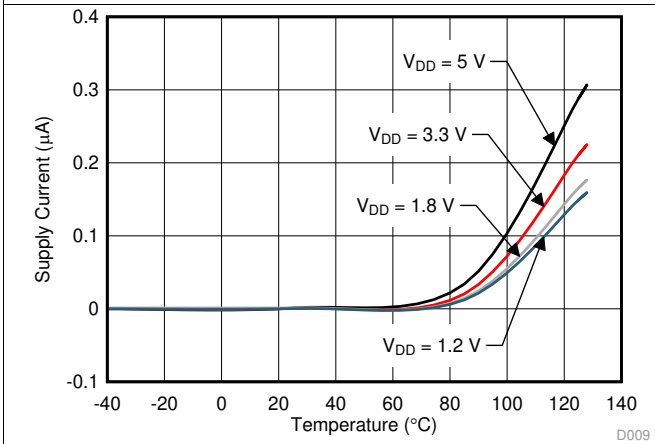
V_{DD} = 3.3 V

图 7. Leakage Current vs Temperature



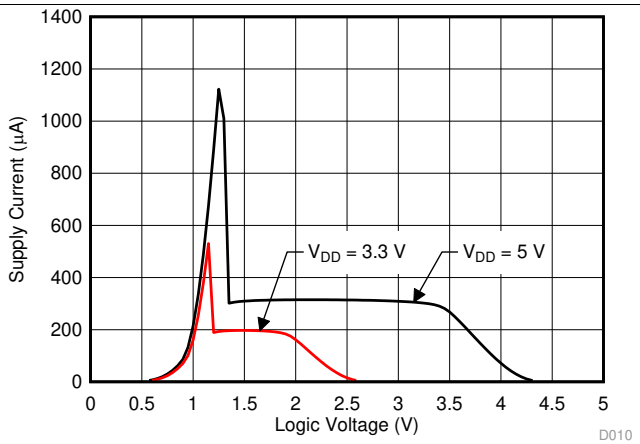
V_{DD} = 5 V

图 8. Leakage Current vs Temperature



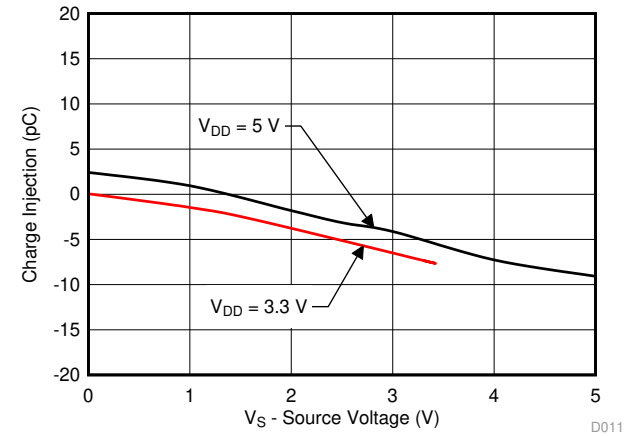
V_{SEL} = 5.5 V

图 9. Supply Current vs Temperature



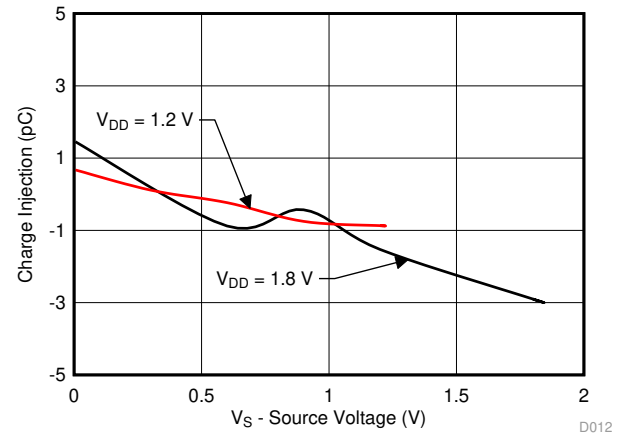
T_A = 25°C

图 10. Supply Current vs Logic Voltage



T_A = -40°C to 125°C

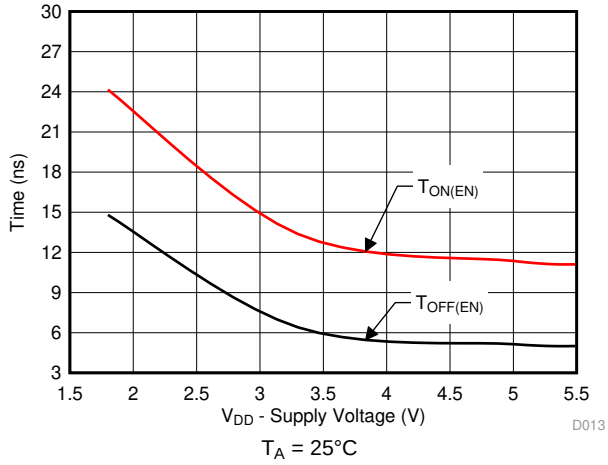
图 11. Charge Injection vs Source Voltage



T_A = -40°C to 125°C

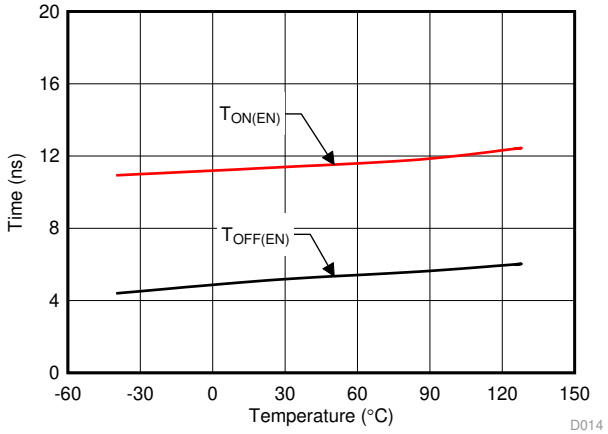
图 12. Charge Injection vs Source Voltage

Typical Characteristics (接下页)



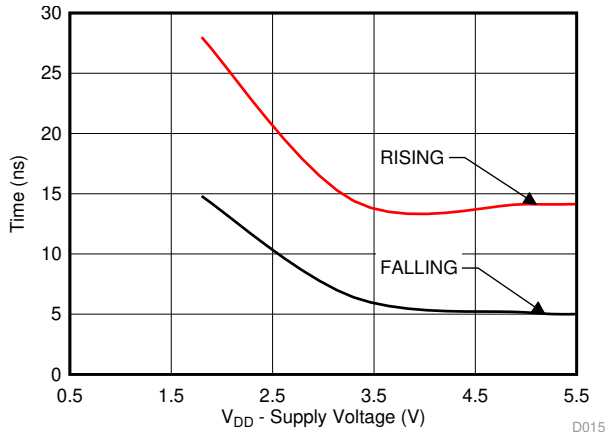
T_A = 25°C

图 13. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Supply Voltage



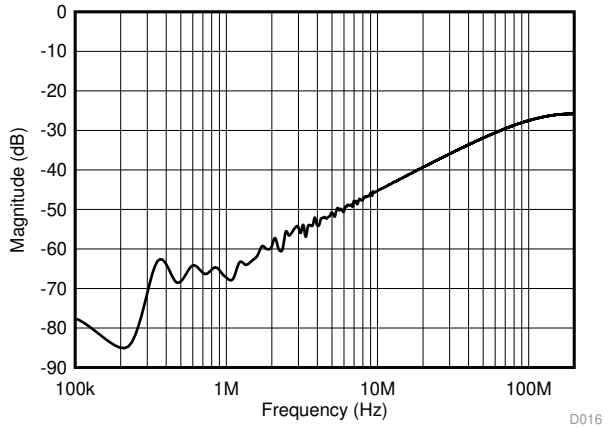
V_{DD} = 5 V

图 14. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Temperature



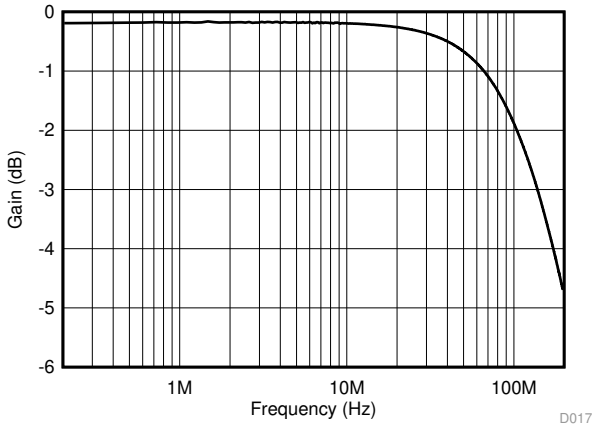
T_A = 25°C

图 15. Output $T_{TRANSITION}$ vs Supply Voltage



T_A = 25°C

图 16. Xtalk and Off-Isolation vs Frequency



T_A = 25°C

图 17. On Response vs Frequency

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 18. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

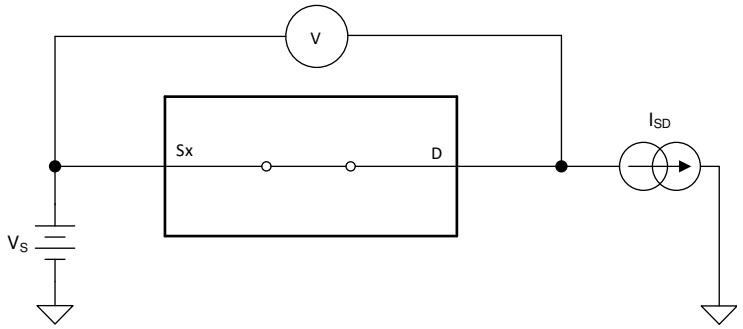


图 18. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 19.

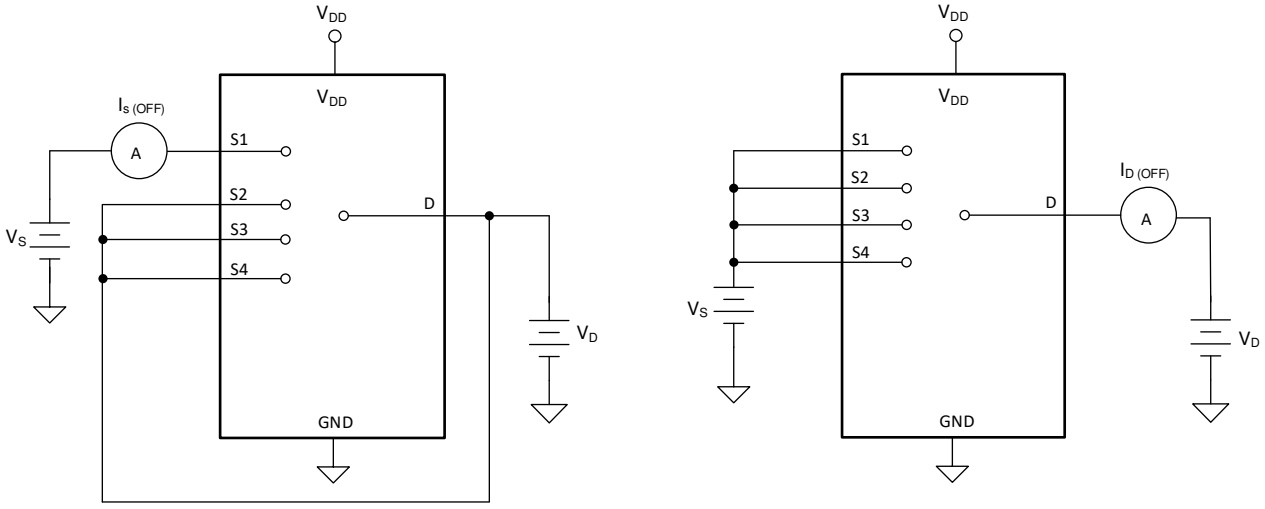


图 19. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 20 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

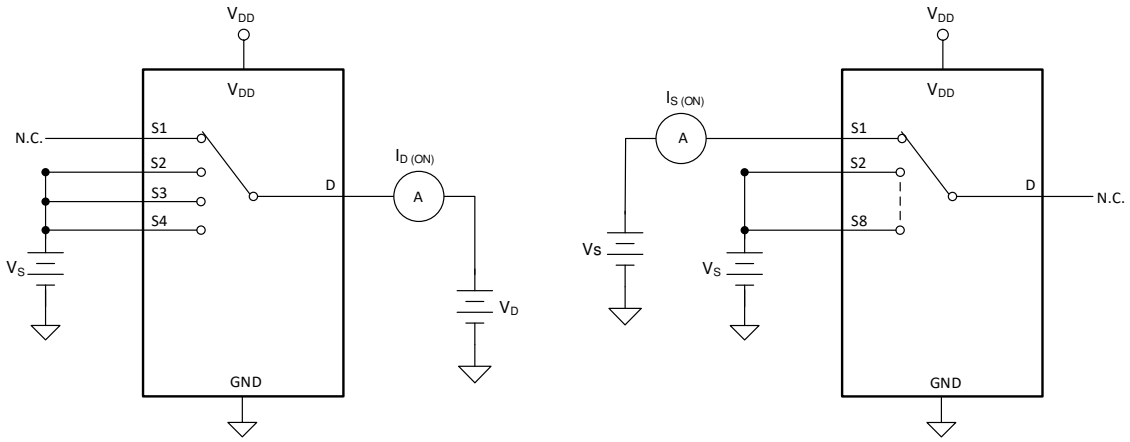


图 20. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 21 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

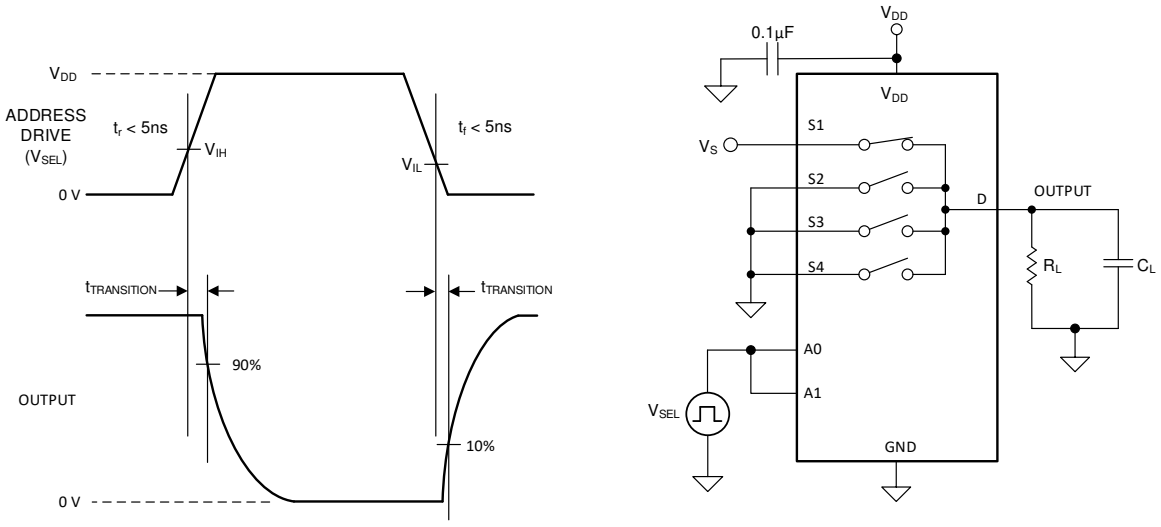


图 21. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 22 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

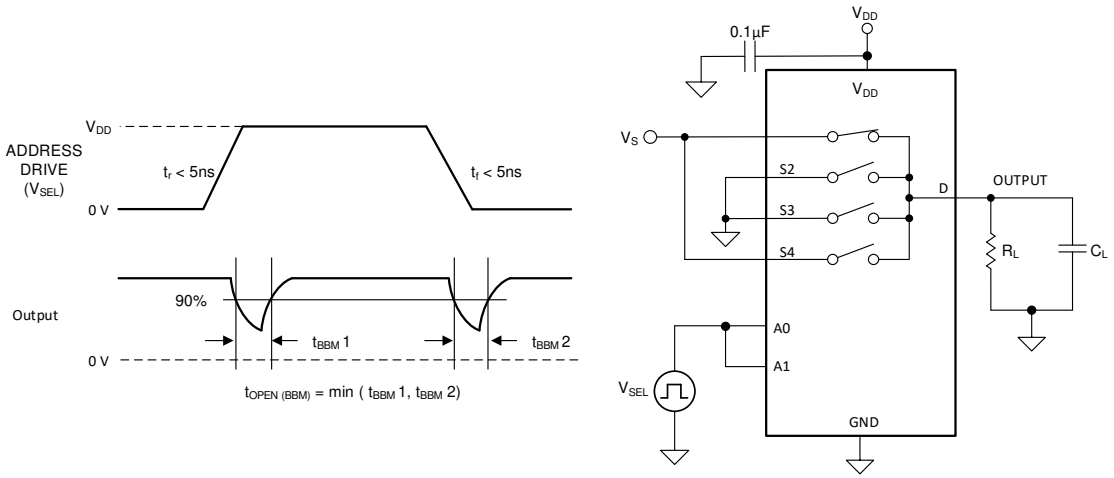


图 22. Break-Before-Make Delay Measurement Setup

7.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 23 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 23 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

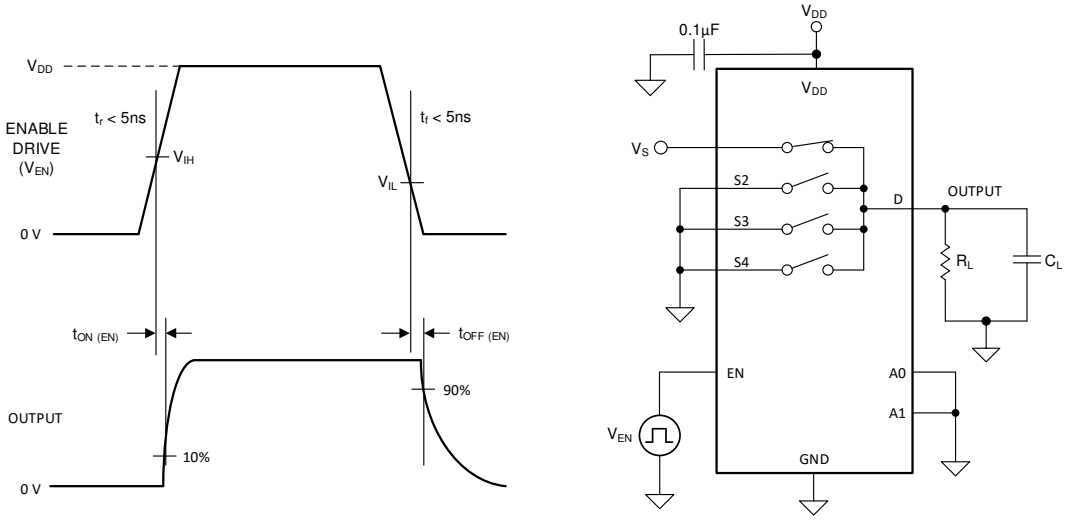


图 23. Turn-On and Turn-Off Time Measurement Setup

7.7 Charge Injection

The TMUX1104 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 图 24 shows the setup used to measure charge injection from source (Sx) to drain (D).

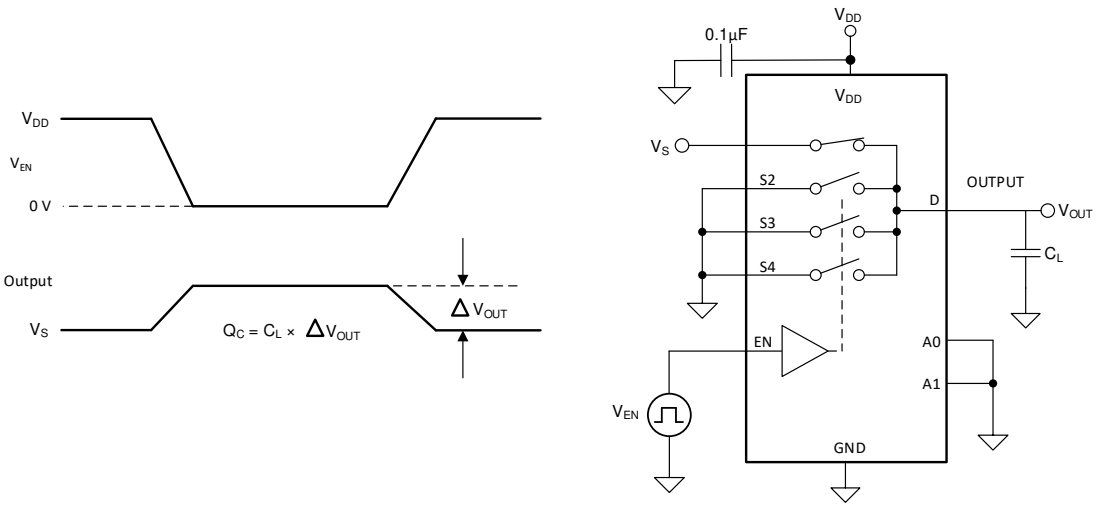


图 24. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 25 shows the setup used to measure, and the equation used to calculate off isolation.

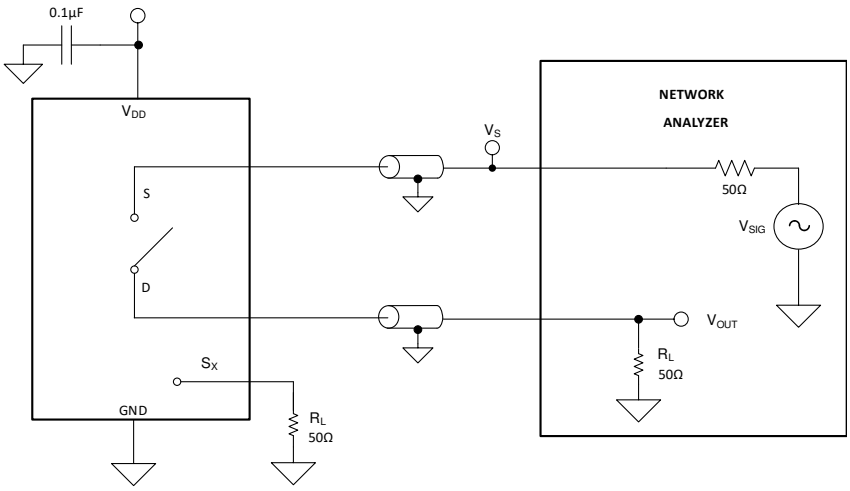


图 25. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 26 shows the setup used to measure, and the equation used to calculate crosstalk.

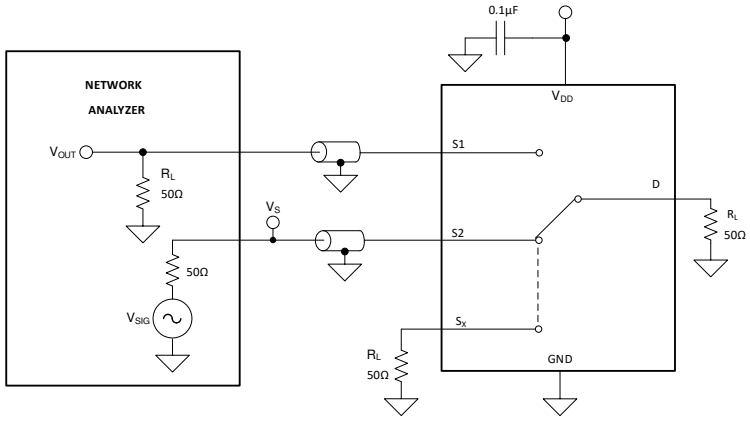


图 26. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 27 shows the setup used to measure bandwidth.

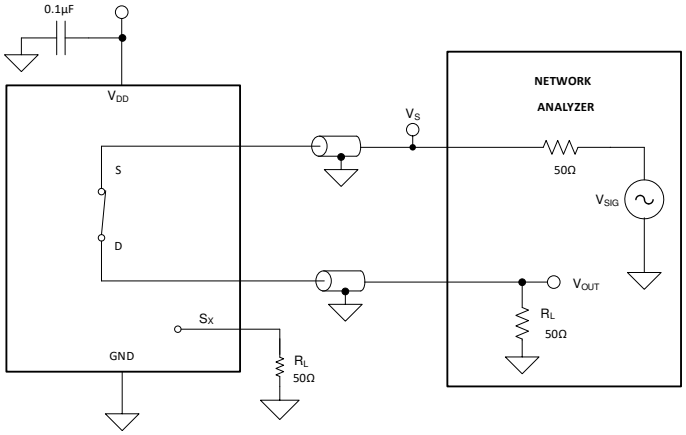


图 27. Bandwidth Measurement Setup

8 Detailed Description

8.1 Functional Block Diagram

The TMUX1104 is an 4:1, 1-channel (single-ended) multiplexer or demultiplexer. Each input is turned on or turned off based on the state of the address lines and enable pin.

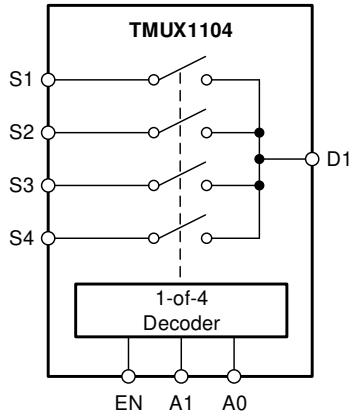


图 28. TMUX1104 Functional Block Diagram

8.2 Feature Description

8.2.1 Bidirectional Operation

The TMUX1104 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.2.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1104 ranges from GND to V_{DD}.

8.2.3 1.8 V Logic Compatible Inputs

The TMUX1104 has 1.8-V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allows the TMUX1104 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

8.2.4 Fail-Safe Logic

The TMUX1104 supports Fail-Safe Logic on the control input pins (EN, A0, A1) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1104 to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX1104 with V_{DD} = 1.2 V while allowing the select pins to interface with a logic level of another device up to 5.5 V.

Feature Description (接下页)

8.2.5 Ultra-low Leakage Current

The TMUX1104 provides extremely low on-leakage and off-leakage currents. The TMUX1104 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. 图 29 shows typical leakage currents of the TMUX1104 versus temperature.

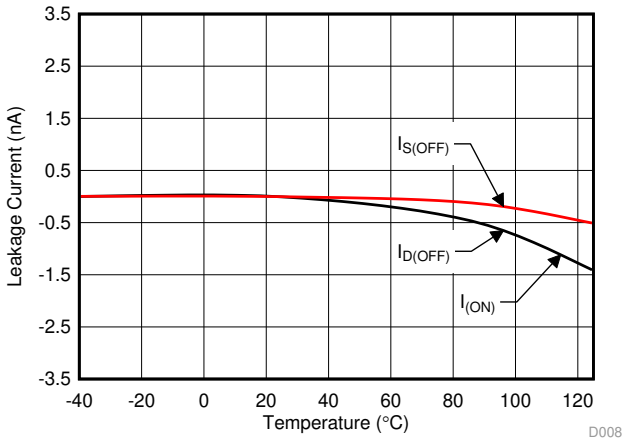


图 29. Leakage Current vs Temperature

8.2.6 Ultra-low Charge Injection

The TMUX1104 has a transmission gate topology, as shown in 图 30. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

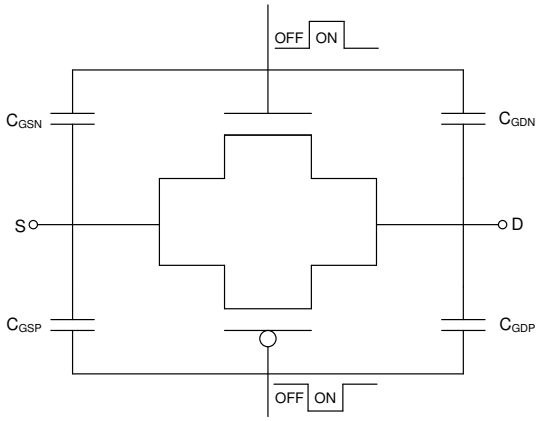


图 30. Transmission Gate Topology

Feature Description (接下页)

The TMUX1104 has special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to 1.5 pC at V_S = 1 V as shown in 图 31.

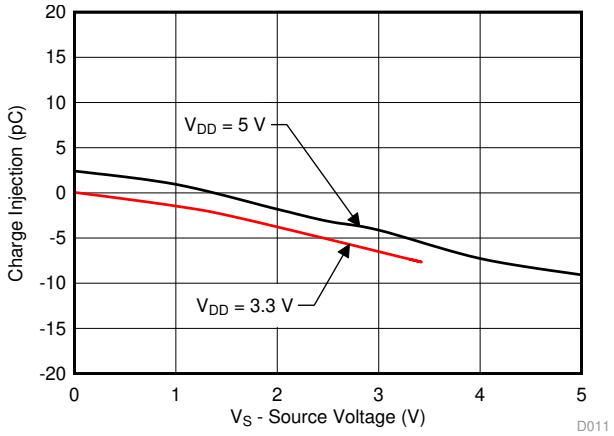


图 31. Charge Injection vs Source Voltage

8.3 Device Functional Modes

When the EN pin of the TMUX1104 is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state regardless of the state of the address lines. The control pins can be as high as 5.5 V.

8.4 Truth Tables

表 1 show the truth tables for the TMUX1104.

表 1. TMUX1104 Truth Table

EN	A1	A0	Selected Input Connected To Drain (D) Pin
0	X(1)	X(1)	All channels are off
1	0	0	S1
1	0	1	S2
1	1	0	S3
1	1	1	S4

(1) X denotes *don't care*.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX11xx family offers ulta-low input/output leakage currents and low charge injection. These devices operate up to 5.5 V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX1104 has a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

9.2 Typical Application

图 32 shows a 16-bit, 4 input, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion for precision measurements. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision amplifier, and a 4 input mux.

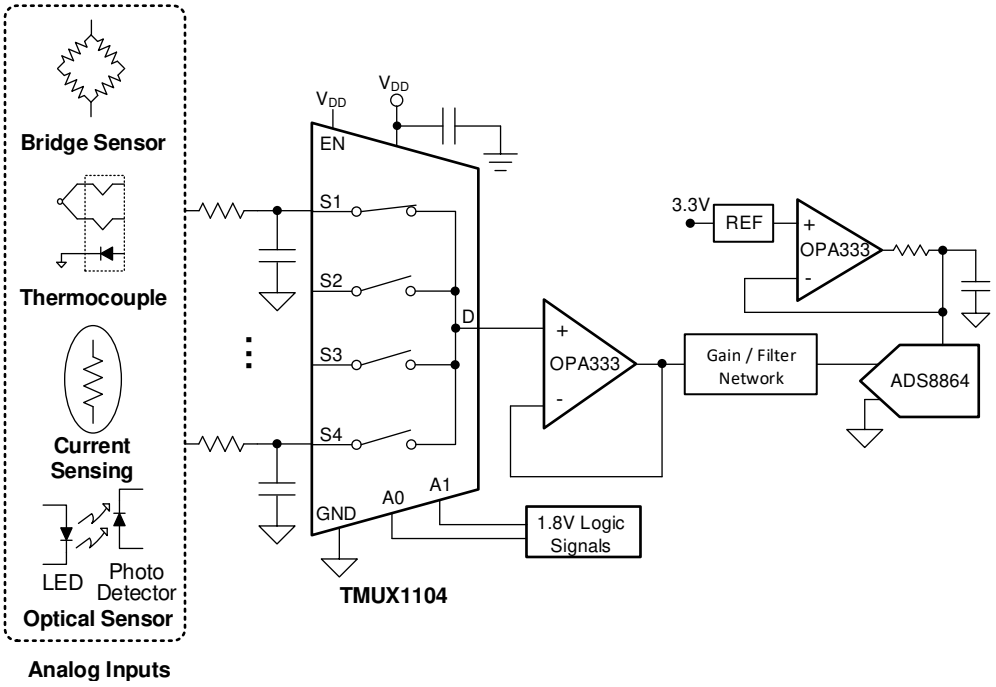


图 32. Multiplexing Signals to External ADC

9.3 Design Requirements

For this design example, use the parameters listed in 表 2.

表 2. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3 V
I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible

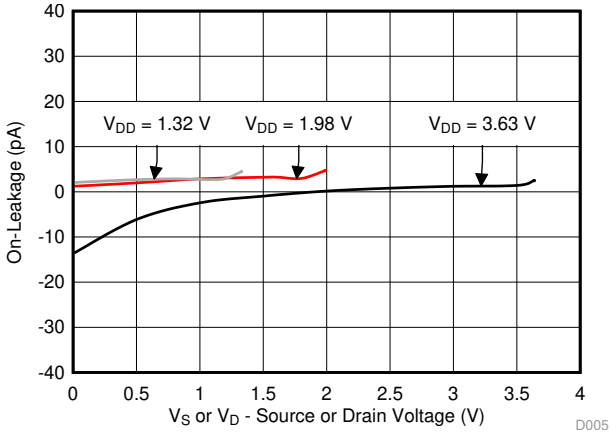
9.4 Detailed Design Procedure

The TMUX1104 can be operated without any external components except for the supply decoupling capacitors. If the desired power-up state is disabled, the enable pin should have a weak pull-down resistor and be controlled by the MCU via GPIO. All inputs being muxed to the ADC must fall within the recommend operating conditions of the TMUX1104, including signal range and continuous current. For this design with a supply of 3.3V the signal range can be 0 V to 3.3 V, and the max continuous current can be 30 mA.

The design example highlights a multiplexed data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in 图 32. The circuit is a multichannel data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, SAR ADC driver, and a reference buffer. The architecture provides a cost-effective solution for fast sampling of multiple channels using a single ADC.

9.5 Application Curve

The TMUX1104 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents.



T_A = 25°C

图 33. On-Leakage vs Source or Drain Voltage

10 Power Supply Recommendations

The TMUX1104 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.图 34 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

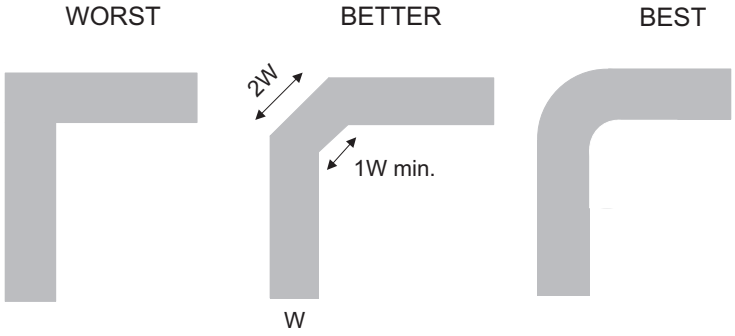


图 34. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 35 illustrates an example of a PCB layout with the TMUX1104. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

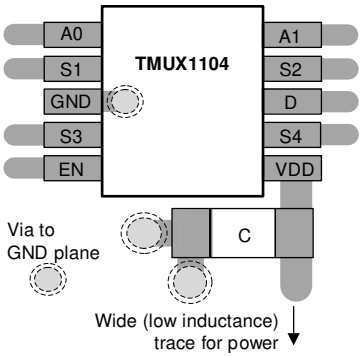


图 35. TMUX1104 Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

德州仪器 (TI)，*《真差分 4 x 2 多路复用器、模拟前端、同步采样 ADC 电路》*。

德州仪器 (TI)，*《使用低 CON 多路复用器改善稳定性问题》*。

德州仪器 (TI)，*《使用 1.8V 逻辑多路复用器和开关简化设计》*。

德州仪器 (TI)，*《利用关断保护信号开关消除电源排序》*。

德州仪器 (TI)，*《高电压模拟多路复用器的系统级保护》*。

德州仪器 (TI)，*《QFN/SON PCB 连接》*。

德州仪器 (TI)，*《四方扁平封装无引线逻辑封装》*。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1104DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1D7	Samples
TMUX1104DQAR	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	104	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

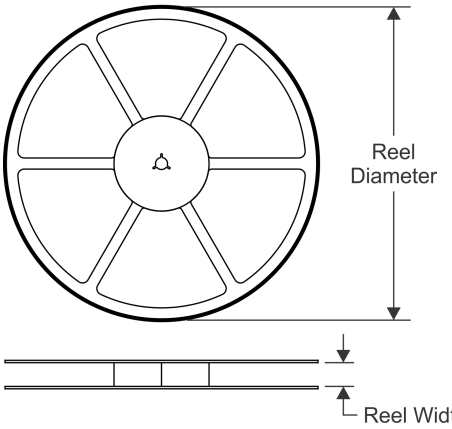
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

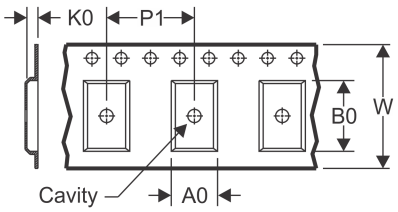
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

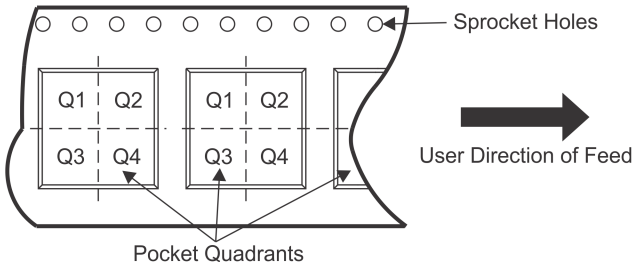


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

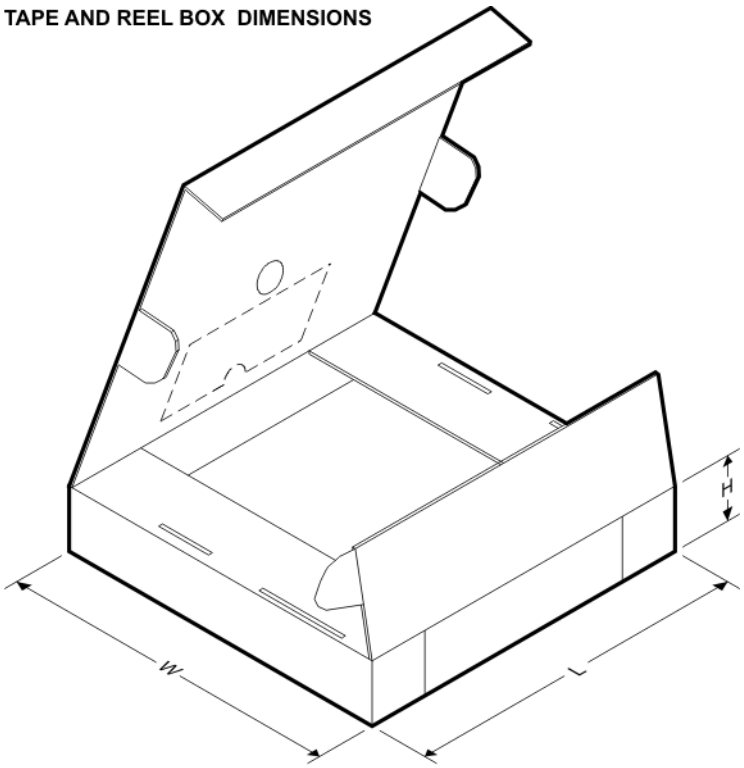
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1104DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMUX1104DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

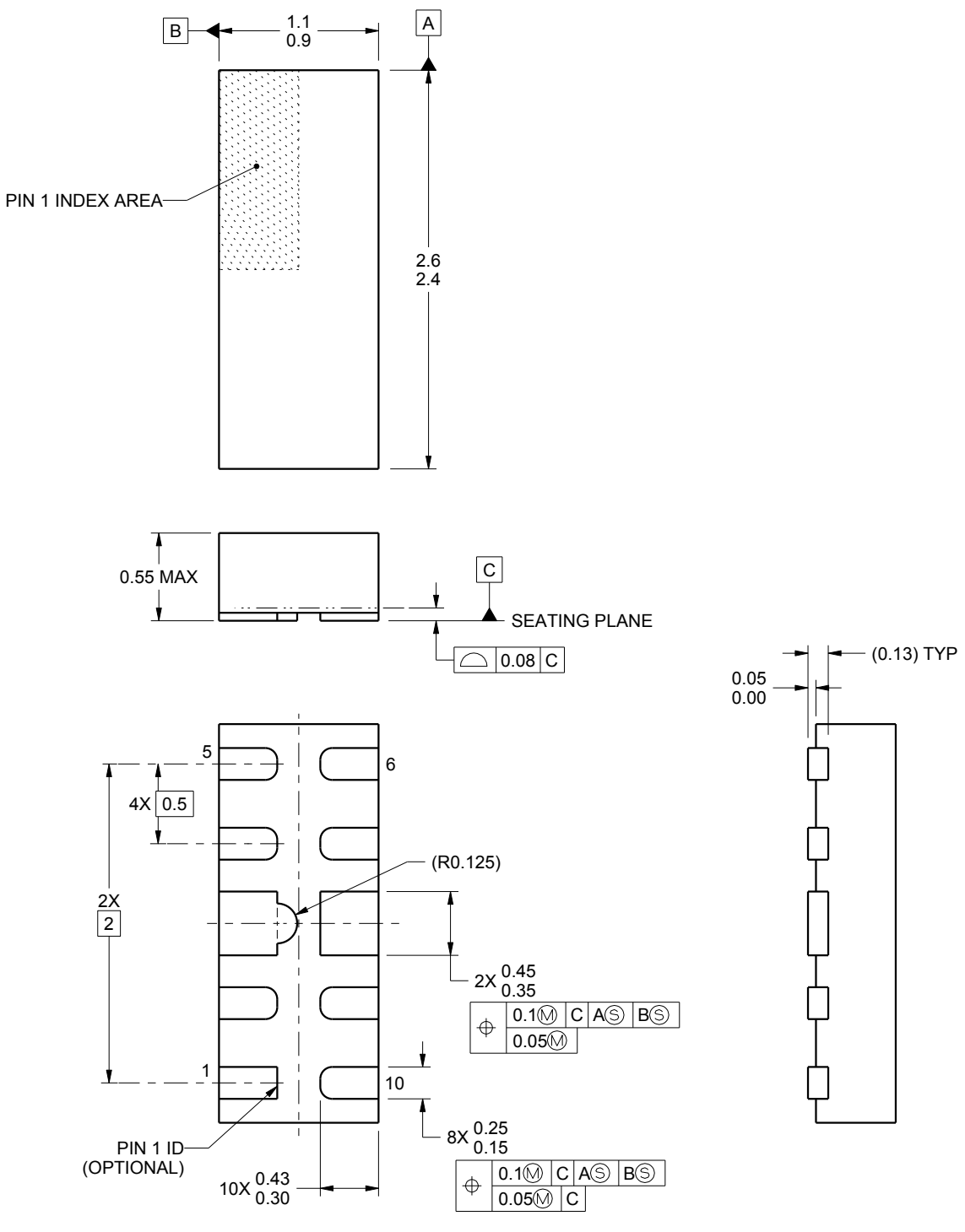
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1104DGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
TMUX1104DQAR	USON	DQA	10	3000	189.0	185.0	36.0

PACKAGE OUTLINE

DQA0010A

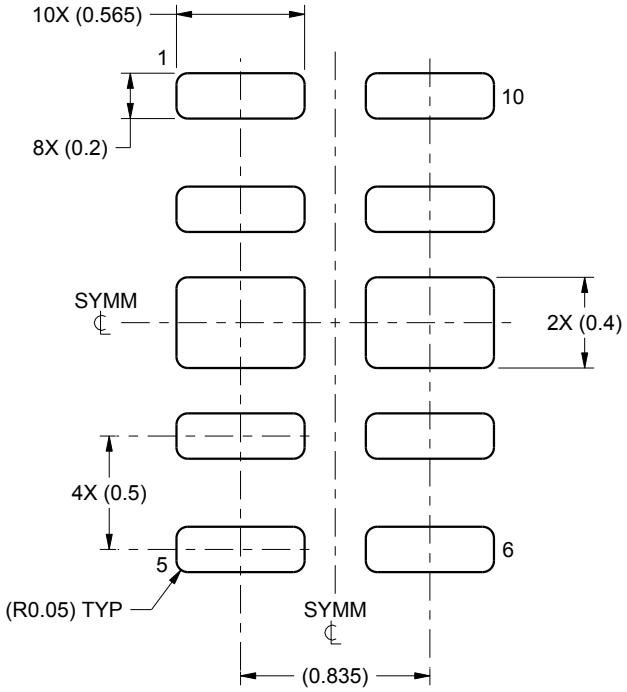
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

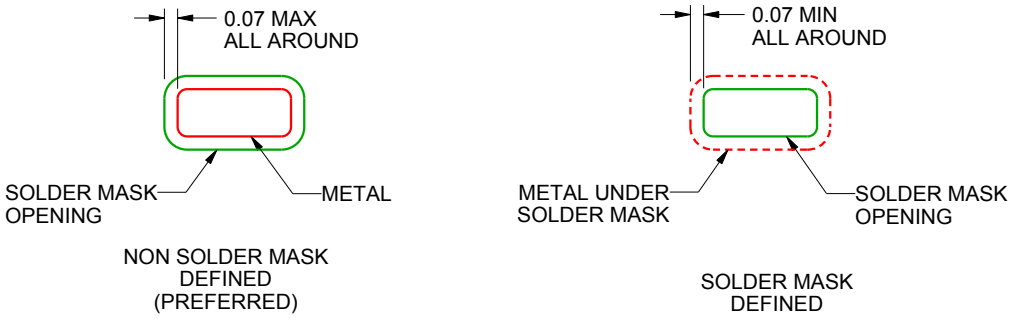


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

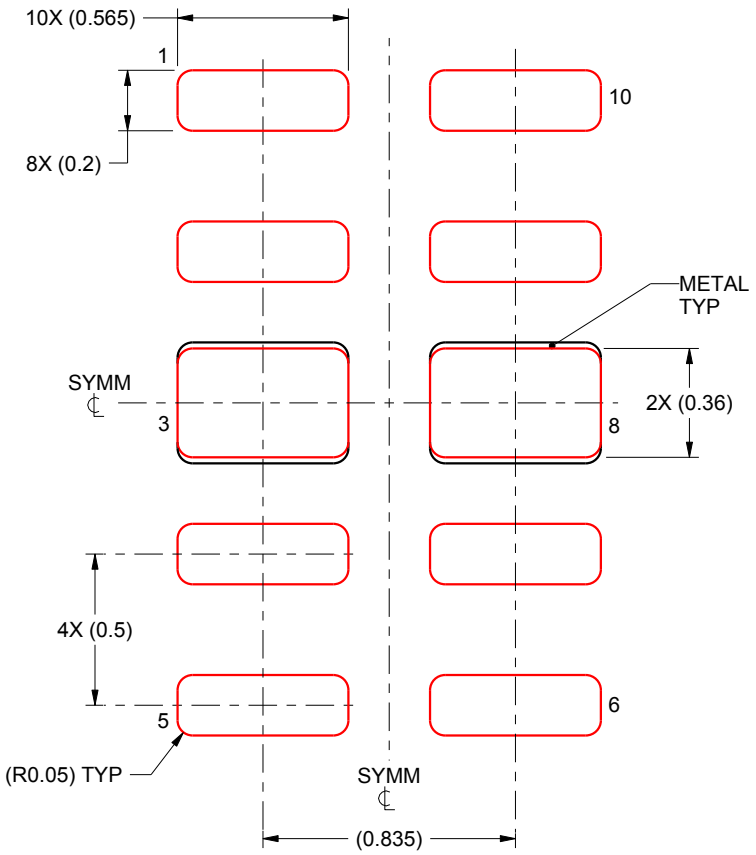
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

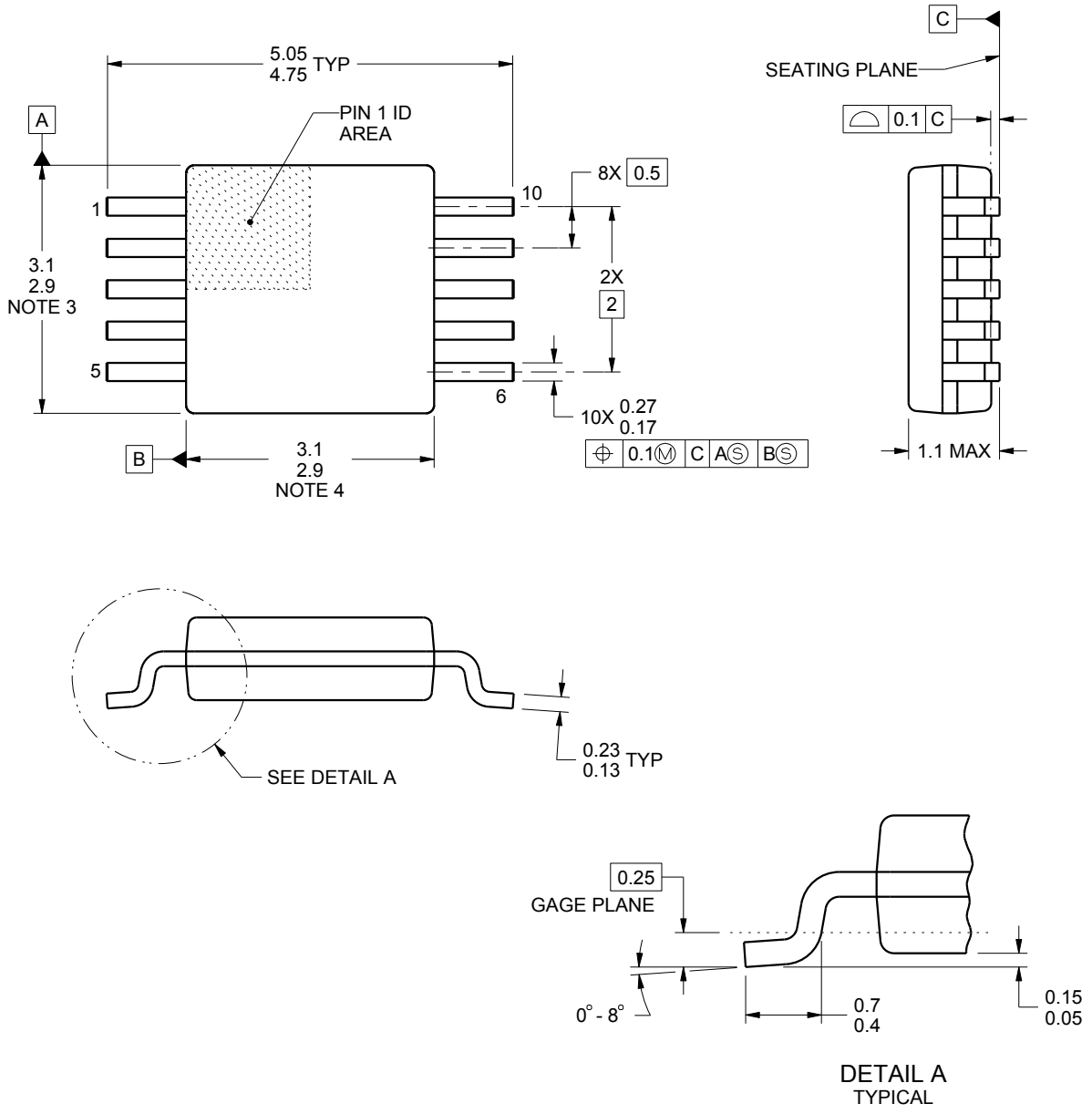
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

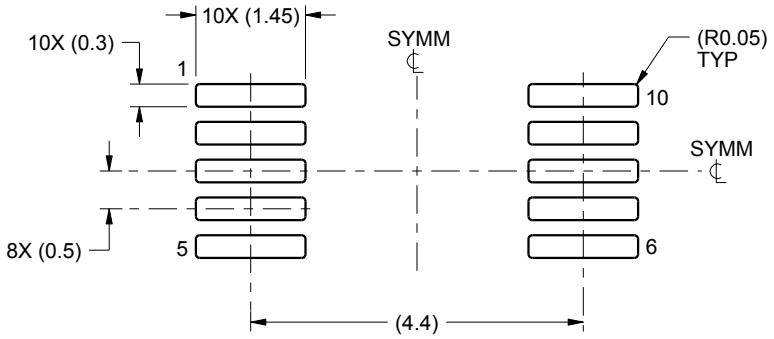
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

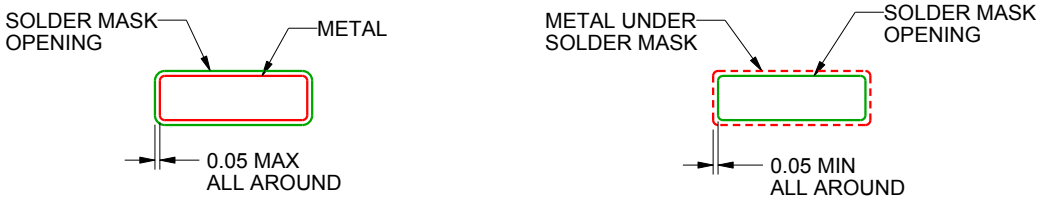


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

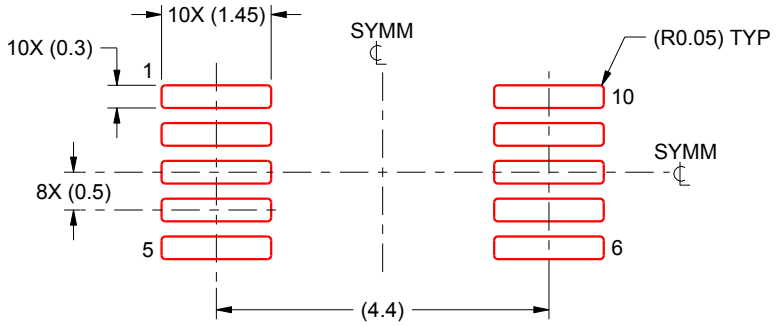


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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