

## AMC1302-Q1 精密、±50mV 输入、增强型隔离放大器

### 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1: - 40 °C 至 125 °C、T<sub>A</sub>
- ±50mV 输入电压范围，针对使用分流电阻器测量电流进行了优化
- 固定增益：41
- 低直流误差：
  - 失调电压误差：±50 μV (最大值)
  - 温漂：±0.8 μV/°C (最大值)
  - 增益误差：±0.2% (最大值)
  - 增益漂移：±35 ppm/°C (最大值)
  - 非线性度：0.03% (最大值)
- 高侧和低侧以 3.3V 或 5V 电压运行
- 失效防护输出
- 高 CMTI：100kV/μs (最小值)
- 低 EMI，符合 CISPR-11 和 CISPR-25 标准
- 安全相关认证：
  - 7071-V<sub>PK</sub> 增强型隔离，符合 DIN VDE V 0884-11：2017-01
  - 符合 UL1577 标准且长达 1 分钟的 5000V<sub>RMS</sub> 隔离

### 2 应用

- 基于分流电阻器的电流感应，可用于：
  - HEV/EV 充电桩
  - HEV/EV 车载充电器 (OBC)
  - HEV/EV 直流/直流转换器
  - HEV/EV 牵引逆变器

### 3 说明

AMC1302-Q1 是一款隔离式精密放大器，此放大器的输出与输入电路由抗电磁干扰性能极强的隔离层隔开。该隔离栅经认证可提供高达 5kV<sub>RMS</sub> 的增强型电隔离，符合 VDE V 0884-11 和 UL1577 标准，并且可支持最高 1.5kV<sub>RMS</sub> 的工作电压。

该隔离栅可将系统中以不同共模电压电平运行的各器件隔开，并保护电压较低的器件免受高电压冲击。

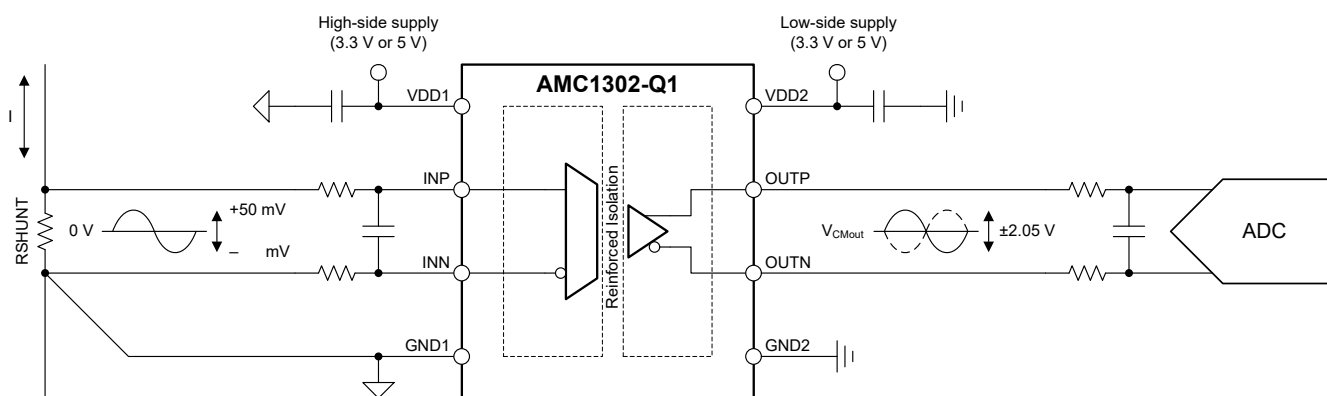
AMC1302-Q1 的输入针对直接连接低阻抗分流电阻器或其他具有低信号电位的低阻抗电压源的情况进行了优化。出色的直流精度和低温漂支持在 -40°C 至 +125°C 的整个汽车温度范围内，在 PFC 级、直流/直流转换器、牵引逆变器和 OBC 中进行精确的电流控制。

集成的无分流器和无高侧电源检测功能可简化系统级设计和诊断。

#### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
AMC1302-Q1	SOIC (8)	5.85mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用



## Table of Contents

<b>1 特性</b> .....	1	7.1 Overview.....	17
<b>2 应用</b> .....	1	7.2 Functional Block Diagram.....	17
<b>3 说明</b> .....	1	7.3 Feature Description.....	17
<b>4 Revision History</b> .....	2	7.4 Device Functional Modes.....	19
<b>5 Pin Configuration and Functions</b> .....	3	<b>8 Application and Implementation</b> .....	20
<b>6 Specifications</b> .....	4	8.1 Application Information.....	20
6.1 Absolute Maximum Ratings .....	4	8.2 Typical Application.....	20
6.2 ESD Ratings .....	4	8.3 What to Do and What Not to Do.....	22
6.3 Recommended Operating Conditions .....	4	<b>9 Power Supply Recommendations</b> .....	23
6.4 Thermal Information .....	5	<b>10 Layout</b> .....	24
6.5 Power Ratings .....	5	10.1 Layout Guidelines.....	24
6.6 Insulation Specification .....	6	10.2 Layout Example.....	24
6.7 Safety-Related Certifications .....	7	<b>11 Device and Documentation Support</b> .....	25
6.8 Safety Limiting Values .....	7	11.1 Device Support.....	25
6.9 Electrical Characteristics .....	8	11.2 Documentation Support.....	25
6.10 Switching Characteristics .....	9	11.3 接收文档更新通知.....	25
6.11 Timing Diagram.....	9	11.4 支持资源.....	25
6.12 Insulation Characteristics Curves.....	10	11.5 Trademarks.....	25
6.13 Typical Characteristics.....	11	11.6 静电放电警告.....	25
<b>7 Detailed Description</b> .....	17	11.7 术语表.....	25

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (October 2018) to Revision A (April 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式 .....	1
• 将安全相关认证特性项目符号中的 VDE 认证从“DIN V VDE V 0884-11 (VDE V 0884-11)”更改为 <i>DIN VDE V 0884-11</i> .....	1
• 将 CMTI 规格从 140kV/μs (典型值), 70kV/μs (最小值) 更改为 100kV/μs (最小值) (在特性部分) .....	1
• Changed C <sub>IO</sub> from ~1 pF to ~1.5 pF .....	6
• Changed V <sub>OS</sub> from - 100 μV / ±10 μV / 100 μV to - 50 μV / ±2.5 μV / 50 μV (min / typ / max).....	8
• Changed E <sub>G</sub> from - 0.3% / ±0.05% / 0.3% to - 0.2% / ±0.04% / 0.2% (min / typ / max) .....	8
• Changed TCE <sub>G</sub> from - 50 ppm/°C / ±15 ppm/°C / 50 ppm/°C to - 35 ppm/°C / ±3 ppm/°C / 35 ppm/°C (min / typ / max) .....	8
• Changed V <sub>Fail-safe</sub> from - 2.6 V / - 2.5 V (typ / max) to - 2.63 V / - 2.57 V / - 2.53 V (min / typ / max).....	8
• Changed CMTI from 55 kV/μs / 80 kV/μs to 100 kV/μs, 150 kV/μs (min / typ) .....	8
• Changed VDD1 <sub>POR</sub> from 1.75 V / 2.15 V / 2.7 V to 2.4 V / 2.6 V / 2.8 V (min / typ / max) .....	8
• Changed <i>Timing Diagram</i> .....	9
• Changed <i>Power-Supply Rejection Ratio vs Ripple Frequency</i> figure .....	11

## 5 Pin Configuration and Functions

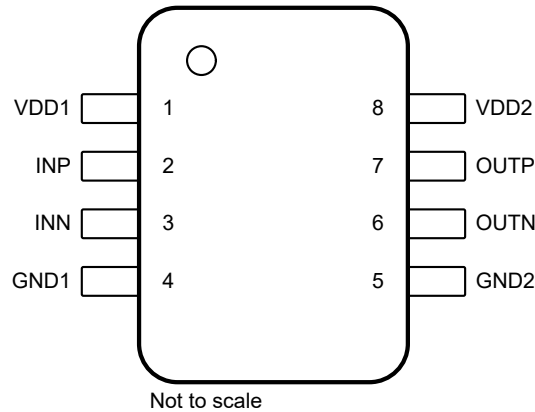


图 5-1. DWV Package, 8-Pin SOIC, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply. <sup>(1)</sup>
2	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage. <sup>(2)</sup>
3	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage. <sup>(2)</sup>
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply. <sup>(1)</sup>

- (1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.  
 (2) See the [Layout](#) section for details.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	- 0.3	6.5	V
	Low-side VDD2 to GND2	- 0.3	6.5	V
Analog input voltage	INP, INN	GND1 - 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 - 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	- 10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	- 65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> , HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
<b>POWER SUPPLY</b>						
	High-side power supply	VDD1 to GND1	3	5	5.5	V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
<b>ANALOG INPUT</b>						
V <sub>Clipping</sub>	Differential input voltage before clipping output	V <sub>IN</sub> = V <sub>INP</sub> - V <sub>INN</sub>		±64		mV
V <sub>F<sub>SR</sub></sub>	Specified linear differential full-scale voltage	V <sub>IN</sub> = V <sub>INP</sub> - V <sub>INN</sub>	- 50		50	mV
V <sub>CM</sub>	Operating common-mode input voltage	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to GND1	- 0.032	VDD1 - 2.2		V
<b>TEMPERATURE RANGE</b>						
T <sub>A</sub>	Operating ambient temperature		- 55		125	°C
	Specified ambient temperature		- 40		125	

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		AMC1302-Q1	UNIT
		DWV (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	4.8	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$P_D$	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
$P_{D1}$	Maximum power dissipation (high-side)	VDD1 = 3.6 V	31	mW
		VDD1 = 5.5 V	54	
$P_{D2}$	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

## 6.6 Insulation Specification

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
<b>GENERAL</b>				
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	≥ 8.5	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance) of the double isolation (2 x 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>	I-III	
<b>DIN V VDE 0884-11 (VDE V 0884-11): 2017-01<sup>(2)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage	2121	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave)	1500	V <sub>RMS</sub>
		DC voltage	2121	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification test)	7071	V <sub>PK</sub>
		V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 1 s (100% production test)	8485	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(1)</sup>	Test method per IEC 60065, 1.2/50 μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 12800 V <sub>PK</sub> (qualification)	8000	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(3)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> = 2545 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> = 3394 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> = 3977 V <sub>PK</sub> , t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(4)</sup>	V <sub>IO</sub> = 0.4 × sin(2πft), f = 1 MHz	~1.5	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(4)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		55/125/21	
<b>UL 1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 5000 V <sub>RMS</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 6000 V <sub>RMS</sub> , t = 1 s (100% production)	5000	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (4) All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	Certificate number: E181974

## 6.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_S$	Safety input, output, or supply current	$R_{\theta JA} = 85.4^\circ\text{C}/\text{W}$ , $V_{DDX} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$			266	mA
$I_S$	Safety input, output, or supply current	$R_{\theta JA} = 85.4^\circ\text{C}/\text{W}$ , $V_{DDX} = 3.6\text{ V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$			407	mA
$P_S$	Safety input, output, or total power	$R_{\theta JA} = 85.4^\circ\text{C}/\text{W}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$			1464	mW
$T_S$	Maximum safety temperature				150	$^\circ\text{C}$

- (1) The maximum safety temperature,  $T_S$ , has the same value as the maximum junction temperature,  $T_J$ , specified for the device. The  $I_S$  and  $P_S$  parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of  $I_S$  and  $P_S$ . These limits vary with the ambient temperature,  $T_A$ .

The junction-to-air thermal resistance,  $R_{\theta JA}$ , in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

$T_{J(\text{max})} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(\text{max})}$  is the maximum junction temperature.

$P_S = I_S \times V_{DD\text{max}}$ , where  $V_{DD\text{max}}$  is the maximum supply voltage for high-side and low-side.

## 6.9 Electrical Characteristics

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $\text{INP} = -50\text{ mV}$  to  $+50\text{ mV}$ , and  $\text{INN} = \text{GND1}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ , and  $V_{DD2} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
$V_{\text{CMov}}$	Common-mode overvoltage detection level	$(V_{\text{INP}} + V_{\text{INN}}) / 2$ to GND1	$V_{\text{DD1}} - 2$			V
	Hysteresis of common-mode overvoltage detection level		60			mV
$V_{\text{OS}}$	Input offset voltage <sup>(1)</sup>	$T_A = 25^\circ\text{C}$ , $V_{\text{INP}} = V_{\text{INN}} = \text{GND1}$	- 50	$\pm 2.5$	50	$\mu\text{V}$
$\text{TCV}_{\text{OS}}$	Input offset drift <sup>(1)</sup>		- 0.8	$\pm 0.15$	0.8	$\mu\text{V}/^\circ\text{C}$
CMRR	Common-mode rejection ratio	$f_{\text{IN}} = 0\text{ Hz}$ , $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$	- 100			dB
		$f_{\text{IN}} = 10\text{ kHz}$ , $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$	- 98			
$C_{\text{IN}}$	Single-ended input capacitance <sup>(2)</sup>	$\text{INN} = \text{GND1}$ , $f_{\text{IN}} = 300\text{ kHz}$	4			pF
$C_{\text{IND}}$	Differential input capacitance <sup>(2)</sup>	$f_{\text{IN}} = 300\text{ kHz}$	2			
$R_{\text{IN}}$	Single-ended input resistance <sup>(2)</sup>	$\text{INN} = \text{GND1}$	4.75			k $\Omega$
$R_{\text{IND}}$	Differential input resistance <sup>(2)</sup>		4.9			
$I_{\text{IB}}$	Input bias current	$\text{INP} = \text{INN} = \text{GND1}$ ; $I_{\text{IB}} = (I_{\text{IBP}} + I_{\text{IBN}}) / 2$	- 48.5	- 36	- 28.5	$\mu\text{A}$
$\text{TCI}_{\text{IB}}$	Input bias current drift		$\pm 1.5$			$\text{nA}/^\circ\text{C}$
$I_{\text{IO}}$	Input offset current	$I_{\text{IO}} = I_{\text{IBP}} - I_{\text{IBN}}$	$\pm 10$			nA
<b>ANALOG OUTPUT</b>						
	Nominal gain		41			
$E_{\text{G}}$	Gain error <sup>(1)</sup>	$T_A = 25^\circ\text{C}$	- 0.2%	$\pm 0.04\%$	0.2%	
$\text{TCE}_{\text{G}}$	Gain error drift <sup>(1)</sup>		- 35	$\pm 3$	35	$\text{ppm}/^\circ\text{C}$
	Nonlinearity <sup>(1)</sup>		- 0.03%	$\pm 0.01\%$	0.03%	
	Nonlinearity drift		1			$\text{ppm}/^\circ\text{C}$
THD	Total harmonic distortion	$f_{\text{IN}} = 10\text{ kHz}$	- 85			dB
	Output noise	$\text{INP} = \text{INN} = \text{GND1}$ , $f_{\text{IN}} = 0\text{ Hz}$ , $\text{BW} = 100\text{ kHz}$ brickwall filter	260			$\mu\text{V}_{\text{RMS}}$
SNR	Signal-to-noise ratio	$f_{\text{IN}} = 1\text{ kHz}$ , $\text{BW} = 10\text{ kHz}$	80	84		dB
		$f_{\text{IN}} = 10\text{ kHz}$ , $\text{BW} = 100\text{ kHz}$	70			
PSRR	Power-supply rejection ratio <sup>(3)</sup>	PSRR vs $V_{\text{DD1}}$ , at DC	- 113			dB
		PSRR vs $V_{\text{DD1}}$ , 100-mV and 10-kHz ripple	- 108			
		PSRR vs $V_{\text{DD2}}$ , at DC	- 116			
		PSRR vs $V_{\text{DD2}}$ , 100-mV and 10-kHz ripple	- 87			
$V_{\text{CMout}}$	Common-mode output voltage		1.39	1.44	1.49	V
$V_{\text{CLIPout}}$	Clipping differential output voltage	$V_{\text{OUT}} = (V_{\text{OUTP}} - V_{\text{OUTN}})$ ; $ V_{\text{IN}}  =  V_{\text{INP}} - V_{\text{INN}}  >  V_{\text{Clipping}} $	- 2.52	$\pm 2.49$	2.52	V
$V_{\text{Failsafe}}$	Failsafe differential output voltage	$V_{\text{CM}} \geq V_{\text{CMov}}$ , or $V_{\text{DD1}}$ missing	- 2.63	- 2.57	- 2.53	V
BW	Output bandwidth		220	280		kHz
$R_{\text{OUT}}$	Output resistance	On $\text{OUTP}$ or $\text{OUTN}$	< 0.2			$\Omega$
	Output short-circuit current	On $\text{OUTP}$ or $\text{OUTN}$ , sourcing or sinking, $\text{INN} = \text{INP} = \text{GND1}$ , outputs shorted to either $\text{GND2}$ or $V_{\text{DD2}}$	$\pm 14$			mA
CMTI	Common-mode transient immunity	$ \text{GND1} - \text{GND2}  = 1\text{ kV}$	100	150		$\text{kV}/\mu\text{s}$

## 6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $\text{INP} = -50\text{ mV}$  to  $+50\text{ mV}$ , and  $\text{INN} = \text{GND1}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ , and  $V_{DD2} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$V_{DD1\text{POR}}$	VDD1 power-on-reset threshold voltage	VDD1 falling	2.4	2.6	2.8	V
IDD1	High-side supply current	$3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$		6.2	8.5	mA
		$4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$		7.2	9.8	
IDD2	Low-side supply current	$3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$		5.3	7.2	
		$4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$		5.9	8.1	

- (1) The typical value includes one sigma statistical variation.
- (2) Also see the Analog Input section for more details.
- (3) This parameter is output referred.

## 6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output signal rise time			1.5		$\mu\text{s}$
$t_f$	Output signal fall time			1.5		$\mu\text{s}$
	$V_{\text{INx}}$ to $V_{\text{OUTx}}$ signal delay (50% - 10%)	unfiltered output		1	1.5	$\mu\text{s}$
	$V_{\text{INx}}$ to $V_{\text{OUTx}}$ signal delay (50% - 50%)	unfiltered output		1.6	2.1	$\mu\text{s}$
	$V_{\text{INx}}$ to $V_{\text{OUTx}}$ signal delay (50% - 90%)	unfiltered output		2.5	3	$\mu\text{s}$
$t_{\text{AS}}$	Analog settling time	VDD1 step to 3.0 V with $V_{DD2} \geq 3.0\text{ V}$ , to $\text{OUTP}$ and $\text{OUTN}$ valid, 0.1% settling		500		$\mu\text{s}$

## 6.11 Timing Diagram

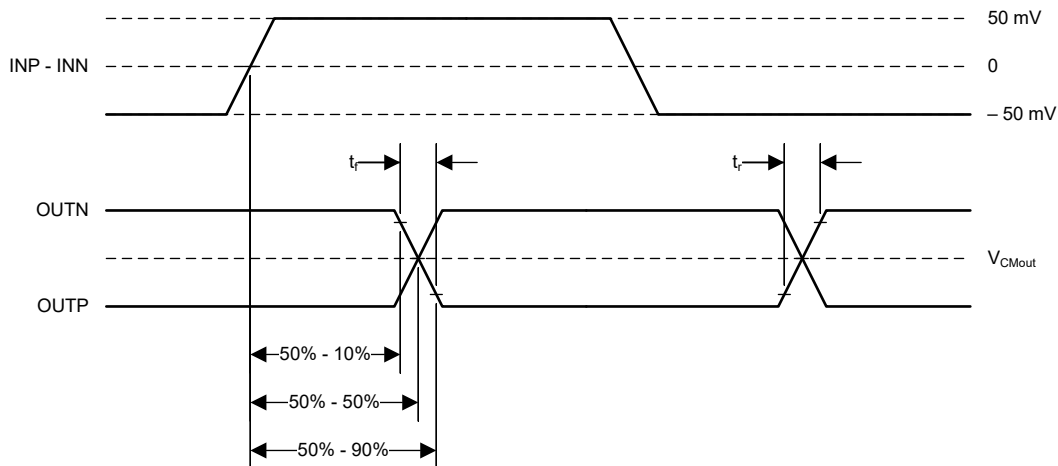
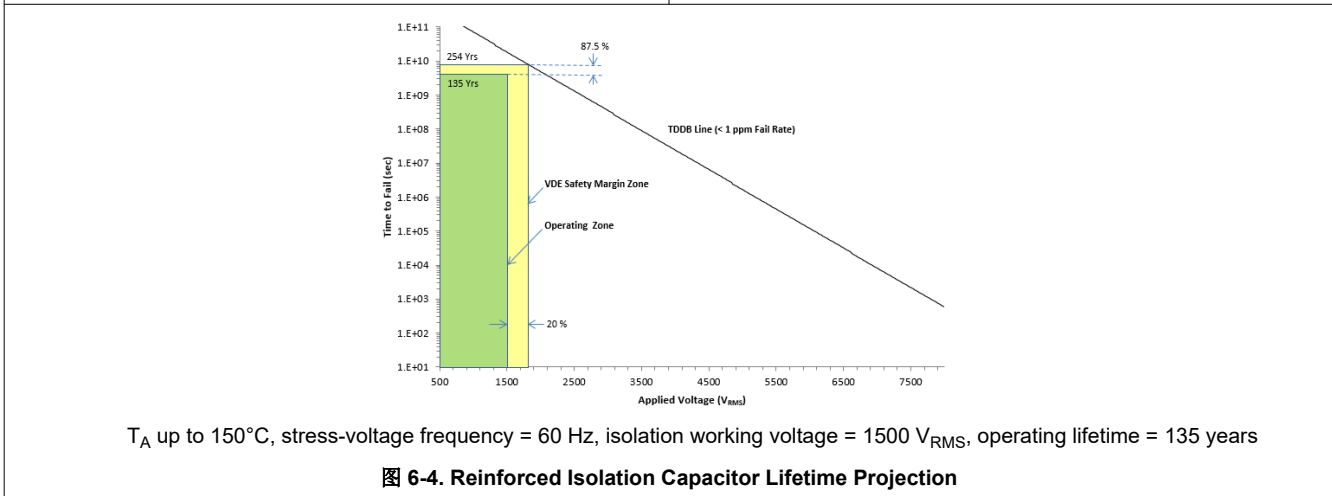
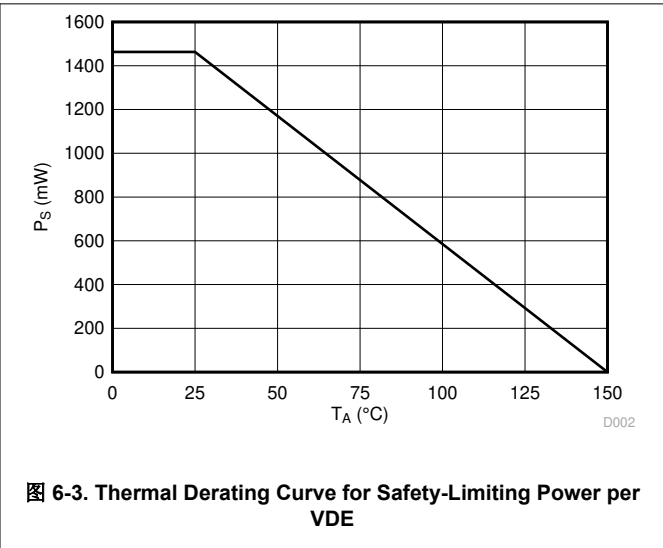
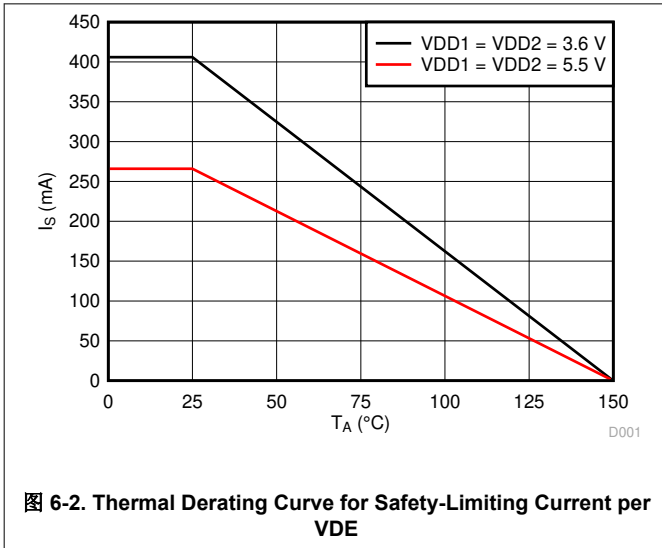


图 6-1. Rise, Fall, and Delay Time Waveforms

### 6.12 Insulation Characteristics Curves



### 6.13 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $\text{INP} = -50\text{ mV to } 50\text{ mV}$ ,  $\text{INN} = \text{GND1}$ , and  $f_{\text{IN}} = 10\text{ kHz}$  (unless otherwise noted)

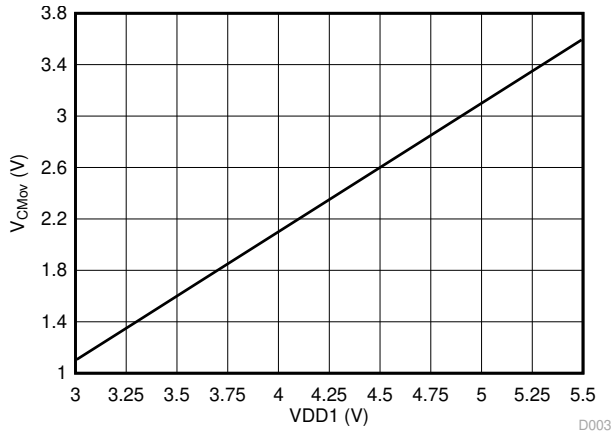


图 6-5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

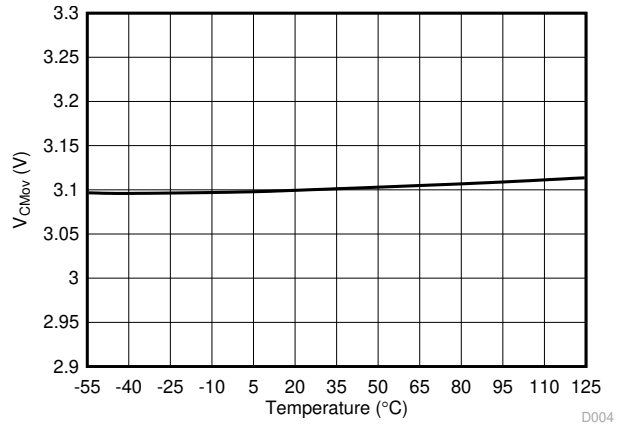


图 6-6. Common-Mode Overvoltage Detection Level vs Temperature

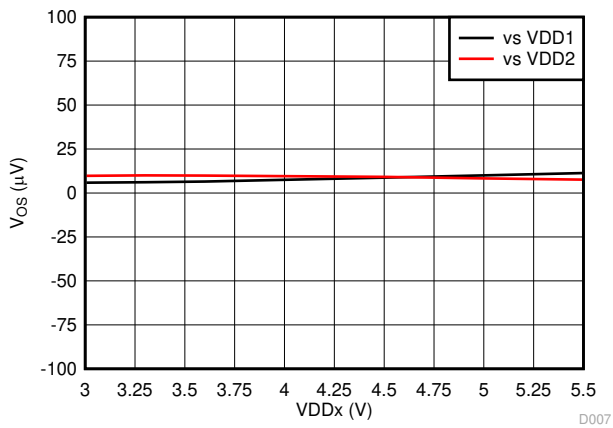


图 6-7. Input Offset Voltage vs Supply Voltage

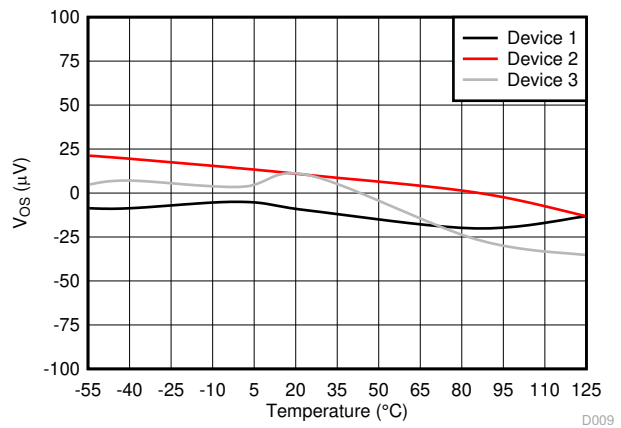


图 6-8. Input Offset Voltage vs Temperature

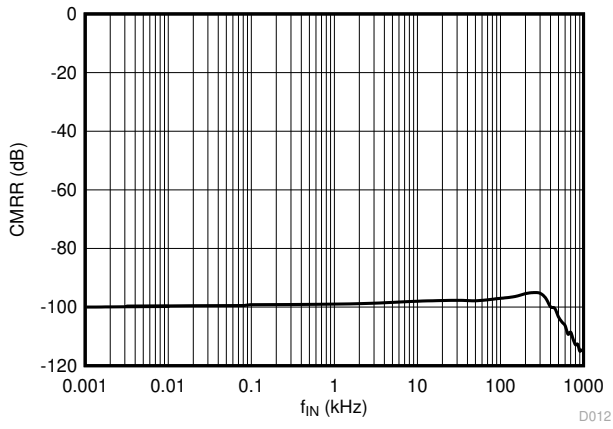


图 6-9. Common-Mode Rejection Ratio vs Input Frequency

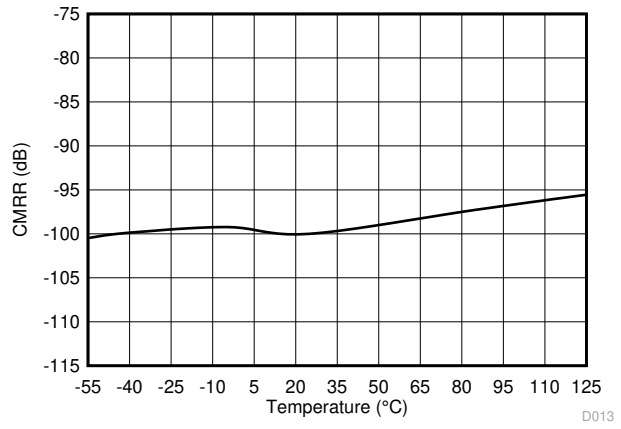


图 6-10. Common-Mode Rejection Ratio vs Temperature

### 6.13 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $\text{INP} = -50\text{ mV to } 50\text{ mV}$ ,  $\text{INN} = \text{GND1}$ , and  $f_{\text{IN}} = 10\text{ kHz}$  (unless otherwise noted)

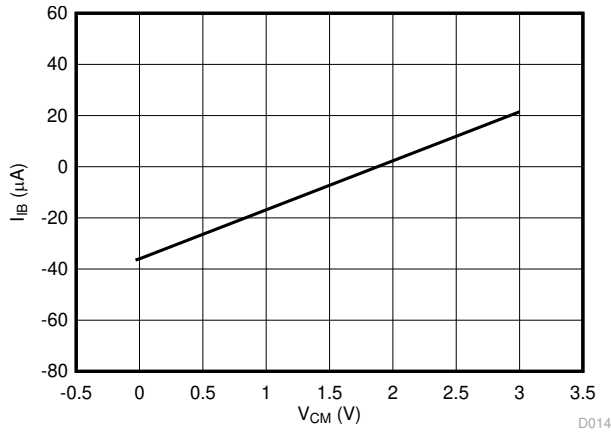


图 6-11. Input Bias Current vs Common-Mode Input Voltage

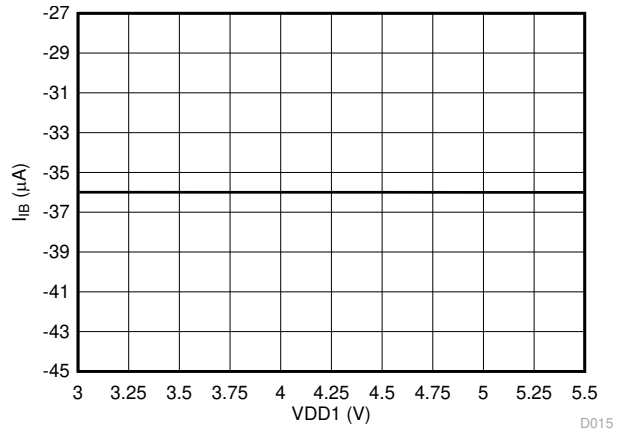


图 6-12. Input Bias Current vs High-Side Supply Voltage

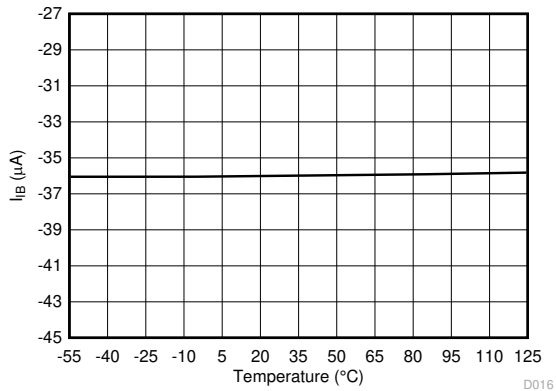


图 6-13. Input Bias Current vs Temperature

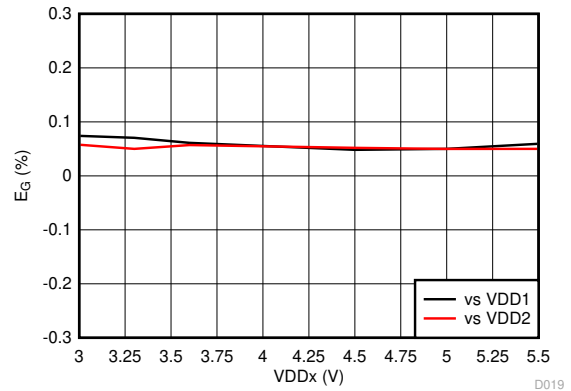


图 6-14. Gain Error vs Supply Voltage

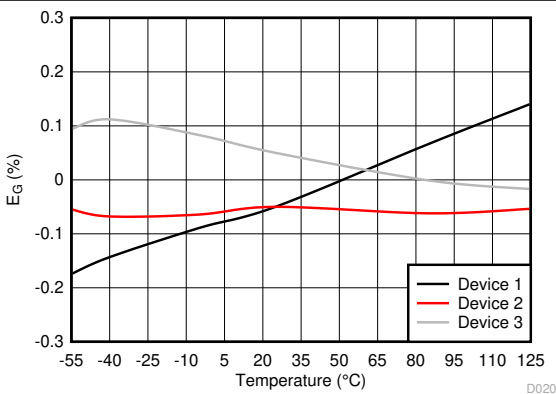


图 6-15. Gain Error vs Temperature

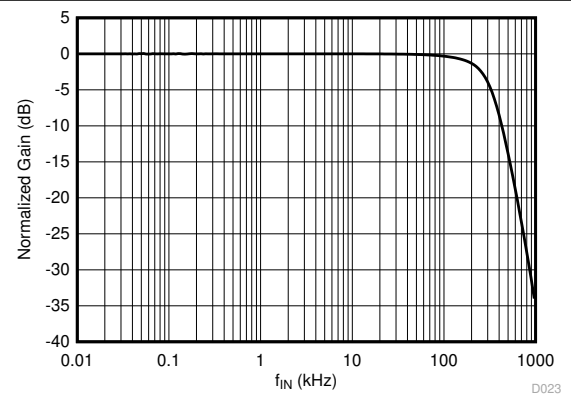
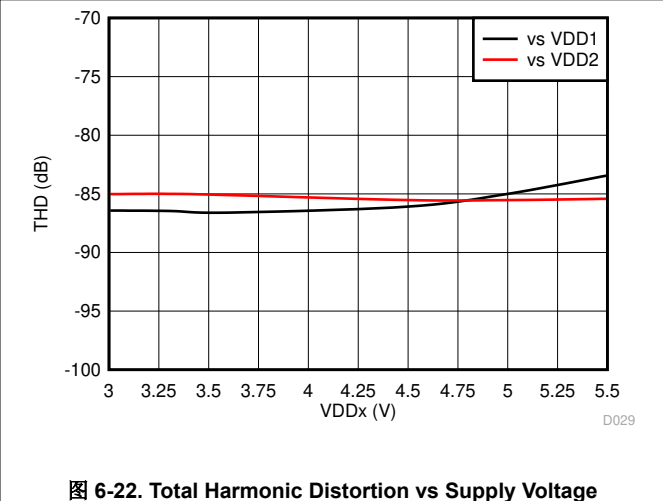
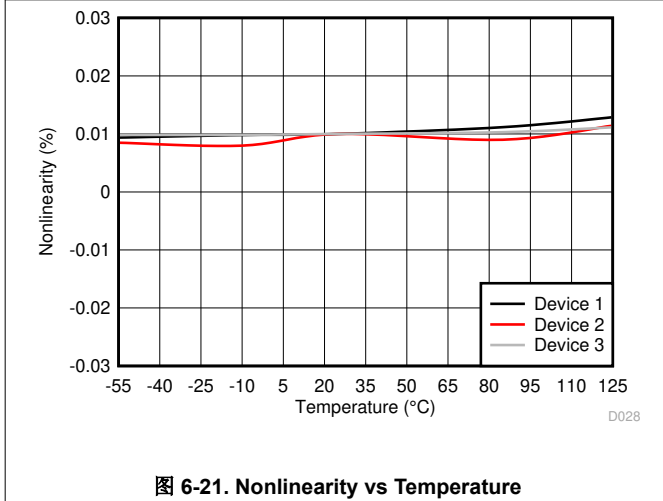
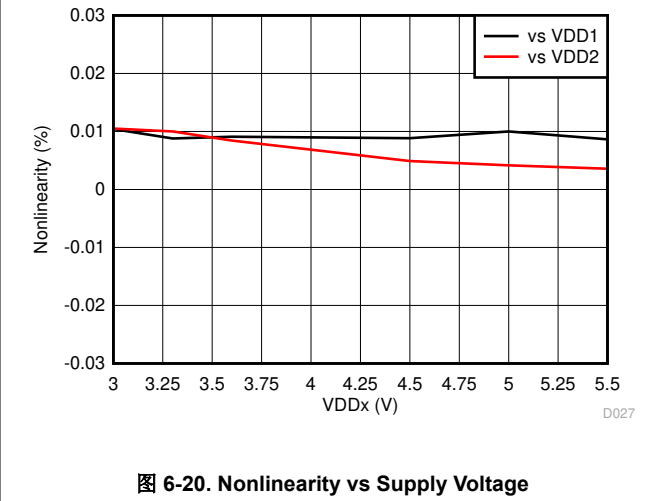
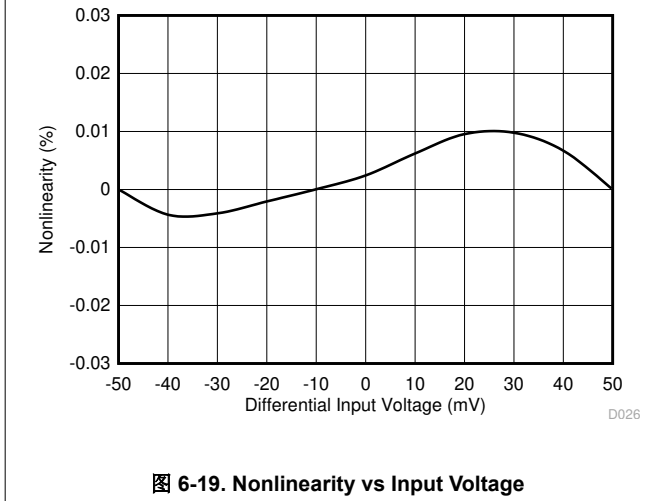
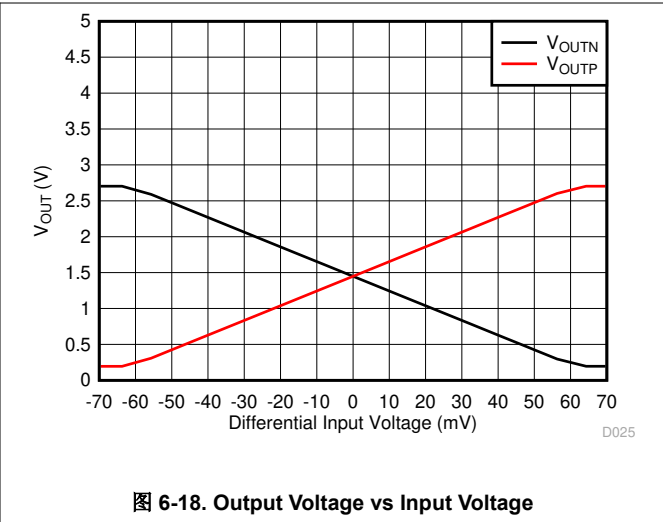
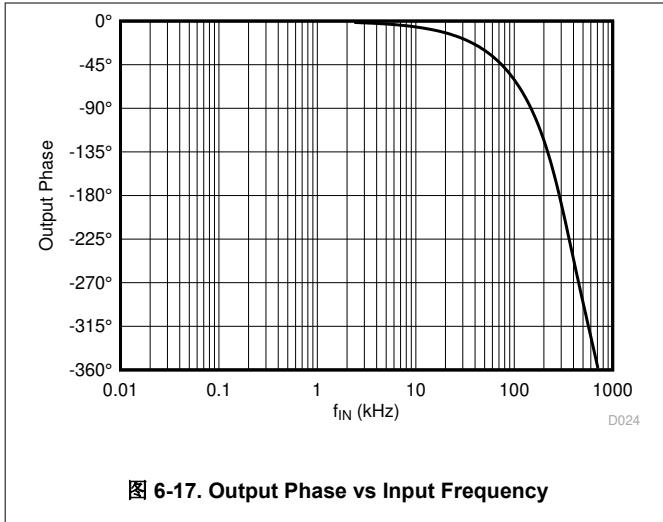


图 6-16. Normalized Gain vs Input Frequency

### 6.13 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $\text{INP} = -50\text{ mV to } 50\text{ mV}$ ,  $\text{INN} = \text{GND1}$ , and  $f_{\text{IN}} = 10\text{ kHz}$  (unless otherwise noted)



### 6.13 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $\text{INP} = -50\text{ mV to } 50\text{ mV}$ ,  $\text{INN} = \text{GND1}$ , and  $f_{\text{IN}} = 10\text{ kHz}$  (unless otherwise noted)

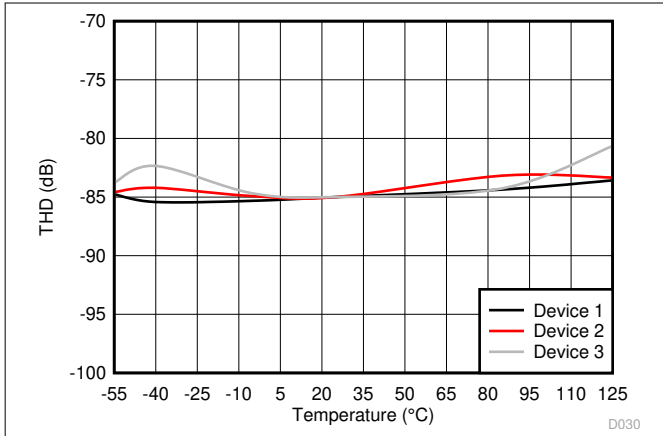


图 6-23. Total Harmonic Distortion vs Temperature

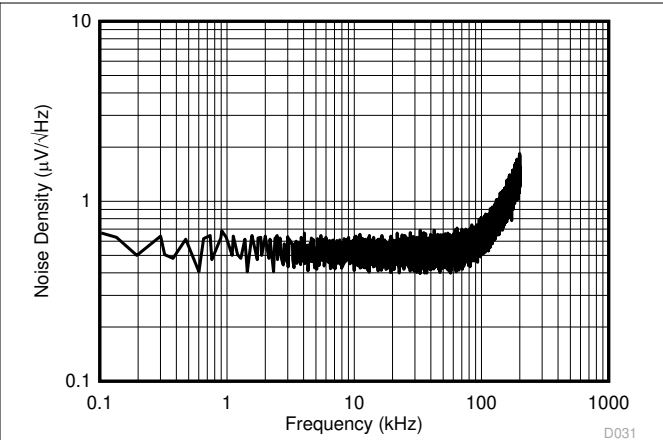


图 6-24. Output Noise Density vs Frequency

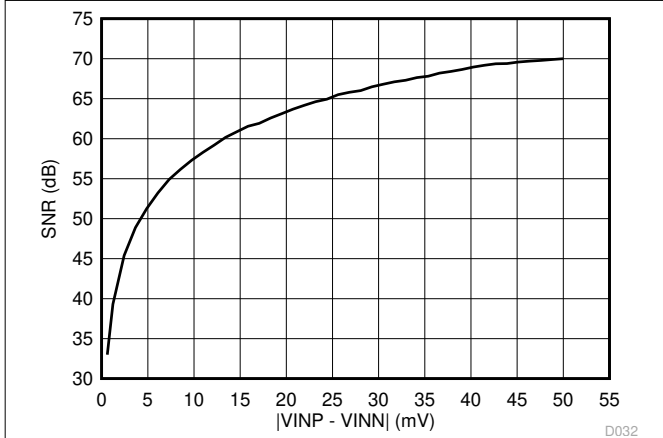


图 6-25. Signal-to-Noise Ratio vs Input Voltage

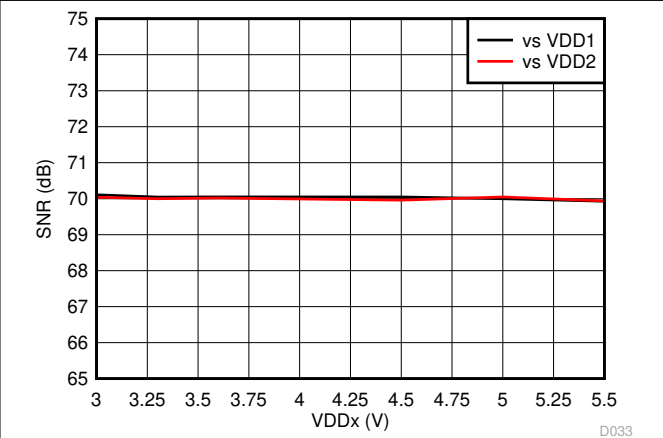


图 6-26. Signal-to-Noise Ratio vs Supply Voltage

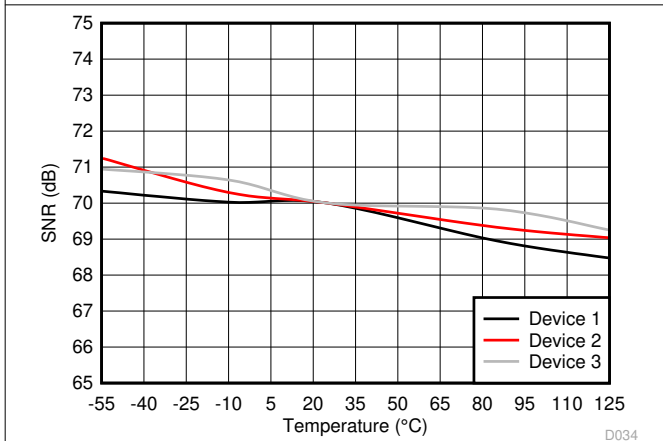


图 6-27. Signal-to-Noise Ratio vs Temperature

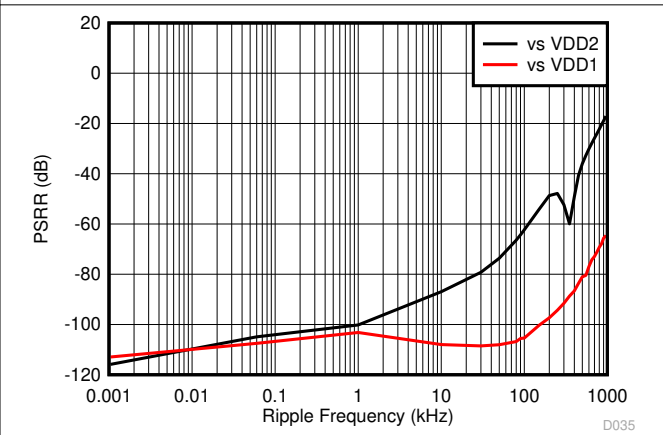


图 6-28. Power-Supply Rejection Ratio vs Ripple Frequency

### 6.13 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $\text{INP} = -50\text{ mV to } 50\text{ mV}$ ,  $\text{INN} = \text{GND1}$ , and  $f_{\text{IN}} = 10\text{ kHz}$  (unless otherwise noted)

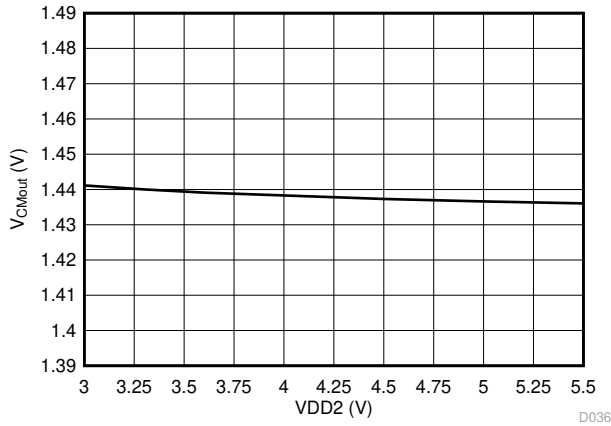


图 6-29. Output Common-Mode Voltage vs Low-Side Supply Voltage

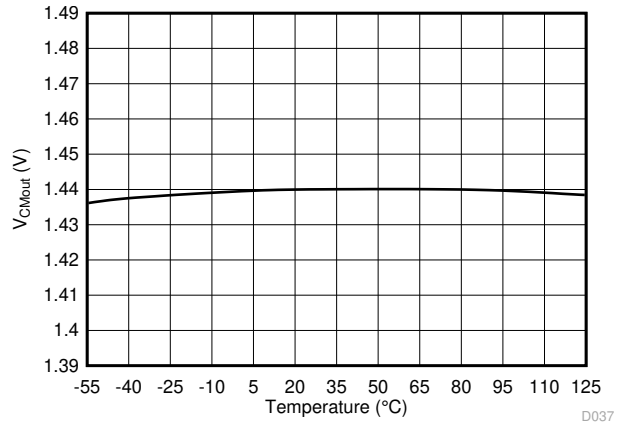


图 6-30. Output Common-Mode Voltage vs Temperature

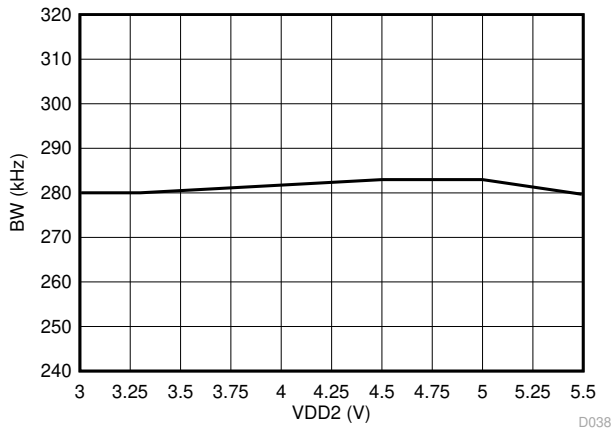


图 6-31. Output Bandwidth vs Low-Side Supply Voltage

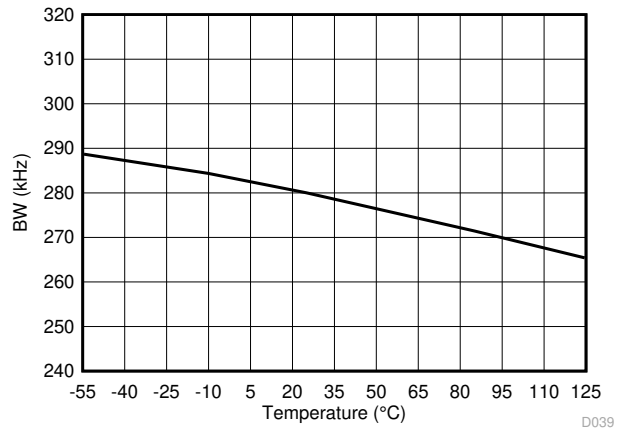


图 6-32. Output Bandwidth vs Temperature

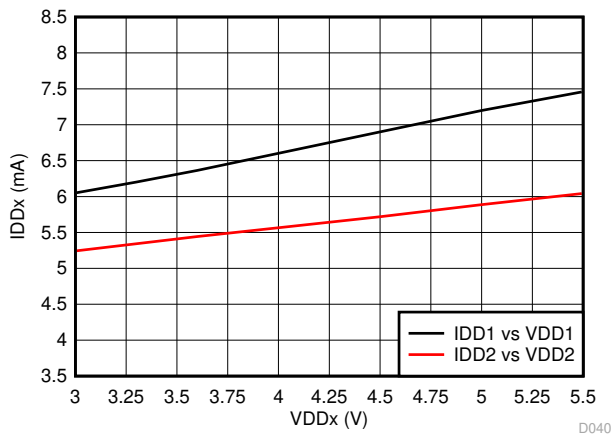


图 6-33. Supply Current vs Supply Voltage

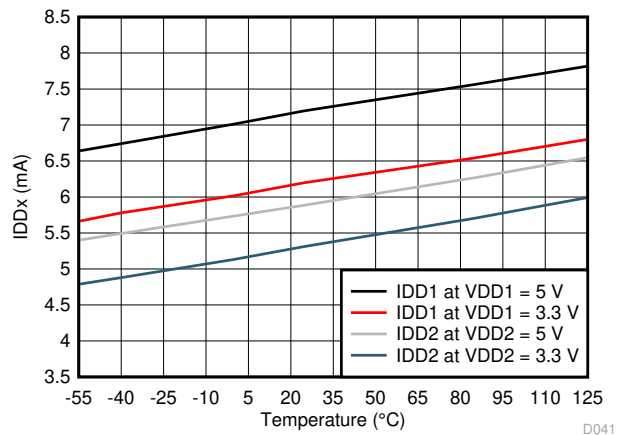


图 6-34. Supply Current vs Temperature

### 6.13 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ ,  $\text{INP} = -50\text{ mV to } 50\text{ mV}$ ,  $\text{INN} = \text{GND1}$ , and  $f_{\text{IN}} = 10\text{ kHz}$  (unless otherwise noted)

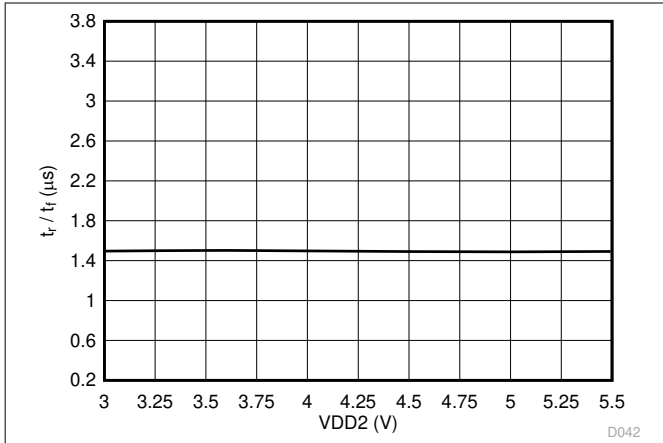


图 6-35. Output Rise and Fall Time vs Low-Side Supply Voltage

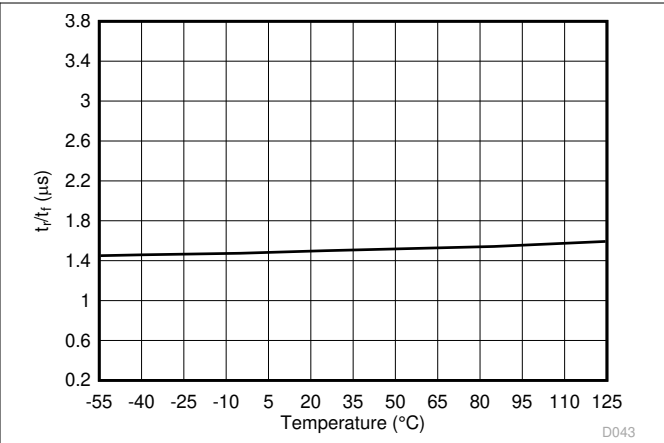


图 6-36. Output Rise and Fall Time vs Temperature

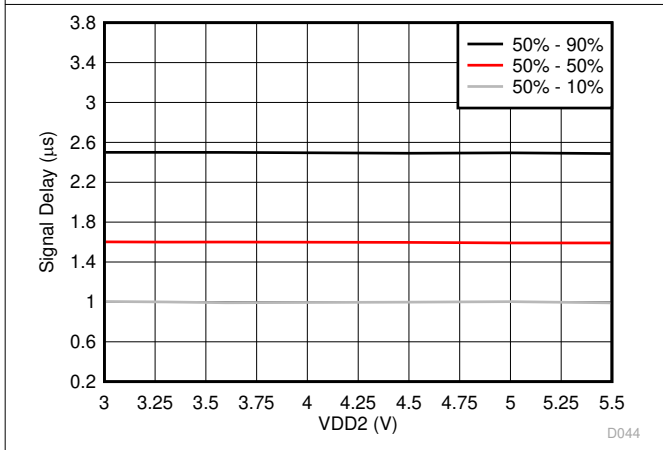


图 6-37.  $V_{\text{IN}}$  to  $V_{\text{OUT}}$  Signal Delay vs Low-Side Supply Voltage

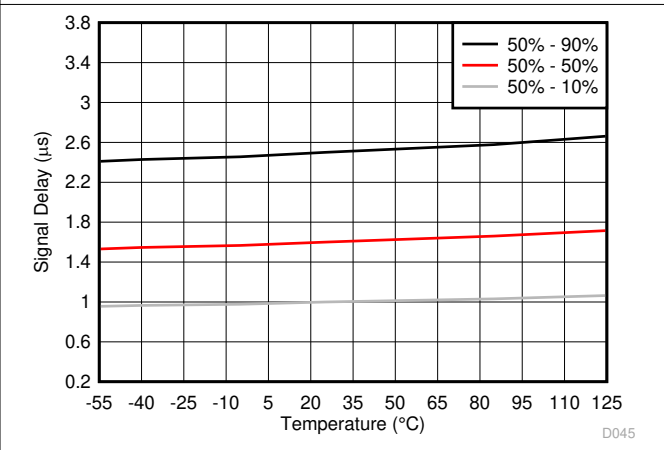


图 6-38.  $V_{\text{IN}}$  to  $V_{\text{OUT}}$  Signal Delay vs Temperature

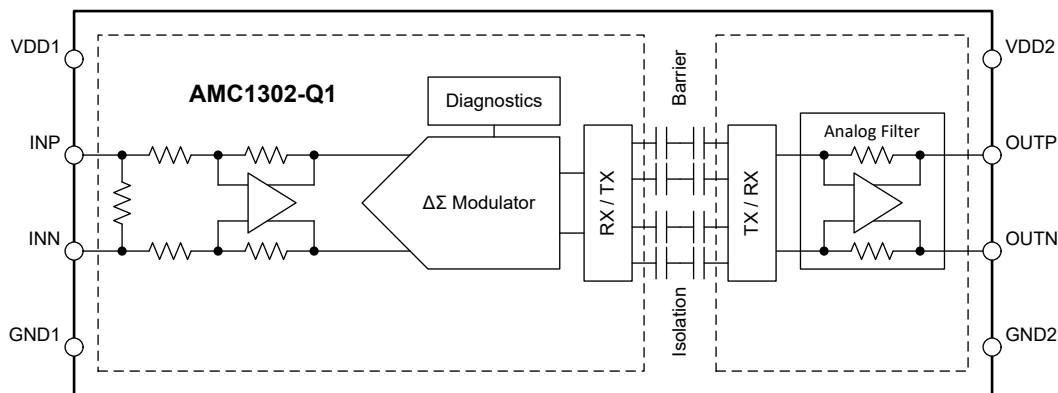
## 7 Detailed Description

### 7.1 Overview

The AMC1302-Q1 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The SiO<sub>2</sub>-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application report](#). The digital modulation used in the AMC1302-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Analog Input

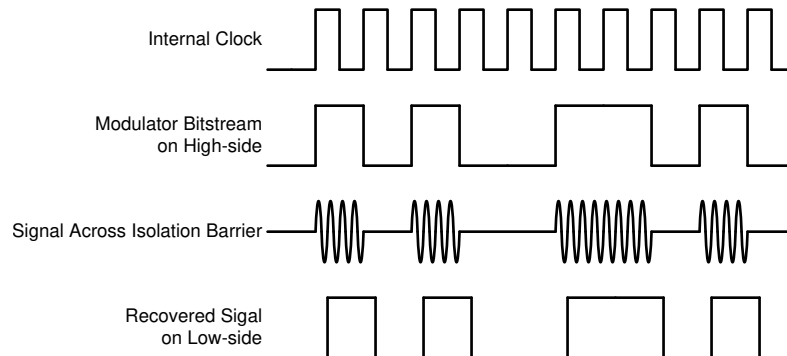
The differential amplifier input stage of the AMC1302-Q1 feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of  $R_{IND}$ . The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

There are two restrictions on the analog input signals INP and INN. First, if the input voltages  $V_{INP}$  or  $V_{INN}$  exceed the range specified in the [Absolute Maximum Ratings](#) table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range ( $V_{FSR}$ ) and within the common-mode input voltage range ( $V_{CM}$ ) as specified in the [Recommended Operating Conditions](#) table.

### 7.3.2 Isolation Channel Signal Transmission

The AMC1302-Q1 uses an on-off keying (OOK) modulation scheme, as shown in [图 7-1](#), to transmit the modulator output bitstream across the SiO<sub>2</sub>-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1302-Q1 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the 4th-order analog filter. The AMC1302-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.



**图 7-1. OOK-Based Modulation Scheme**

### 7.3.3 Analog Output

The AMC1302-Q1 offers a differential analog output comprised of the OOUTP and OOUTN pins. For differential input voltages ( $V_{INP} - V_{INN}$ ) in the range from  $-50\text{ mV}$  to  $50\text{ mV}$ , the device provides a linear response with a nominal gain of 41. For example, for a differential input voltage of  $50\text{ mV}$ , the differential output voltage ( $V_{OOUTP} - V_{OOUTN}$ ) is  $2.05\text{ V}$ . At zero input (INP shorted to INN), both pins output the same common-mode output voltage  $V_{CMout}$ , as specified in the [Electrical Characteristics](#) table. For absolute differential input voltages greater than  $50\text{ mV}$  but less than  $64\text{ mV}$ , the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of  $V_{CLIPout}$ , as shown in [Figure 7-2](#), if the differential input voltage exceeds the  $V_{Clipping}$  value.

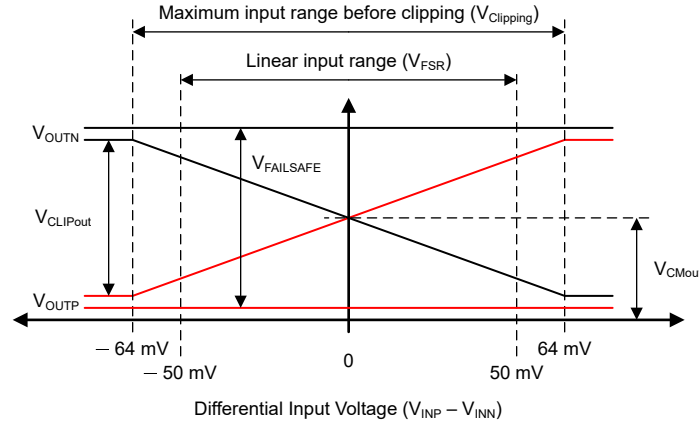


图 7-2. Output Behavior of the AMC1302-Q1

The AMC1302-Q1 offers a fail-safe feature that simplifies diagnostics on system level. [Figure 7-2](#) shows the fail-safe mode, in which the AMC1302-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

- When the high-side supply is missing or below the  $V_{DD1UV}$  threshold
- When the common-mode input voltage, that is  $V_{CM} = (V_{INP} + V_{INN}) / 2$ , exceeds the common-mode overvoltage detection level  $V_{CMov}$

Use the maximum  $V_{FAILSAFE}$  voltage specified in the [Electrical Characteristics](#) table as a reference value for fail-safe detection on system level.

### 7.4 Device Functional Modes

The AMC1302-Q1 is operational when the power supplies  $V_{DD1}$  and  $V_{DD2}$  are applied, as specified in the [Recommended Operating Conditions](#) table.

## 8 Application and Implementation

### Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the a high-performance solution for automotive applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

### 8.2 Typical Application

The AMC1302-Q1 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages.

图 8-1 shows the AMC1302-Q1 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1302-Q1. The AMC1302-Q1 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents that signal as a differential voltage on the output pins.

The differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1302-Q1 ensure reliable and accurate operation even in high-noise environments.

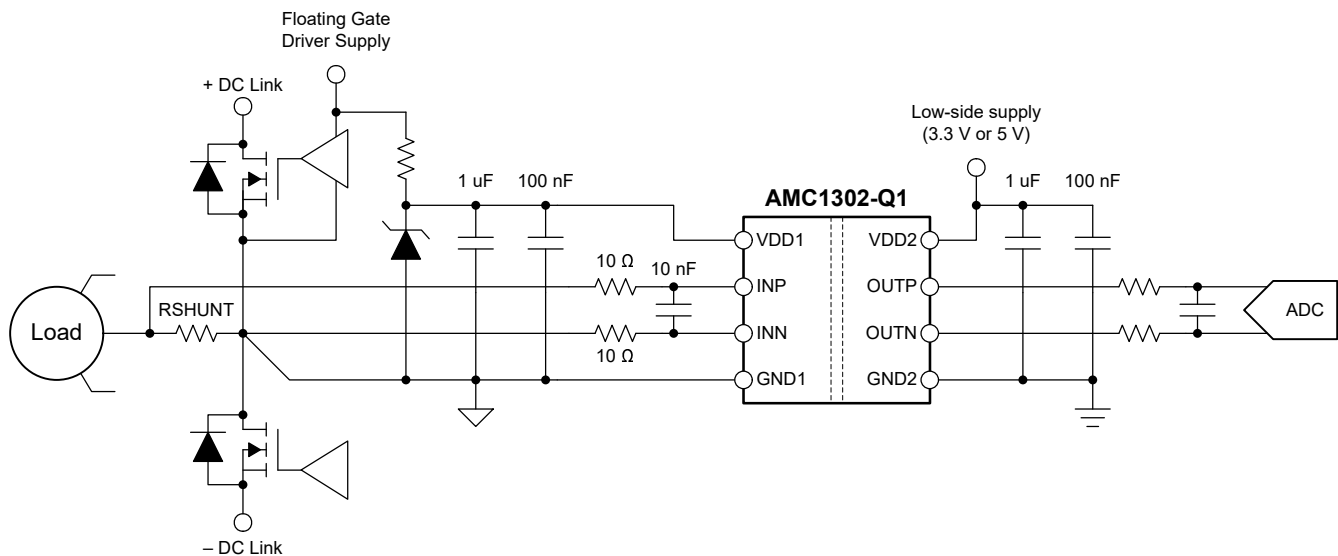


图 8-1. Using the AMC1302-Q1 for Current Sensing in a Typical Application

## 8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±50 mV (maximum)
Signal delay (50% V <sub>IN</sub> to 90% OUTP, OUTN)	3 μs (maximum)

## 8.2.2 Detailed Design Procedure

In 图 8-1, the high-side power supply (VDD1) for the AMC1302-Q1 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1302-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1302-Q1 are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the [Layout](#) section for more details.

### 8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V<sub>SHUNT</sub>) for the desired measured current: V<sub>SHUNT</sub> = I × RSHUNT.

Consider the following two restrictions when selecting the value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response: |V<sub>SHUNT</sub>| ≤ |V<sub>FSR</sub>|
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: |V<sub>SHUNT</sub>| ≤ |V<sub>Clipping</sub>|

### 8.2.2.2 Input Filter Design

TI recommends placing an RC-filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in 图 8-2 achieves excellent performance.

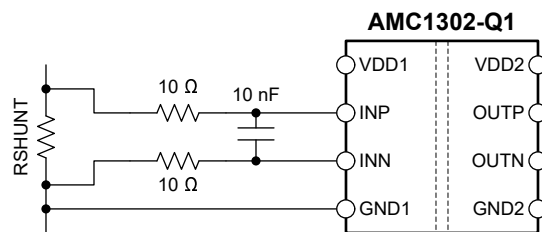


图 8-2. Differential Input Filter

### 8.2.2.3 Differential to Single-Ended Output Conversion

图 8-3 shows an example of a TLV313-Q1-based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With  $R1 = R2 = R3 = R4$ , the output voltage equals  $(V_{OUTP} - V_{OUTN}) + V_{REF}$ . Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications,  $R1 = R2 = R3 = R4 = 3.3 \text{ k}\Omega$  and  $C1 = C2 = 330 \text{ pF}$  yields good performance.

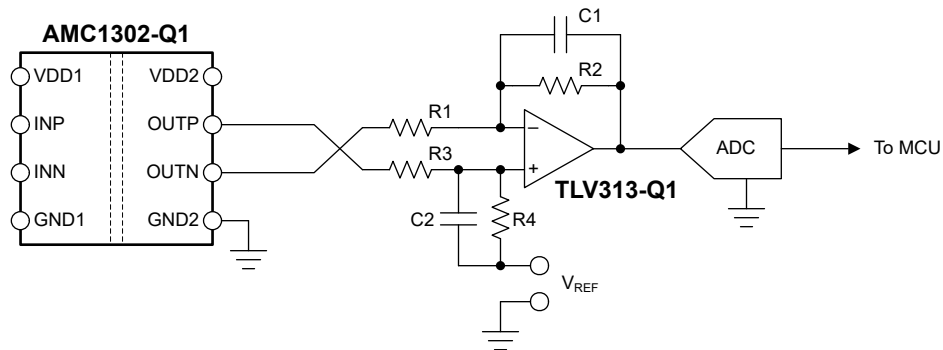


图 8-3. Connecting the AMC1302-Q1 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guides, available for download at [www.ti.com](http://www.ti.com).

### 8.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. 图 8-4 shows the typical full-scale step response of the AMC1302-Q1.



图 8-4. Step Response of the AMC1302-Q1

## 8.3 What to Do and What Not to Do

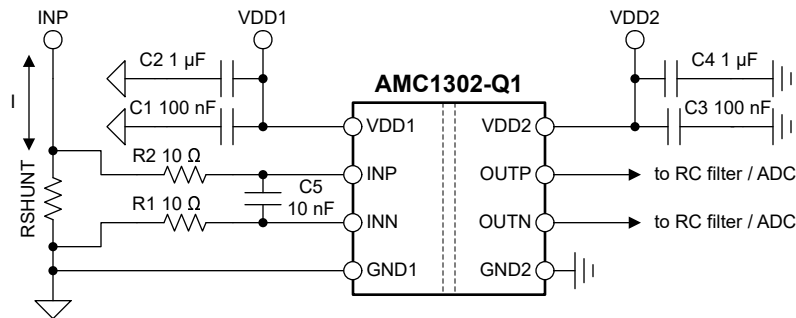
Do not leave the inputs of the AMC1302-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the device outputs the fail-safe voltage as described in the [Analog Output](#) section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the [Recommended Operating Conditions](#) table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the [Layout](#) section for more details.

## 9 Power Supply Recommendations

The AMC1302-Q1 does not require any specific power up sequencing. The high-side power-supply (VDD1) is decoupled with a low-ESR 100-nF capacitor (C1) parallel to a low-ESR 1- $\mu$ F capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR 100-nF capacitor (C3) parallel to a low-ESR 1- $\mu$ F capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace (as shown in [Figure 9-1](#)) to make this connection instead of shorting GND1 to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt.



**图 9-1. Decoupling of the AMC1302-Q1**

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

## 10 Layout

### 10.1 Layout Guidelines

Figure 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1302-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1302-Q1 and keep the layout of both connections symmetrical.

### 10.2 Layout Example

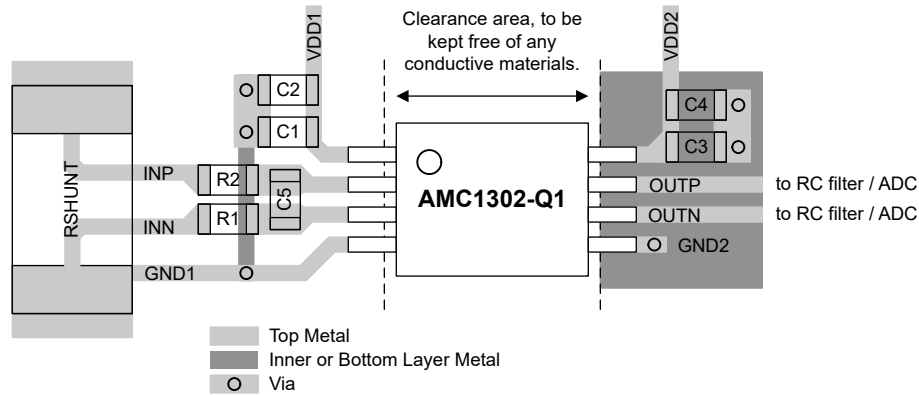


Figure 10-1. Recommended Layout of the AMC1302-Q1

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

Texas Instruments, [Isolation Glossary application report](#)

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary application report](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application report](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application report](#)
- Texas Instruments, [TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 750- \$\mu\$ V Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems data sheet](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise reference guide](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power reference guide](#)
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator design tool](#)

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### 11.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1302QDWVQ1	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q	<a href="#">Samples</a>
AMC1302QDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

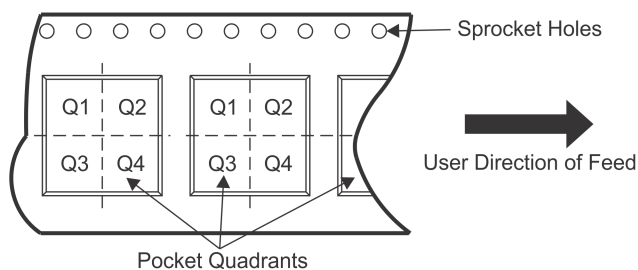
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


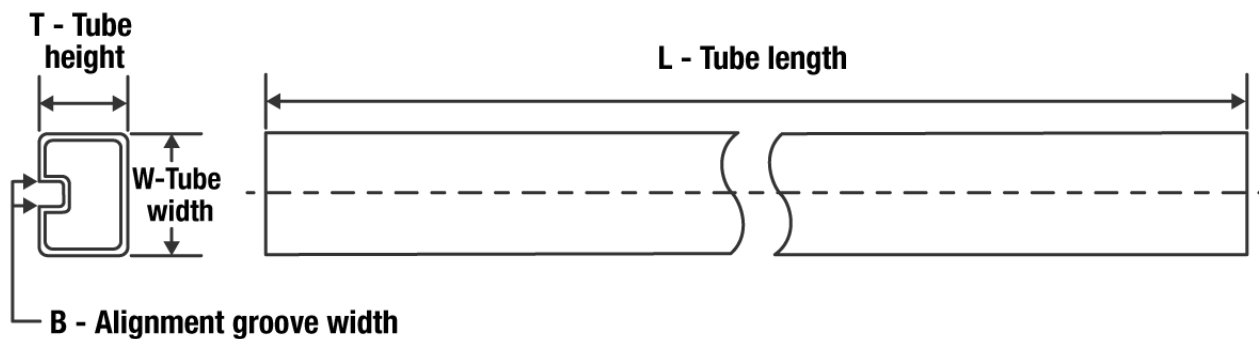
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1302QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1302QDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

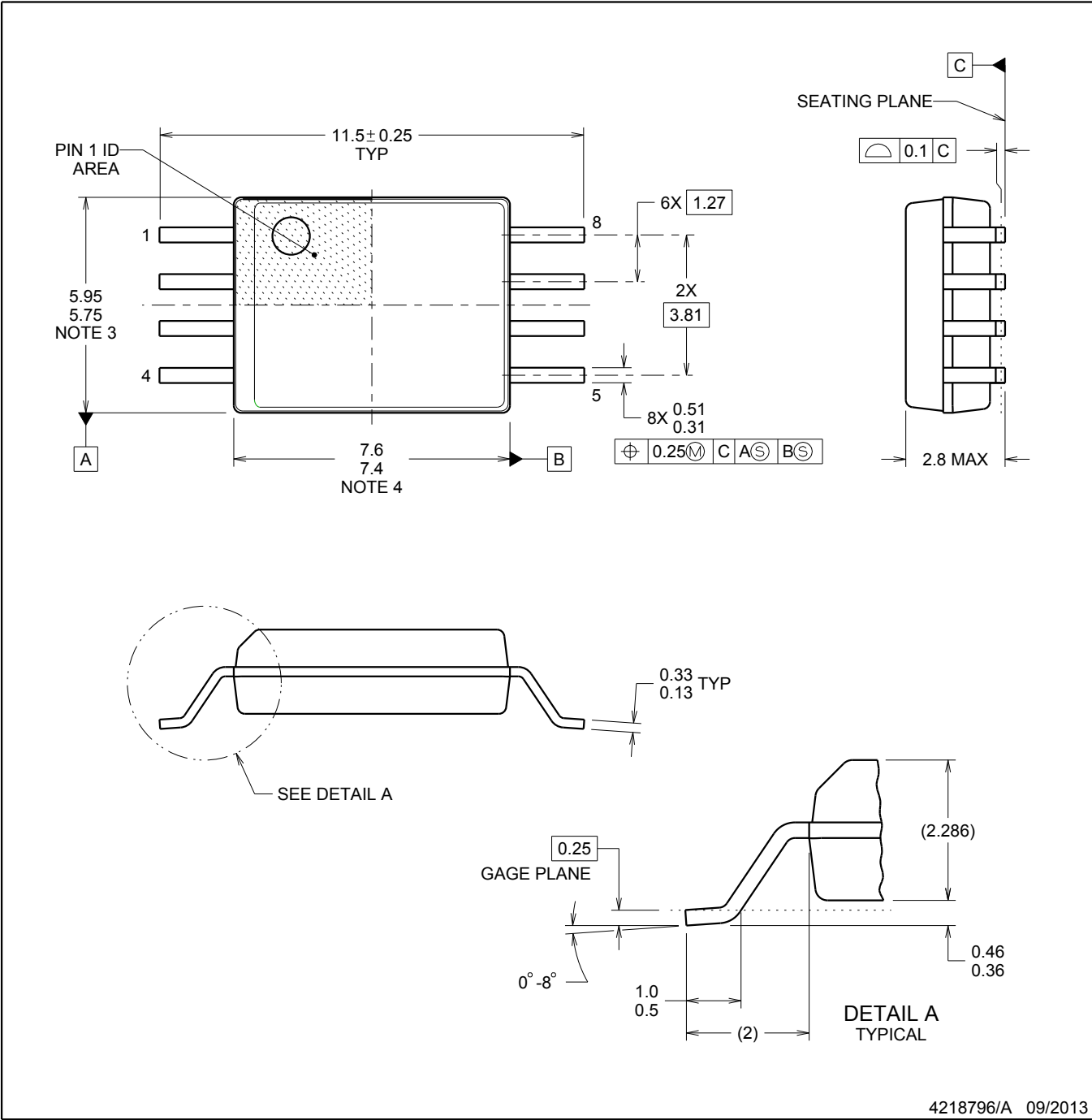
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
AMC1302QDWVQ1	DWV	SOIC	8	64	505.46	13.94	4826	6.6



DWV0008A

SOIC - 2.8 mm max height

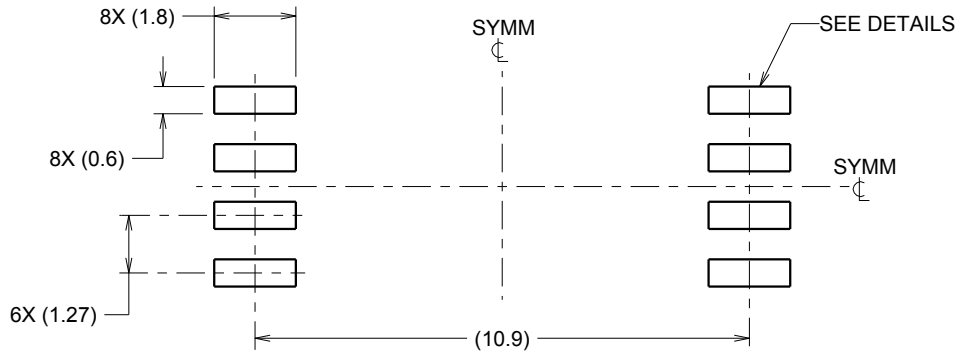
SOIC



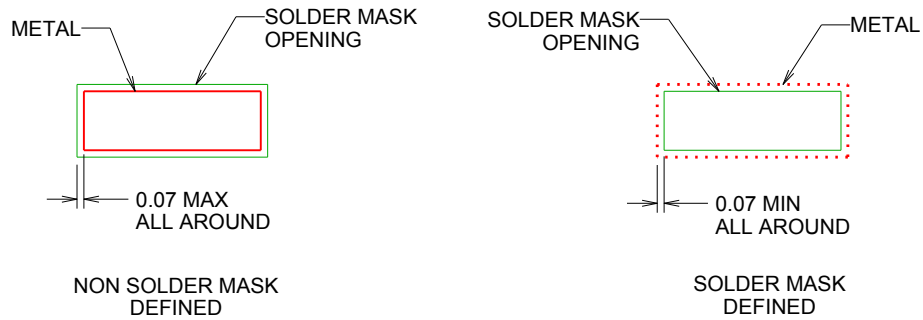
4218796/A 09/2013

NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE  
 9.1 mm NOMINAL CLEARANCE/CREEPAGE  
 SCALE:6X

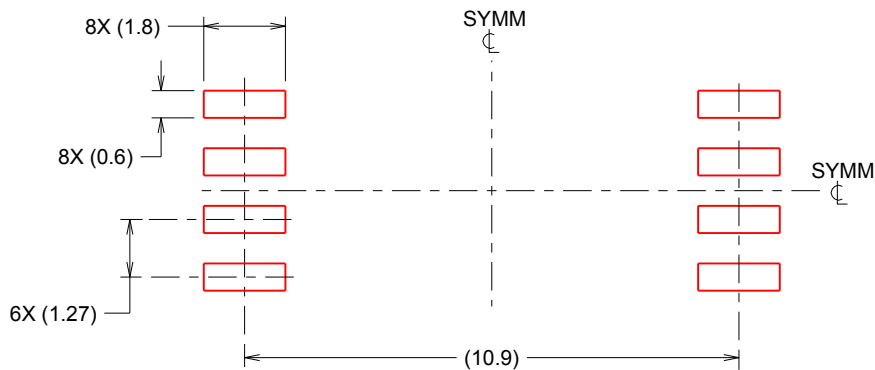


SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

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NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

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