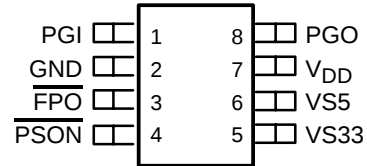


- Overvoltage Protection and Lockout for 12 V, 5 V, 3.3 V
- Undervoltage Protection and Lockout for 5 V and 3.3 V
- Fault Protection Output With Open-Drain Output Stage
- Open-Drain Power Good Output Signal for Power Good Input, 3.3 V and 5 V
- Power Good Delay; 300-ms TPS3510, 150-ms TPS3511
- 75-ms Delay for 5-V and 3.3-V Power Supply Short-Circuit Turnon Protection
- 2.3-ms $\overline{\text{PSON}}$ Control to $\overline{\text{FPO}}$ Turnoff Delay
- 38-ms $\overline{\text{PSON}}$ Control Debounce
- 73- μs Width Noise Deglitches
- Wide Supply Voltage Range From 4 V to 15 V

D OR P PACKAGE
(TOP VIEW)



description

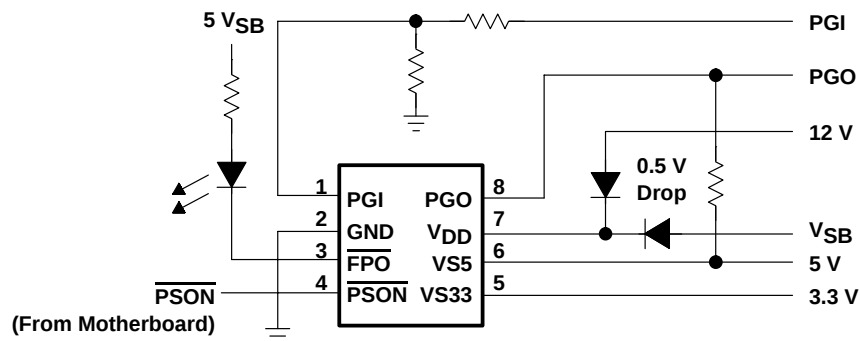
The TPS3510/1 is designed to minimize external components of personal-computer switching power supply systems. It provides protection circuits, power good indicator, fault protection output ($\overline{\text{FPO}}$) and $\overline{\text{PSON}}$ control.

Overvoltage protection (OVP) monitors 3.3 V, 5 V, and 12 V (12-V signal detects via V_{DD} pin). Undervoltage protection (UVP) monitors 3.3 V and 5 V. When an OV or UV condition is detected, the power good output (PGO) is set to low and $\overline{\text{FPO}}$ is latched high. $\overline{\text{PSON}}$ from low to high resets the protection latch. UVP function is enabled 75 ms after $\overline{\text{PSON}}$ is set low and debounced. Furthermore, there is a 2.3-ms delay (and an additional 38-ms debounce) at turnoff. There is no delay during turnon.

Power good feature monitors PGI, 3.3 V and 5 V and issues a power good signal when the output is ready.

The TPS3510/1 is characterized for operation from -40°C to 85°C .

typical application



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TPS3510,TPS3511

PC POWER SUPPLY SUPERVISORS

SLVS312A – JULY 2000 – REVISED DECEMBER 2002

FUNCTION TABLE

PGI	$\overline{\text{PSON}}$	UV CONDITION (3.3 V OR 5 V)	OV CONDITION (3.3 V, 5 V, OR 12 V)	$\overline{\text{FPO}}$	PGO
<0.95 V	L	no	no	L	L
<0.95 V	L	no	yes	H	L
<0.95 V	L	yes	no	L	L
0.95 V < PGI < 1.15 V	L	no	no	L	L
0.95 V < PGI < 1.15 V	L	no	yes	H	L
0.95 V < PGI < 1.15 V	L	yes	no	H	L
PGI > 1.15 V	L	no	no	L	H
PGI > 1.15 V	L	no	yes	H	L
PGI > 1.15 V	L	yes	no	H	L
x	H	x	x	H	L

x = don't care

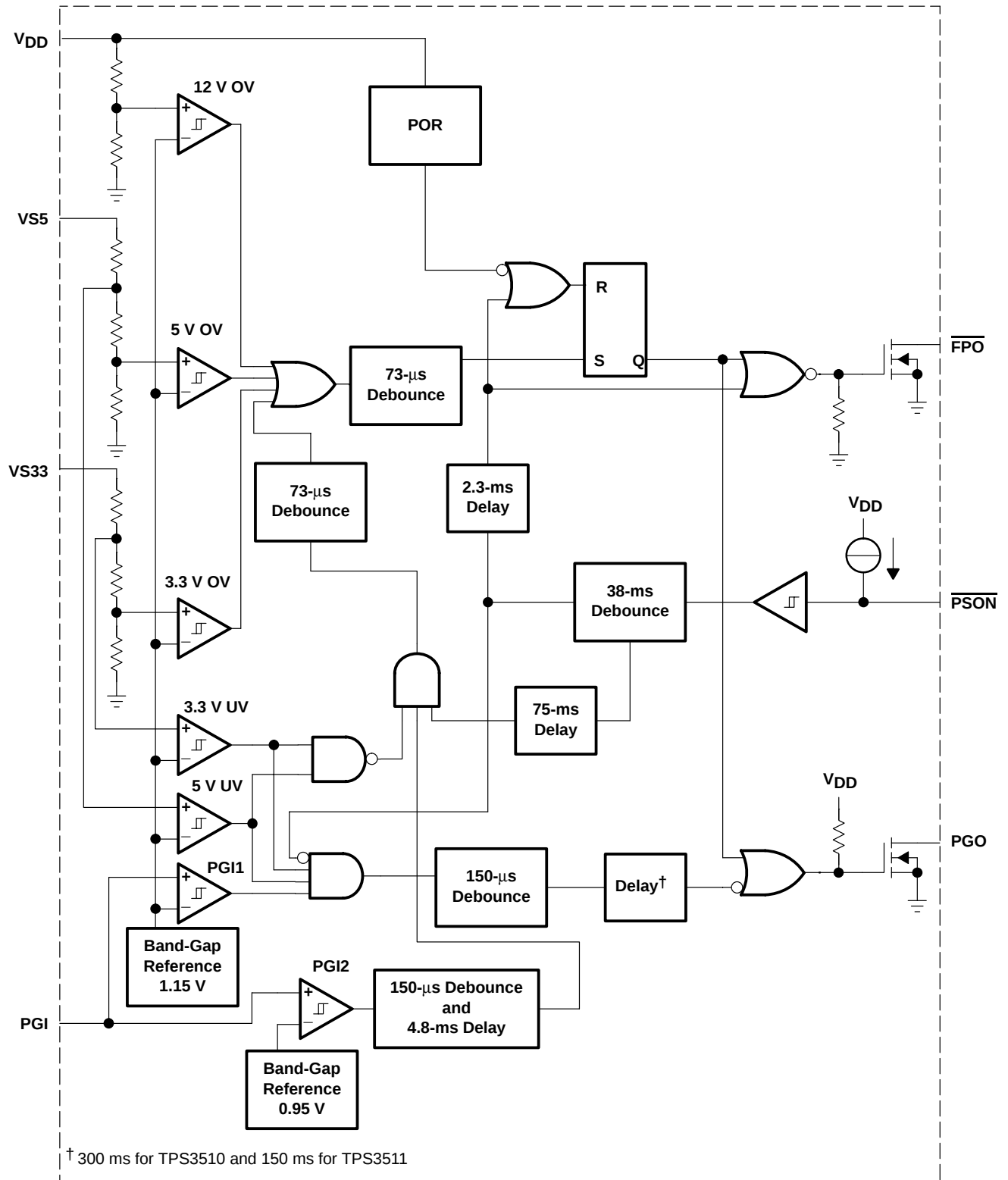
$\overline{\text{FPO}}$ = L means: fault IS NOT latched

$\overline{\text{FPO}}$ = H means: fault IS latched

PGO = L means: fault

PGO = H means: NO fault

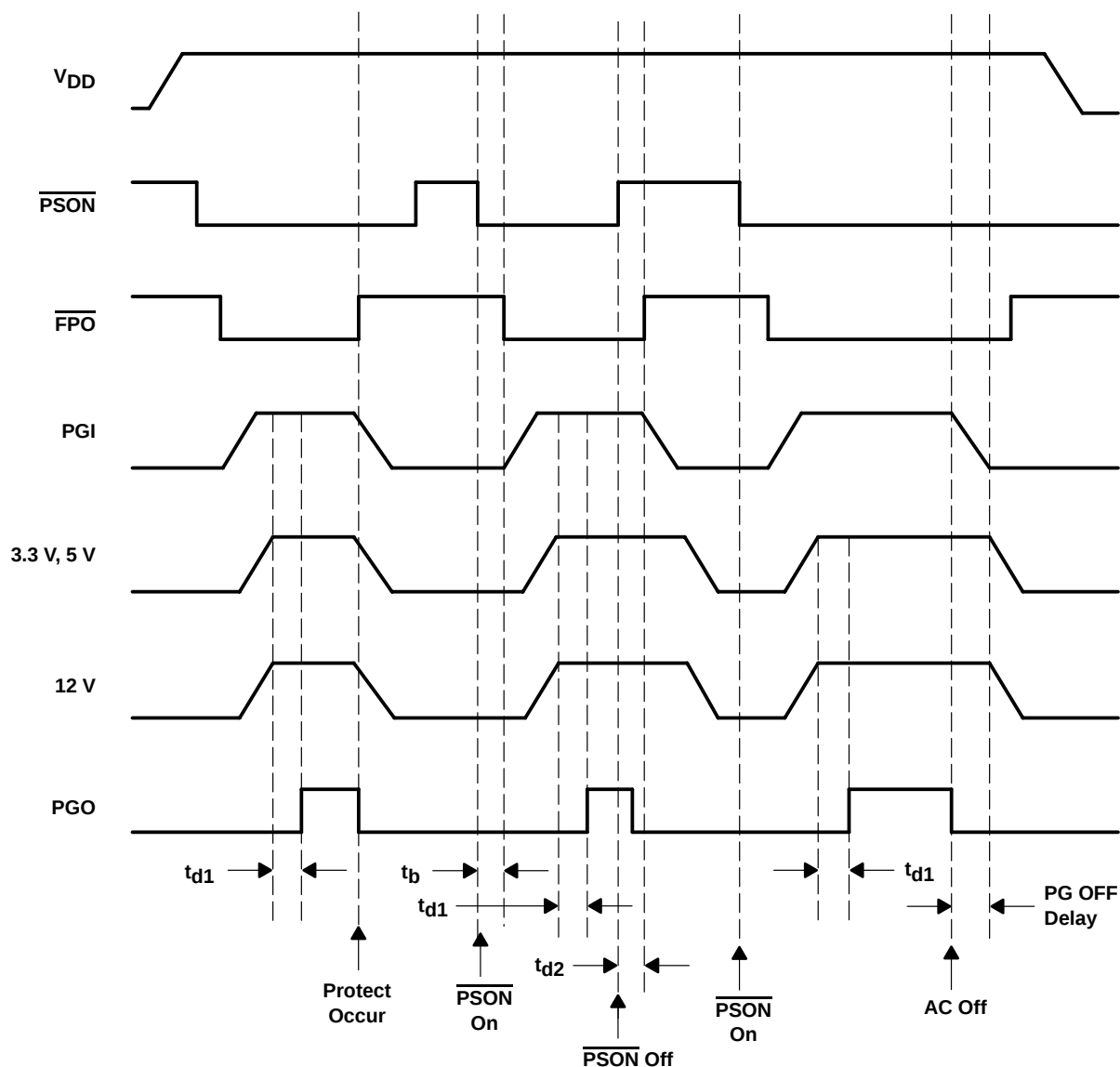
functional block diagram



TPS3510,TPS3511 PC POWER SUPPLY SUPERVISORS

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timing diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{FPO}$	3	O	Inverted fault protection output, open drain output stage
GND	2		Ground
PGI	1	I	Power good input
PGO	8	O	Power good output, open drain output stage
$\overline{PSON}$	4	I	ON/OFF control
V_{DD}	7	I	Supply voltage/12 V overvoltage protection input pin
VS33	5	I	3.3 V over/undervoltage protection
VS5	6	I	5 V over/undervoltage protection

detailed description

power good and power good delay

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. PGO is a power-good signal and should be asserted high by the PC power supply to indicate that the 5-V and 3.3-V outputs are above the under-voltage threshold limit. At this time the converter should be able to provide enough power to ensure continuous operation within the specification. Conversely, when either the 5-V or the 3.3-V output voltages fall below the under-voltage threshold, or when ac power has been removed for a time sufficiently long so that power supply operation is no longer ensured, PGO should be de-asserted to a low state.

Figure 1 represents the timing characteristics of the power good (PGO), dc enable ($\overline{\text{PSON}}$), and the 5 V/3.3 V supply rails.

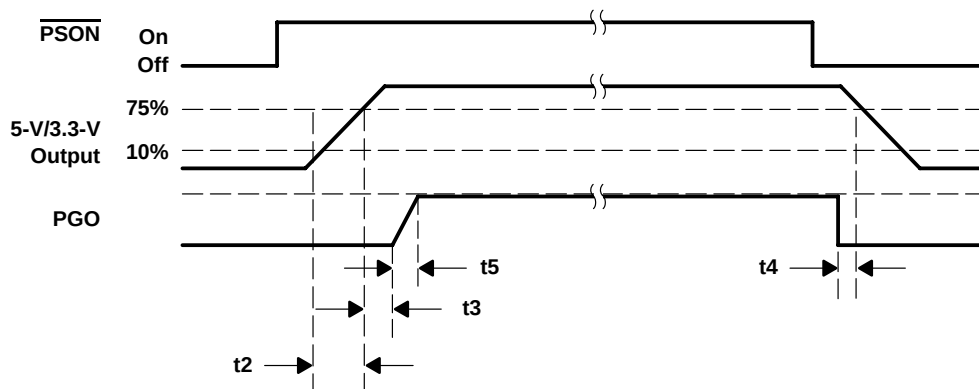


Figure 1. Timing of $\overline{\text{PSON}}$ and PGO

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

$$2 \text{ ms} \leq t_2 \leq 20 \text{ ms}, 100 \text{ ms} < t_3 < 2000 \text{ ms}, t_4 > 1 \text{ ms}, t_5 \leq 10 \text{ ms}$$

Furthermore motherboards should be designed to comply with the previously recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3510/1 family of power-supply supervisors provides a power-good output (PGO) for the 3.3-V and 5-V supply voltage rails and a separate power-good input (PGI). An internal timer is used to generate a power-good delay. If the voltage signals at PGI, VS33, and VS5 rise above the under-voltage threshold, the open-drain power-good output (PGO) goes high after a delay of 150 ms or 300 ms. When the PGI voltage or either the 3.3-V and 5-V power rails drops below the under-voltage threshold, PGO is disabled immediately (after 150- μ s debounce).

power supply remote on/off ($\overline{\text{PSON}}$) and fault protect output ($\overline{\text{FPO}}$)

Since the latest personal computer generation focuses on easy turnon and power saving functions, the PC power supply requires two characteristics. One is a dc power supply remote on/off function, the other is standby voltage to achieve very low power consumption of the PC system. Thus the main power needs to be shut down.

The power supply remote on/off ($\overline{\text{PSON}}$) is an active low signal that turns on all of the main power rails including 3.3 V, 5 V, -5 V, 12 V, and -12 V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output ($\overline{\text{FPO}}$) also goes high. Thus, the main power rails should not deliver current and should be held at 0 V.

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power supply remote on/off ($\overline{\text{PSON}}$) and fault protect output ($\overline{\text{FPO}}$)(continued)

When the $\overline{\text{FPO}}$ signal is held high due to an occurring fault condition, the fault status is latched and the outputs of the main power rails should not deliver current but are held at 0 V. Toggling the power supply remote on/off ($\overline{\text{PSON}}$) from low to high resets the fault-protection latch. During this fault condition only the standby power is not affected.

When $\overline{\text{PSON}}$ goes from high to low or low to high, the 38-ms debounce block is active to avoid a glitch on the input that disables/enables the $\overline{\text{FPO}}$ output. During this period the under-voltage function is disabled for 75 ms to prevent turnon failure. At turnoff, there is an additional delay of 2.3 ms from $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$.

Power should be delivered to the rails only if the $\overline{\text{PSON}}$ signal is held at ground potential, thus $\overline{\text{FPO}}$ is active-low. The $\overline{\text{FPO}}$ pin can be connected to 5 V (or up to 15 V) through a pullup resistor.

undervoltage protection

The TPS3510/1 provides under-voltage protection (UVP) for the 3.3-V and 5-V rails. When an undervoltage condition appears at either one of the 3.3-V (VS33) or 5-V (VS5) input pins for more than 146 μs , the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition is latched until $\overline{\text{PSON}}$ is toggled from low to high or V_{DD} is removed.

The need for undervoltage protection is often overlooked in off-line switching power supply system design. But it is very important in battery-powered or hand-held equipment since the TTL or CMOS logic often results in malfunction.

In flyback or forward-type off-line switching power supplies, usually designed for low power, the overload protection design is very simple. Most of these types of power supplies are only sensing the input current for an overload condition. The trigger point needs to be set much higher than the maximum load in order to prevent false turnon.

However, this causes one critical problem. If the connected load is larger than the maximum allowable load but smaller than the trigger point, the system always becomes overheated with failure and damage occurring.

overvoltage protection

The overvoltage protection (OVP) of TPS3510/1 monitors 3.3 V, 5 V, and 12 V (12 V is sensed via the V_{DD} pin). When an overvoltage condition appears at one of the 3.3-V, 5-V, or 12-V input pins for more than 73 μs , the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition is latched until $\overline{\text{PSON}}$ is toggled from low to high or V_{DD} is removed. During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide overvoltage protection within the power supply.

Because TTL and CMOS circuits are very vulnerable to overvoltages, it is becoming industry standard to provide overvoltage protection on all 3.3-V and 5-V outputs. However, not only the 3.3-V and 5-V rails for the logic circuits on the motherboard need to be protected, but also the 12-V peripheral devices such as the hard disk, floppy disk, and CD-ROM players etc., need to be protected.

short-circuit power supply turnon

During safety testing the power supply might have tied the output voltage direct to ground. If this happens during the normal operating, this is called a short-circuit or over-current condition. When it happens before the power supply turns on, this is called a short-circuit power supply turnon. It can happen during the design period, in the production line, at quality control inspection or at the end user. The TPS3510/1 provides an undervoltage protection function with a 75-ms delay after $\overline{\text{PSON}}$ is set low.



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electrical characteristics over recommended operating conditions (unless otherwise noted)

overvoltage protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage threshold	VS33		3.7	3.9	4.1	V
	VS5		5.7	6.1	6.5	
	V _{DD}		13.2	13.8	14.4	
I _{LKG}	Leakage current ($\overline{\text{FPO}}$)	V($\overline{\text{FPO}}$) = 5 V			5	μA
V _{OL}	Low-level output voltage ($\overline{\text{FPO}}$)	V _{DD} = 5 V, I _{sink} = 20 mA			0.7	V
Noise deglitch time OVP		V _{DD} = 5 V	35	73	110	μs

PGI and PGO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{PGI}	Input threshold voltage (PGI)	PGI1	1.1	1.15	1.2	V
		PGI2	0.9	0.95	1	
V _{IT}	Undervoltage threshold	VS33	2	2.2	2.4	V
		VS5	3.3	3.5	3.7	
I _{LKG}	Leakage current (PGO)	PGO = 5 V			5	μA
V _{OL}	Low-level output voltage (PGO)	V _{DD} = 4 V, I _{sink} = 10 mA			0.4	V
Short-circuit protection delay		3.3 V, 5 V	49	75	114	ms
t _{d1}	Delay time	PGI to PGO	200	300	450	ms
			100	150	225	
			3.2	4.8	7.2	
Noise deglitch time		PGI to PGO	88	150	225	μs
		PGI to $\overline{\text{FPO}}$	180	296	445	
		UVP to $\overline{\text{FPO}}$	82	146	220	

PSON control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _I	Input pullup current	PSON = 0 V		120		μA
V _{IH}	High-level input voltage		2.4			V
V _{IL}	Low-level input voltage				1.2	V
t _b	Debounce time ($\overline{\text{PSON}}$)	V _{DD} = 5 V	24	38	57	ms
t _{d2}	Delay time ($\overline{\text{PSON}}$ to $\overline{\text{FPO}}$)	V _{DD} = 5 V	t _b +1.1	t _b +2.3	t _b +4	ms

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	Supply current	PSON = 5 V			1	mA



TYPICAL CHARACTERISTICS

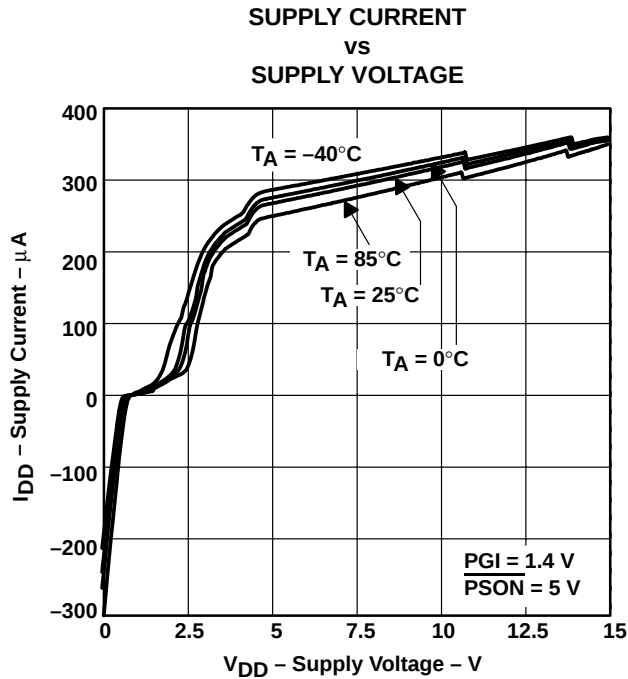


Figure 2

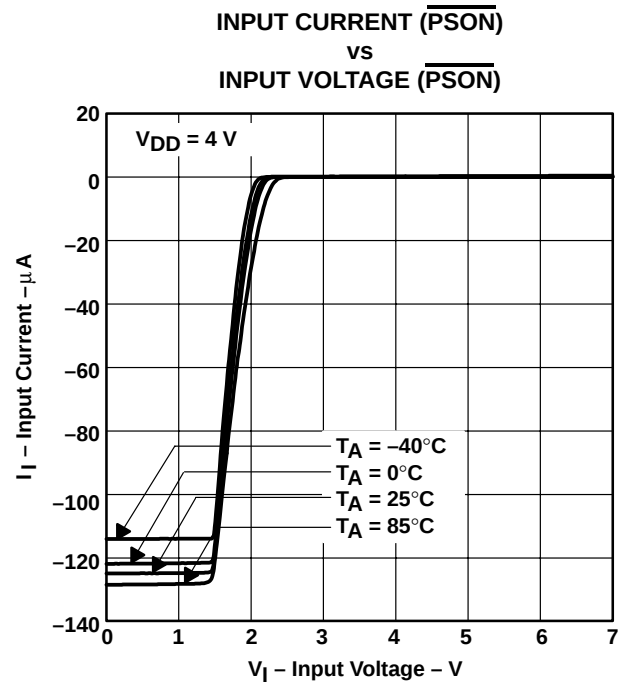


Figure 3

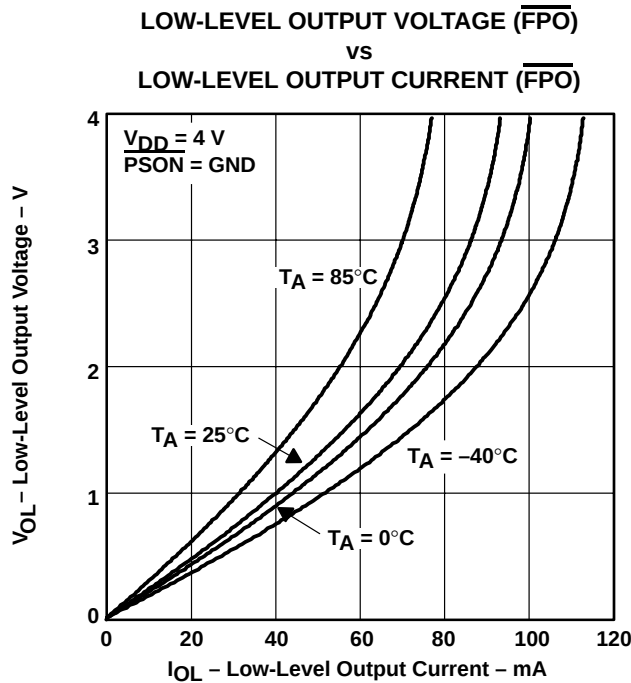


Figure 4

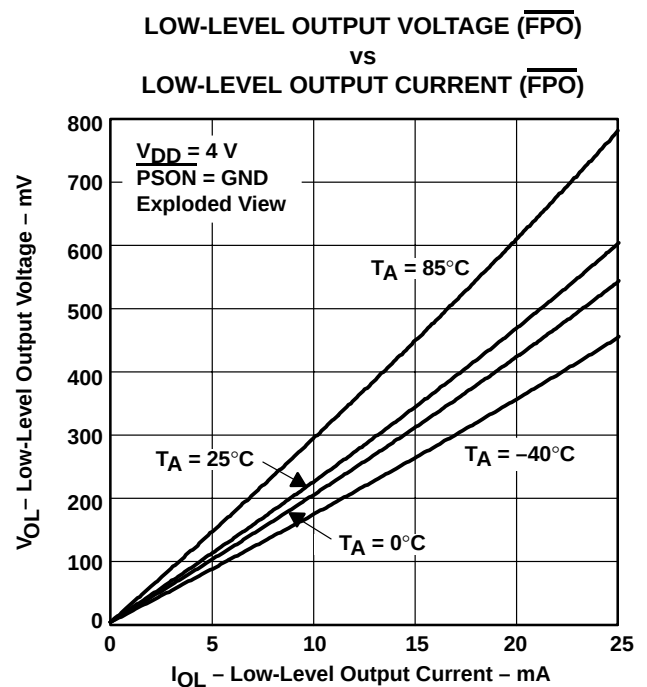


Figure 5

TPS3510,TPS3511 PC POWER SUPPLY SUPERVISORS

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TYPICAL CHARACTERISTICS

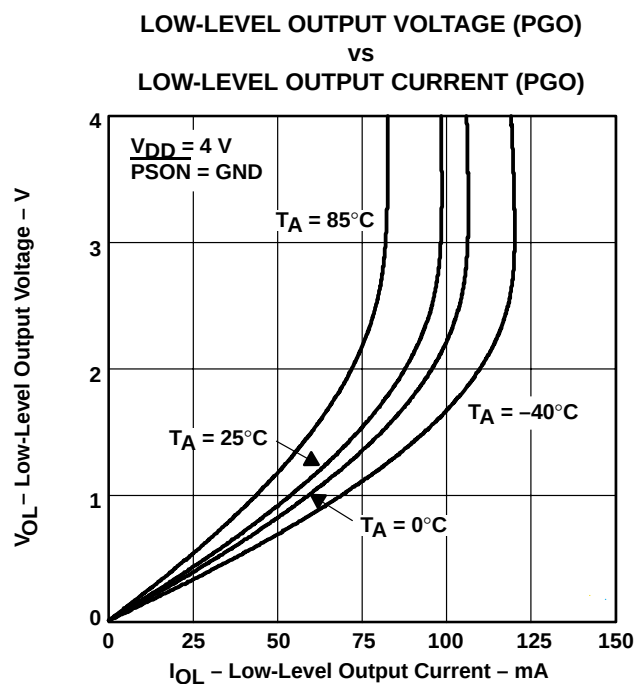


Figure 6

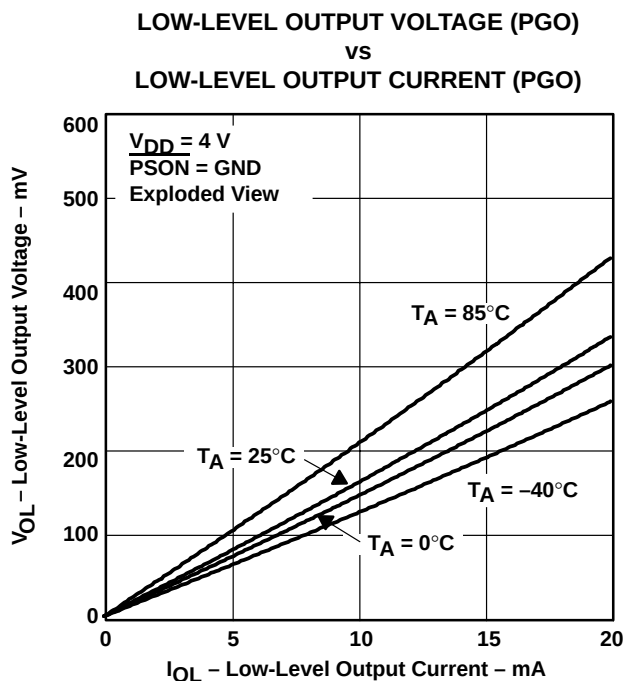


Figure 7

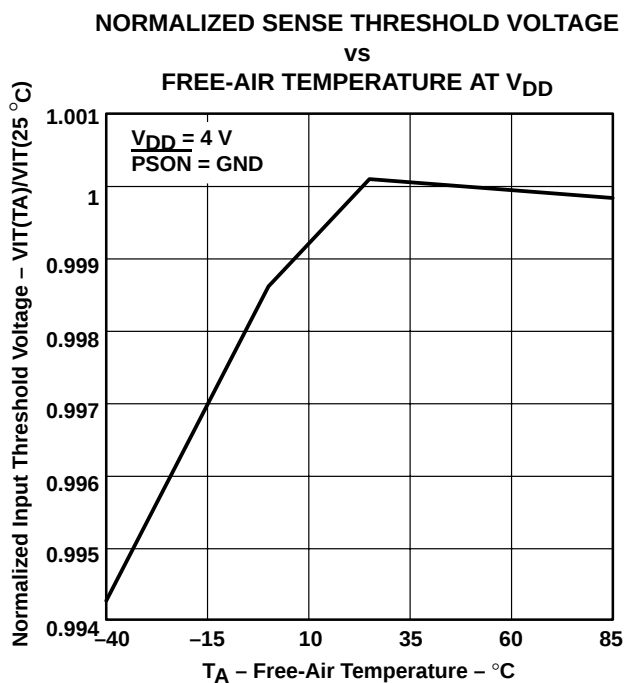


Figure 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3510D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS3510	Samples
TPS3510DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS3510	Samples
TPS3510DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS3510	Samples
TPS3510P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TPS3510P	Samples
TPS3510PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TPS3510P	Samples
TPS3511D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PS3511	Samples
TPS3511DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PS3511	Samples
TPS3511DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PS3511	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3510DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3511DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3510DR	SOIC	D	8	2500	340.5	336.1	25.0
TPS3511DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

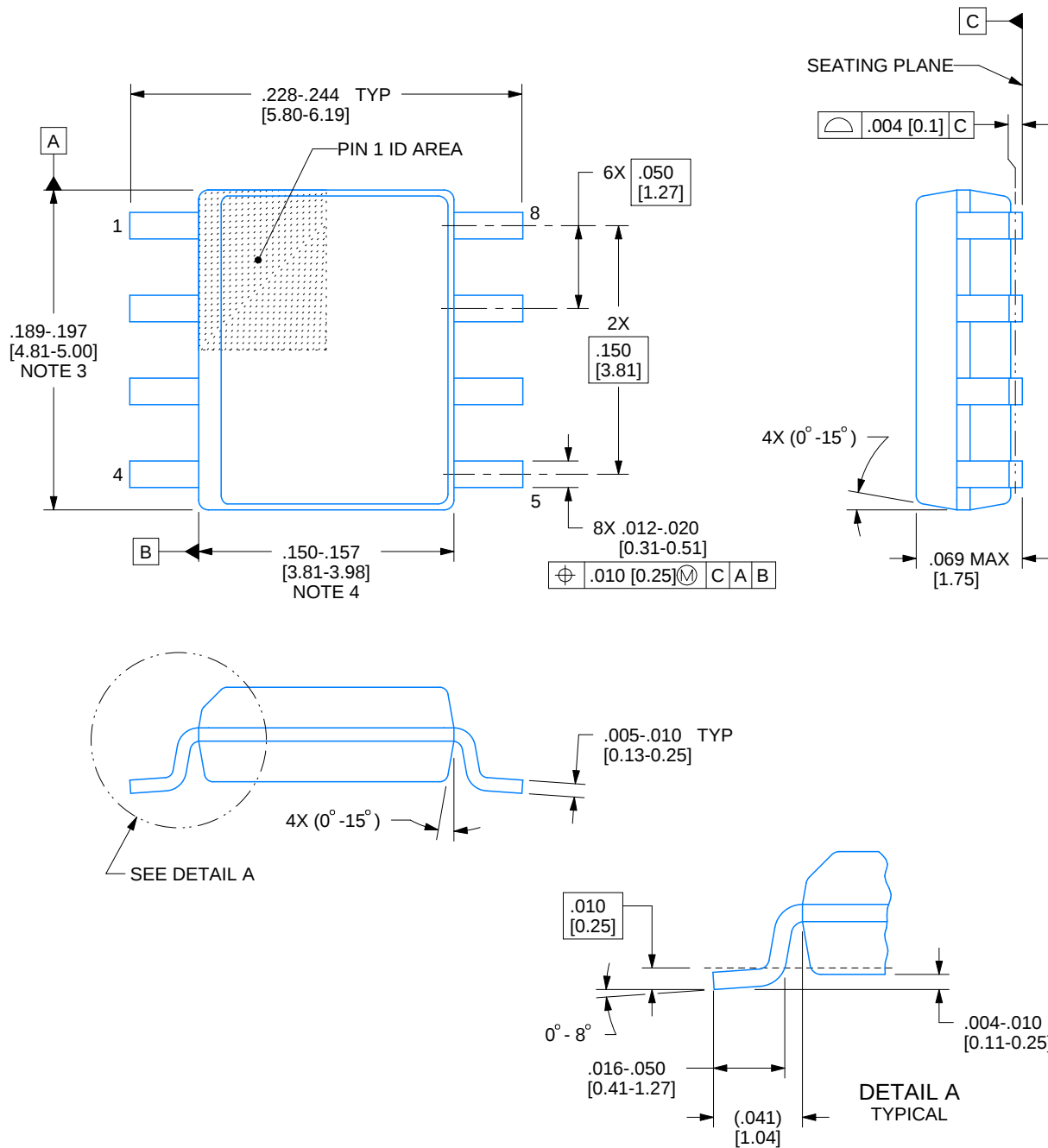
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS3510D	D	SOIC	8	75	507	8	3940	4.32
TPS3510P	P	PDIP	8	50	506	13.97	11230	4.32
TPS3510PE4	P	PDIP	8	50	506	13.97	11230	4.32
TPS3511D	D	SOIC	8	75	507	8	3940	4.32

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

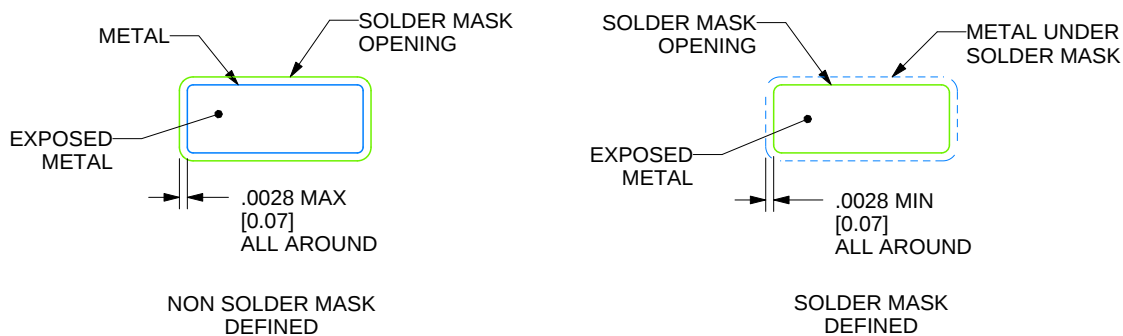
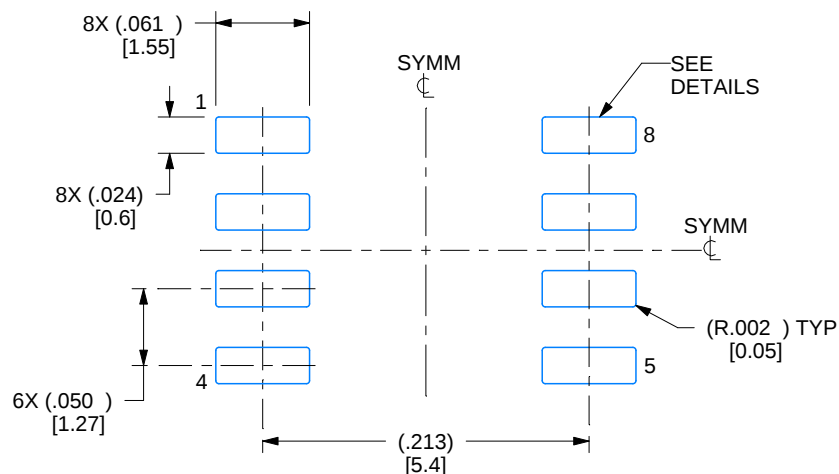
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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