CSD25501F3 –20V P 沟道 FemtoFET™ MOSFET

1 特性

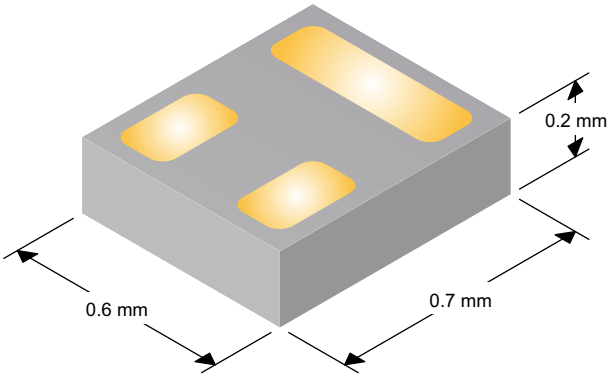
- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 超小尺寸
  - 0.7mm × 0.6mm
- 薄型
  - 最大高度为 0.22mm
- 集成型 ESD 保护二极管
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

此 –20V、64mΩ、P 沟道 FemtoFET™ MOSFET 经过设计和优化，能够尽可能减小许多手持式和移动应用中的空间占用。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。集成的 10kΩ 钳位电阻器 (R_C) 可根据占空比让栅极电压 (V_{GS}) 高于最大内部栅极氧化值 –6V。通过二极管的栅极泄漏 (I_{GSS}) 随着 V_{GS} 增加到高于 –6V 而增加。



典型部件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	总栅极电荷 (–4.5V)	1.02		nC
Q_{gd}	栅极电荷 (栅极到漏极)	0.09		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = –1.8V	120	mΩ
		V_{GS} = -2.5V	86	
		V_{GS} = –4.5V	64	
$V_{GS(th)}$	阈值电压	-0.75		V

器件信息

器件(1)	数量	包装介质	封装	配送
CSD25501F3	3000	7 英寸卷带	Femto 0.73mm × 0.64mm 基板栅格阵列 (LGA)	卷带包装
CSD25501F3T	250			

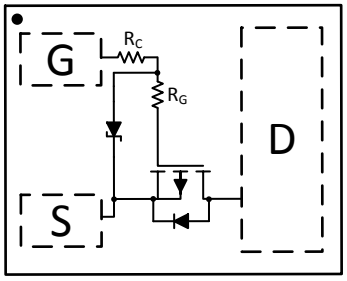
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C (除非另外注明)		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-20	V
I_D	持续漏极电流(1)	–3.6	A
I_{DM}	脉冲漏极电流(1) (2)	–13.6	A
P_D	功率耗散(1)	500	mW
$V_{(ESD)}$	人体放电模式 (HBM)	4000	V
	组件充电模式 (CDM)	2000	
T_J、T_{stg}	运行结温、贮存温度	–55 至 150	°C

(1) 安装在覆铜区域极小的 FR4 材料上时的典型 $R_{\theta JA}$ = 255°C/W。

(2) 脉冲持续时间 ≤ 100 µs，占空比 ≤ 1%。



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (January 2018) to Revision B (October 2021)	Page
• Added footnote with link to support document	8

Changes from Revision * (October 2017) to Revision A (January 2018)	Page
• Added mechanical dimension information and 表 7-1	7

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –6 V			–50	nA
		V_{DS} = 0 V, V_{GS} = –16 V			–1	mA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.45	–0.75	–1.05	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		120	260	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.4 A		86	125	
		V_{GS} = –4.5 V, I_{DS} = –0.4 A		64	76	
g_{fs}	Transconductance	V_{DS} = –2 V, I_{DS} = –0.4 A		3.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 100 kHz		295	385	pF
C_{oss}	Output capacitance			70	91	pF
C_{rss}	Reverse transfer capacitance			4.1	5.3	pF
R_G	Series gate resistance			33		Ω
R_C	Series clamp resistance			10,000		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.4 A		1.02	1.33	nC
Q_{gd}	Gate charge gate-to-drain			0.09		nC
Q_{gs}	Gate charge gate-to-source			0.45		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.36		nC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1.8		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.4 A, R_G = 0 Ω		474		ns
t_r	Rise time			428		ns
$t_{d(off)}$	Turnoff delay time			1154		ns
t_f	Fall time			945		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.4 A, V_{GS} = 0 V		–0.73	–0.95	V
Q_{rr}	Reverse recovery charge	V_{DS} = –10 V, I_F = –0.4 A, di/dt = 200 A/μs		3.0		nC
t_{rr}	Reverse recovery time			7.4		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	°C/W

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

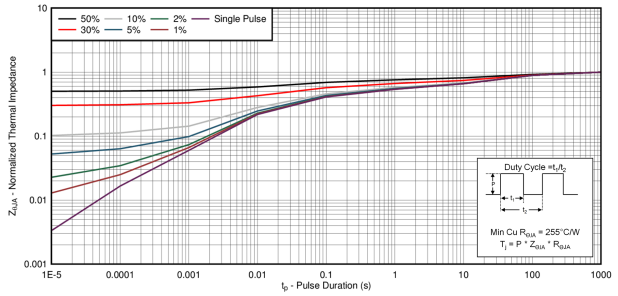


图 5-1. Transient Thermal Impedance

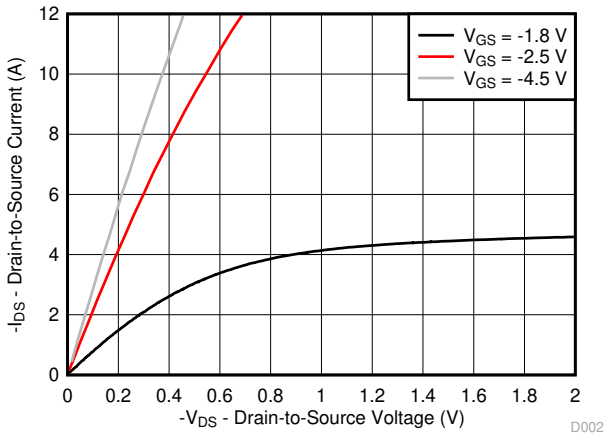
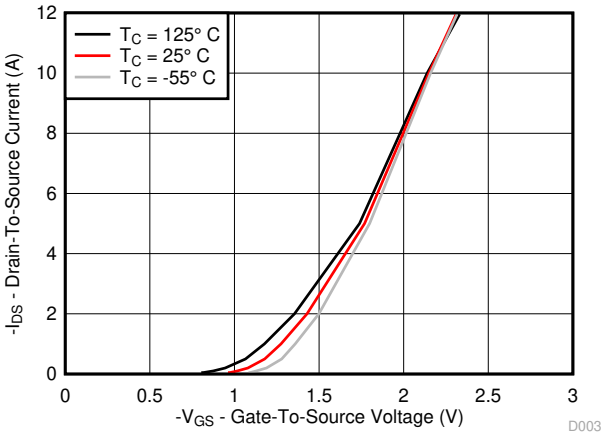
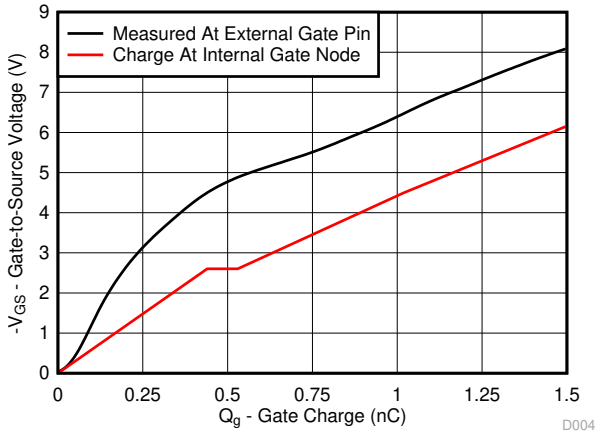


图 5-2. Saturation Characteristics



V_{DS} = – 5 V

图 5-3. Transfer Characteristics



I_D = – 0.4 A V_{DS} = – 10 V

图 5-4. Gate Charge

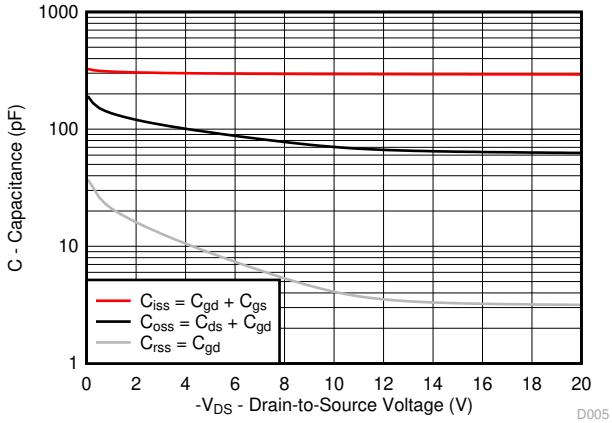
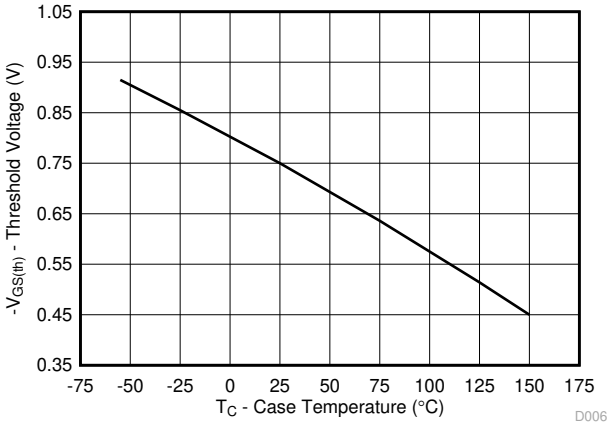


图 5-5. Capacitance

5.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = –250 µA

图 5-6. Threshold Voltage vs Temperature

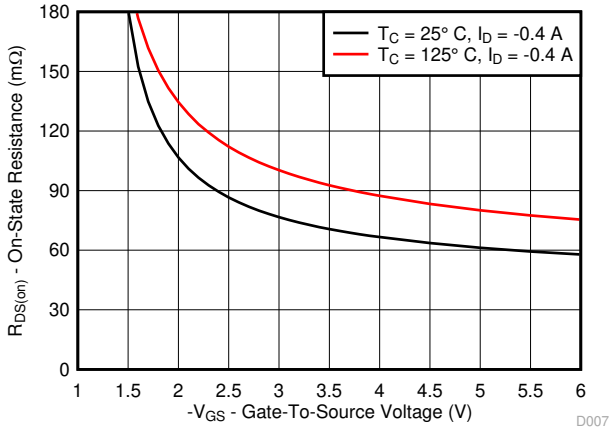
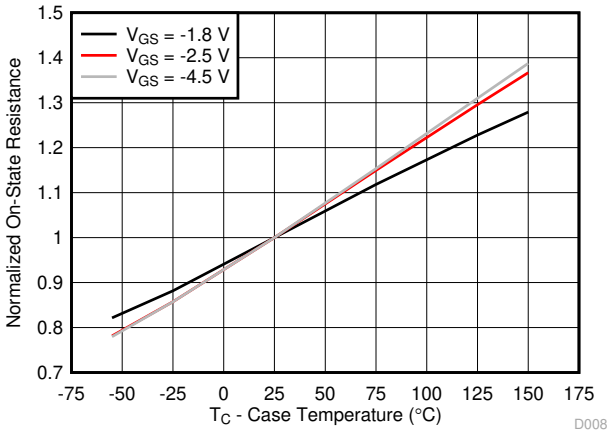


图 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.4 A

图 5-8. Normalized On-State Resistance vs Temperature

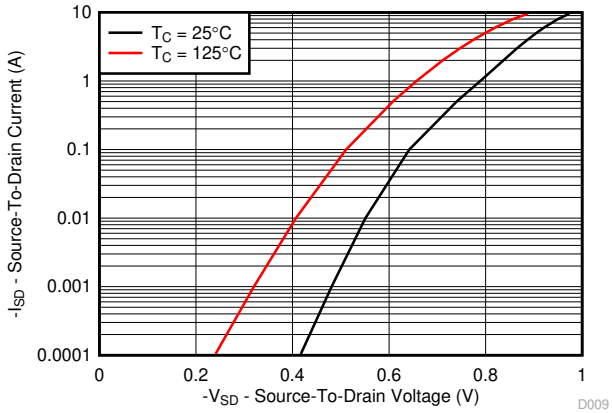
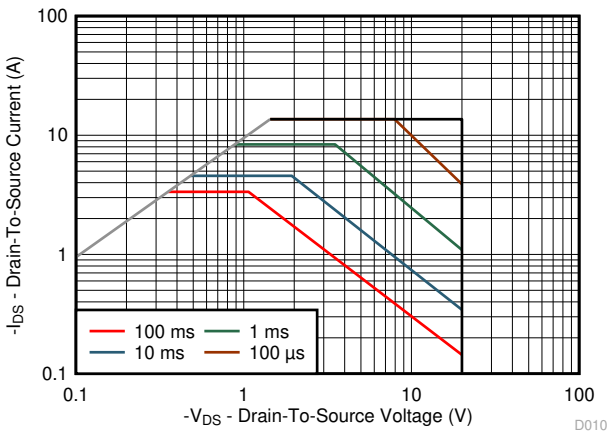
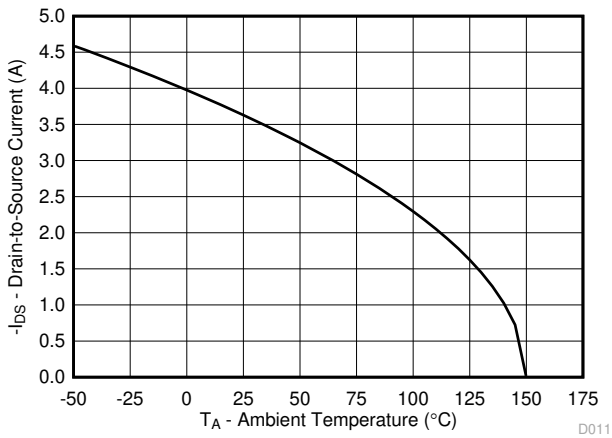


图 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 255°C/W

图 5-10. Maximum Safe Operating Area



Typical $R_{\theta JA}$ = 90°C/W

图 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

6.3 Trademarks

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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

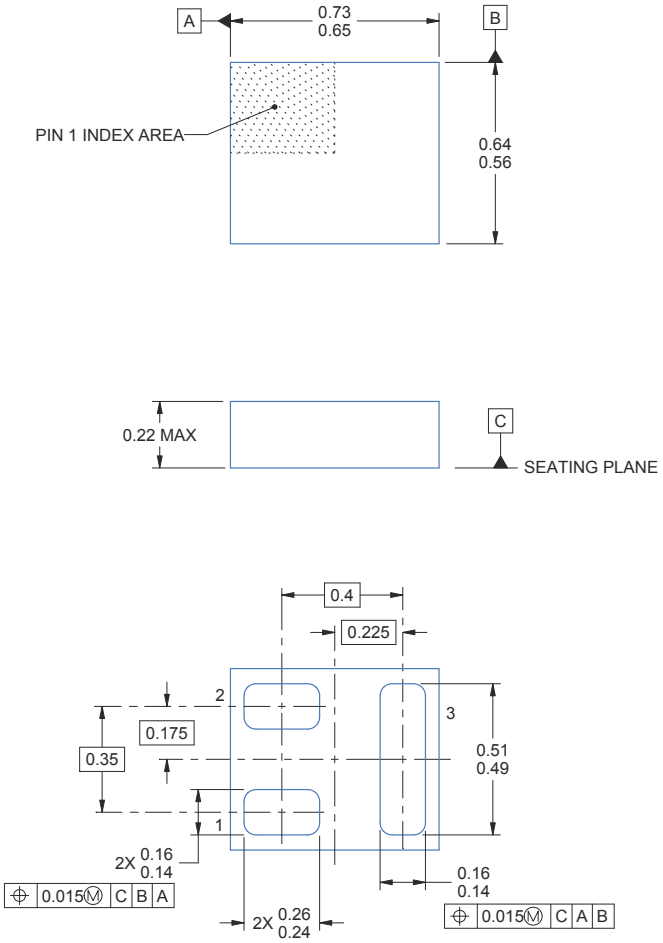
6.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



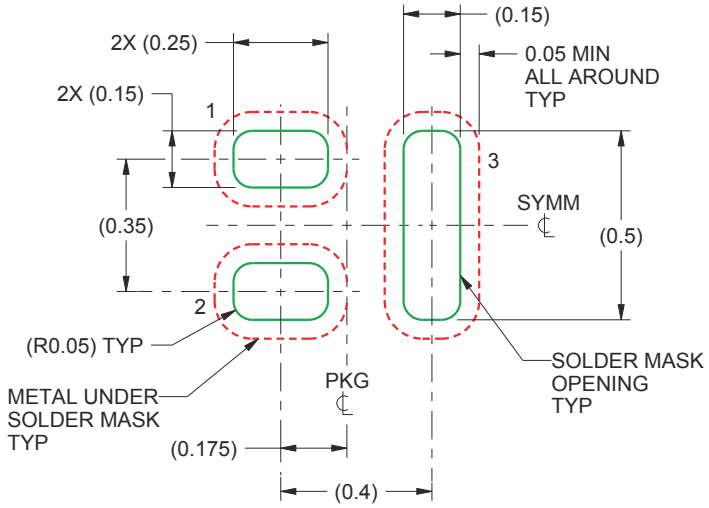
4223685/A 05/2017

A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
B. This drawing is subject to change without notice.
C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

表 7-1. Pin Configuration

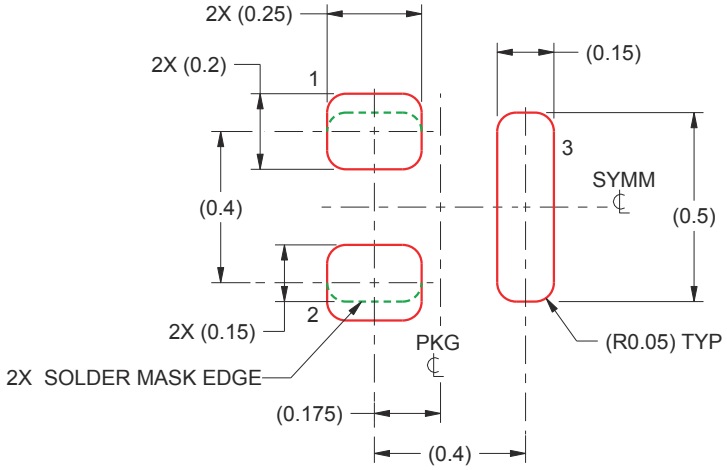
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25501F3	ACTIVE	PICOSTAR	YJN	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	V	Samples
CSD25501F3T	ACTIVE	PICOSTAR	YJN	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

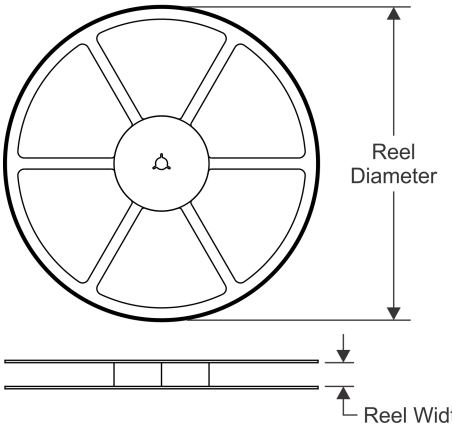
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

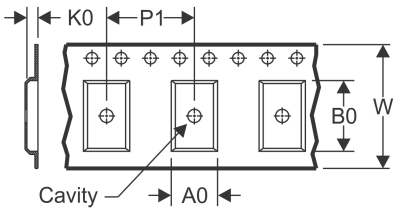
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

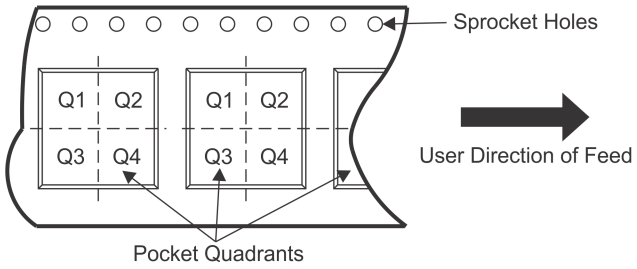


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

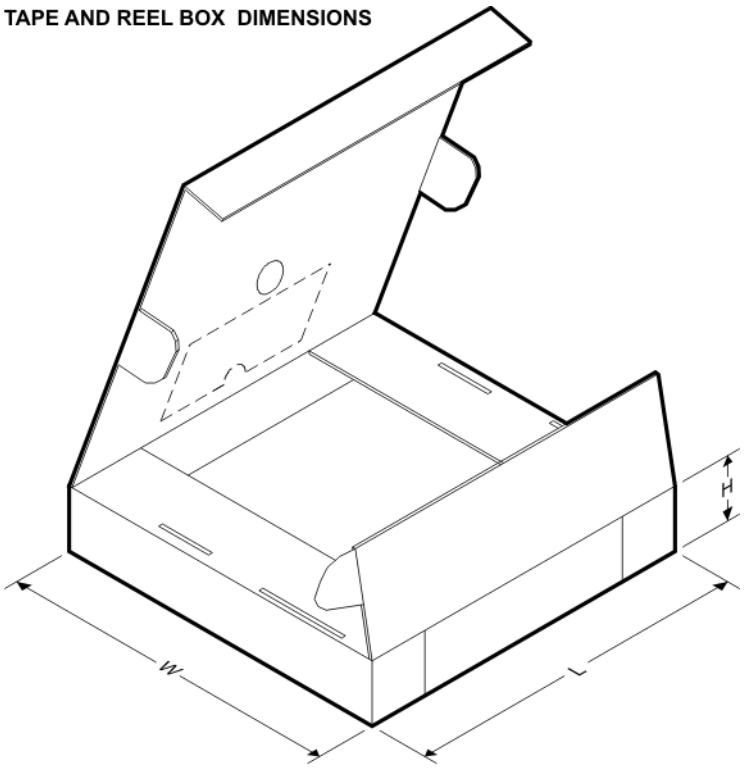
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25501F3	PICOSTAR	YJN	3	3000	180.0	8.4	0.7	0.79	0.31	4.0	8.0	Q2
CSD25501F3T	PICOSTAR	YJN	3	250	180.0	8.4	0.7	0.79	0.31	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25501F3	PICOSTAR	YJN	3	3000	182.0	182.0	20.0
CSD25501F3T	PICOSTAR	YJN	3	250	182.0	182.0	20.0

重要声明和免责声明

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