

SN74HSTL16918

9-BIT TO 18-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

SCES096C – APRIL 1997 – REVISED JANUARY 1999

- Member of the Texas Instruments Widebus™ Family
- Inputs Meet JEDEC HSTL Std JESD 8-6 and Outputs Meet Level III Specifications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Thin Shrink Small-Outline Package

description

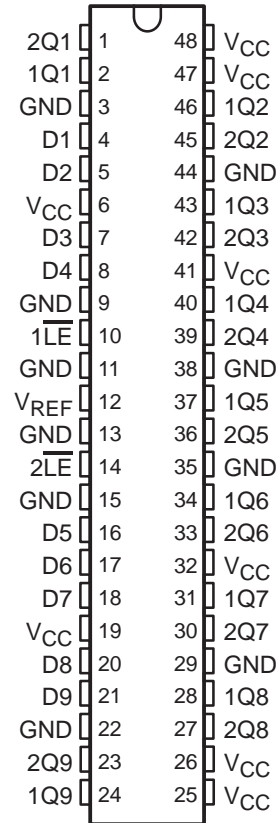
This 9-bit to 18-bit D-type latch is designed for 3.15-V to 3.45-V V_{CC} operation. The D inputs accept HSTL levels and the Q outputs provide LVTTL levels.

The SN74HSTL16918 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable (\overline{LE}) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While \overline{LE} is low, the Q outputs of the corresponding nine latches follow the D inputs. When \overline{LE} is taken high, the Q outputs are latched at the levels set up at the D inputs.

The SN74HSTL16918 is characterized for operation from 0°C to 70°C.

**DGG PACKAGE
(TOP VIEW)**



FUNCTION TABLE

INPUTS		OUTPUT
\overline{LE}	D	Q
L	H	H
L	L	L
H	X	Q_0^\dagger

† Output level before the indicated steady-state input conditions were established



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

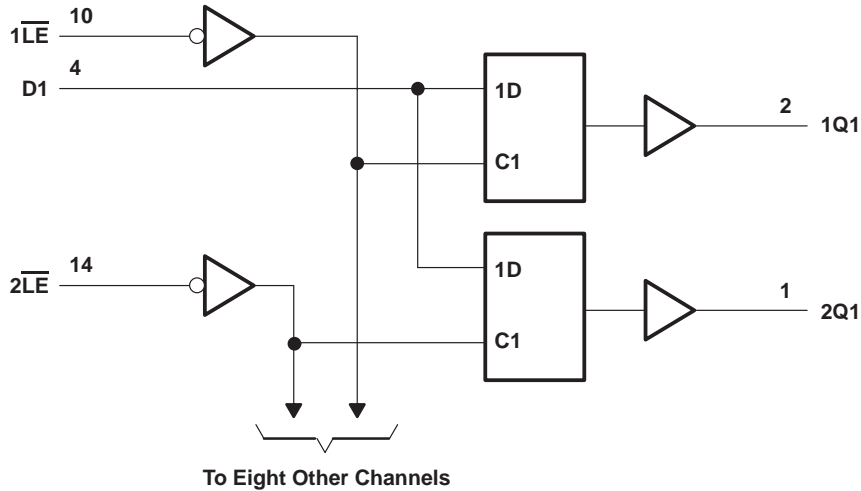
Copyright © 1999, Texas Instruments Incorporated

SN74HSTL16918

9-BIT TO 18-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

SCES096C – APRIL 1997 – REVISED JANUARY 1999

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	89°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.15		3.45	V
V_{REF}	Reference voltage	0.68	0.75	0.9	V
V_I	Input voltage	0		1.5	V
V_{IH}	AC high-level input voltage	All inputs		$V_{REF} + 200$ mV	V
V_{IL}	AC low-level input voltage	All inputs		$V_{REF} - 200$ mV	V
V_{IH}	DC high-level input voltage	All inputs		$V_{REF} + 100$ mV	V
V_{IL}	DC low-level input voltage	All inputs		$V_{REF} - 100$ mV	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN74HSTL16918

9-BIT TO 18-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

SCES096C – APRIL 1997 – REVISED JANUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3.15\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 3.15\text{ V}$,	$I_{OH} = -24\text{ mA}$	2.4			V
V_{OL}		$V_{CC} = 3.15\text{ V}$,	$I_{OL} = 24\text{ mA}$			0.5	V
I_I	Control inputs	$V_{CC} = 3.45\text{ V}$	$V_I = 0\text{ or }1.5\text{ V}$			±5	μA
	Data inputs		$V_I = 0\text{ or }1.5\text{ V}$			±5	
	V_{REF}		$V_{REF} = 0.68\text{ V or }0.9\text{ V}$			90	
I_{CC}		$V_{CC} = 3.45\text{ V}$,	$V_I = 0\text{ or }1.5\text{ V}$		50	100	mA
C_i	Control inputs	$V_{CC} = 0\text{ or }3.3\text{ V}$,	$V_I = 0\text{ or }3.3\text{ V}$		2		pF
	Data inputs	$V_{CC} = 0\text{ or }3.3\text{ V}$,	$V_I = 0\text{ or }3.3\text{ V}$		2.5		
C_o	Outputs	$V_{CC} = 0$,	$V_O = 0$		4		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 3.3\text{ V}$ $\pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_w	Pulse duration, \overline{LE} low		3		ns
t_{su}	Setup time, D before $\overline{LE}\uparrow$		2		ns
t_h	Hold time	D after $\overline{LE}\uparrow$	1		ns
t_{ldr}^\ddagger	Data race condition time	D after $\overline{LE}\downarrow$		0	ns

‡ This is the maximum time after \overline{LE} switches low that the data input can return to the latched state from the opposite state without producing a glitch on the output.

switching characteristics over recommended operating free-air temperature range, $V_{REF} = 0.75\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_{pd}	D	Q	1.9	3.4	ns
	\overline{LE}		1.9	4.2	

simultaneous switching characteristics over recommended operating free-air temperature range, $V_{REF} = 0.75\text{ V}$ §

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_{pd}	D	Q	1.9	4.4	ns
	\overline{LE}		1.9	5.2	

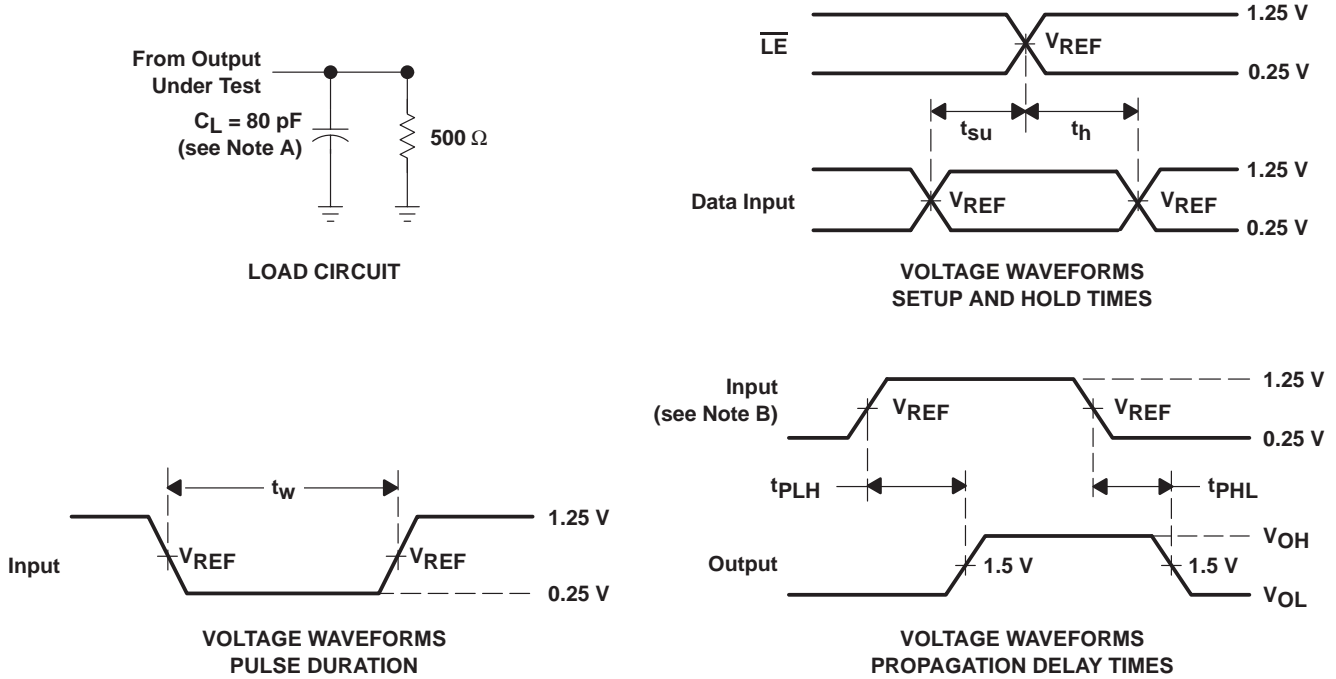
§ All outputs switching

SN74HSTL16918

9-BIT TO 18-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

SCES096C – APRIL 1997 – REVISED JANUARY 1999

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 1 \text{ ns}$, $t_f \leq 1 \text{ ns}$.
 - C. The outputs are measured one at a time with one transition per measurement.
 - D. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HSTL16918DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HSTL16918	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

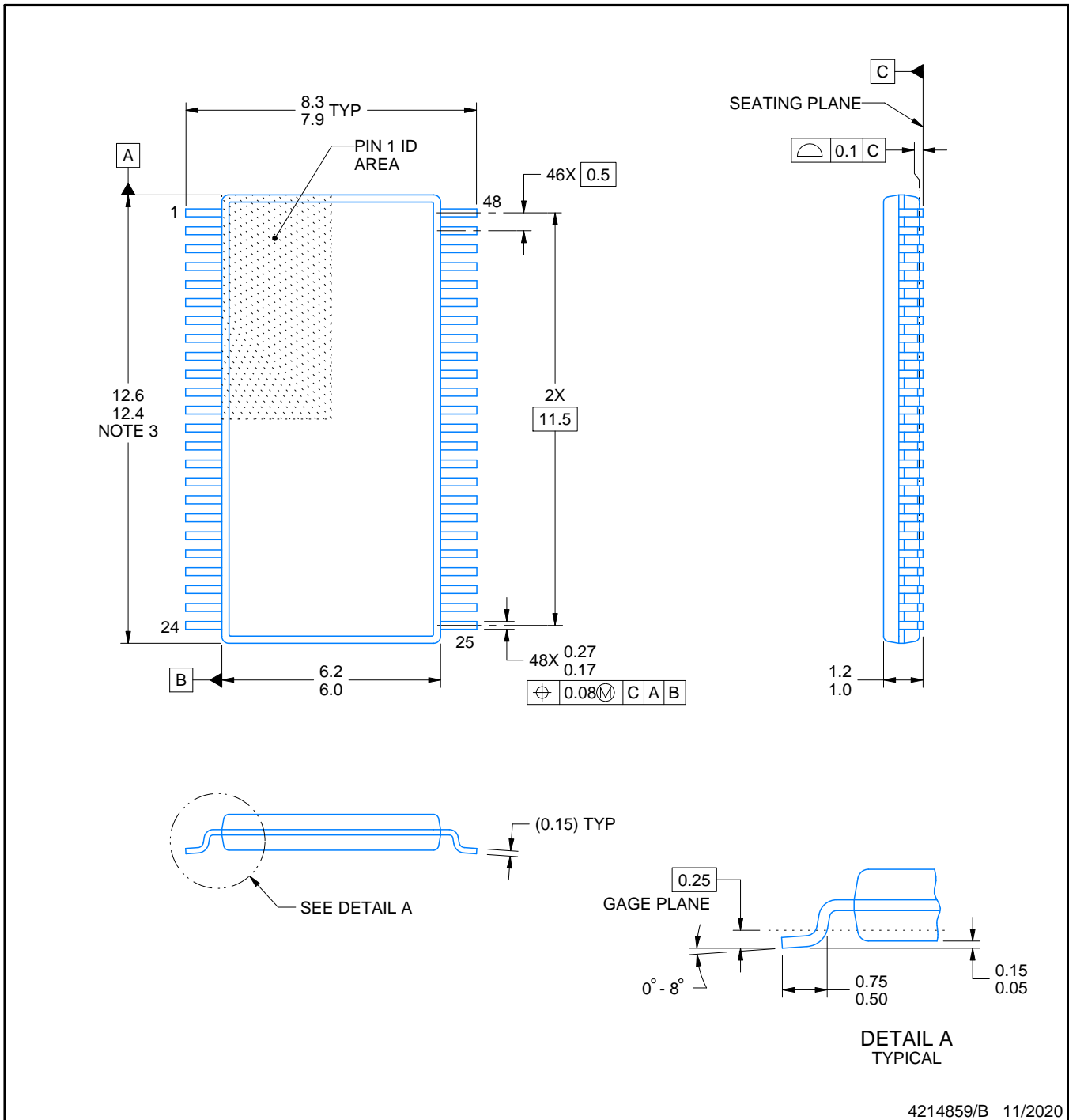
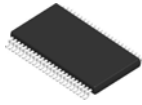
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HSTL16918DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HSTL16918DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0



4214859/B 11/2020

NOTES:

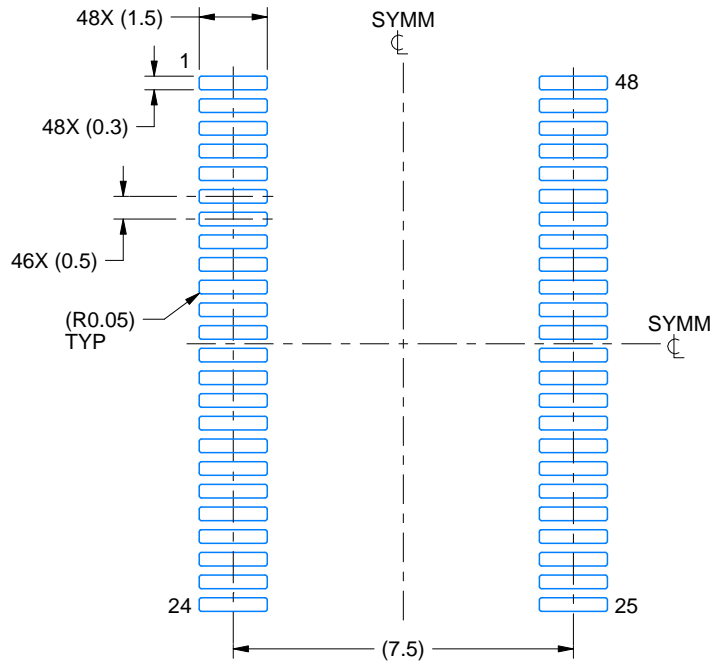
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

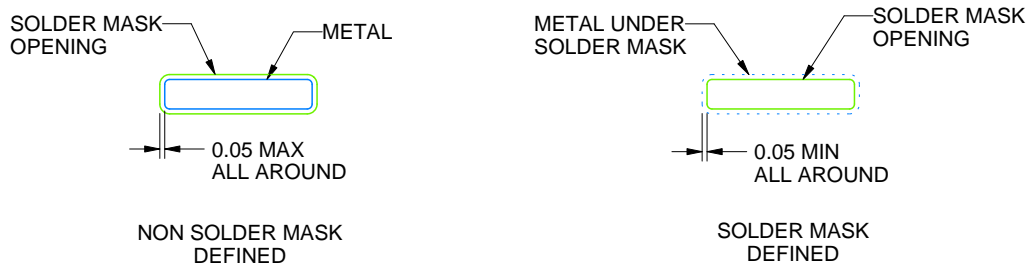
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

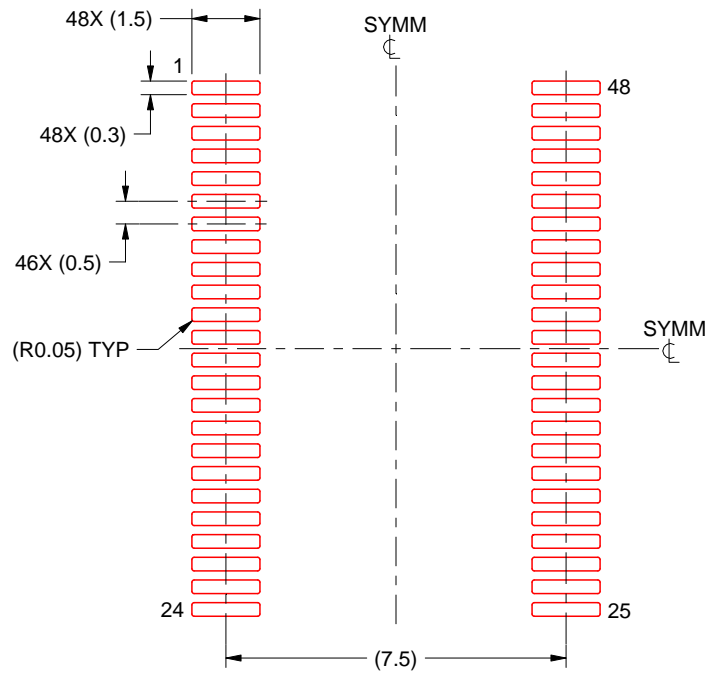
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated