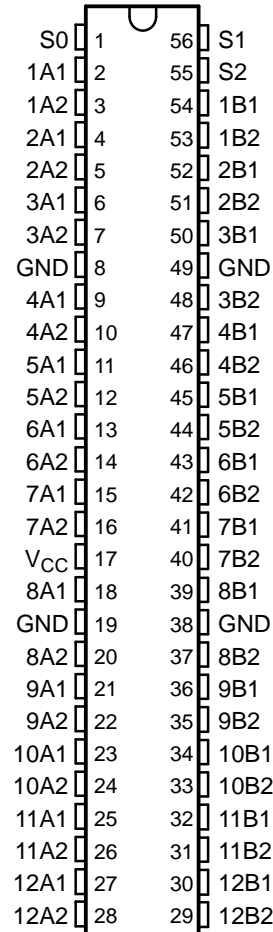


## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Output Voltage Translation Tracks  $V_{CC}$
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
  - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V  $V_{CC}$
  - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V  $V_{CC}$
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 5 \Omega$  Typ)
- Low Input/Output Capacitance Minimizes Loading ( $C_{io(OFF)} = 9 \text{ pF}$  Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 70 \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0-V to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model(A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, PCI Interface, USB Interface, Memory Interleaving, and Bus Isolation
- Ideal for Low-Power Portable Equipment

DGG OR DGV PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN74CB3T16212 is a high-speed TTL-compatible FET bus-exchange switch, with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks  $V_{CC}$ . The SN74CB3T16212 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

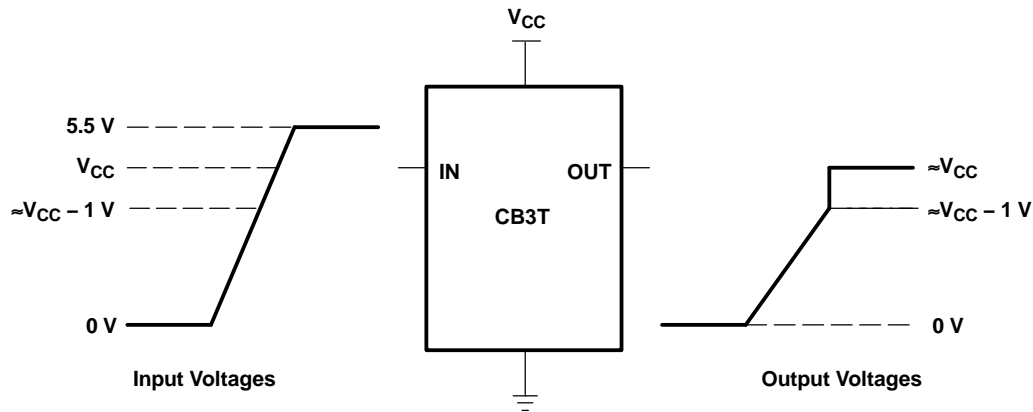


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN74CB3T16212**  
**24-BIT FET-BUS-EXCHANGE SWITCH, 2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH**  
**WITH 5-V-TOLERANT LEVEL SHIFTER**

SCDS157A—OCTOBER 2003—REVISED FEBRUARY 2005



NOTE: If the input high-voltage ( $V_{IH}$ ) level is greater than or equal to  $V_{CC} - 1\text{ V}$  and less than or equal to 5.5 V, the output high-voltage ( $V_{OH}$ ) level is equal to approximately the  $V_{CC}$  voltage level.

**Figure 1. Typical DC Voltage Translation Characteristics**

The SN74CB3T16212 operates as a 24-bit bus switch or as a 12-bit bus exchange that provides data exchanging between four signal ports. The select (S0, S1, S2) inputs control the data path of the bus-exchange switch. When the bus-exchange switch is ON, the A port is connected to the B port, allowing bidirectional data flow between ports. When the bus-exchange switch is OFF, a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

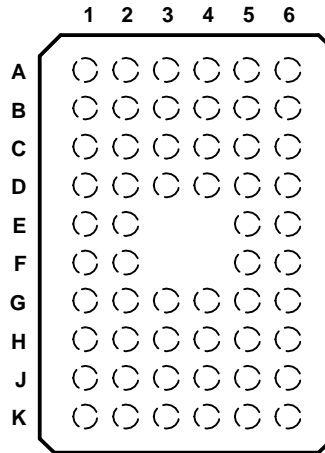
To ensure the high-impedance state during power up or power down, each select input should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74CB3T16212DGGR	CB3T16212
	TVSOP – DGV	Tape and reel	SN74CB3T16212DGVR	KR212
	VFBGA – GQL	Tape and reel	SN74CB3T16212GQLR	KR212
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74CB3T16212ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**GQL OR ZQL PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS**

	1	2	3	4	5	6
<b>A</b>	1A2	1A1	S0	S1	S2	1B1
<b>B</b>	3A1	2A2	2A1	1B2	2B1	2B2
<b>C</b>	4A1	GND	3A2	3B1	GND	3B2
<b>D</b>	5A2	4A2	5A1	4B2	4B1	5B1
<b>E</b>	6A2	6A1			5B2	6B1
<b>F</b>	7A1	7A2			7B1	6B2
<b>G</b>	V <sub>CC</sub>	GND	8A1	8B1	GND	7B2
<b>H</b>	8A2	9A1	9A2	9B2	9B1	8B2
<b>J</b>	10A1	10A2	11A1	11B1	10B2	10B1
<b>K</b>	11A2	12A1	12A2	12B2	12B1	11B2

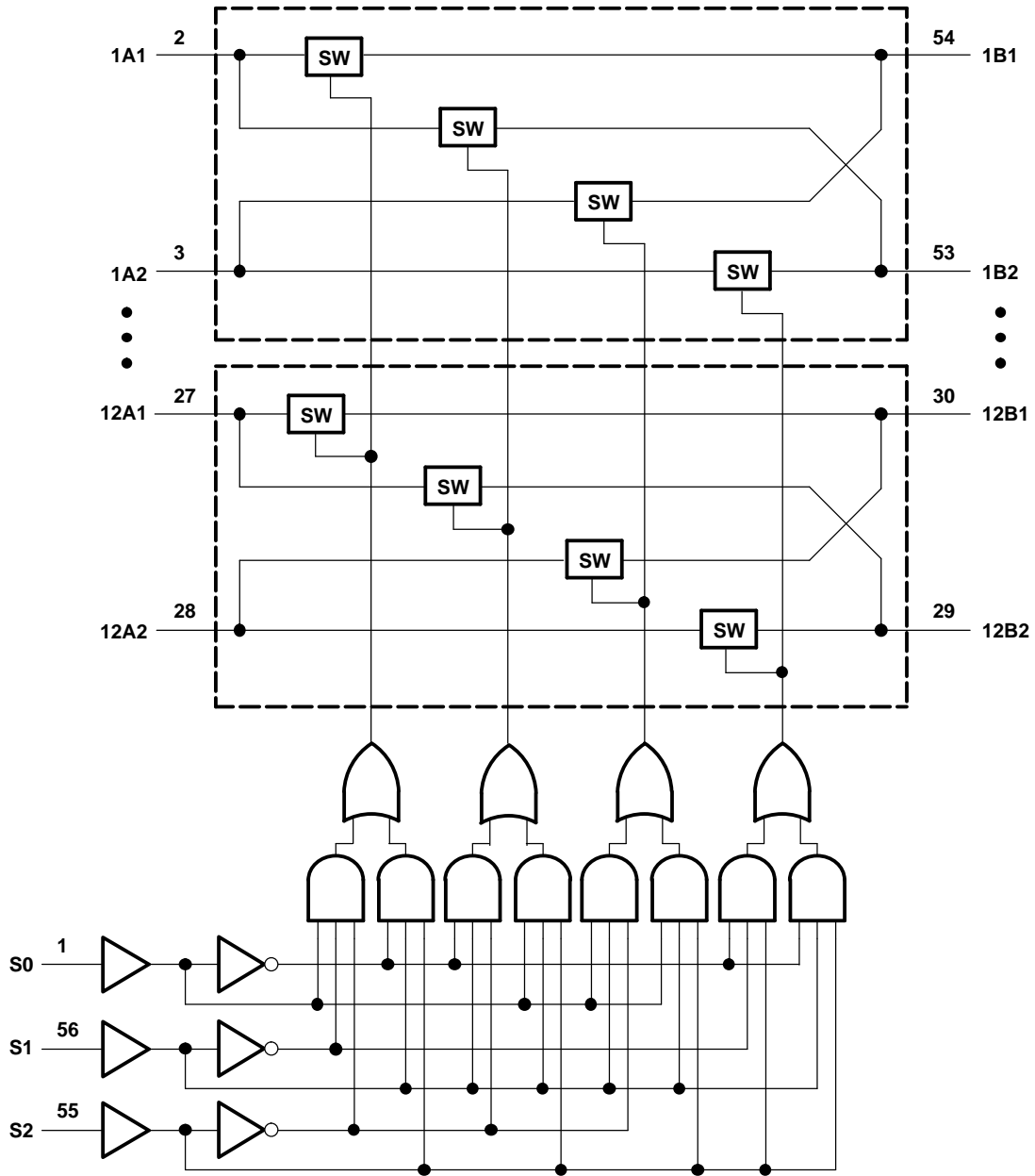
**FUNCTION TABLE**

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1 port	Z	A1 port = B1 port
L	H	L	B2 port	Z	A1 port = B2 port
L	H	H	Z	B1 port	A2 port = B1 port
H	L	L	Z	B2 port	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
H	H	H	B2 port	B1 port	A1 port = B2 port A2 port = B1 port

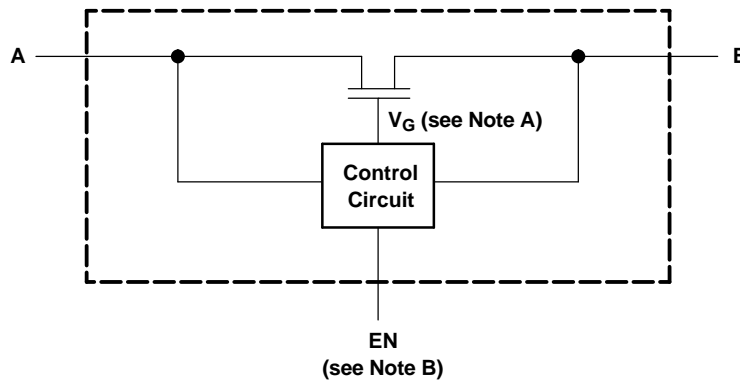
**SN74CB3T16212**  
**24-BIT FET BUS-EXCHANGE SWITCH, 2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH**  
**WITH 5-V-TOLERANT LEVEL SHIFTER**

SCDS157A—OCTOBER 2003—REVISED FEBRUARY 2005

**LOGIC DIAGRAM (POSITIVE LOGIC)**



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



- A. Gate voltage ( $V_G$ ) is equal to approximately  $V_{CC} + V_T$  when the switch is ON and  $V_I > V_{CC} + V_T$ .
- B. EN is the internal enable signal applied to the switch.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(2)</sup>	-0.5	7	V
$V_{IN}$	Control input voltage range <sup>(2)(3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)(4)</sup>	-0.5	7	V
$I_{IK}$	Control input clamp current		-50	mA
$I_{I/OK}$	I/O port clamp current		-50	mA
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		±128	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(6)</sup>	DGG package	64	°C/W
		DGV package	48	
		GQL/ZQL package	42	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2.3	3.6	V	
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	5.5	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	0.8	
$V_{I/O}$	Data input/output voltage	0	5.5	V	
$T_A$	Operating free-air temperature	-40	85	°C	

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT		
$V_{IK}$		$V_{CC} = 3\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V		
$V_{OH}$		See Figures 3 and 4						
$I_{IN}$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_{IN} = 3.6\text{ V to } 5.5\text{ V or GND}$			$\pm 10$	$\mu\text{A}$		
$I_I$		$V_{CC} = 3.6\text{ V}$ , $V_{IN} = V_{CC}$ or GND, Switch ON	$V_I = V_{CC} - 0.7\text{ V to } 5.5\text{ V}$		$\pm 20$	$\mu\text{A}$		
			$V_I = 0.7\text{ V to } V_{CC} - 0.7\text{ V}$		-40			
			$V_I = 0\text{ to } 0.7\text{ V}$		$\pm 5$			
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 3.6\text{ V}$ , $V_I = 0$ , $V_{IN} = V_{CC}$ or GND, $V_O = 0\text{ to } 5.5\text{ V}$ , Switch OFF			$\pm 10$	$\mu\text{A}$		
$I_{off}$		$V_{CC} = 0$ , $V_I = 0$ , $V_O = 0\text{ to } 5.5\text{ V}$			10	$\mu\text{A}$		
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $V_{IN} = V_{CC}$ or GND, $I_{I/O} = 0$ , Switch ON or OFF	$V_I = V_{CC}$ or GND		70	$\mu\text{A}$		
			$V_I = 5.5\text{ V}$		70			
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND			300	$\mu\text{A}$		
$C_{in}$	Control inputs	$V_{CC} = 3.3\text{ V}$ , $V_{IN} = V_{CC}$ or GND		4		pF		
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$ , $V_{IN} = V_{CC}$ or GND, $V_{I/O} = 5.5\text{ V}$ , $3.3\text{ V}$ , or GND, Switch OFF		9		pF		
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$ , $V_{IN} = V_{CC}$ or GND, Switch ON	$V_{I/O} = 5.5\text{ V or } 3.3\text{ V}$		8	pF		
			$V_{I/O} = \text{GND}$		23			
$r_{ON}$ <sup>(5)</sup>		$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$ , $V_I = 0$	$I_O = 24\text{ mA}$		5	9.5	$\Omega$	
			$I_O = 16\text{ mA}$		5	9.5		
		$V_{CC} = 3\text{ V}$ , $V_I = 0$		$I_O = 64\text{ mA}$		5		8.5
				$I_O = 32\text{ mA}$		5		8.5

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

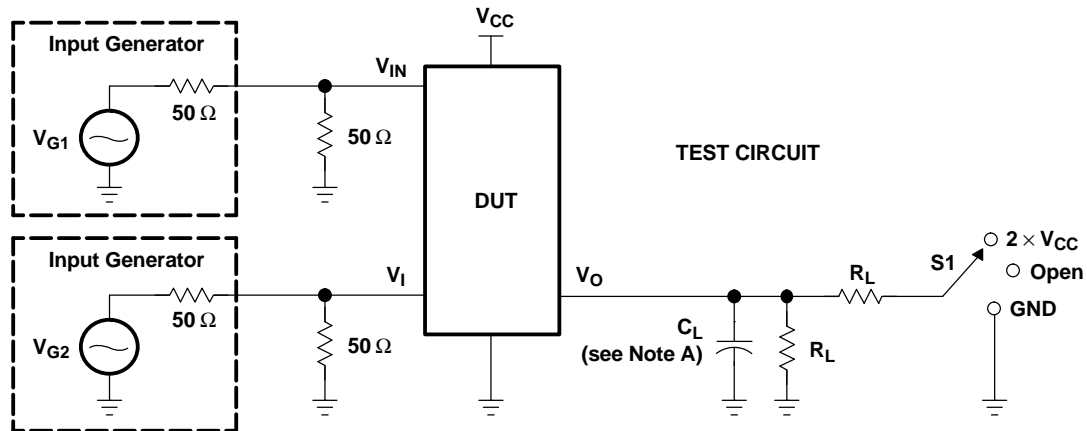
**SWITCHING CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

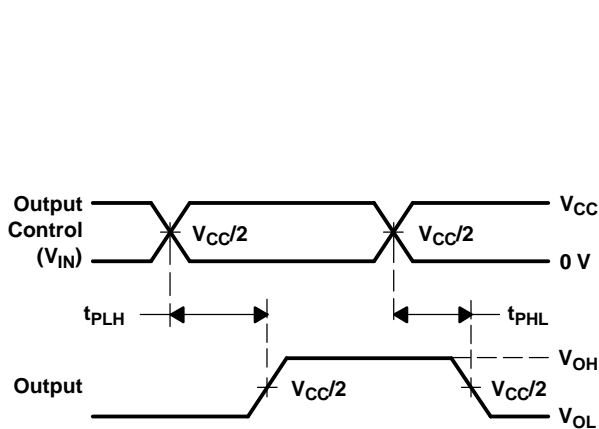
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$ <sup>(1)</sup>	A or B	B or A	0.15		0.25		ns
$t_{pd(s)}$	S	A	1	15.5	1	11.5	ns
$t_{en}$	S	B	1	15	1	12	ns
$t_{dis}$	S	B	1	12	1	10.5	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

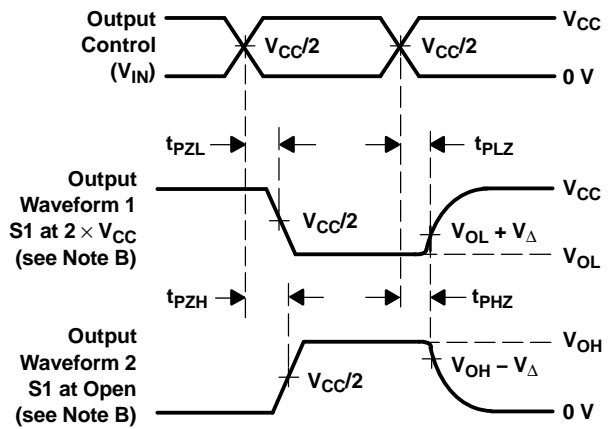
PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd</sub> (s)	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × V <sub>CC</sub>	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (t<sub>pd</sub>(s))



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

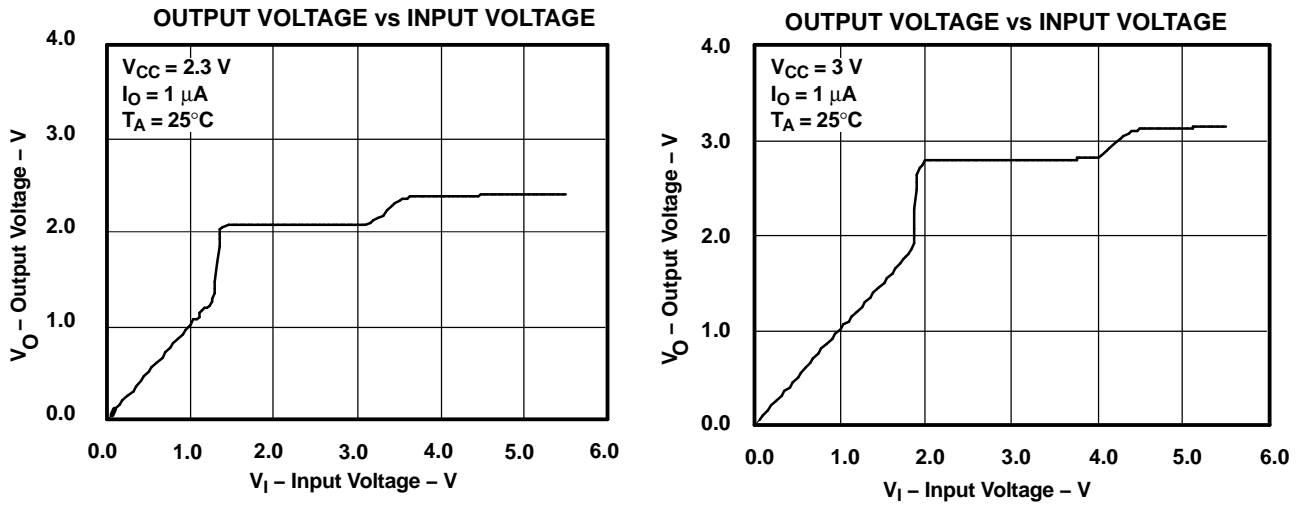


Figure 3. Data Output Voltage vs Data Input Voltage

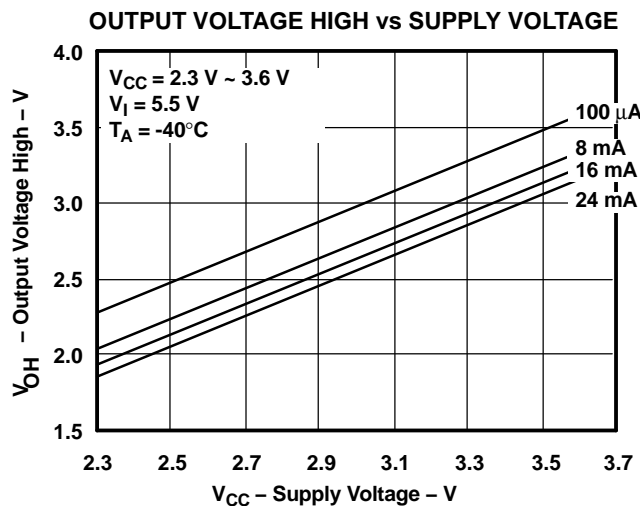
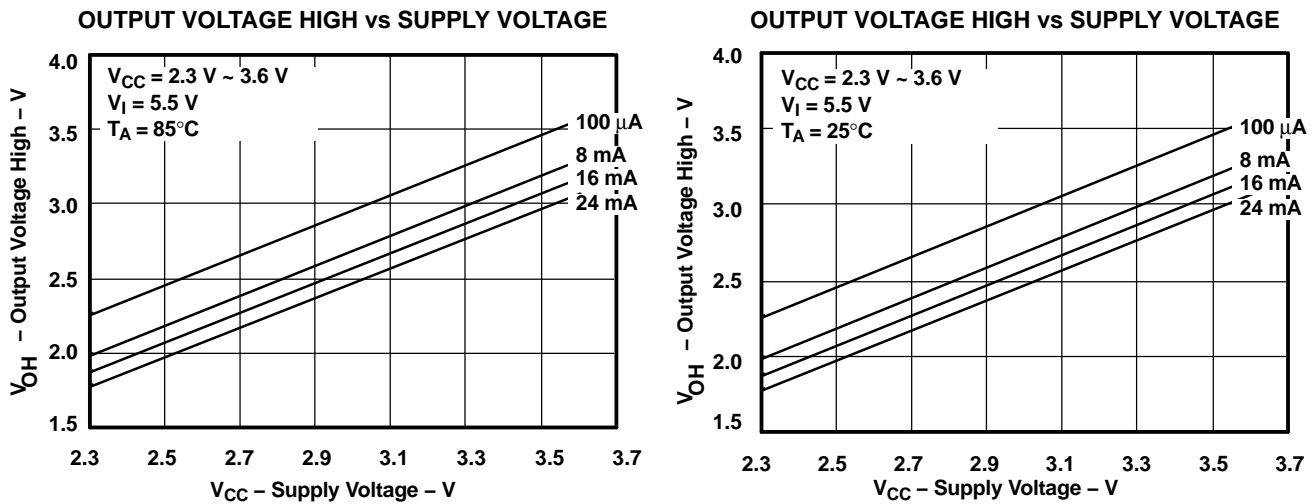


Figure 4.  $V_{OH}$  Values

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3T16212DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16212	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

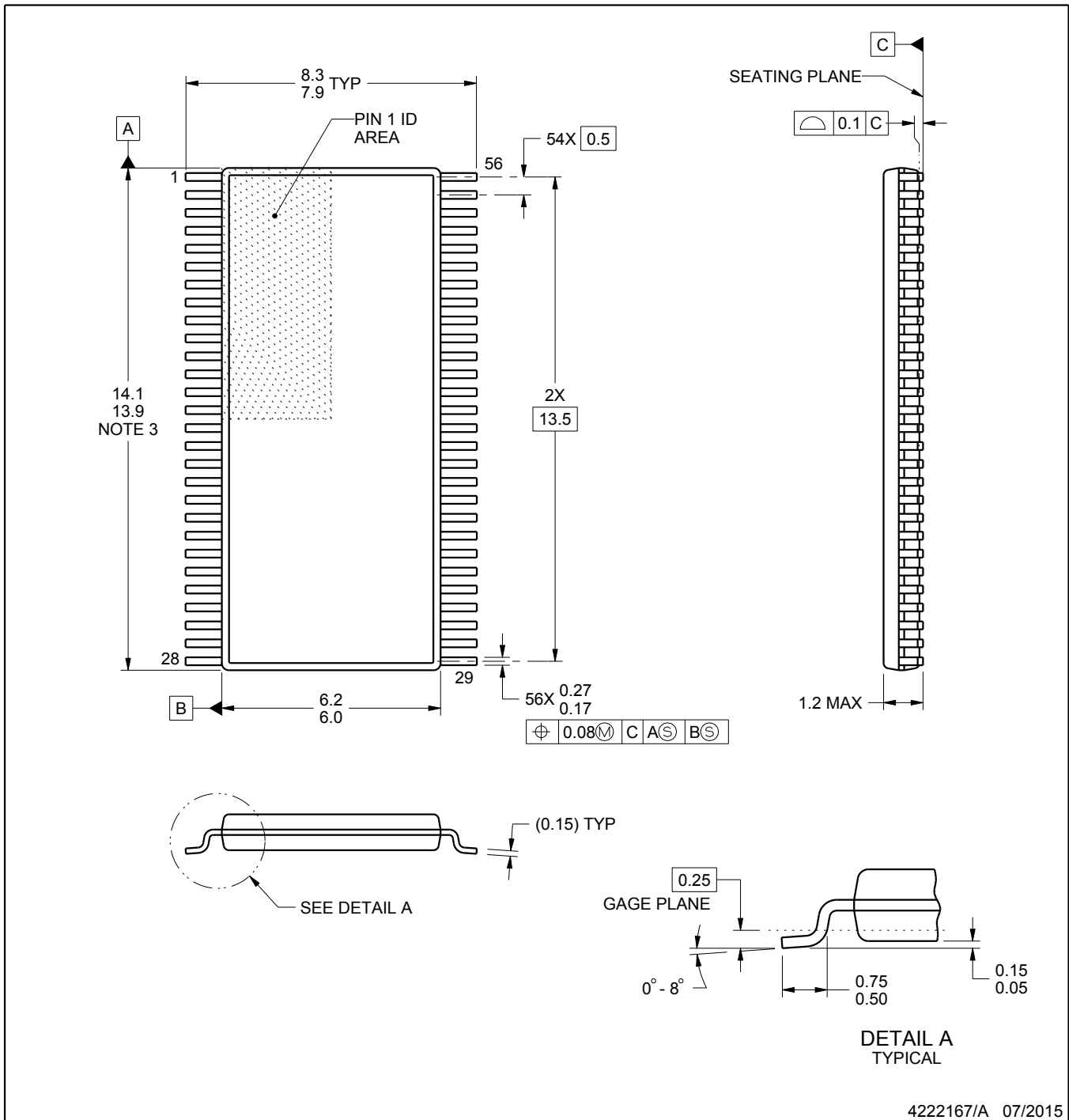
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T16212DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T16212DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0



4222167/A 07/2015

NOTES:

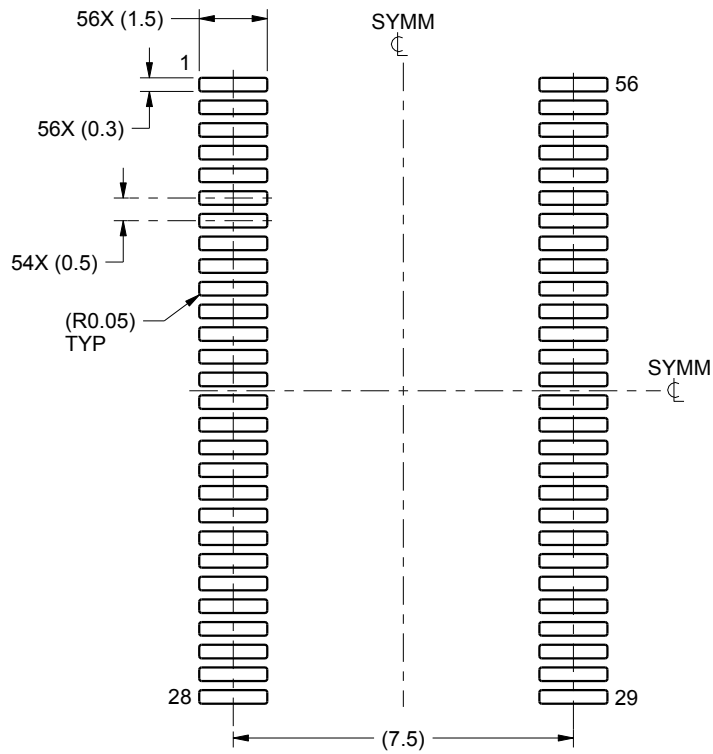
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

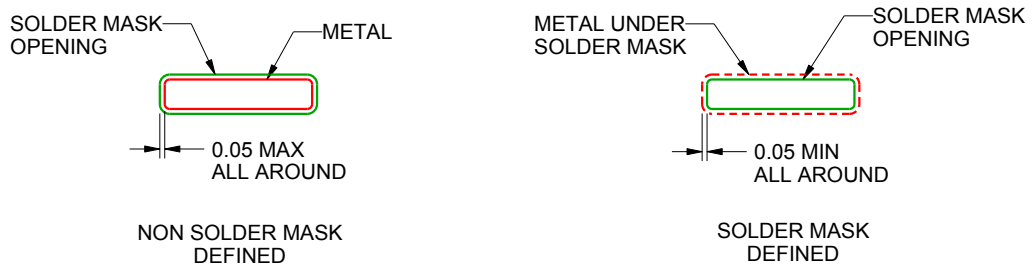
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

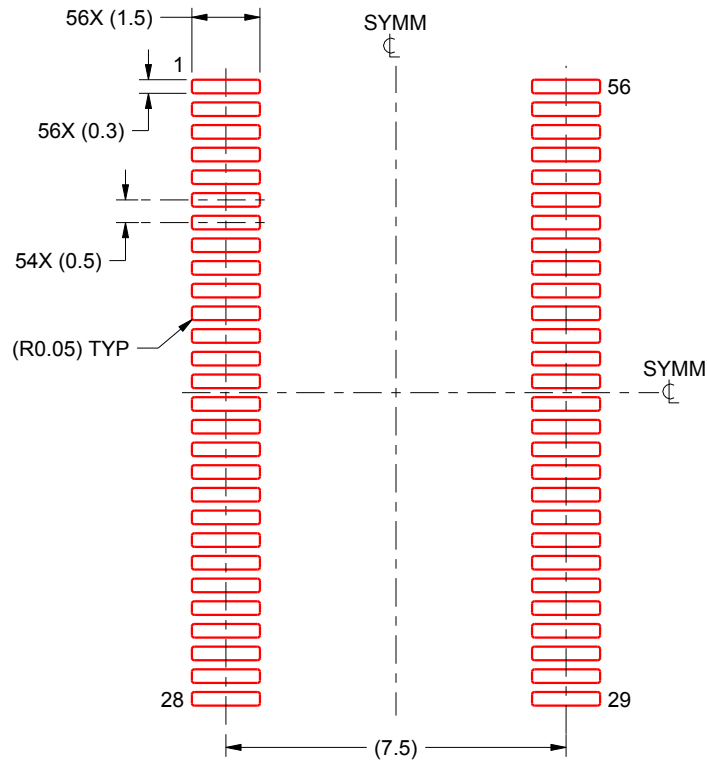
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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