具有 SPI 接口的 TPS92682-Q1 双通道恒压恒流控制器

1 特性

- 符合 AEC-Q100 1 级标准
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 宽输入电压范围：4.5V 至 65V
- 在 –40°C 至 150°C 结温范围内的 LED 电流精度为 ±4%
- SPI 通信接口
- SPI 可编程特性：
  - 通过扩频改善了 EMI
  - 软启动计时
  - ILED 电流和输出电压设置
  - 电流限制，过压，故障计时器
  - 单相与双相
  - CV 和 CC 模式配置
- 双通道峰值电流模式 (PCM) 控制器
- 低输入失调电压轨至轨电流感应放大器
- 模拟调光
- 采用集成 P 通道驱动器接口的外部串联 FET PWM 调光
  - PWM 调光范围超过 1000:1
- 每个通道配备漏极开路故障标志指示器
- 高达 1MHz 的可编程开关频率，具有外部时钟同步功能
- 全面可编程故障保护电路
- 采用可湿性侧面 VQFN 封装

2 应用

- 汽车前灯照明
- 紧急车辆
- 通用照明

3 说明

TPS92682-Q1 是一种带有 SPI 通信接口的双通道峰值电流模式控制器。通过编程，该器件可在恒压 (CV) 或恒流 (CC) 模式下运行。

在 CV 模式下，TPS92682-Q1 可通过编程用作两个独立或双相升压稳压器。可使用外部电阻分压器和 SPI 可编程 8 位 DAC 对输出电压进行编程。

在 CC 模式下，器件设计用于支持双通道升压或降压 LED 驱动器拓扑。可使用模拟调光或 PWM 调光技术来单独调制 LED 电流。使用可编程的 8 位 DAC 可获得高于 28:1 的模拟调光范围。可以借助所需占空比直接调制 PWM 输入引脚或使用 SPI 可编程 10 位 PWM 计数器来实现 LED 电流的 PWM 调光。可选 PDRV 栅极驱动器输出可用于驱动外部 P 通道系列 MOSFET。

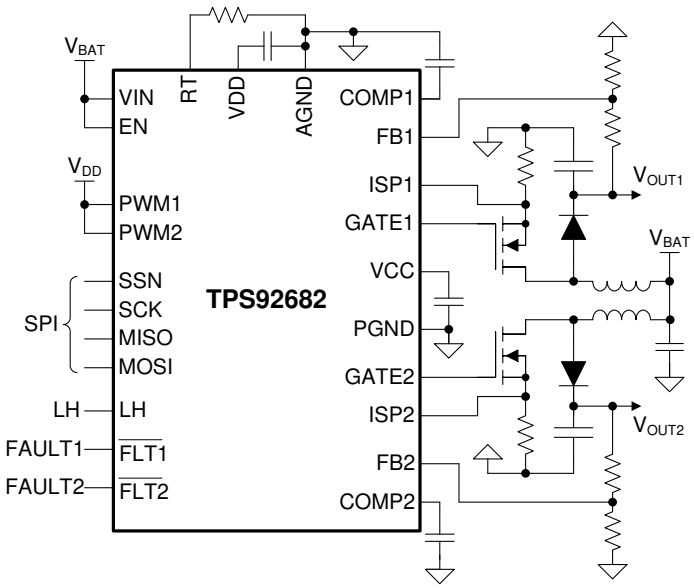
TPS92682-Q1 整合了高级 SPI 可编程诊断和故障保护机制，包括逐周期电流限制、输出过压和欠压保护、ILED 过流保护以及热警告。该器件的每个通道都包含一个漏极开路故障指示器输出。

TPS92682-Q1 包含一个 LH 引脚，在拉高时，会进入跛行回家 (LH) 状态。在 LH 模式下，该器件使用一组独立的 SPI 可编程寄存器。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
TPS92682-Q1	VQFN (32)	5.0mm x 5.0mm
TPS92682-Q1	HTSSOP (32)	11.0mm x 6.1mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Revision History 2
5 Pin Configuration and Functions 3
6 Specifications 5
6.1 Absolute Maximum Ratings 5
6.2 ESD Ratings 5
6.3 Recommended Operating Conditions 5
6.4 Thermal Information 6
6.5 Electrical Characteristics 7
6.6 Typical Characteristics 11
7 Detailed Description 15
7.1 Overview 15
7.2 Functional Block Diagram 15
7.3 Feature Description 18
7.4 Device Functional Modes 31
7.5 Programming 35
7.6 TPS92682 Registers 37
8 Application and Implementation 53
8.1 Application Information General Design Considerations 53
8.2 Application Information CC Mode 55
8.3 Typical Application CV Mode 62
8.4 Typical Application CC Mode 69
8.5 Typical Application CV Mode 77
9 Power Supply Recommendations 83
10 Layout 84
10.1 Layout Guidelines 84
10.2 Layout Example 84
11 Device and Documentation Support 86
11.1 接收文档更新通知 86
11.2 支持资源 86
11.3 Trademarks 86
11.4 静电放电警告 86
11.5 术语表 86
12 Mechanical, Packaging, and Orderable Information 86

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (July 2020) to Revision C (March 2021)	Page
• 添加了 RHB (VQFN) 封装	1
• Added RHB package thermal information	6
• Added 方程式 12 for the BUCK-BOOST FET RMS current	53
• Added *Programming Example for Two-Channel CC Mode* section	60
• Added *Programming Example for Two-Phase CV BOOST* section	67

Changes from Revision A (August 2019) to Revision B (July 2020)	Page
• 向特性 添加了功能安全项目符号	1
• 更新了整个文档的表、图和交叉参考的编号格式。	1
• Added HTSSOP package	3
• Added DAP package thermal information	6

Changes from Revision * (March 2019) to Revision A (August 2019)	Page
• 将“预告信息”更改为“量产数据”	1

5 Pin Configuration and Functions

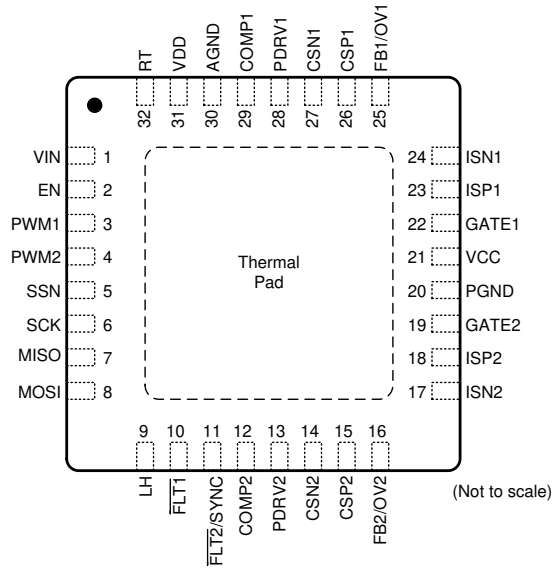


图 5-1. RHM/RHB Package 32-Pin VQFN with PowerPAD Top View

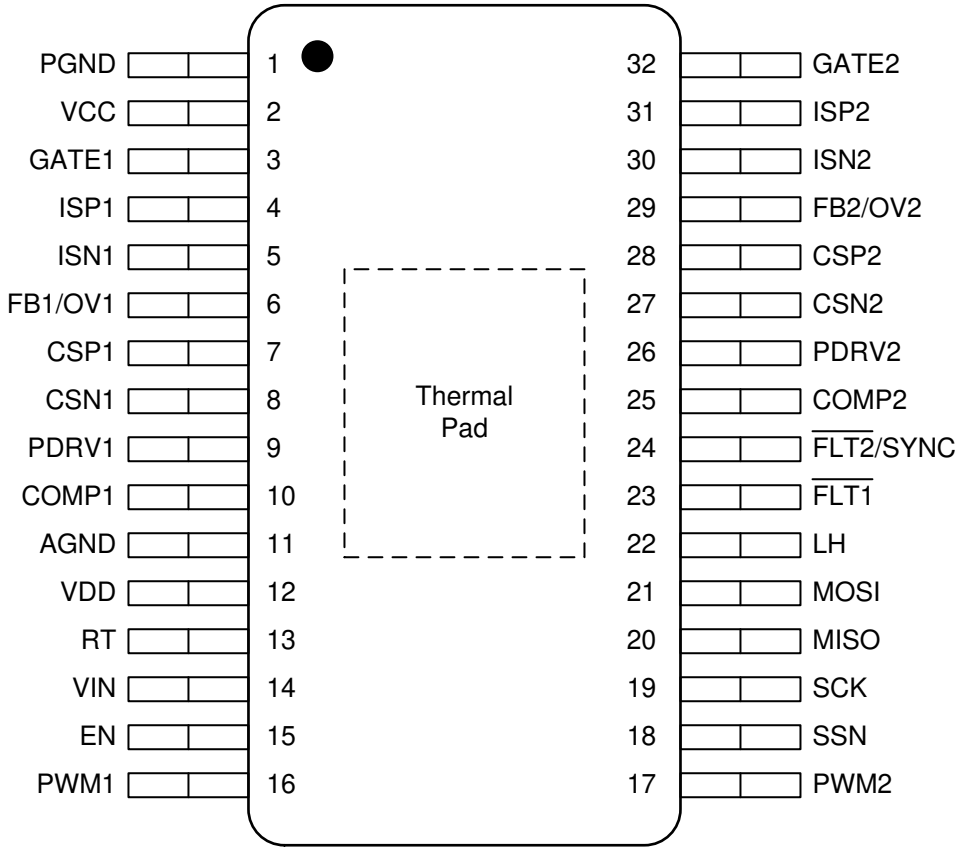


图 5-2. DAP Package 32-Pin TSSOP with PowerPAD Top View

表 5-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	VQFN NO.	HTSSOP NO.		
AGND	30	11	P	Signal ground
COMP1	29	10	I/O	Connect to an integral or integral-proportional compensation network to ensure stability for channel-1.
COMP2	12	25	I/O	Connect to an integral or integral-proportional compensation network to ensure stability for channel-2.
CSN1	27	8	I	High-side current sense amplifier input (–) for channel-1
CSN2	14	27	I	High-side current sense amplifier input (–) for channel-2
CSP1	26	7	I	High-side current sense amplifier input (+) for channel-1
CSP2	15	28	I	High-side current sense amplifier input (+) for channel-2
EN	2	15	I	Hardware enable. Pull this pin low to enter shutdown.
FB1/OV1	25	6	I/O	Connect using a resistor divider to VOUT1 to set OVP threshold (and VOUT in CV mode) for channel-1.
FB2/OV2	16	29	I/O	Connect using a resistor divider to VOUT2 to set OVP threshold (and VOUT in CV mode) for channel-2.
$\overline{\text{FLT1}}$	10	23	O	Open-drain fault output for channel-1 (or both channels if PIN-11 is programmed to be SYNC).
$\overline{\text{FLT2}}$/ SYNC	11	24	I/O	Dual function pin (programmable) either open-drain fault output for channel-2 or SYNC input
GATE1	22	3	I/O	Channel-1 gate driver output for external N-channel FET
GATE2	19	32	I/O	Channel-2 gate driver output for external N-channel FET
ISN1	24	5	I	Switch current sense input (-) for channel-1. Connect to the GND connection of the external switch-current sense resistor.
ISN2	17	30	I	Switch current sense input (-) for channel-2. Connect to the GND connection of the external switch-current sense resistor.
ISP1	23	4	I	Switch current sense input (+) for channel-1. Connect to external switch current sense resistor between N-channel FET and ground.
ISP2	18	31	I	Switch current sense input (+) for channel-2. Connect to external switch current sense resistor between N-channel FET and ground.
LH	9	22	I	Digital input, when set high, the device enters the limp home mode.
MISO	7	20	O	SPI slave data output
MOSI	8	21	I	SPI slave data input
PDRV1	28	9	I/O	Channel-1 P-channel gate driver. Connect to gate of external series P-channel FET switch.
PDRV2	13	26	I/O	Channel-2 P-channel gate driver. Connect to gate of external series P-channel FET switch.
PWM1	3	16	I	Connect to external PWM signal to enable PWM dimming for channel-1.
PWM2	4	17	I	Connect to external PWM signal to enable PWM dimming for channel-2.
PGND	20	1	P	Power ground
RT	32	13	I/O	Set internal clock frequency by connecting a resistor to ground
SCK	6	19	I	SPI clock input
SSN	5	18	I	SPI chip select input
VCC	21	2	P	7.5-V low-dropout regulator output
VDD	31	12	P	5-V LDO output
VIN	1	14	P	High-voltage input (65 V) to internal LDO

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage	VIN, EN, CSPx, CSNx	–0.3	65	V
	CSPx to CSNx (3)	–0.3	0.3	V
	ISPx, ISNx	–0.3	8.8	V
	SSN, SCK, MOSI, LH, RT, $\overline{FLTx}$	–0.3	5.5	V
	FBx/OVx	–0.3	5.5	V
	PWMx	–0.3	5.5	V
Output voltage(4)	VCC, GATEx	–0.3	8.8	V
	VDD	–0.3	5.5	V
	PDRV	V_{CSP} – 8.8	V_{CSP}	V
	MISO	–0.3	5.5	V
	COMPx	–0.3	4	V
Source current	I_{GATE}, (pulsed < 20 ns)		500	mA
	I_{PDRV}, (pulsed < 10 µs)		50	mA
Sink current	I_{GATE} (pulse < 20 ns)		500	mA
	I_{DDRV} (pulse < 10 µs)		50	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}			165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted
(3) Continuous sustaining voltage
(4) All output pins are not specified to have an external voltage applied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, all pins(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage	6.5	14	65	V
VIN, crank	Supply input, battery crank voltage	4.5			V
V_{CSP}, V_{CSN}	Current sense common mode voltage (1)	0		60	V
f_{SW}	Switching frequency	100		700	kHz
f_{SYNC}	Synchronization frequency range, vs f_{CLK} set by RT	0.8×f_{CLK}		1.2×f_{CLK}	Hz
F_{SS}	Spread-spectrum modulation frequency	0.1		10	kHz
T_A	Operating ambient temperature	–40		125	°C

(1) For current sense common mode voltage below 6.5 V, PFET dimming may not be applied

6.4 Thermal Information

THERMAL METRIC[1]		TPS92682-Q1			UNIT
		RHM (VQFN)	RHB (VQFN)	DAP (HTSSOP)	
		32 PINS	32 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.2	31.6	27.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.9	22.0	18.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.1	11.7	9.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.3	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.0	11.7	9.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	2.3	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

–40°C < T_J < 150°C, V_{IN}= 14V, VIADJDACx = 0xDF, C_{VCC} = 1 μF, C_{VDD} = 1 μF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 50kΩ, V_{PWM} = 5V, no load on GATE and PDRV, DIV=4 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
$I_{IN-SHDN}$	Input shutdown current	V_{EN} = 0 V, V_{CSP} = V_{CSN} = V_{PDRV} = 0 V		10		μA
		V_{EN} = 0 V, V_{CSP} = 14 V		10.5		
$I_{IN-STBY}$	Input standby current	Software EN1 and EN2 = 0, V_{PWM1} = V_{PWM2} = 0 V		2.3		mA
I_{IN-SW}	Supply switching current	VCC=7.5V, C_{GATEx} = 1nF, Both channels are switching		10		mA
VCC BIAS SUPPLY						
VCC_{UVLO}	Supply under-voltage protection	VCC rising threshold, V_{VIN} = 8 V		4.5	4.9	V
		VCC falling threshold, V_{VIN} = 8 V	3.7	4.1		V
		Hysteresis		411		mV
$VCC_{(REG)}$	VCC regulation voltage	No load	7	7.5	8	V
$I_{VCC(LIMIT)}$	VCC current limit	V_{VCC} = 0 V	40			mA
VCC_{DO}	VCC LDO dropout voltage	I_{VCC} = 30 mA, V_{VIN} = 4.5 V		300	475	mV
VDD BIAS SUPPLY						
$VDD_{(REG)}$	VDD regulation voltage	No load	4.85	5	5.25	V
$VDD_{(POR-RISE)}$	VDD rising threshold	V_{VIN} = 5 V			4.1	V
$VDD_{(POR-FALL)}$	VDD falling threshold	V_{VIN} = 5 V	2.58			V
VDD_{DO}	VDD LDO dropout voltage	I_{VDD} = 15 mA, V_{VIN} = 4.5 V			400	mV
$I_{VDD(LIMIT)}$	VDD current limit	V_{VDD} = 0 V	30	39	50	mA
ENABLE INPUT						
V_{EN}	EN voltage threshold		1.12	1.21	1.3	V
V_{EN-HYS}	EN pin hysteresis	Difference between rising and falling threshold		100		mV
I_{EN}	EN PIN input bias current	V_{EN} = 14 V		5		μA
OSCILLATOR						
f_{SW}	Switching frequency	RT = 200kΩ, DIV=4	85	100	115	kHz
		RT = 50kΩ, DIV=4	340	400	460	kHz
V_{RT}	RT PIN voltage			1		V
SPREAD SPECTRUM DAC						
$DAC_{DT-BITs}$	Internal DAC resolution			8		Bits
DAC_{DT-MAX}	DAC maximum voltage			1.156		V
DAC_{DT-MIN}	DAC minimum voltage			855		mV
GATE DRIVER						
R_{GH}	Driver pull-up resistance	I_{GATE} = – 10 mA		5.1	11.2	Ω
R_{GL}	Driver pull-down resistance	I_{GATE} = 10 mA		4.1	10.5	Ω
SWITCH CURRENT SENSE and ILIMIT						

6.5 Electrical Characteristics (continued)

–40°C < T_J < 150°C, V_{IN}= 14V, VIADJDACx = 0xDF, C_{VCC} = 1 µF, C_{VDD} = 1 µF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 50kΩ, V_{PWM} = 5V, no load on GATE and PDRV, DIV=4 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ILIM(THR)}$	ILIM threshold PWM = LOW	V_{PWMx}= 0 V, CHxILIM = XX	649	711	769	mV
	ILIM threshold PWM = HIGH	V_{PWMx}= 5 V, CHxILIM = 11	228	253	277	mV
		V_{PWMx}= 5 V, CHxILIM = 10	132	151	171	mV
		V_{PWMx}= 5 V, CHxILIM = 01	82	100.6	119	mV
		V_{PWMx}= 5 V, CHxILIM = 00	57	75.2	93	mV
$t_{IS(BLANK)}$	Leading edge blanking	CHxLEB = 0		75		ns
		CHxLEB = 1		150		ns
$t_{ILIMIT(DELAY)}$	ISx to GATEx delay			86		ns
PWM COMPARATOR						
D_{MAX}	Maximum duty cycle			90		%
$V_{LVx-Delta}$	Difference between CH1 and CH2 PWM comparator offset		–17.5		17.5	mV
I_{LVx}	IS level shift bias current	No slope compensation added		40		µA
$T_{PWM-Delta}$	Turn-off propagation delay from input of PWM comp. to gate output			100		ns
$T_{PWMDEL-Delta}$	Difference between CH1 and CH2 PWM comp. propagation delay		–30		30	ns
CURRENT SENSE AMPLIFIER (CSP, CSN)						
$V_{(CSP-CSN)x}$	Current Sense REG Voltage	$V_{CSP(CM)}$ = 14 V, IADJDAC = 0×FF	165.8	172.7	179.6	mV
		$V_{CSP(CM)}$ = 14V, IADJDAC = 0x95	96.5	100.8	104.5	mV
		$V_{CSP(CM)}$ = 14V, IADJDAC = 0×0F		10.3		mV
$CS_{(BW)}$	Current sense unity gain bandwidth			500		kHz
G_{CS}	Current Sense Gain = $V_{IADJ}/V_{(CSP-CSN)}$	V_{CS} = 150 mV, V_{CSP} = 60 V		14		V/V
$K_{(OCP)}$	Ratio of over-current detection threshold to V_{IADJ}	$K_{(OCP)} = V_{(OCP-THR)}/V_{IADJ}$	1.41	1.53	1.66	V/V
$K_{(UC)}$	Ratio of under-current detection threshold to V_{IADJ}	$K_{(UC)} = V_{(UC-THR)}/V_{IADJ}$		0.5		V/V
$I_{CSP(BIAS)}$	CSP bias current	$V_{CSP} = V_{CSN} = V_{PDRV}$ = 14 V		59		µA
$I_{CSN(BIAS)}$	CSN bias current	$V_{CSP} = V_{CSN} = V_{PDRV}$ = 14 V		59		µA
SSDAC						
$DAC_{SS-BITs}$	Internal DAC resolution			8		Bits
DAC_{SS-FS}	DAC full scale voltage			2.8		V
CALDAC						
$DAC_{CAL-BITs}$	Switch current sense calibration DAC			3		Bits
$DAC_{CAL-RES}$	Offset-per-Bit applied to the switch current sense			2.5		mV
FAULT FLAG ($\overline{FLT}$x)						
$R_{(\overline{FLT})}$	Open-drain pull down resistance			36		Ω
VIADJDAC						
$DAC_{ADJ-BITs}$	Internal DAC resolution			8		Bits
DAC_{ADJ-FS}	DAC full scale voltage		2.32	2.4	2.48	V
ERROR AMPLIFIER (COMP)						

6.5 Electrical Characteristics (continued)

–40°C < T_J < 150°C, V_{IN}= 14V, VIADJDACx = 0xDF, C_{VCC} = 1 µF, C_{VDD} = 1 µF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 50kΩ, V_{PWM} = 5V, no load on GATE and PDRV, DIV=4 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
g_M	Transconductance	HG = 0		122		µA/V
		HG = 1		914		
$I_{COMP(SRC)}$	COMP source current capacity	IADJx = 0×95, $V_{(CSP-CSN)}$ = 0 V, HG = 0		129		µA
		IADJx = 0×95, $V_{(CSP-CSN)}$ = 0 V, HG = 1		777		
$I_{COMP(SINK)}$	COMP sink current capacity	IADJx = 0×00, $V_{(CSP-CSN)}$ = 0.1 V, HG = 0		129		µA
		IADJx = 0×00, $V_{(CSP-CSN)}$ = 0.1 V, HG = 1		783		
$EA_{(BW)}$	Error amplifier bandwidth	Gain = –3 dB, HG = 0		5		MHz
		Gain = –3 dB, HG = 1		1		
$V_{COMP(RST)}$	V_{COMP} reset voltage			100		mV
$R_{COMP(DCH)}$	COMPx discharge FET R_{DSON}			248		Ω
$R_{COMP(DIFF)}$	COMP1 to COMP2 short path resistance			300		Ω
SLOPEDAC						
DAC_{SLP-FS}	DAC full scale voltage			0.36		V
VFB						
VFB_{ERR}	Regulation voltage error		–4		4	%
VFB_{BIAS}	V_{FB} pin pull up bias current			200		nA
OVDAC						
$V_{OV(THR)}$	OV limit threshold, 0%	CHxOVDAC = 000	1.2	1.237	1.27	V
	OV limit threshold, 2.5%	CHxOVDAC = 001		1.268		V
	OV limit threshold, 5%	CHxOVDAC = 010		1.299		V
	OV limit threshold, 7.5%	CHxOVDAC = 011		1.329		V
	OV limit threshold, 10%	CHxOVDAC = 100		1.36		V
	OV limit threshold, 12.5%	CHxOVDAC = 101		1.391		V
	OV limit threshold, 15%	CHxOVDAC = 110		1.422		V
	OV limit threshold, 20%	CHxOVDAC = 111		1.483		V
I_{OV-HYS}	OV hysteresis current		11.5	20.5	28.5	µA
UV (Output Under Voltage)						
$V_{UV(THR)}$	Under voltage protection threshold		40	53.2	67	mV
$t_{UV(BLANK)}$	Under voltage blanking period			5		µs
DIGITAL INPUTs (PWMx, SYNC, LH, SSN, SCK, MOSI)						
I_{BIAS}	Input bias current	Except PWM inputs			1	µA
$VT_{INPUT-FALL}$	Falling threshold		0.7			V
$VT_{INPUT-RISE}$	Rising threshold				1.85	V
PWM INPUT (PWM)						
$R_{PWM(PD)}$	PWM pull-down resistance			10		MΩ
$t_{DLY(RISE)}$	PWM rising to PDRV delay	C_{PDRV} = 1 nF		235		ns
$t_{DLY(FALL)}$	PWM falling to PDRV delay	C_{PDRV} = 1 nF		222		ns
PFET GATE DRIVE						
$V_{PDRV(OFF)}$	PDRV off-state voltage	V_{CSP} = 14 V		14		V
$V_{PDRV(ON)}$	PDRV on-state voltage	V_{CSP} = 14 V		7.34		V

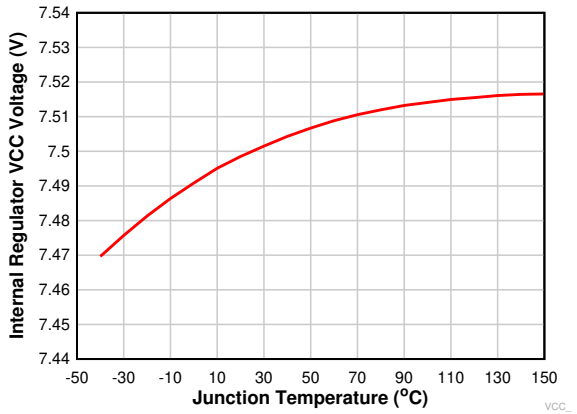
6.5 Electrical Characteristics (continued)

–40°C < T_J < 150°C, V_{IN}= 14V, VIADJDACx = 0xDF, C_{VCC} = 1 µF, C_{VDD} = 1 µF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 50kΩ, V_{PWM} = 5V, no load on GATE and PDRV, DIV=4 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PDRV(SINK)}$	PDRV sink current	V_{CSP} – V_{PDRV} = 5 V, pulsed < 100 µs		29		mA
R_{PDRV}	PDRV pull up resistance	V_{CSP} – V_{PDRV} = 0 V, pulsed < 100 µs		83.5		Ω
SPI INTERFACE						
$V_{OL-MISO}$	Output low voltage threshold	$I_{(MISO)}$ = 10 mA		0.25		V
$R_{DS-MISO}$				25		Ω
C_{MISO}				10		pF
t_{SS-SU}	SSN setup time	Falling edge of SSN to 1st SCK rising edge	500			ns
t_{SS-H}	SSN hold time	Falling edge of 16th SCK to SSN rising edge	250			ns
t_{SS-HI}	SSN high time	Time SSN must remain high between transactions	1			µs
t_{SCK}	SCK period	Clock period	500			ns
D_{SCK}	SCK duty cycle	Clock duty cycle	40		60	%
$t_{MOSI-SU}$	MOSI setup time	MOSI valid to rising edge SCK	125			ns
t_{MOSI-H}	MOSI hold time	MOSI valid after rising edge SCK	140			ns
$t_{MISO-HIZ}$	MISO tristate time	Time to tristate MISO after SSN rising edge	110		320	ns
$t_{MISO-HL}$	MISO valid high-to-low	Time to place valid "0" on MISO after falling SCK edge.			320	ns
$t_{MISO-LH}$	MISO valid low-to-high	Time to tri-state MISO after falling SCK edge. t_{RC} is the time added by the application total capacitance and resistance.			320+t_{RC}	ns
T_{ZO-HL}	MISO drive time high-to-low	SSN Falling Edge to MISO Falling			320	ns

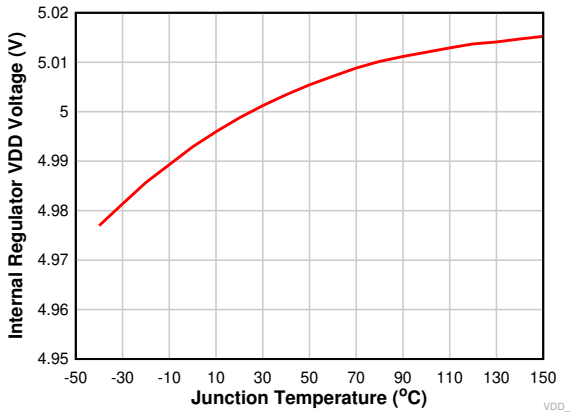
6.6 Typical Characteristics

T_A = 25°C free air, VIN = 14 V, DIV = 2 (CHxDIV = 0x00) unless otherwise specified



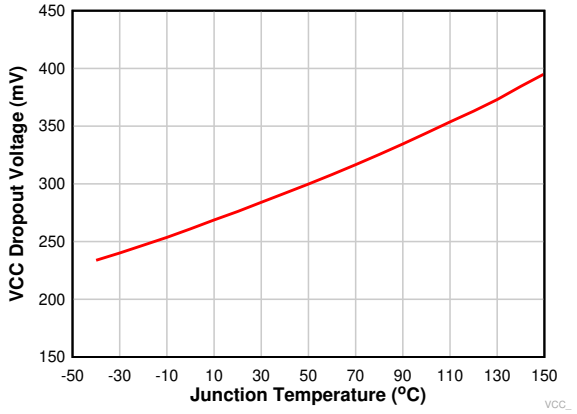
I_{VCC} = 20 mA

图 6-1. Regulated VCC Voltage vs Junction Temperature



I_{VDD} = 20 mA

图 6-2. Regulated VDD Voltage vs Junction Temperature



V_{IN} = 4.5 V, I_{VCC} = 30 mA

图 6-3. VCC Dropout Voltage vs Junction Temperature

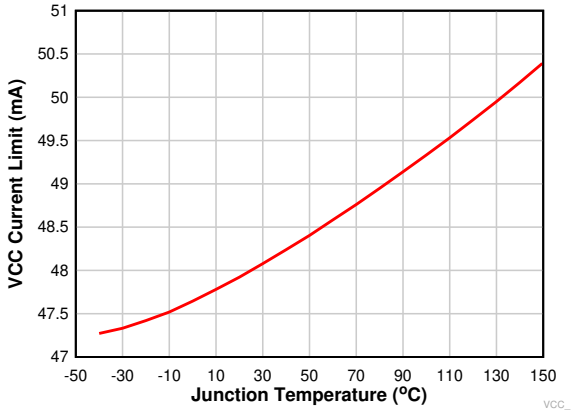


图 6-4. VCC Current Limit vs Junction Temperature

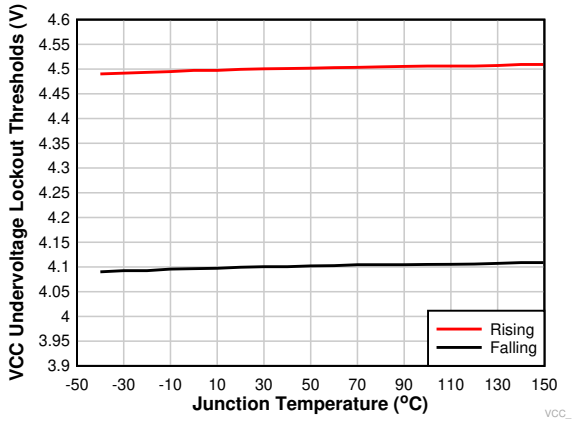


图 6-5. VCC UVLO Threshold vs Junction Temperature

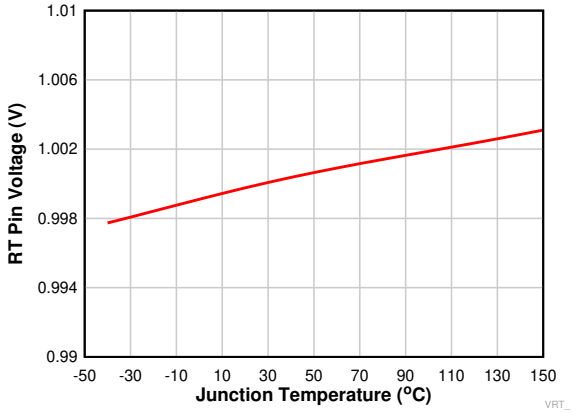
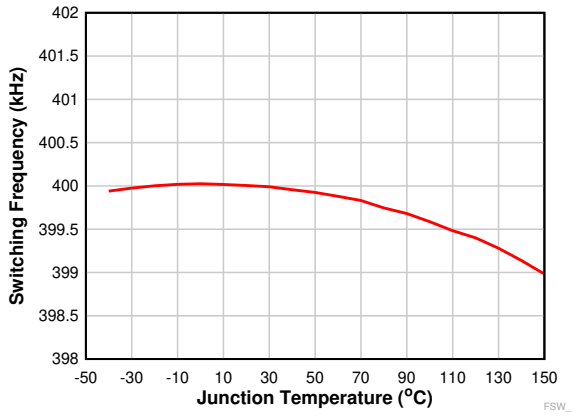


图 6-6. RT Pin Voltage vs Junction Temperature

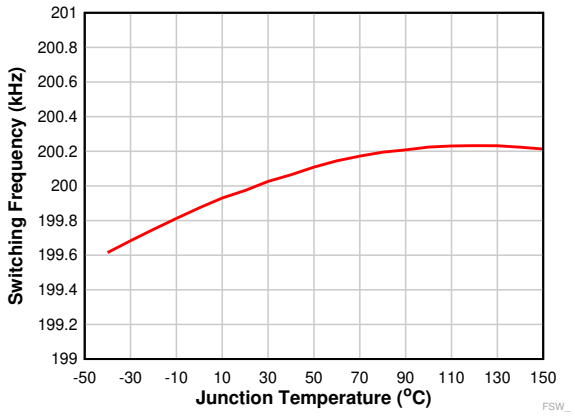
6.6 Typical Characteristics (continued)

T_A = 25°C free air, VIN = 14 V, DIV = 2 (CHxDIV = 0x00) unless otherwise specified



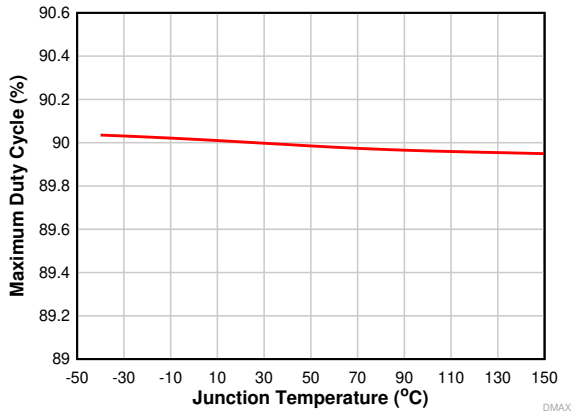
RT = 50 kΩ, CHxDIV = 01

图 6-7. Switching Frequency vs Junction Temperature



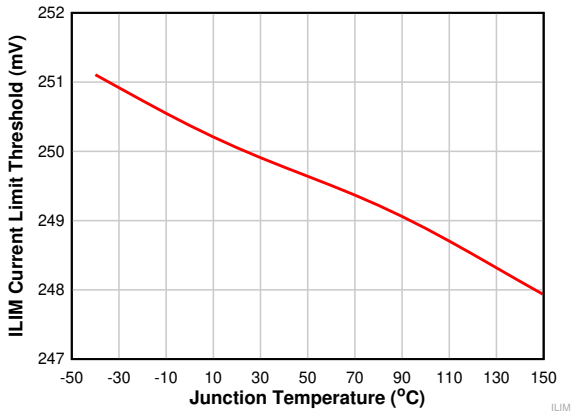
RT = 100 kΩ, CHxDIV = 01

图 6-8. Switching Frequency vs Junction Temperature



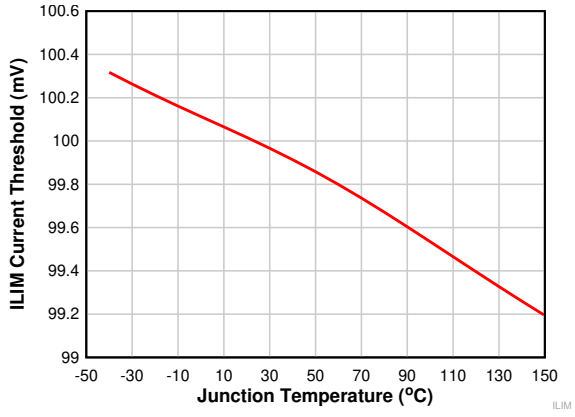
RT = 50 kΩ, CHxDIV = 01

图 6-9. Maximum Duty Cycle vs Junction Temperature



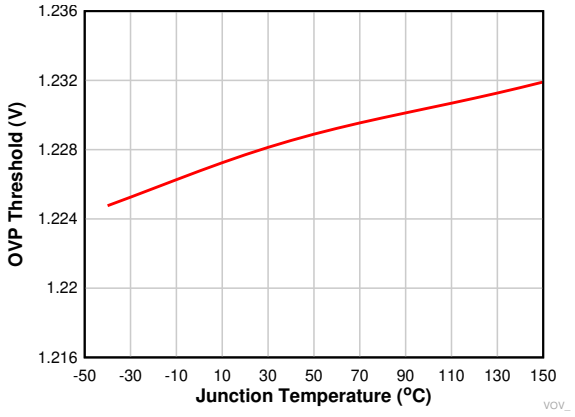
CHxILIM = 11

图 6-10. ISP Current Limit Threshold vs Junction Temperature



CHxILIM = 01

图 6-11. ISP Current Limit Threshold vs Junction Temperature

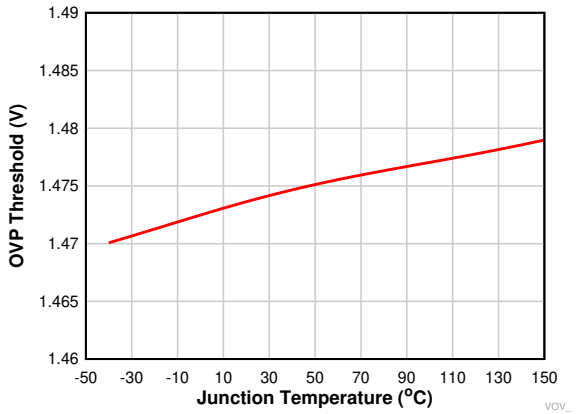


CHxOV = 000

图 6-12. Over Voltage Protection Threshold vs Junction Temperature

6.6 Typical Characteristics (continued)

T_A = 25°C free air, VIN = 14 V, DIV = 2 (CHxDIV = 0x00) unless otherwise specified



CHxOV = 111

图 6-13. Over Voltage Protection Threshold vs Junction Temperature

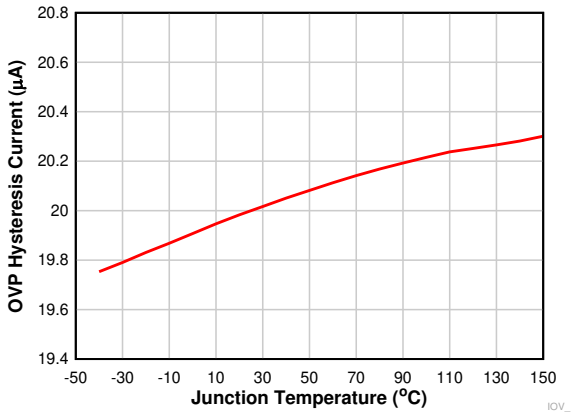
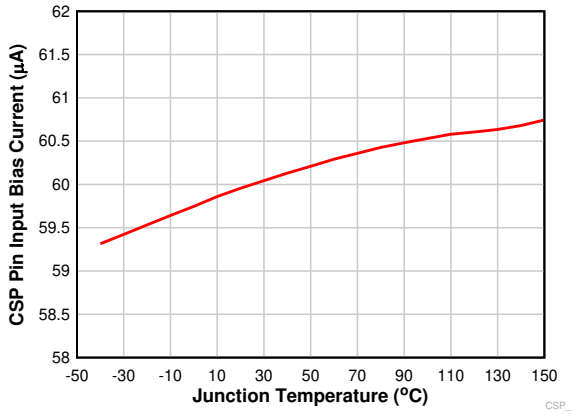
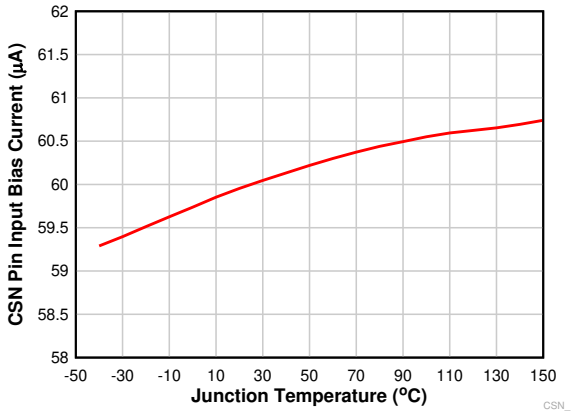


图 6-14. OVP Hysteresis Current vs Junction Temperature



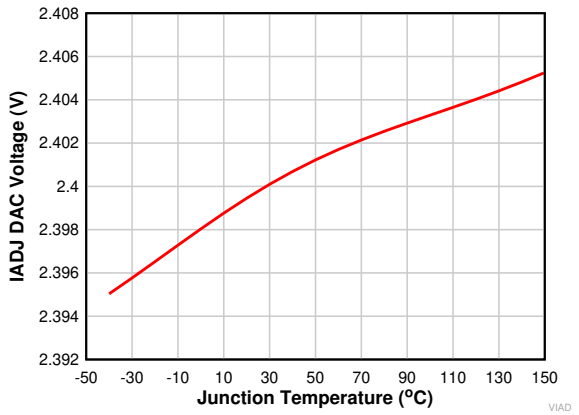
V_{CSP} = 14 V

图 6-15. CSP Pin Input Bias Current vs Junction Temperature



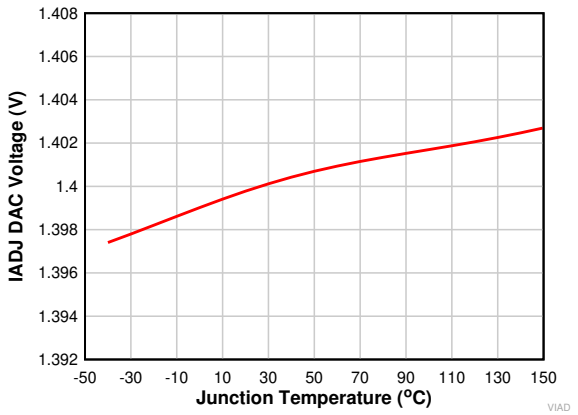
V_{CSN} = 14 V

图 6-16. CSN Pin Input Bias Current vs Junction Temperature



CHxIADJ = FF (hex)

图 6-17. VIADJ Voltage vs Junction Temperature

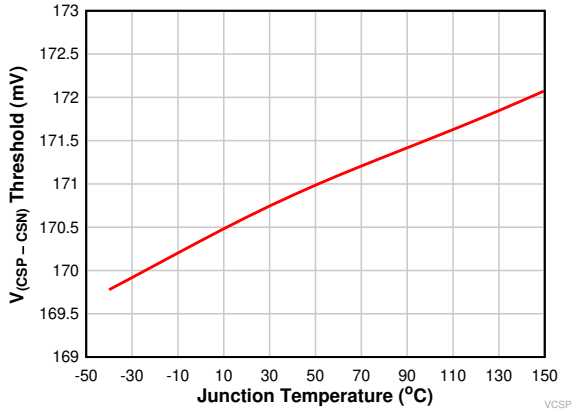


CHxIADJ = 95 (hex)

图 6-18. VIADJ Voltage vs Junction Temperature

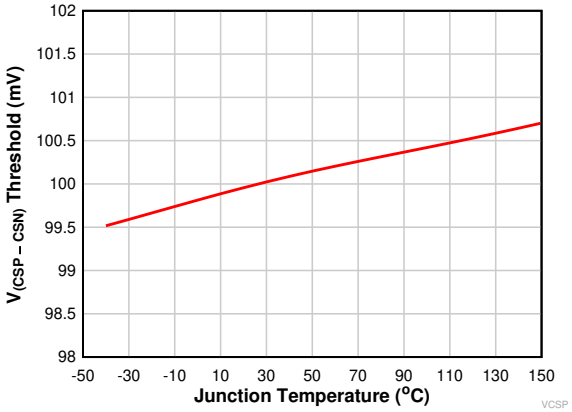
6.6 Typical Characteristics (continued)

T_A = 25°C free air, VIN = 14 V, DIV = 2 (CHxDIV = 0x00) unless otherwise specified



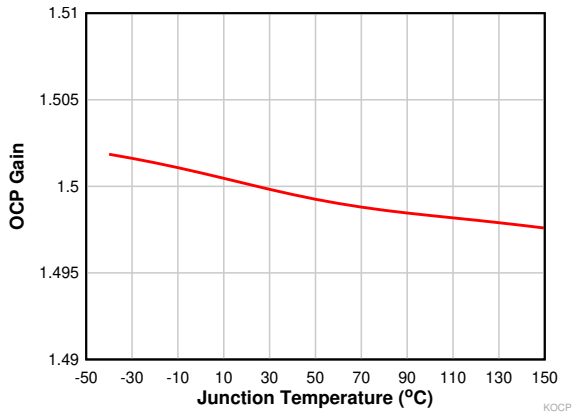
CHxIADJ = FF (hex)

图 6-19. $V_{(CSP - VCSN)}$ Voltage vs Junction Temperature



CHxIADJ = 95 (hex)

图 6-20. $V_{(CSP - VCSN)}$ Voltage vs Junction Temperature



CHxIADJ = 95 (hex)

图 6-21. Over Current Protection Gain vs Junction Temperature

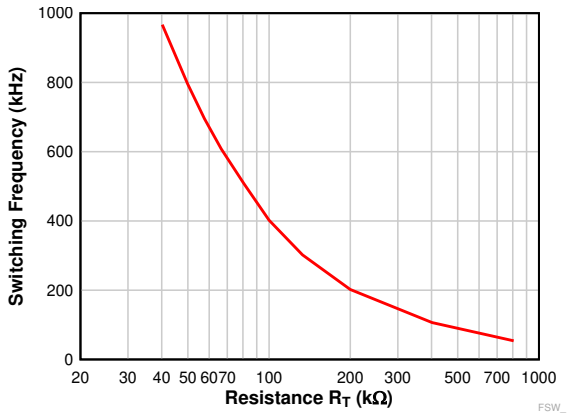


图 6-22. Channel Switching Frequency F_{SW} vs R_T Resistance

7 Detailed Description

7.1 Overview

The TPS92682-Q1 device is an automotive-grade two-channel controller with Serial Peripheral Interface (SPI) interface, ideally suited for exterior lighting applications. The device is optimized to achieve high-performance solutions and features all of the functions necessary to implement LED drivers based on step-up or step-down power converter topologies with a small form-factor at a lower cost.

The two channels of the TPS92682-Q1 device can be configured independently as CC (constant current) or CV (constant voltage) mode. The device implements fixed-frequency peak current mode control to achieve regulation and fast dynamic response. Each channel can be configured as boost, boost-to-battery, SEPIC, or other converter topologies.

In CC mode, the integrated low offset and rail-to-rail current sense amplifier provide the flexibility required to power a single string consisting of 1 to 20 series connected LEDs while maintaining 4% current accuracy over the operating temperature range. The LED current regulation threshold is set by the analog adjust input CHxIADJ register over 28:1 dimming range. The TPS92682-Q1 incorporates an internal 10-bit counter for the PWM dimming function for each channel. The PWM width and frequency are programmable through the SPI registers. Alternatively, the device can also be configured to implement direct PWM dimming based on the duty cycle of the external PWM signal connected to PWM1 or PWM2 pins for channel-1 or channel-2, respectively. The internal PWM signals control the GATEx and PDRVx outputs, which control the external N-channel switching FETs and P-channel dimming FETs connected in series with LED strings.

The TPS92682-Q1 can be configured in CV mode. In this mode, the device regulates the voltage connected to the FBx/OVx pins to an internal programmable reference voltage, set by the CHxIADJ register. In CV mode, the TPS92682-Q1 can be used as the first stage of a two-stage LED driver in an ECU (electronic control unit) of an exterior lighting application. The device can also be configured to operate in two-phase mode, where the switching frequencies of the two channels are phase-shifted by 180° and the channel-1 compensation loop, including COMP1 and the FB1/OV1, is shared between the two channels.

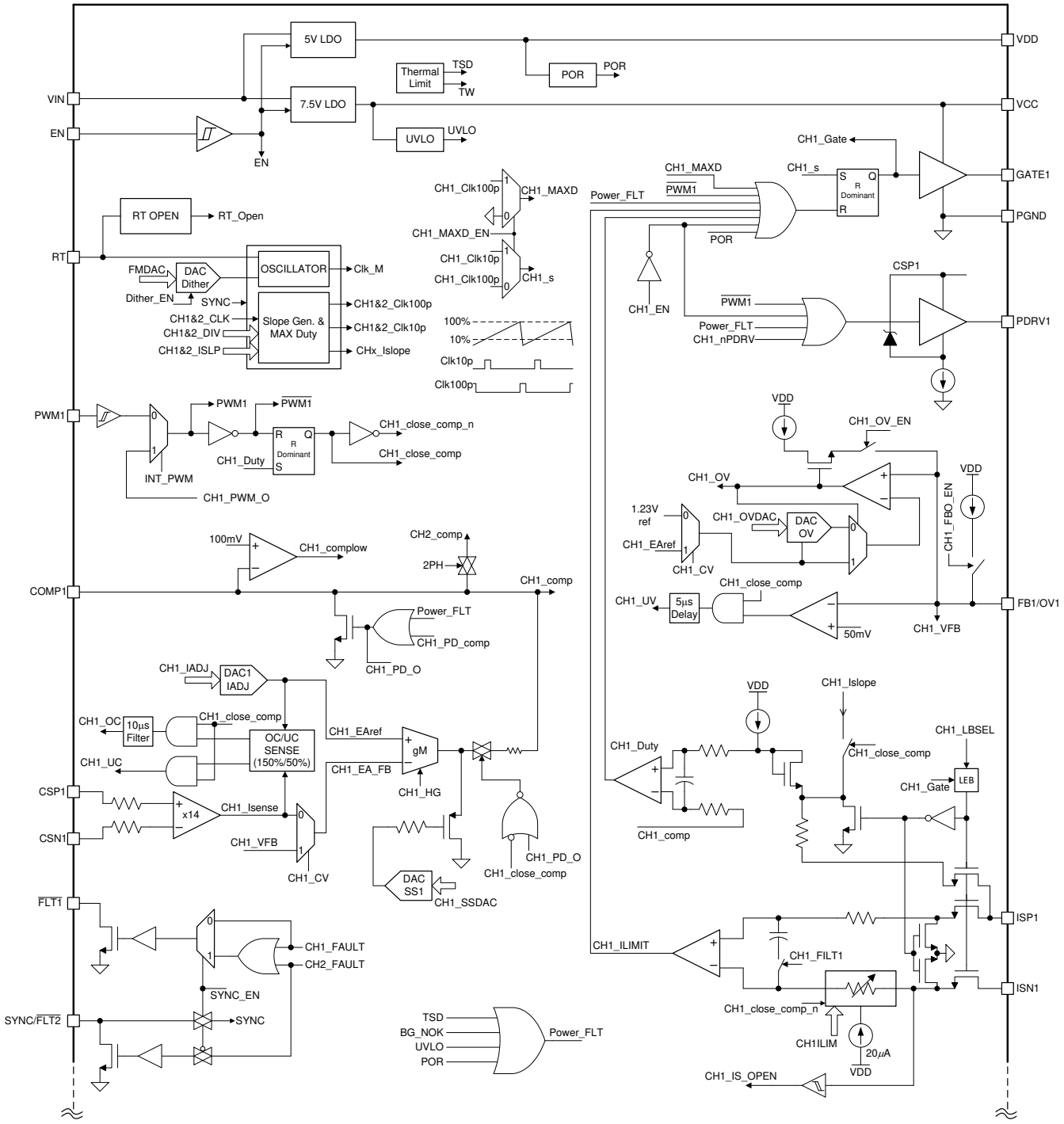
The TPS92682-Q1 incorporates an enhanced programmable fault feature. A selected number of faults, including ILIMIT (cycle-by-cycle current limit), OV (output Overvoltage), UV (output Undervoltage), and OC (LED Overcurrent), can be programmed to be latched faults, or automatically re-start the channel when the fault is cleared and after a programmed timer is expired. In addition, the TPS92682-Q1 includes open-pin faults for the FBx, ISNx, and RT pins. Other fault and diagnostic features include Thermal Shutdown (TSD), Thermal Warning (TW), LED Undercurrent (UC), and POR. Each channel includes an active-low fault pin ($\overline{\text{FLT}}$) that is pulled low when a fault occurs. For each fault, there is an associated fault read-bit in the register map that can be read through SPI communication interface. For a complete list of the fault and diagnostic features, refer to the *Faults and Diagnostics* section.

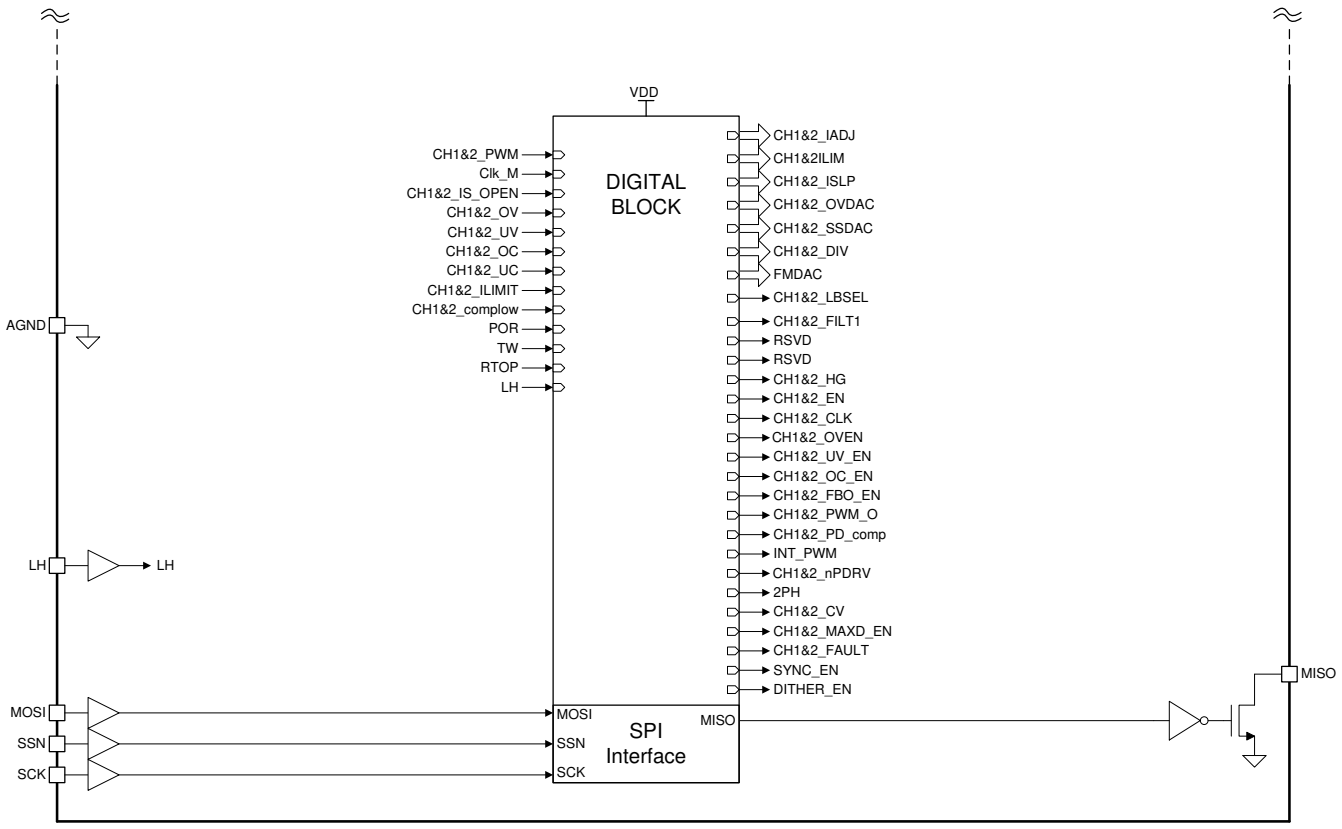
The TPS92682-Q1 includes a limp home (LH) function that is initiated when the LH pin is set high. In LH mode, the operation of the device is set by the LH registers. The LH registers are programmed upon initialization of the device. To exit the LH mode, the LH pin must be set low and the LH bit in the CFG1 register must be written to “0”.

The TPS92682-Q1 device has numerous enhanced programmable features that can be accessed through the 4-wire SPI bus. The SPI bus consists of four signals: SSN, SCK, MOSI, and MISO. The SSN, SCK, and MOSI pins are TTL inputs into the device.

7.2 Functional Block Diagram

The block diagram below shows the associated blocks for channel-1. Channel-2 has a similar configuration.




VDD
DIGITAL BLOCK
CH1&2_PWM
Clk_M
CH1&2_IS_OPEN
CH1&2_OV
CH1&2_UV
CH1&2_OC
CH1&2_UC
CH1&2_ILIMIT
CH1&2_complow
POR
TW
RTOP
LH
CH1&2_IADJ
CH1&2ILIM
CH1&2_ISLP
CH1&2_OVDAC
CH1&2_SSDAC
CH1&2_DIV
FMDAC
CH1&2_LBSEL
CH1&2_FILT1
RSVD
RSVD
CH1&2_HG
CH1&2_EN
CH1&2_CLK
CH1&2_OVEN
CH1&2_UV_EN
CH1&2_OC_EN
CH1&2_FBO_EN
CH1&2_PWM_O
CH1&2_PD_comp
INT_PWM
CH1&2_nPDRV
2PH
CH1&2_CV
CH1&2_MAXD_EN
CH1&2_FAULT
SYNC_EN
DITHER_EN
AGND
LH
LH
MOSI
SSN
SCK
MOSI
SSN
SCK
SPI Interface
MISO
MISO

7.3 Feature Description

The TPS92682-Q1 device implements a fixed frequency Peak Current Mode (PCM) control. In PCM, the switching cycle starts with a rising edge of the clock. The switching cycle ends when the sensed switch current, V_{iSW} (added with V_{SLOPE}), exceeds the compensator voltage, V_{COMP}. As shown in 图 7-1 and 图 7-2, a transconductance g_M error amplifier generates an error signal by comparing the feedback signal and the reference voltage, V_{REF}. The resulting error current generates the compensator voltage V_{COMP}, through a compensator impedance, connected to the COMPx pin.

For stability at high duty cycle and better noise immunity, a compensation ramp V_{SLOPE} is added to the sensed switch current V_{iSW}.

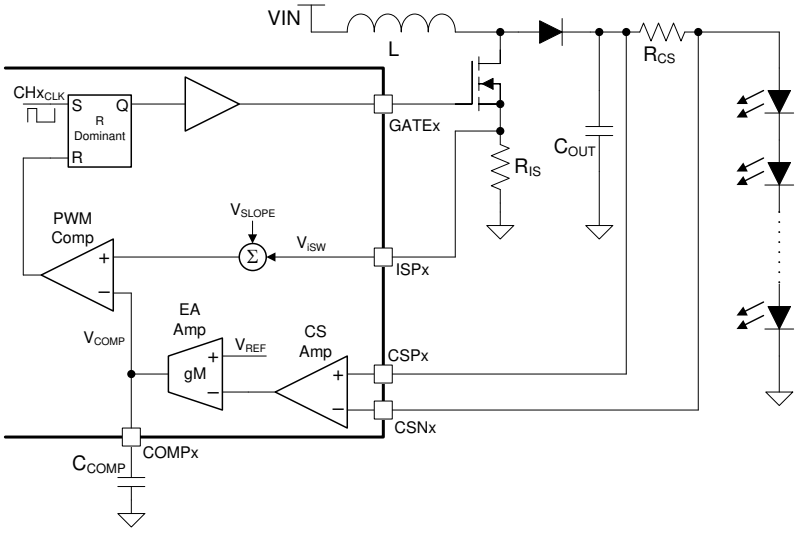


图 7-1. PCM Control in CC Mode

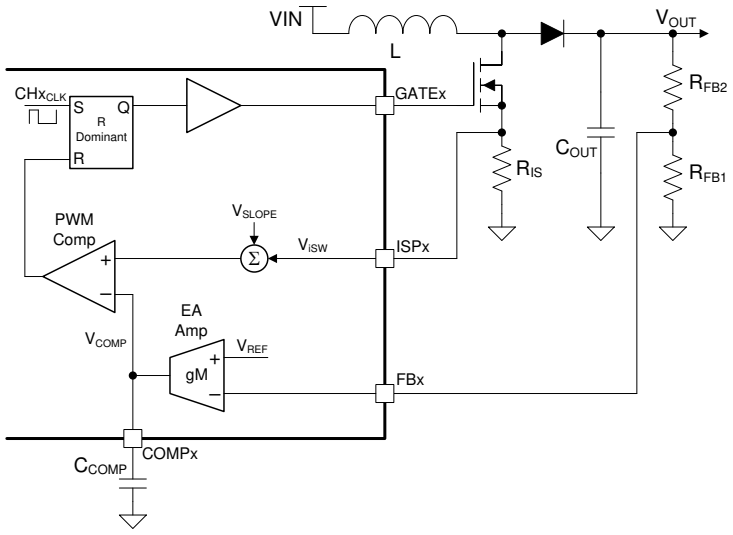


图 7-2. PCM Control in CV Mode

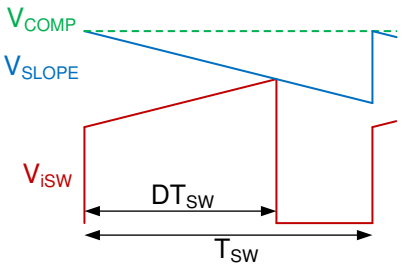


图 7-3. PCM Control and Ramp Compensation

7.3.1 Device Enable

The TPS92682-Q1 can be enabled or disabled by the EN pin or the software enable bits. When EN pin is pulled low, the device enters shutdown state, where the quiescent current of the device is decreased to $I_{IN-SHDN}$. In shutdown state, the internal regulators are turned off and the registers are reset. When the voltage on the enable pin is increased above the voltage threshold of V_{EN}, the two channels can be enabled. In addition to the EN pin, there are two enable bits for the two channels of the TPS92682-Q1 as shown in 表 7-2. In order for each channel to be turned on, the associated CHxEN bit must be set to "1" in *EN Register*.

In addition to the EN pin and the CHxEN bits, the PWMx signals (hardware or software) must be set high and the associated CHxIADJ must be set to a value greater than eight (refer to the *CH1IADJ Register*) in order for the associated channel to be turned on.

7.3.2 Internal Regulator and Undervoltage Lockout (UVLO)

The device incorporates 65-V input voltage rated linear regulators to generate the 7.5-V (typical) VCC bias supply, the 5-V (typical) VDD supply, and other internal reference voltages. The device monitors the VCC output to implement UVLO protection. Operation is enabled when VCC exceeds the 4.5-V (typ) threshold and is disabled when VCC drops below the 4.1-V (typical) threshold. The UVLO comparator provides a hysteresis to avoid chatter during transitions. The UVLO thresholds are internally fixed and cannot be adjusted. An internal current limit circuit is implemented to protect the device during VCC pin short-circuit conditions. The VCC supply powers the internal circuitry and the N-channel gate driver outputs, GATEx. Place a bypass capacitor in the range of 2.2 μF to 4.7 μF across the VCC output and GND to ensure proper operation. The regulator operates in dropout when input voltage VIN falls below 7.5 V. The VCC is a regulated output of the internal regulator and is not recommended to be driven with an external power supply.

The internal VDD regulator is used to generate supply voltage for various internal analog and digital circuits. The supply current is internally limited to protect the device from output overload and short-circuit conditions. Place a bypass capacitor in the range of 2.2 μF to 4.7 μF across the VDD output to GND to ensure proper operation. The POR circuit of the device is placed at the output of the VDD regulator. The POR rise and fall thresholds are provided in the *Electrical Characteristics*.

7.3.3 Oscillator

The internal clock frequency of the TPS92682-Q1 device is programmable by a single external resistor, connected between the RT pin and the GND. The relationship between the resistor R_T and the internal main clock (CLK_M) frequency is shown in 方程式 1 and Channel Switching Frequency F_{SW} vs R_T Resistance.

$$f_{CLKM} = \frac{10^{12}}{12.5 \times R_T} \tag{1}$$

The relationship between the channel clock, CHx_{CLK} (or the channel switching frequency f_{SW}), and f_{CLKM} is shown in the *SWDIV Register* section. TI recommends a switching frequency setting between 100 kHz to 700 kHz for best efficiency and for optimal performance over input and output voltage operating range. Operation at higher switching frequencies requires careful selection of N-channel MOSFET characteristics as well as detailed analysis of switching losses.

To use the synchronization functionality of the TPS92682-Q1, the SYNCEN bit shown in 表 7-3 must be set to "1", and a square wave signal with the desired f_{CLKM} frequency must be applied to the SYNC pin.

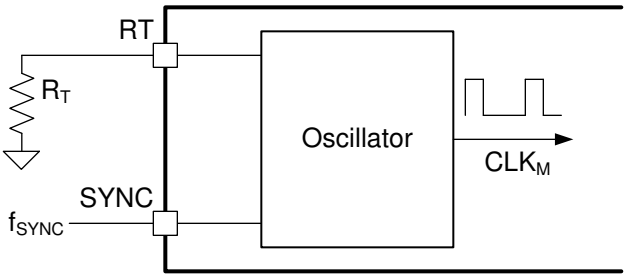


图 7-4. TPS92682 SYNC Function

7.3.4 Spread Spectrum Function

The main clock of the TPS92682-Q1, CLK_M, is generated using an internal ramp generator as shown in 图 7-5. The internal ramp, $RAMP_{CLKM}$, is compared with a reference voltage of $VOSC_{REF}$ to reset the ramp at the end of the clock period, T_{CLKM}. When the reference voltage $VOSC_{REF}$ is constant (1 V), the main clock frequency is fixed. The frequency modulation of the main clock is achieved using an internal 8-bit digital counter DAC, and by modulating the reference voltage as shown in 图 7-6. Both modulation frequency, F_M, and the modulation magnitude, ΔF_M, are programmable in the *FM Register*.

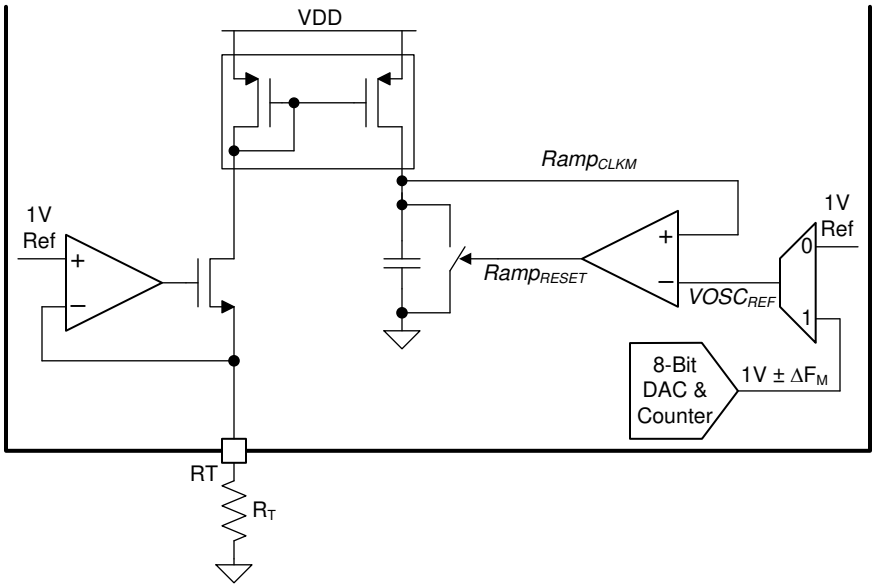


图 7-5. Internal Ramp for CLK_M Generation

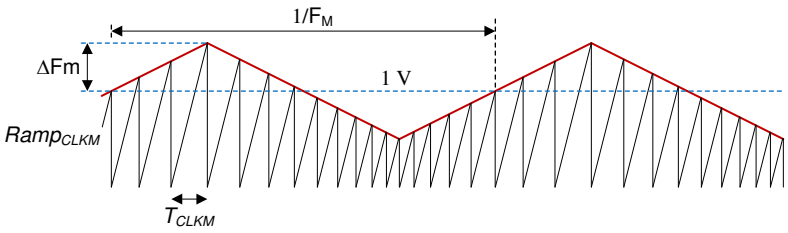


图 7-6. Internal Ramp Waveform

To achieve maximum attenuation in average-EMI scan, set a modulation frequency of F_M ranging from 100 Hz to 1.2 kHz. A low modulating frequency has a small impact on the quasi-peak EMI scan. Set the modulation frequency to 10 KHz or higher to achieve attenuation for quasi-peak EMI measurements. A modulation

frequency higher than the receiver resolution bandwidth (RBW) of 9 kHz impacts only the quasi-peak EMI scan and has little impact on the average EMI measurement. The TPS92682-Q1 device simplifies EMI compliance by providing the means to tune the modulation frequency, F_M, and modulation magnitude, ΔF_M, based on the measured EMI signature.

Equation 2 shows the relation between the channel switching frequency, f_{SW}, and the desired modulation frequency F_M.

$$F_M = \frac{DIV \times f_{SW}}{FM_{FREQ}} \quad (2)$$

In Equation 2, DIV is the division factor between CLK_M and the CHx_{CLK} provided in *SWDIV Register*, and FM_{FREQ} is the division factor given in the *FM Register*.

The output of the FM 8-bit digital counter always resets and starts from 1 V when a register write is performed to *FM Register*.

7.3.5 Gate Driver

The TPS92682-Q1 contains an N-channel gate driver that switches the output GATEx between V_{CC} and GND. A peak source and sink current of 500 mA allows controlled slew-rate of the MOSFET gate and drain voltages, limiting the conducted and radiated EMI generated by switching.

The gate driver supply current, $I_{CC(GATE)}$, depends on the total gate drive charge (QG) of the MOSFET and the operating frequency of the converter, f_{SW}, $I_{CC(GATE)}$ = QG × f_{SW}. Select a MOSFET with a low gate charge specification to limit the junction temperature rise and switch transition losses.

It is important to consider a MOSFET threshold voltage when operating in the dropout region (input voltage VIN is below the VCC regulation level). TI recommends a logic level device with a threshold voltage below 5 V when the device is required to operate at an input voltage less than 7 V.

7.3.6 Rail-to-Rail Current Sense Amplifier

The internal rail-to-rail current sense amplifier measures the average LED current based on the differential voltage drop between the CSPx and CSNx inputs over a common mode range of 0 V to 65 V. The differential voltage, $V_{(CSPx-CSNx)}$, is amplified by a voltage-gain factor of 14 and is connected to the negative input of the transconductance error amplifier. Accurate LED current feedback is achieved by limiting the cumulative input offset voltage (represented by the sum of the voltage-gain error, the intrinsic current sense offset voltage, and the transconductance error amplifier offset voltage) over the recommended common-mode voltage and temperature range.

An optional common-mode (C_{FCM}) or differential mode (C_{FDM}) low-pass filter implementation, as shown in 图 7-7, can be used to filter the effects of large output current ripple, and switching current spikes caused by diode reverse recovery. TI recommends a filter resistance in the range of 10 Ω to 100 Ω to limit the additional offset caused by amplifier bias current mismatch to achieve the best accuracy and line regulation.

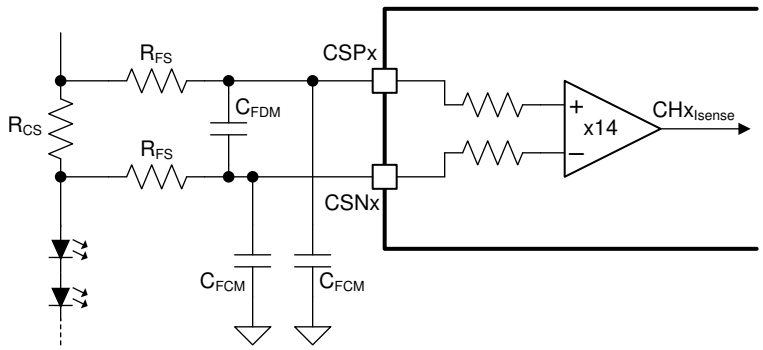


图 7-7. Current Sense Amplifier

7.3.7 Transconductance Error Amplifier

As shown in 图 7-8, the internal transconductance error amplifier generates an error signal proportional to the difference between the internal programmable 8-bit CHxIADJ-DAC (*CH1IADJ Register*) and the feedback signal. The feedback signal is the sensed current CHx_{Isense} in CC mode, or the sense output voltage, CHx_{VFB}, in CV mode. The gain g_M of the error amplifier is programmable through the CHx_HG bit in the *CFG1 Register*. The gain values for CHx_HG = 0 or 1 are provided in the *Electrical Characteristics*. Based on the value of CHx_CV bit in 表 7-4, either CHx_{Isense} or CHx_{VFB} is connected to the input of the error amplifier. Therefore, the TPS92682-Q1 device either operates in CV or CC mode.

The output of the error amplifier is connected to an external compensation network to achieve closed-loop LED current (CC), or output voltage (CV) regulation. In most LED driver applications, a simple integral compensation circuit consisting of a capacitor connected from COMPx output to GND provides a stable response over a wide range of operating conditions. TI recommends a capacitor value between 10 nF and 100 nF as a good starting point. To achieve higher closed-loop bandwidth, a proportional-integral compensator, consisting of a series resistor and a capacitor network connected across the COMPx output and GND, is required. *Application and Implementation* includes a summarized detailed design procedure.

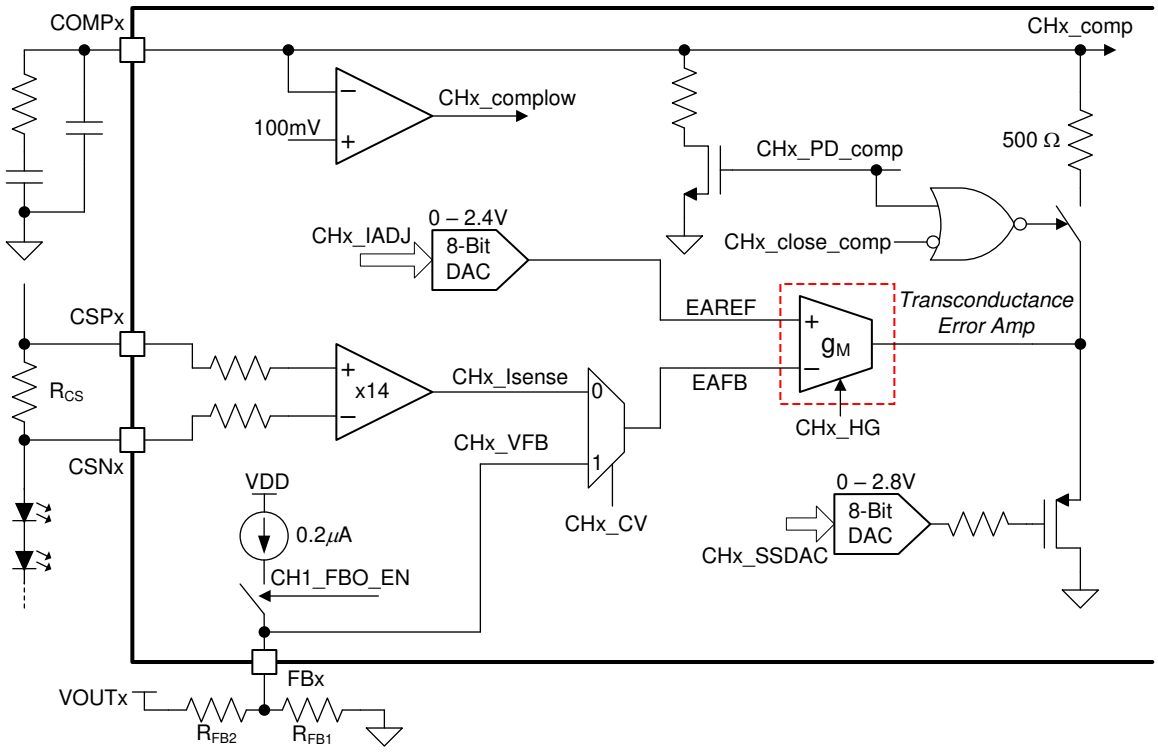


图 7-8. Feedback Connection to the Error Amplifier

7.3.8 Switch Current Sense

图 7-9 shows the simplified block diagram of the switch current sense circuitry. The ISPx input pin monitors the main MOSFET current to implement peak current mode control. The GATEx output duty cycle is derived by comparing the peak switch current, measured by the R_{IS} resistor, to the internal CHx_COMP voltage threshold. An internal slope signal, CHx_ISLOPE, is added to the measured sense voltage to prevent sub-harmonic oscillations for duty cycles greater than 50%.

An internal leading-edge blanking (LEB) is applied to the switch current sense at the beginning of each switching cycle by shunting the ISPx input to the ISNx (GND connection of the R_{IS}) for the duration of the LEB time. The LEB circuit prevents unwanted duty cycle termination due to MOSFET switching-current spike at the beginning of the new switching cycle. The LEB time can be set to 150 ns or 75 ns (typical) using the CHxLEB bit set in 表

7-5. For additional noise suppression, connect an external low-pass RC filter with resistor values ranging from 100 Ω to 500 Ω and a 1000-pF capacitor across R_{IS}.

Cycle-by-cycle current limit is accomplished by a separate internal comparator. The current limit threshold is set based on the status of internal PWM signal and the CHxILIM setting. The current limit threshold is set to a value programmed in the CHxILIM in 表 7-17 when PWM signal is high. The current limit threshold is set to 700 mV (typical) when PWM signal is low. In CC mode, the transition between the two thresholds in conjunction with the slope compensation and the error amplifier circuit allows for higher inductor current immediately after the PWM transition, to improve LED current transient response in PWM dimming.

The device immediately terminates the GATEx and PDRVx outputs when the sensed voltage at the ISPx input exceeds the current limit threshold. For more detail on the cycle-by-cycle current limit, refer to the *Faults and Diagnostics* section.

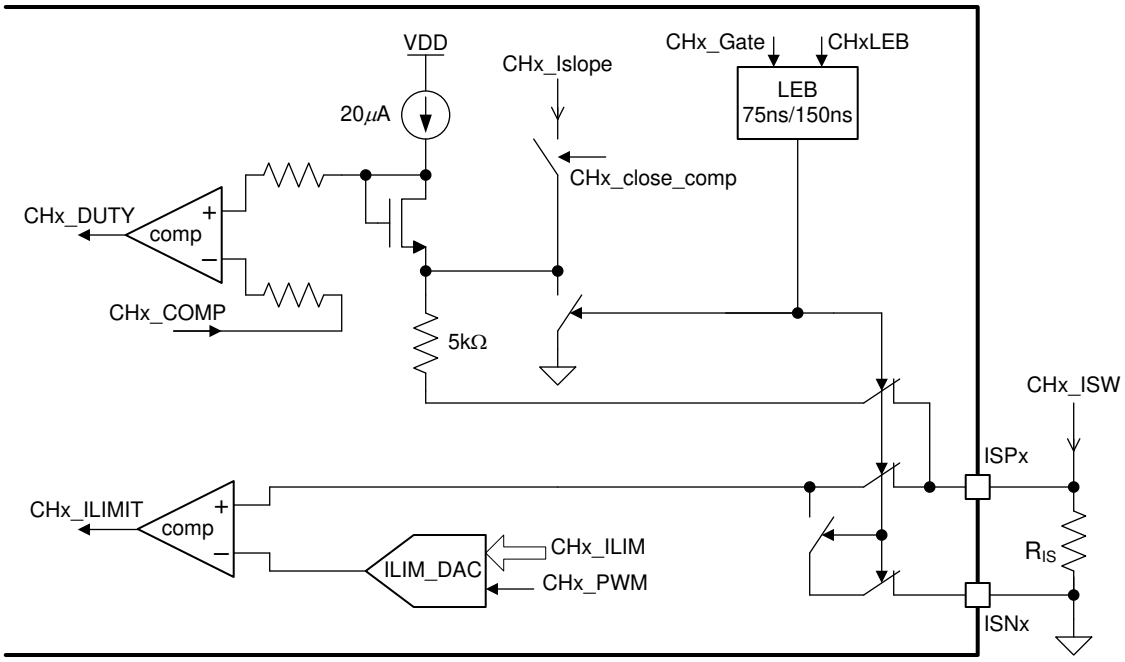


图 7-9. Switch Current Sense and Current Limit

7.3.9 Slope Compensation

Switching converters with peak current mode control are subject to subharmonic oscillation for duty cycles greater than 50%. To avoid instability, the control scheme adds an artificial ramp to the sensed switch current (shown in 图 7-9). The required slope of the artificial ramp depends on the input voltage, V_{IN}, output voltage, V_O, inductor L, and switch current sense resistor R_{IS}. The TPS92682-Q1 device provides a programmable slope compensation with seven levels of slope magnitude to simplify and enhance the performance of common switching converter topologies, such as boost, boost-to-battery, and SEPIC. The slope magnitude can be programmed through CHxISLP in the *ISLOPE Register*. The *Application and Implementation* section includes calculations for the choice of correct slope magnitude for a given application.

7.3.10 ILED Setting in CC Mode

In CC mode, as shown in 图 7-8, the voltage across the LED current sense resistor, $V_{(CSP-CSN)}$, is regulated to the output of the programmable 8-bit CHxIADJ-DAC, scaled by the current sense amplifier voltage gain of 14. The LED current can be linearly adjusted by writing a different value to the CHxIADJ register. The 8-bit DAC output can be set in the range of 85 mV (CHxIADJ = 9) to 2.4 V (CHxIADJ = 255). The associated channel is turned off for CHxIADJ ≤ 8.

7.3.11 Output Voltage Setting in CV Mode

In CV mode, as shown in 图 7-8, the voltage at the FBx pin (output voltage divider) is regulated to the output of the programmable 8-bit CHxIADJ-DAC. The FBx voltage can be adjusted in the range of 85 mV (CHxIADJ = 9) to 2.4 V (CHxIADJ = 255). The associated channel is turned off for CHxIADJ ⩽ 8.

7.3.12 PWM Dimming

As shown in 图 7-10, the TPS92682-Q1 device incorporates both internal and external PWM dimming. To select between external or internal PWM dimming, the INTPWM bit in *CFG1 Register* must be set to "0" or "1", respectively. If internal PWM dimming operation is selected, the state of the PWMx pins do not have any effect on the operation of the device. For external PWM dimming, apply a square-wave signal to the PWMx pin with the rising and falling thresholds provided in the *Electrical Characteristics*. The LED current modulates based on the duty cycle of the external PWM signal, $D_{PWM(EXT)}$.

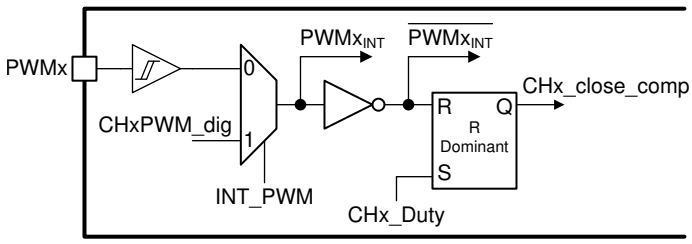


图 7-10. PWM Dimming Circuit

To use internal PWM dimming, the INTPWM bit in *CFG1 Register* must be set to "1". The TPS92682-Q1 device incorporates a 10-bit PWM counter for each channel. The duty cycle of the internal PWM can be set using a 10-bit value in the CHxPWML and CHxPWMH registers. Because CHxPWM is a 10-bit value, a PWM duty cycle update can require two SPI writes, one to the CHxPWMH and another to the CHxPWML register. To prevent transferring incoherent values, the contents of the two registers transfer to the CHxPWM counter only upon the write to the CHxPWML register. Therefore, for an update to the PWM duty cycle, it is recommended consecutively writing to CHxPWMH first and CHxPWML second. In addition, in order to avoid corrupting the progress of the current PWM duty cycle, the update from the CHxPWM registers to the CHxPWM counter occurs two PWM_{CLK} before the end of each PWM period (at the count of 1022).

Due to synchronization of the external PWM with internal clock, when switching from external PWM to internal PWM, a glitch for the total of one PWM period can be observed in the output.

The clock to the 10-bit PWM counter is related to the main clock, CLK_M, by a division factor set by a 3-bit value in the *PWMDIV Register*. The relation between the PWM_{CLK} and PWM frequency with CLK_M frequency are shown in Equation 3 and Equation 4.

$$PWM_{CLK} = \frac{f_{CLKM}}{PWM_{DIV}} \tag{3}$$

$$PWM_{FREQ} = \frac{PWM_{CLK}}{1024} \tag{4}$$

For example, if the CLK_M frequency is set to f_{CLKM} = 800 kHz and PWM_{DIV} = 001 (division value of 2), the PWM frequency is $PWM_{FREQ} \approx$ 390 Hz.

The phase between the internal PWM dimming for the two channels can be set to 180° if the PWMPH bit in *CFG1 Register* is set to 0. For PWMPH = 1, there is zero phase shift between the internal 10-bit PWM counters of the two channels.

The PWM signal controls the GATEx and PDRVx outputs. If PWM_{xINT} is set low, the associated channel is turned off, the COMPx pin is disconnected from the error amplifier, and the PDRVx output is set to V_{CSP} to maintain the charge on the compensation network and output capacitors. On the rising edge of the PWM_{xINT}, the

GATEx and PDRVx outputs are enabled to ramp the inductor current to the previous steady-state value. The COMPx pin connects to the error amplifier only when the switch current sense voltage V_{ISPx} exceeds the COMPx voltage, CHx_comp. This connection immediately forces the converter into steady-state operation with minimum LED current overshoot. When dimming is not required, connect the PWMx pins to the VDD pin. An internal pull-down resistor sets the PWM inputs to logic-low and disables the device when the pins are disconnected or left floating, and the INTPWM bit in *CFG1 Register* is set to the default value of "0".

7.3.13 P-Channel FET Gate Driver Output

The PDRVx output is a function of the internal PWM signal and is capable of sinking and sourcing up to 50 mA of peak current to control a high-side series connected P-channel dimming FET. The PDRV switches between VCSP and (VCSP – 7 V) is based on the status of the PWM signal to completely turn off and turn on the external P-channel dimming FET. In CC mode, a series dimming FET is required to achieve high contrast ratio since it ensures fast rise and fall times of the LED current in response to the PWM input. Without any dimming FET, the rise and fall times are limited by the inductor slew rate and the closed-loop bandwidth of the system. In CC mode, leave the PDRVx pin unconnected if not used. In CV mode, the PDRVx together with CSPx and CSNx pins can be connected to GND to limit the shutdown current. The PDRVx can also be disabled by setting the CHxPDRVEN bit in 表 7-3 to zero.

7.3.14 Soft Start

The soft start feature helps the regulator gradually reach the steady-state operating point, thus reducing start-up stresses and current surges. The device clamps the COMPx pin to the output of the SSDAC plus the threshold voltage of a P-FET, until the LED current or the output voltage approaches the regulation threshold. The soft start is controlled with an 8-bit DAC which ramps from 0 V to 2.8 V during start-up of an associated channel. The rate of the soft-start ramp (or the ramp time) can be controlled by programming the clock of the internal digital ramp counter. The clock of the digital ramp counter is related to the associated channel clock (switching frequency f_{SW}) by:

$$SS_{CLK} = \frac{CHx_{CLK}}{SSx_{DIV}} \tag{5}$$

The SSx_{DIV} is a division factor provided in the *SOFTSTART Register*. For example, if the channel switching frequency is set to 400 kHz, the soft-start ramp time can be programmed between 1.3 ms and 64 ms. It is important to note that the ramp time is the time for the SSDAC output to ramp from 0 V to 2.8 V (digital ramp counter to count from 0 to 255), but the controller can reach the regulation point before the ramp is completed.

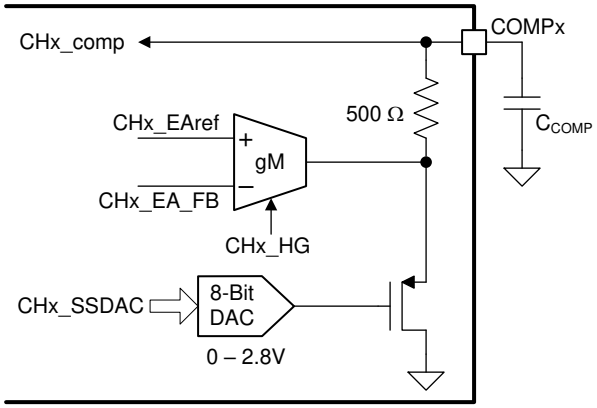


图 7-11. Soft-Start Circuit

When programming the soft-start ramp, It is essential to ensure that the soft-start ramp time is longer than the time required to charge the output capacitor.

To initiate the soft-start ramp, the PWM signal (internal or external) must be set high. If PWM dimming occurs during the soft-start period, the digital ramp counter holds the ramp value when PWM = LOW, and re-starts the ramp from the last ramp value when PWM = HIGH. 图 7-12 shows an example of this feature.

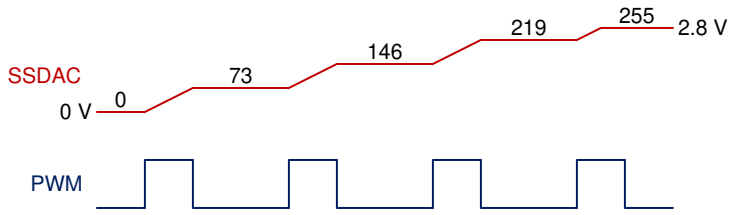


图 7-12. Soft-start Period During PWM Dimming

7.3.15 Two-Phase Operation

The TPS92682-Q1 device can be programmed in two-phase mode by setting the 2PH bit to "1" in *CFG1 Register*. In two-phase mode, the CH1_comp is internally connected to the CH2_comp with 500 Ω (max) of resistance. In this case, the error amplifier of channel-2 is disabled and only the error amplifier of channel-1 connects to both COMP1 and COMP2 pins. TI recommends that external compensators be connected to both COMP1 and COMP2 pins, and that these two pins be shorted together externally.

Two-phase mode uses only the channel-1 soft-start DAC and controls both phases. To generate the channel clocks, only the division factor for the channel-1, programmed in *SWDIV Register*, is used. The two channel clocks (switching frequency f_{SW}) are the same and are 180° out-of-phase.

In two-phase mode, in the case of internal PWM, only CH1PWM is used for both channels. When external PWM is used, it is recommended to short both PWMx pins together and use only one PWM signal for both channels.

A selected number of the faults (CH2_OV, CH2_UV, CH2_OC, and CH2_UC) have no effect in the operation of two-phase mode. For more detail about faults and diagnostics in TPS92682-Q1, refer to *Faults and Diagnostics* section.

7.3.15.1 Current Sharing In Two-Phase

In two-phase operation, the current sharing between the two phases depends on the mismatch between the current sense circuitry of the two channels. The TPS92682-Q1 incorporates a feature and a register setting to improve the current sharing in two-phase operation. 表 7-40 includes three bits of calibration settings, CHxCAL2:0, which introduce an offset of 0 to 17.5 mV (with a resolution of 2.5 mV) to the channel switch current sense voltage. The calibration offset can be used to compensate for the mismatch offset between the two channels.

The following procedure is recommended for offset calibration between the two phases in a CV two-phase design:

- In two-phase CV, Comp1 and Comp2 pins are connected together.
- Configure the registers for the application and turn on the two-phase converter.
- Set the load at the output of the two-phase converter to half of the maximum load in the application.
- Set CH2GOFF = 1 and CH1GOFF = 0 in 表 7-40. This setting turns off channel-2. Measure the COMP voltage as shown in 图 7-13 and record the measurement as V_{COMP1}.
- Set the CH1GOFF = 1 and CH2GOFF = 0 in 表 7-40. This setting turns off channel-1. Measure the COMP voltage and record the measurement as V_{COMP2}.
- The difference between the two measurements, $\Delta V_{OFST} = V_{COMP1} - V_{COMP2}$, is the offset mismatch between the two phases.
- By setting a similar offset voltage through CHxCAL bits, the mismatch can be corrected (offset must be set in CH2CAL if $V_{COMP1} > V_{COMP2}$, and in CH1CAL if $V_{COMP1} < V_{COMP2}$).
- At the end of the procedure, set both CH1GOFF and CH2GOFF bits to zero.

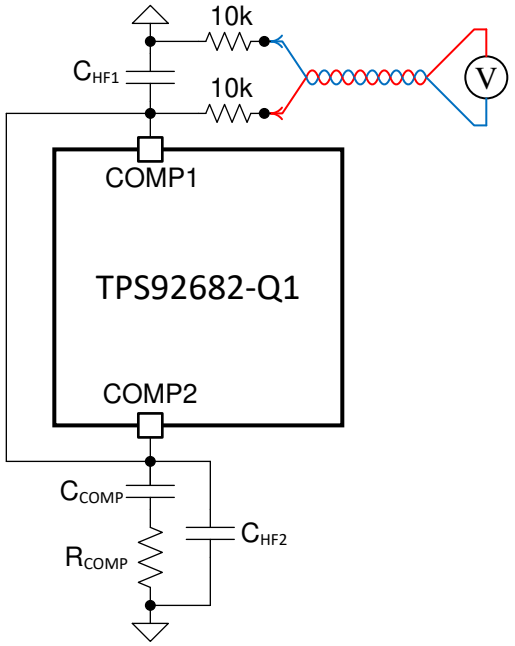


图 7-13. Current Sharing Calibration Setup

7.3.16 Faults and Diagnostics

The TPS92682-Q1 includes a comprehensive configurable faults and diagnostics feature. 表 7-1 shows the list of the faults and diagnostics. A selected number of the faults (UVLO, RTOPEN, TW, TSD, and POR) are shared between the two channels.

As shown in 表 7-1, a selected number of the faults can be enabled or disabled using FLT EN-bits in the *FEN1* and *FEN2* registers. The rest of the faults and diagnostics feature are always enabled and operational.

All the faults and diagnostics features, except FBOPEN, TSD, and UVLO, have an associated Fault-Read-bit in the *FLT1* and *FLT2* registers. Upon occurrence of the fault, the associated Fault-Read-bit is set in the register map. Reading these registers clears the bits that are set if the condition no longer exists. The clearing of the Fault-Read-bits happens at the end of the SPI transfer read response, not at the end of the read command. Although FBOPEN fault does not have a dedicated Fault-Read-bit, this fault sets the OV-fault read bit.

In TPS92682-Q1, the OV, UV, ILIM, and OC faults can be configured to be a non-latched fault in the *FLATEN Register*. If a fault is configured as non-latched, upon occurrence of the fault, the associated channel turns off. The channel performs a soft start after expiration of a configurable fault timer and when the fault is cleared. In latched fault condition, the associated channel is turned off and remains off until the channel enable-bits are re-programmed in the *EN Register*.

表 7-1. TPS92682 Faults and Diagnostics

LIST	DESCRIPTION	FAULT OR DIAGNOS.	FLT EN-BIT	FLT R-BIT	ENABLE FTIMER	F-PIN TRIGGER	DISABLE LATCH
OV	Output over voltage fault	Fault	Yes	Yes	No	Yes	Yes
UV	Output under voltage fault	Fault	Yes	Yes	Yes	Yes	Yes
ILIM	Cycle/Cycle switch current limit	Fault	Yes	Yes	Yes	Yes	Yes
UVLO	Input under voltage lockout	Fault	No	No	No	No	No
OC	ILED over current	Fault	Yes	Yes	Yes	Yes	Yes
UC	ILED under current	Diagnos.	No	Yes	No	No	No
ISNOPEN	ISNx open pin fault	Fault	Yes	Yes	No	Yes	No
RTOPEN	RT open pin fault	Fault	No	Yes	No	Yes	No
FBOPEN	FB pin open pin fault	Fault	Yes	No	No	Yes	No

表 7-1. TPS92682 Faults and Diagnostics (continued)

LIST	DESCRIPTION	FAULT OR DIAGNOS.	FLT EN-BIT	FLT R-BIT	ENABLE FTIMER	F-PIN TRIGGER	DISABLE LATCH
TW	Thermal warning at 150°C (typ.)	Diagnos.	No	Yes	No	No	No
TSD	Thermal shutdown	Fault	No	No	No	Yes	No
POR	Power On Reset	Fault	No	Yes	No	Yes	No

As shown in 表 7-1, all faults, except UVLO, UC, and TW, set the active low fault pins, $\overline{FLT1}$ and $\overline{FLT2}$. 图 7-14 shows the functionality of the fault pins. SYNC/ $\overline{FLT2}$ is a dual function pin. When the SYNCEN bit in the *EN Register* is set to "1", SYNC/ $\overline{FLT2}$ is an input pin and a square wave signal with the desired f_{CLKM} frequency must be applied to this pin. In this case, faults on both channels are ORed and applied to the $\overline{FLT1}$ pin.

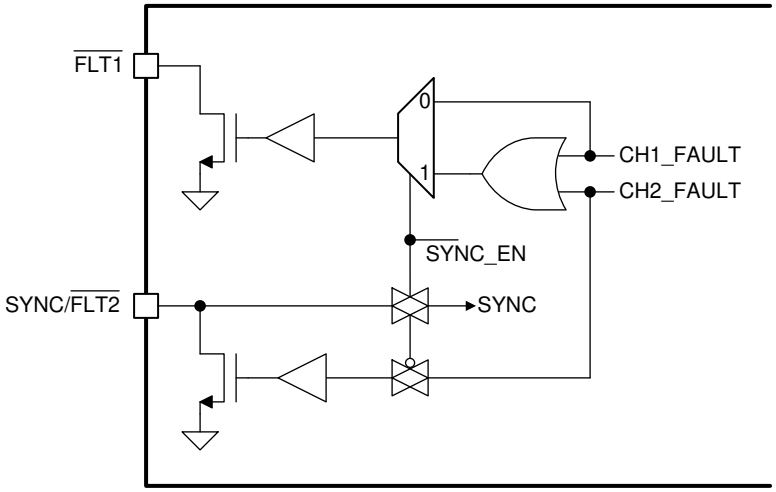


图 7-14. Fault PINs

7.3.16.1 Main Fault Timer (MFT)

For each channel of the TPS92682-Q1, there is a 14-bit counter that implements a main fault timer. The timer can be programmed by a 4-bit value for each channel in the *MFT Register*. The MFT time can be set to a value between 1000 and 16383 times the input clock period. The input clock of the MFT is the channel clock, CHx_{CLK} (the switching frequency f_{SW}). For example, for a channel with a switching frequency of f_{SW} = 400 kHz, the timer can be programmed from 2.5 to 41 ms.

Only UV and OC faults can trigger the MFT. When either of these two faults are enabled as a non-latched fault, the fault event turns off the channel and triggers the MFT. The associated channel is turned back on by a soft-start process when the MFT count is completed and the fault is cleared.

7.3.16.2 OV Fault

If CHxOVEN is set to "1" in the *FEN1 Register*, the output over voltage fault is enabled. When V_{FBx} exceeds the threshold voltage OV_{THR}, the CHx_OV fault is set high and turns off the associated channel. The OV_{THR} voltage is set by OV_DAC; OV_{THR} = VFB_{REF} × $OV_{\%}$, where $OV_{\%}$ is provided in the *OV Register*. The VFB_{REF} in CC mode is set to 1.228 V (typical), and in CV mode, is set to the output of the *CHxIADJ register*. When CHx_OV is high, OV_{THR} is set to VFB_{REF} and a 20 µA hysteresis current is applied to the feedback resistor divider. For the boost converter with the output voltage sensing according to 图 7-15, V_{OUT} must decrease to a level shown in Equation 6 for the CHx_OV to be cleared.

$$V_O \le \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times VFB_{REF} - I_{20\mu} \times R_{FB2} \quad (6)$$

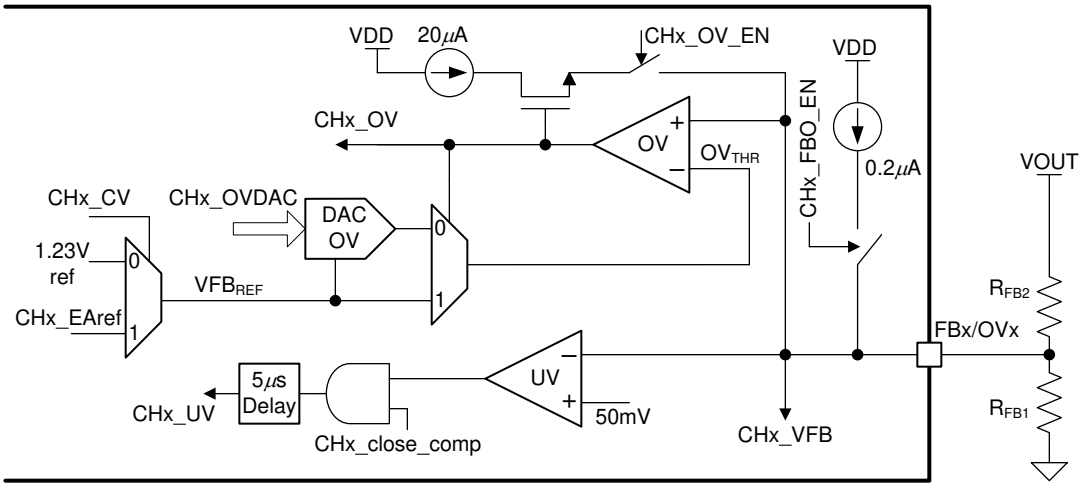


图 7-15. OV and UV Faults

If the CHxOVFL bit is set to "1" in the *FLATEN Register*, the OV fault is configured as a latched fault and the associated channel turns off with the rising edge of CHx_OV. The channel can be turned on again only by re-setting the CHxEN bit in the *EN Register*.

For CHxOVFL = 0, the OV fault is a non-latched fault. In this case, the associated channel turns off when the OV fault occurs, but the channel goes through a restart and soft-start ramp when CHx_OV goes low. 图 7-16 shows a non-latched OV situation for a converter in CV mode, where the output voltage (V_{FBx}) is regulated to VFB_{REF} in normal condition.

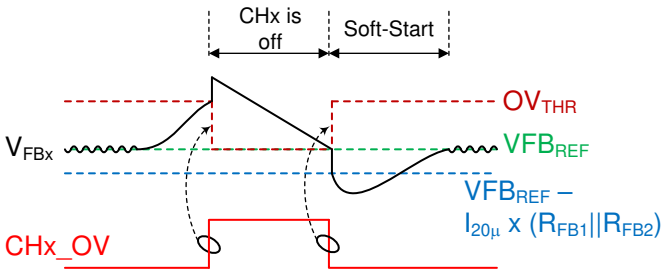


图 7-16. Non-latched OV Fault in CV Mode

7.3.16.3 UV Fault

If CHxUVEN is set to "1" in the *FEN1 Register*, the output under voltage fault is enabled. 图 7-15 shows when V_{FBx} decreases below the UV_{THR} of 50 mV (typ.), CHx_UV is set high and turns off the associated channel. If the CHxUVFL bit is set to "1" in the *FLATEN Regiser*, the UV fault is configured as a latched fault and the associated channel turns off and remains off with the rising edge of CHx_UV. The channel can be turned on again only by re-setting the CHxEN bit to "1". For CHxUVFL = 0, the UV fault is a non-latched fault. In this case, the associated channel turns off when a UV fault occurs, but the channel goes through a restart and soft-start ramp when CHx_UV is cleared and the MFT is expired.

The UV fault is disabled during the soft-start ramp if the CHxRFEN bit is set to "0" in the *FEN1 Register*.

7.3.16.4 ILIM Fault

图 7-9 shows that the cycle-by-cycle switch current limit is achieved by comparing the sensed switch current with a programmable ILIM threshold and terminating the duty cycle when $V_{ISPx} \geqslant V_{ILIM(THR)}$. The $ILIM_{THR}$ can be set using a 2-bit value in the *ILIM Register*. If CHxILIMEN is set to zero in the *FEN2 Register*, the ILIM fault is disabled. However, the cycle-by-cycle current limit is always active as long as the sensed switch current exceeds $ILIM_{THR}$.

If CHxILIMEN is set to "1", the ILIM fault is enabled, and it can be set as a latched or non-latched fault. There is an ILIM event counter for each channel that counts the number of ILIM fault events. When the ILIM event counter reaches a programmed value, the associated channel is turned off. The maximum number of ILIM fault events can be set using a 2-bit CHxILIMCNT in *ILIM Register*. The ILIM event counter is reset every 100-CHx_{CLK} cycles to prevent transients and non-real faults, resulting in an unwanted channel disable.

If CHxILIMFL is set to "1" in the *FLATEN Register*, the ILIM event is set to a latched fault. The associated channel is turned off and remains off when the ILIM event counter reaches the programmed value. The channel can be turned on again only by re-setting the CHxEN bit to "1" in the *EN Register*.

For CHxILIMFL = 0, the ILIM fault is a non-latched fault. When the ILIM event counter reaches the programmed value, the associated channel is turned off and an ILIM fault timer, IFT, is triggered. The associated channel is turned back on by a soft-start ramp when the ILIM fault timer count is completed and the output of the ILIM event counter is cleared. The ILIM fault timer can be programmed using a 2-bit value CHxIFT in the *IFT Register*. The IFT time can be set to a value between four and 32 cycles of the input clock. The input clock of the IFT is the channel clock, CHx_{CLK} (the switching frequency f_{SW}). For example, for a channel with a switching frequency of f_{SW} = 400 kHz, the timer can be programmed from 10 to 80 µs.

图 7-17 shows the simplified functional block diagram of the ILIM fault. 图 7-18 shows the progress of the cycle by cycle current limit, the ILIM event counter (IFEC), the ILIM Fault Timer (IFT), and the restart of the channel for a non-latched ILIM fault.

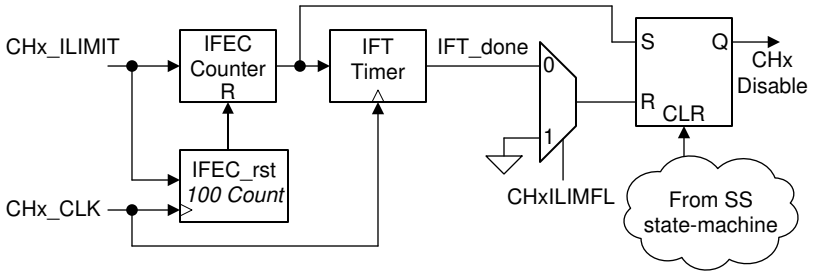


图 7-17. ILIM Fault Diagram

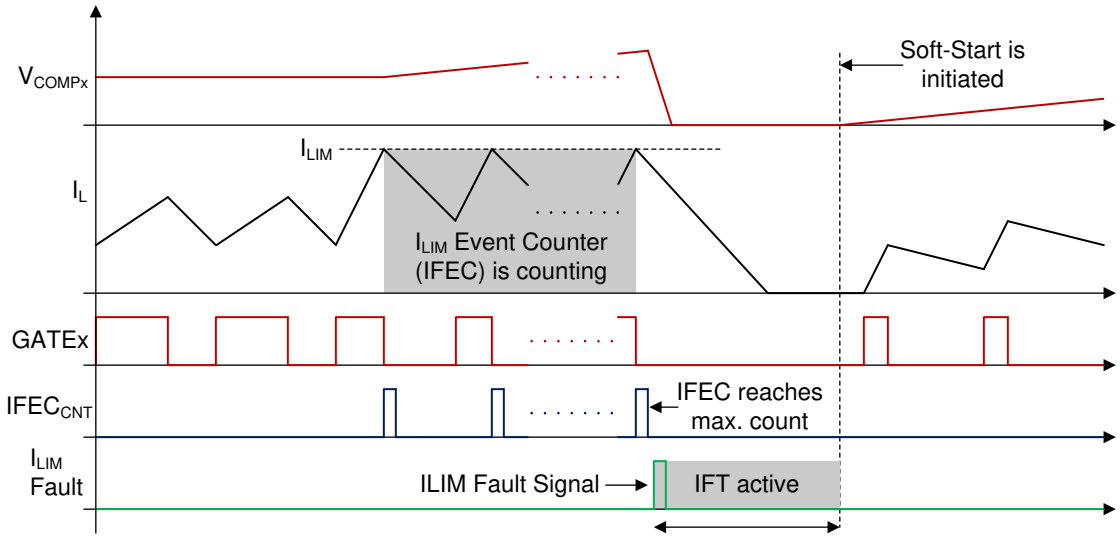


图 7-18. ILIM Fault

The ILIM fault in CV mode is disabled during the soft-start ramp if the CHxRFEN bit is set to "0" in the *FEN1 Register*.

As stated before, it is important to note that the cycle-by-cycle switch current limit is always active even if the ILIM fault is disabled.

7.3.16.5 UVLO

For details on the UVLO fault, refer to the *Internal Regulator and Undervoltage Lockout* section.

7.3.16.6 ILED Over Current (OC)

When CHxOCEN is set to "1" in *FEN2 Register*, the ILED overcurrent fault is enabled, and the voltage across the current sense inputs (CSPx and CSNx) is monitored. The device sets the OC fault signal when the voltage at the output of the current sense amplifier exceeds the regulation set point V_{IADJ} by 50%. The OC fault threshold is calculated as follows:

$$V_{(CSPx-CSNx)} = 1.5 \times \frac{V_{IADJ}}{14} \quad (7)$$

If the CHxOCFL bit is set to "1" in *FLATEN Register*, the OC fault is configured as a latched fault and the associated channel turns off and remains off with the rising edge of CHx_OC. The channel can be turned on again only by re-setting the CHxEN bit to "1" in *EN Register*. For CHxOCFL = 0, the OC fault is a non-latched fault. In this case, the associated channel turns off when an OC fault occurs, but the channel goes through a restart and soft-start ramp when CHx_OC is cleared and the MFT is expired.

7.3.16.7 ILED Undercurrent (UC)

The ILED Undercurrent (UC) is a diagnostic feature and not a fault event. Therefore, the UC event sets the fault read bits in the *FLT2* register only, and does not have any effect on the operation of the associated channel or trigger the fault pins.

The device sets the UC event when the voltage at the output of the current sense amplifier decreases by 50% from the regulation set point V_{IADJ}. The UC threshold is calculated as follows:

$$V_{(CSPx-CSNx)} = 0.5 \times \frac{V_{IADJ}}{14} \quad (8)$$

When PWM dimming, the UC fault read bit might be set during the time when PWM is low.

7.3.16.8 ISNOPEN, FBOPEN, and RTOPEN Faults

The device can detect open pin fault on ISNx, FBx, and RT pins. If any of these pins are opened during operation, the device turns off the associated channel (or both channels for RT open pin). The channels can be turned on again only by re-setting the CHxEN bits high and if the faults are removed.

7.3.16.9 TW and TSD

The thermal warning (TW) bit is set in the *FLT1 Register* when the junction temperature exceeds 150°C (typ). The TW event is a diagnostic feature and not a fault event. As a result, TW does not have any effect on the operation of the device.

Internal thermal shutdown (TSD) circuitry is implemented to protect the controller in the event the junction temperature exceeds a value of 175°C. In the event of TSD, the controller is forced into a shutdown mode, disabling the internal regulator. This feature is designed to prevent overheating and damage to the device.

7.3.16.10 COMPx Pull-Down and Comp-Low signal

As shown in 图 7-8, an internal switch pulls down the COMPx pin when there is a fault. The Comp-Pull-Down discharges the compensator capacitors, such that the converter start-up always begins from a known state.

The converter does not start unless the COMPx voltage decreases below 100 mV (when CHx_complow goes high).

7.4 Device Functional Modes

The TPS92682-Q1 operates in the functional modes shown in 图 7-19.

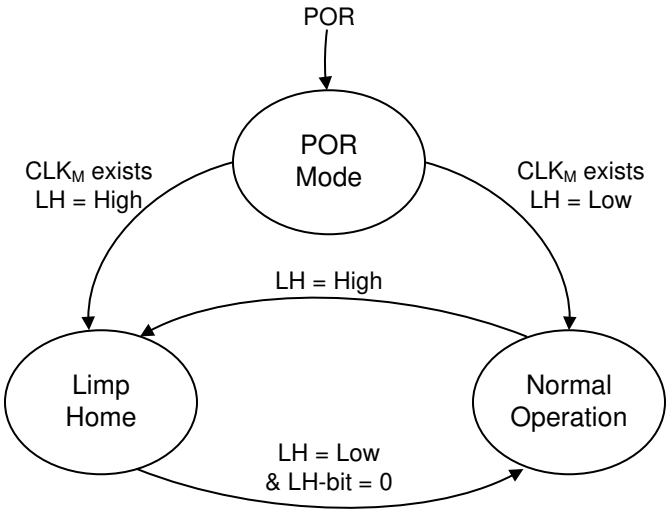


图 7-19. TPS92682 Functional Mode

7.4.1 POR Mode

Upon POR, all the register settings are reset to their default values and both channels are turned off. The device enters functional modes if the main clock, CLK_M, is active.

7.4.2 Normal Operation

In Normal operation mode, the registers can be programmed and the channels can be turned on. To operate in this mode, the LH pin must be low. The state machine for this mode is shown in 图 7-20 and 图 7-21.

Note

The operational mode shown in 图 7-20 and 图 7-21 is only intended to describe the operation of the internal state machine and is not meant to be used as a guideline for the firmware development.

- State 0: After POR, all the registers are reset to their default values, and the two channels are off.
- State 1 (CHx_EN-BIT = 0): In this state, the device registers are ready to be programmed. Read FLT1 and FLT2 registers to clear all the fault read bits and the PC bit. Set the FPINRST bit in the EN register in order for the fault pins to be cleared. All the initializations must be completed before turning on the channels. The device stays in state-1 unless the condition of CHx_IADJ > 8 is met.
- State 2 (CHx_EN-BIT = 1): The device advances to state-2 when the CHx_EN bit is set to "1". In this state, all the necessary conditions for initiating the soft-start ramp are checked. The CHx_complow signal and CHx_PWM are high, and the condition of CHx_IADJ > 8 is met. If a latched fault occurs in this state, the CHx_comp pin is pulled low, the CHx_EN bits are set to zero and the device returns to state-1. For a non-latched fault, the device remains in this mode until the fault is removed.
- State 3 (SSDAC_RAMP): The SSDAC_RAMP state begins when all the conditions for the soft-start ramp initialization are met. In this state, the soft-start ramp DAC increments only when CHx_PWM is high. For CHx_PWM = LOW, the ramp is held constant. The DAC ramp re-starts the increment from the previous value at the next PWM dimming cycle, and when CHx_PWM = HIGH. If a latched-fault occurs in this state, the CHx_comp pin is pulled low, the CHx_EN bit is set to zero, and the device returns to state-1. For a non-latched fault, the associated channel is turned off, the CHx_comp pin is pulled low and the device returns to state-2. At the end of the soft-start ramp, read the FLT1 and FLT2 registers and set the FPINRST bit in the EN register in order for the fault read-bits and the fault pins to be cleared.

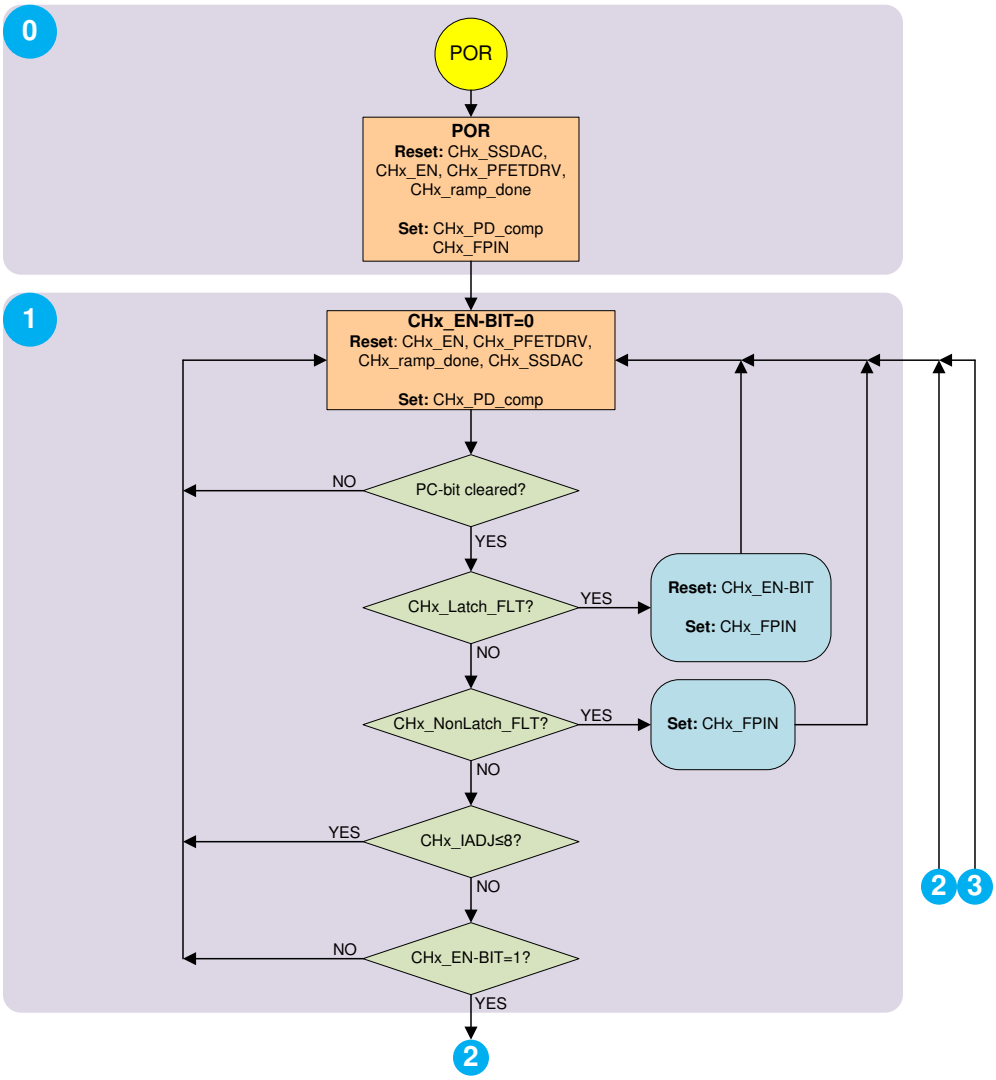


图 7-20. Operational Mode, States 0 and 1

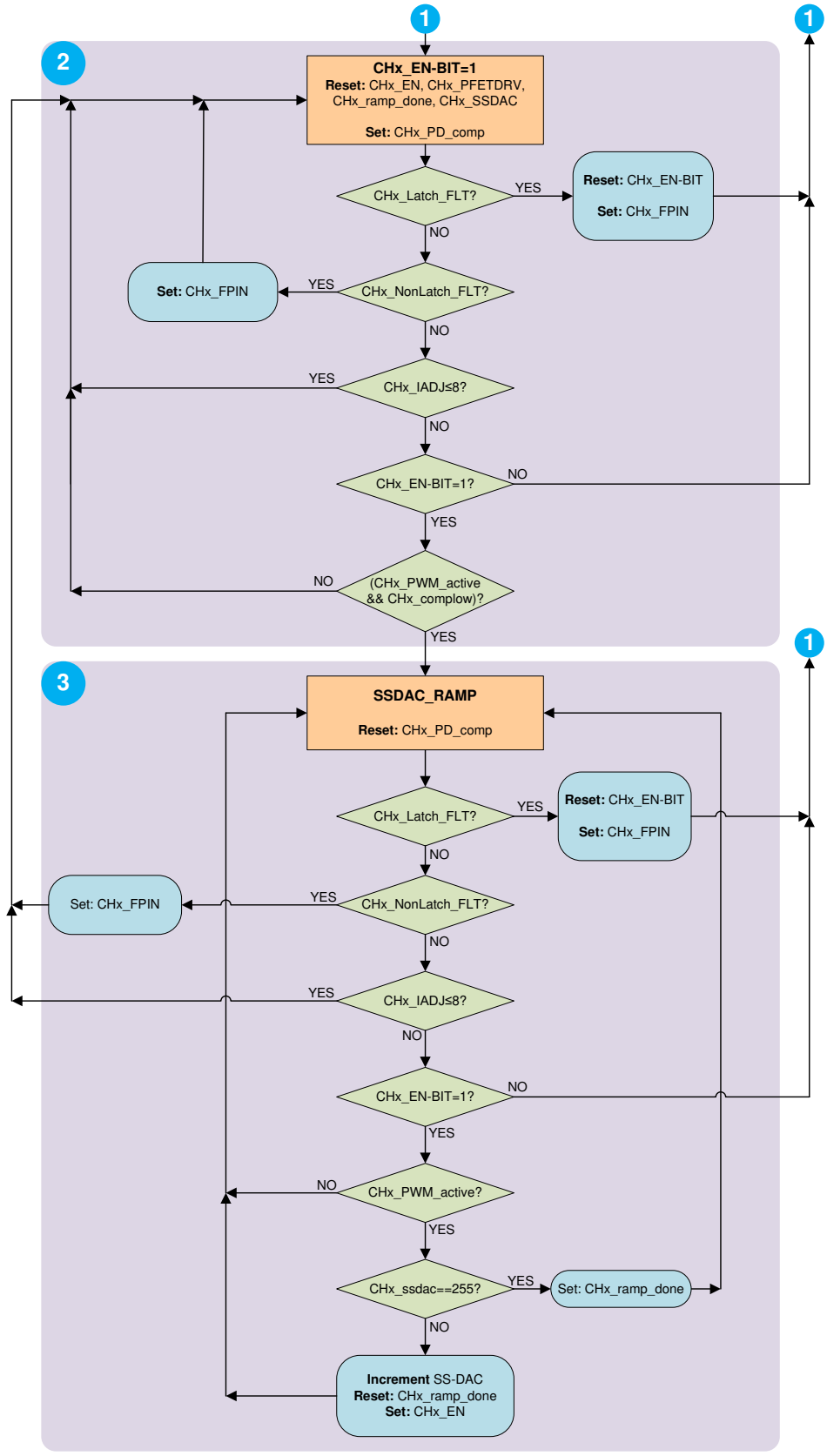


图 7-21. Operational Mode, States 2 and 3

7.4.3 Limp Home

The TPS92682-Q1 device enters the limp home (LH) mode, when the LH pin is pulled high (VDD, or logic level voltage). In LH mode, the device sets the operation of the device based on the SPI programmable LH-registers (register addresses 0x17 to 0x24). The LH-registers should be programmed during initialization of the device. To exit the LH mode, the LH pin must be pulled low, and the LH bit in *CFG1 Register* must be written to "0". The LH bit is set to "1" when the LH pin is pulled high. Writing a value of "1" to the LH bit does not have any effect and does not change the operation of the device.

7.5 Programming

The programming of the TPS92682-Q1 registers can be performed through a serial interface communication. The 4-wire control interface in the TPS92682-Q1 device is compatible with the Serial Peripheral Interface (SPI) bus. A Micro-Controller-Unit (MCU) can write to and read from the device registers to configure the channel operation and enable or disable a specific channel.

7.5.1 Serial Interface

The SPI bus consists of four signals: SSN, SCK, MOSI, and MISO. The SSN, SCK, and MOSI pins are TTL inputs into the TPS92682-Q1 while the MISO pin is an open-drain output. The SPI bus can be configured for both star-connect and daisy chain hardware connections.

A bus transaction is initiated by the MCU creating a falling edge on SSN. While SSN is low, the input data present on the MOSI pin is sampled on the rising edge of SCK, with MS-bit first. The output data is asserted on the MISO pin at the falling edge of the SCK. 图 7-22 shows the data transition and sampling edges of SCK.

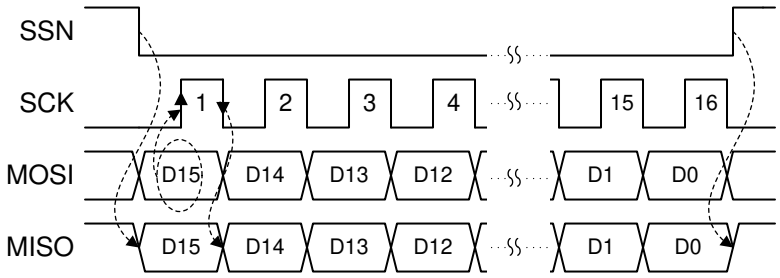


图 7-22. SPI DATA Format

A valid transfer requires a non-zero integer multiple of 16 SCK cycles (16, 32, 48, and so forth). If SSN is pulsed low and no SCK pulses are issued before SSN rises, a SPI error is reported. Similarly, if SSN is raised before the 16th rising edge of SCK, the transfer is aborted and a SPI error is reported. If SSN is held low after the 16th falling edge of SCK and additional SCK edges occur, the data continues to flow through the TPS92682-Q1 shift register and out of the MISO pin. When SSN transitions from low-to-high, the internal digital block decodes the most recent 16 bits that were received prior to the SSN rising edge.

SSN must transition to high after a multiple of 16 SCK cycles for a transaction to be valid and does not set the SPI error bit. In the case of a write transaction, the TPS92682-Q1 logic performs the requested operation when SSN transitions high. In the case of a read transaction, the read data is output during the next frame, regardless of whether a SPI error has occurred.

The data bit on MOSI is shifted into an internal 16-bit shift register (MS-bit first) while data is simultaneously shifted out of the MISO pin. While SSN is high (bus idle), MISO is tri-stated by the open-drain driver. While SSN is low, MISO is driven according to the 16-bit data pattern being shifted out based on the prior received command. At the falling edge of the SSN, to begin a new transaction, MISO is driven with the MS-bit of the outbound data, and is updated on each subsequent falling edge of SCK.

7.5.2 Command Frame

The command frames are the only defined frame-format that are sent from master to slave on MOSI. A command frame can be either a read command or a write command. A Command frame consists of a CMD bit,

six bits of ADDRESS, a PARITY bit (odd parity), and eight bits of DATA. The format of the Command frame is shown in 图 7-23. The bit sequence is as follows:

1. The COMMAND bit (CMD). CMD = 1 means the transfer is a write command; CMD = 0 means it is a read command.
2. Six bits of ADDRESS (A5..A0)
3. The PARITY bit (PAR). This bit is set by the following equation: PARITY = XNOR(CMD, A5..A0, D7..D0).
4. Eight bits of DATA (D7..D0). For read commands, the DATA bits must be set to zero.

Both the Read and the Write Command follow the Command frame format.

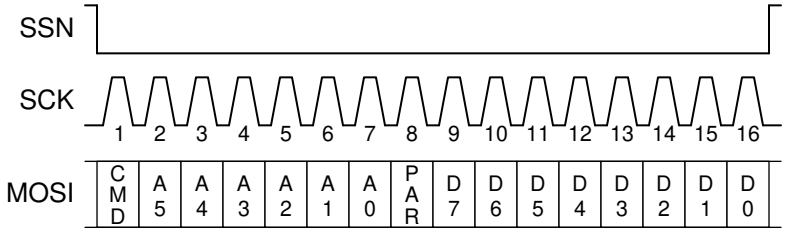


图 7-23. Command Frame Format

7.5.3 Response Frame

There are three possible response frame formats: Read Response, Write Response, and Write Error/POR. These formats are further described below.

7.5.3.1 Read Response Frame Format

The Read Response has the following format:

1. The SPI Error bit (SPE)
2. Four reserved bits (always ‘1100’)
3. The RT Open Fault bit (RTO)
4. The Power-Cycled bit (PC)
5. The Thermal Warning bit (TW)
6. Eight bits of DATA (D7..D0)

This is shown in 图 7-24. This frame is sent out by the TPS92682-Q1 following a read command.

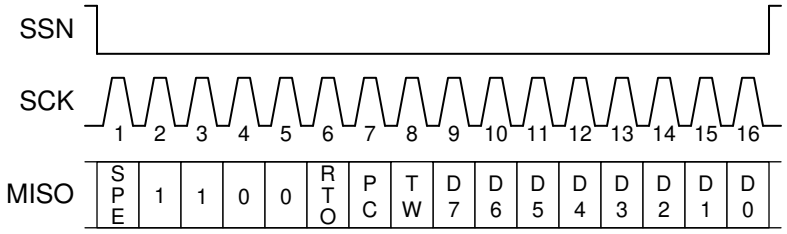


图 7-24. Read Response Frame Format

7.5.3.2 Write Response Frame Format

The Write Response frame has the following format:

1. The SPI Error bit (SPE)
2. The COMMAND bit (CMD)
3. Six bits of ADDRESS (A5..A0)
4. Eight bits of DATA (D7..D0)

This is shown in 图 7-25. This frame is sent out following a write command if the previously received frame was a write command and no SPI Error occurred during that frame.

The data and address bits in the write response are the data and address that were sent in the previous write command.

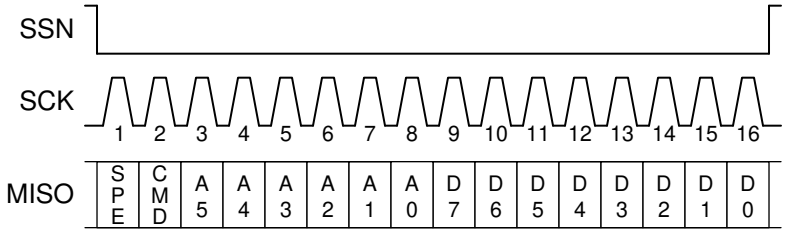


图 7-25. Write Response Frame Format

7.5.3.3 Write Error/POR Frame Format

The Write Error/POR frame is simply a ‘1’ in the MSB, followed by all zeroes (see 图 7-26). This frame is sent out by the TPS92682-Q1 internal digital block during the first SPI transfer following power-on reset, or following a write command with a SPI Error.

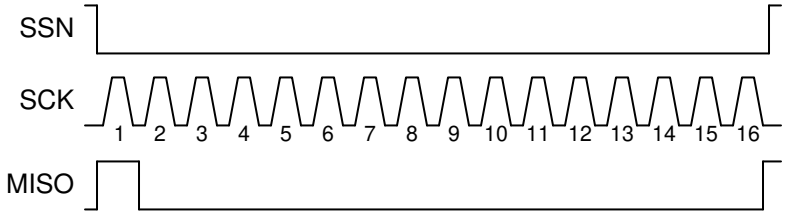


图 7-26. Write Error/POR

7.5.4 SPI Error

The TPS92682-Q1 device records a SPI Error if any of the following conditions occur:

- The SPI command has a non-integer multiple of 16 SCK pulses.
- Any of the DATA bits during a read command are non-zero.
- There is a parity error in the previously received command.

If any of these conditions are true, the TPS92682 sets the SPE bit high in the next response frame. A write command with a SPI Error (not 16-bit aligned or bad parity) does NOT write to the register being addressed. Similarly, a read command to FLT1 or FLT2 does not clear any active fault bits in those registers if the command has a SPI Error.

7.6 TPS92682 Registers

The SPI-accessible registers are 8-bits wide and exist in a 6-bit-addressable register array (0x00 through 0x3F). The registers in the TPS92682 device contain programmed information and operating status. Upon power-up the registers are reset to their default values. Writes to unlisted addresses are not permitted and may result in undesired operation. Reads of unlisted addresses return the zero value.

Reserved bits (“RSVD”) must be written with ‘0’ values when writing. Registers are read/write unless indicated in the description of the register. 表 7-2 lists the TPS92682 register map.

表 7-2. TPS92682 Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	**EN**	FPINRST	SYNCEN	CH2MAXDEN	CH1MAXDEN	CH2PDRVEN	CH1PDRVEN	CH2EN	CH1EN	00111100
01h	**CFG1**	PWMPH	INTPWM	2PH	LH	CH2HG	CH1HG	CH2CV	CH1CV	00000000
02h	**CFG2**	CH2LEB	CH1LEB	RSVD	RSVD	CH2FILT1	RSVD	RSVD	CH1FILT1	00000000
03h	**SWDIV**	RSVD	RSVD	RSVD	RSVD	CH2DIV1:0		CH1DIV1:0		00000000
04h	**ISLOPE**	RSVD	CH2ISLP2:0			RSVD	CH1ISLP2:0			01010101
05h	**FM**	RSVD	RSVD	FMMAG1:0		FMFREQ3:0				00000101
06h	**SOFTSTART**	CH2SS3:0				CH1SS3:0				01110111

表 7-2. TPS92682 Register Map (continued)

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
07h	CH1IADJ	CH1IADJ7:0								00000000
08h	CH2IADJ	CH2IADJ7:0								00000000
09h	PWMDIV	RSVD	RSVD	RSVD	RSVD	RSVD	PWMDIV2:0			00000001
0Ah	CH1PWML	CH1PWM7:0								00000000
0Bh	CH1PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH1PWM9:8		00000000
0Ch	CH2PWML	CH2PWM7:0								00000000
0Dh	CH2PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH2PWM9:8		00000000
0Eh	ILIM	CH2ILIMCNT1:0		CH1ILIMCNT1:0		CH2ILIM1:0		CH1ILIM1:0		00001111
0Fh	IFT	RSVD	RSVD	RSVD	RSVD	CH2IFT1:0		CH1IFT1:0		00001010
10h	MFT	CH2MFT3:0				CH1MFT3:0				10011001
11h	FLT1	RTO	RSVD	PC	TW	CH2OV	CH1OV	CH2UV	CH1UV	read
12h	FLT2	CH2UC	CH1UC	CH2OC	CH1OC	CH2ILIM	CH1ILIM	CH2ISO	CH1ISO	read
13h	FEN1	CH2RFEN	CH1RFEN	CH2FBOEN	CH1FBOEN	CH2OVEN	CH1OVEN	CH2UVEN	CH1UVEN	00111100
14h	FEN2	OVOPT	RSVD	CH2OCEN	CH1OCEN	CH2ILIMEN	CH1ILIMEN	CH2ISOEN	CH1ISOEN	00001111
15h	FLATEN	CH2ILIMFL	CH1ILIMFL	CH2OCFL	CH1OCFL	CH2OVFL	CH1OVFL	CH2UVFL	CH1UVFL	00000000
16h	OV	RSVD	CH2OV2:0			RSVD	CH1OV2:0			00100010
17h	LHCFG	LHPWMPH	LHINTPWM	LHCH2MAXDEN	LHCH1MAXDEN	LHCH2PDRVEN	LHCH1PDRVEN	LHCH2EN	LHCH1EN	00111100
18h	LHCH1IADJ	LHCH1IADJ7:0								00000000
19h	LHCH2IADJ	LHCH2IADJ7:0								00000000
1Ah	LHCH1PWML	LHCH1PWM7:0								00000000
1Bh	LHCH1PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LHCH1PWM9:8		00000000
1Ch	LHCH2PWML	LHCH2PWM7:0								00000000
1Dh	LHCH2PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LHCH2PWM9:8		00000000
1Eh	LHILIM	LHCH2ILIMCNT1:0		LHCH1ILIMCNT1:0		LHCH2ILIM1:0		LHCH1ILIM1:0		00001111
1Fh	LHIFT	RSVD	RSVD	RSVD	RSVD	LHCH2IFT1:0		LHCH1IFT1:0		00001010
20h	LHMFT	LHCH2MFT3:0				LHCH1MFT3:0				10011001
21h	LHFEN1	LHCH2RFEN	LHCH1RFEN	LHCH2FBOEN	LHCH1FBOEN	LHCH2OVEN	LHCH1OVEN	LHCH2UVEN	LHCH1UVEN	00111100
22h	LHFEN2	RSVD	RSVD	LHCH2OCEN	LHCH1OCEN	LHCH2ILIMEN	LHCH1ILIMEN	LHCH2ISOEN	LHCH1ISOEN	00001111
23h	LHFLATEN	LHCH2ILIMFL	LHCH1ILIMFL	LHCH2OCFL	LHCH1OCFL	LHCH2OVFL	LHCH1OVFL	LHCH2UVFL	LHCH1UVFL	00000000
24h	LHOV	RSVD	LHCH2OV2:0			RSVD	LHCH1OV2:0			00100010
25h	CAL	CH2CAL2:0			CH2GOFF	CH1CAL2:0			CH1GOFF	00000000
26h	RESET	RESET7:0								00000000

In the following sub-sections the descriptions of different registers in 表 7-2 are provided.

7.6.1 EN Register

EN is the channel enable register. This register contains bits associated with the enabling of channels and several channel-related functions.

表 7-3. EN Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	EN	FPINRST	SYNCEN	CH2MAXDEN	CH1MAXDEN	CH2PDRVEN	CH1PDRVEN	CH2EN	CH1EN	00111100

- FPINRST:

  Setting this bit to one resets both fault pins, if there are no active faults in the system. Note that this bit is write-only. Any reads of this register return 0 in the FPINRST bit location.

- SYNCEN:

  0: SYNC input is disabled.

  1: SYNC input is enabled.

- CHxMAXDEN:

  0: Maximum duty cycle for the associated channel is disabled.

  1: Maximum duty cycle for the associated channel is enabled.

- CHxPDRVEN:

  0: The associated channel PFET driver is disabled.

  1: The associated channel PFET driver is enabled.

- CHxEN:

  0: The associated channel is disabled.

  1: The associated channel is enabled. SPI writes of ‘1’ to these bits are blocked if the PC bit in the FLT1 register is high.

7.6.2 CFG1 Register

Configuration register 1

表 7-4. CFG1 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
01h	CFG1	PWMPH	INTPWM	2PH	LH	CH2HG	CH1HG	CH2CV	CH1CV	00000000

- PWMPH:

  0: Phase shift of 180° between internal PWM signals

  1: Zero phase shift between internal PWM signals

- INTPWM:

  0: External PWM inputs are used.

  1: Internal PWM inputs are used.

- 2PH:

  0: Single phase, two-channel configuration

  1: Dual phase configuration

- LH:

  This bit is latched high when the LH pin is set high. The LH bit remains high until this bit is written back to zero through SPI (the LH pin cannot set this bit to zero). If the LH bit is high, the LH registers are used to control the logic instead of the normal registers. The part comes out of LH mode when LH pin is pulled low and the LH bit is written to 0.

It is recommended that the LH bit always be written with a ‘1’ during normal programming. This will ensure that a true limp-home event triggered by LH pin is captured.

- CHxHG:

  0: The error-amp of the associated channel is set to low gain.

  1: The error-amp of the associated channel is set to high gain.

- CHxCV:

  0: The associated channel is set in CC mode.

  1: The associated channel is set in CV mode.

7.6.3 CFG2 Register

Configuration register 2

表 7-5. CFG2 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
02h	**CFG2**	CH2LEB	CH1LEB	RSVD	RSVD	CH2FILT1	RSVD	RSVD	CH1FILT1	00000000

- CHxLEB:

  0: Short Leading Edge Blanking

  1: Long Leading Edge Blanking

- CHxFILT1: ILIM comparator filter

7.6.4 SWDIV Register

SWDIV register holds the divider value associated with dividing down the main clock to generate the channel clocks (switching frequency f_{SW}).

表 7-6. SWDIV Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
03h	**SWDIV**	RSVD	RSVD	RSVD	RSVD	CH2DIV1:0		CH1DIV1:0		00000000

- CHxDIV:

  00: Division = 2. $CHx_{CLK} = f_{CLKM} / 2$

  01: Division = 4. $CHx_{CLK} = f_{CLKM} / 4$

  10: Division = 8. $CHx_{CLK} = f_{CLKM} / 8$

  11: Division = 8. $CHx_{CLK} = f_{CLKM} / 8$

7.6.5 ISLOPE Register

The CHxISLP in ISLOPE register programs the CHx_Islope current into a 5-kΩ resistor shown in 图 7-9, which generates a slope compensation ramp with the magnitude of $V_{SLP(PK)}$ = CHx_Islope × 5 kΩ.

表 7-7. ISLOPE Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
04h	**ISLOPE**	RSVD	CH2ISLP2:0			RSVD	CH1ISLP2:0			01010101

- CHxISLP:

  000: $V_{SLP(PK)}$ = 0 mV

  001: $V_{SLP(PK)}$ = 50 mV

  010: $V_{SLP(PK)}$ = 100 mV

011: $V_{SLP(PK)}$ = 150 mV

100: $V_{SLP(PK)}$ = 200 mV

101: $V_{SLP(PK)}$ = 250 mV

110: $V_{SLP(PK)}$ = 300 mV

111: $V_{SLP(PK)}$ = 350 mV

7.6.6 FM Register

FM contains the Frequency Modulation configuration bits.

表 7-8. FM Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
05h	**FM**	RSVD	RSVD	FMMAG1:0		FMFREQ3:0				00000101

- The CLK_M frequency is varied by a percentage defined by FMMAG:

  00: Frequency modulation is disabled.

  01: The modulation magnitude is set to ±3.75%.

  10: The modulation magnitude is set to ±7.5%.

  11: The modulation magnitude is set to ±15%.

- The FMFREQ programs a division factor applied to CLK_M that sets the frequency modulation:

  0000: FM frequency is 1÷4096 of CLK_M frequency.

  0001: FM frequency is 1÷3584 of CLK_M frequency.

  0010: FM frequency is 1÷3072 of CLK_M frequency.

  0011: FM frequency is 1÷2560 of CLK_M frequency.

  0100: FM frequency is 1÷2048 of CLK_M frequency.

  0101: FM frequency is 1÷1536 of CLK_M frequency.

  0110: FM frequency is 1÷1024 of CLK_M frequency.

  0111: FM frequency is 1÷512 of CLK_M frequency.

  1000: FM frequency is 1÷256 of CLK_M frequency.

  1001: FM frequency is 1÷128 of CLK_M frequency.

  1010: FM frequency is 1÷64 of CLK_M frequency.

  1011: FM frequency is 1÷32 of CLK_M frequency.

  1100: FM frequency is 1÷16 of CLK_M frequency.

  1101: FM frequency is 1÷8 of CLK_M frequency.

  1110: Frequency modulation is disabled.

  1111: Frequency modulation is disabled.

7.6.7 SOFTSTART Register

The SOFTSTART register determines the division factor to be applied to the input clock of the soft-start 8-bit ramp counter.

表 7-9. SOFTSTART Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
06h	SOFTSTART	CH2SS3:0				CH1SS3:0				01110111

- CHxSS:

  0000: Soft-start is disabled.

  0001: Division factor = 2

  0010: Division factor = 4

  0011: Division factor = 6

  0100: Division factor = 8

  0101: Division factor = 12

  0110: Division factor = 16

  0111: Division factor = 20

  1000: Division factor = 26

  1001: Division factor = 32

  1010: Division factor = 38

  1011: Division factor = 46

  1100: Division factor = 54

  1101: Division factor = 64

  1110: Division factor = 80

  1111: Division factor = 100

If 2PH is set to '1', only CH1 parameter is used.

7.6.8 CH1IADJ Register

CH1IADJ register programs the 8-bit IADJ DAC for the channel-1. If CH1IADJ ≤ 8, channel-1 is turned off. The DAC output can be set from 85 mV (code 9) to 2.4 V (code 255).

表 7-10. CH1IADJ Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
07h	CH1IADJ	CH1IADJ7:0								00000000

7.6.9 CH2IADJ Register

CH2IADJ register programs the 8-bit IADJ DAC for the channel 2. If CH2IADJ ≤ 8, channel-2 is turned off. The DAC output can be set from 85 mV (code 9) to 2.4 V (code 255).

表 7-11. CH2IADJ Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
08h	CH2IADJ	CH2IADJ7:0								00000000

If 2PH is set to '1', only CH1 parameter is used.

7.6.10 PWMDIV Register

PWMDIV register sets the clock divider for the internal PWM generator block.

表 7-12. PWMDIV Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
09h	PWMDIV	RSVD	RSVD	RSVD	RSVD	RSVD	PWMDIV2:0			00000001

- PWMDIV:

  000: $PWM_{CLK} = CLK_M \div 1$

  001: $PWM_{CLK} = CLK_M \div 2$

  010: $PWM_{CLK} = CLK_M \div 3$

  011: $PWM_{CLK} = CLK_M \div 4$

  100: $PWM_{CLK} = CLK_M \div 5$

  101: $PWM_{CLK} = CLK_M \div 6$

  110: $PWM_{CLK} = CLK_M \div 7$

  111: $PWM_{CLK} = CLK_M \div 8$

7.6.11 CH1PWML Register

CH1PWML register sets the eight LSBs of the PWM-width on a 10-bit counter for channel-1.

表 7-13. CH1PWML Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0Ah	CH1PWML	CH1PWM7:0								00000000

7.6.12 CH1PWMH Register

CH1PWMH register sets the two MSBs of the PWM-width on a 10-bit counter for channel-1.

表 7-14. CH1PWMH Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0Bh	CH1PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH1PWM9:8		00000000

7.6.13 CH2PWML Register

CH2PWML register sets the eight LSBs of the PWM-width on a 10-bit counter for channel-2.

表 7-15. CH2PWML Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0Ch	CH2PWML	CH2PWM7:0								00000000

7.6.14 CH2PWMH Register

CH2PWMH register sets the two MSBs of the PWM-width on a 10-bit counter for channel-2.

表 7-16. CH2PWMH Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0Dh	CH2PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH2PWM9:8		00000000

7.6.15 ILIM Register

ILIM register configures the ILIM event counter and the $V_{ILIM(THR)}$ of channel-1 and channel-2.

表 7-17. ILIM Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0Eh	ILIM	CH2ILIMCNT1:0		CH1ILIMCNT1:0		CH2ILIM1:0		CH1ILIM1:0		00001111

ILIM event counter counts the number of ILIM fault events before disabling the associated channel completely or initiating the ILIM Fault Timer.

- CHxILIMCNT:

  00: ILIM event counter threshold = 1

  01: ILIM event counter threshold = 4

  10: ILIM event counter threshold = 16

  11: ILIM event counter threshold = 32

- The current limit threshold voltage of the associated channel is set by CHxILIM:

  00: $V_{ILIM(THR)}$ = 75 mV

  01: $V_{ILIM(THR)}$ = 100 mV

  10: $V_{ILIM(THR)}$ = 150 mV

  11: $V_{ILIM(THR)}$ = 250 mV

7.6.16 IFT Register

ILIM Fault Timer register, IFT, determines the maximum count value of a 6-bit counter used for the ILIM Fault Timer. The clock for the ILIM Fault Timer is the CHx_{CLK}.

表 7-18. IFT Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0Fh	IFT	RSVD	RSVD	RSVD	RSVD	CH2IFT1:0		CH1IFT1:0		00001010

- CHxIFT:

  00: ILIM Fault Timer maximum count = 4

  01: ILIM Fault Timer maximum count = 8

  10: ILIM Fault Timer maximum count = 16

  11: ILIM Fault Timer maximum count = 32

If 2PH is set to '1', only CH1 parameters are used and only ILIM Fault Timer 1 is active. In this case, ILIM Fault Timer 1 affects both channels.

7.6.17 MFT Register

Main Fault Timer register, MFT, determines the maximum count value of a 14-bit counter, used for the Main Fault Timer. The clock for the MFT is the CHx_{CLK}.

表 7-19. MFT Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
10h	MFT	CH2MFT3:0				CH1MFT3:0				10011001

- CHxMFT:

  0000: Main Fault Timer maximum count = 0 (Main Fault Timer is disabled)

  0001: Main Fault Timer maximum count = 1000

  0010: Main Fault Timer maximum count = 1500

  0011: Main Fault Timer maximum count = 2000

  0100: Main Fault Timer maximum count = 2500

  0101: Main Fault Timer maximum count = 3000

0110: Main Fault Timer maximum count = 3500

0111: Main Fault Timer maximum count = 4000

1000: Main Fault Timer maximum count = 5000

1001: Main Fault Timer maximum count = 6000

1010: Main Fault Timer maximum count = 7000

1011: Main Fault Timer maximum count = 8000

1100: Main Fault Timer maximum count = 10000

1101: Main Fault Timer maximum count = 12000

1110: Main Fault Timer maximum count = 14000

1111: Main Fault Timer maximum count = 16383

If 2PH is set to '1', only CH1 parameters are used and only Fault Timer 1 is active. In this case, Fault Timer 1 affects both channels.

7.6.18 FLT1 Register (read only)

FLT1 register bits are set if a selected fault shown in 表 7-20 occurs. Reading this register clears the bits that are set, if the associated faults no longer exist. Note that the clearing of the bits happens at the end of the read response SPI transfer, not at the end of the read command SPI transfer.

表 7-20. FLT1 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
11h	**FLT1**	RTO	RSVD	PC	TW	CH2OV	CH1OV	CH2UV	CH1UV	read

- RTO: RT pin is open.
- PC: Power Cycled bit; This bit is set at power up and upon POR. Neither of the two channels can be enabled while this bit is set. The PC bit must be cleared before the soft-start DAC state machine can progress and the channels can be turned on. To clear the PC bit, FLT1 register should be read. The clearing of the Fault-Read-bits happens at the end of the SPI transfer read response, not at the end of the read command.
- TW: Thermal Warning bit
- CHxOV: Output overvoltage fault (CH2OV is disabled if 2PH is set to '1').
- CHxUV: Output undervoltage fault (CH2UV is disabled if 2PH is set to '1').

7.6.19 FLT2 Register (read only)

FLT2 register bits are set if a selected fault shown in 表 7-21 occurs. Reading this register clears the bits that are set, if the associated faults no longer exist. Note that the clearing of the bits happens at the end of the read response SPI transfer, not at the end of the read command SPI transfer.

表 7-21. FLT2 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
12h	**FLT2**	CH2UC	CH1UC	CH2OC	CH1OC	CH2ILIM	CH1ILIM	CH2ISO	CH1ISO	read

- CHxUC: CHx output current less than 0.5 times of the set value (CH2UC is disabled if 2PH is set to '1').
- CHxOC: CHx output current more then 1.5 times of the set value (CH2OC is disabled if 2PH is set to '1').
- CHxILIM: ILIM bit is only set after CHxILIMCNT counter has reached the programmed value.
- CHxISO: Open pin detection on ISN pins

7.6.20 FEN1 Register

Fault Enable-1 register, FEN1, determines which of the faults shown in 表 7-22 are enabled. If a fault enable is set to '1', it is enabled and it will affect the operation of the associated channel. The faults that are disabled will not affect the CHx fault pin output.

表 7-22. FEN1 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
13h	FEN1	CH2RFEN	CH1RFEN	CH2FBOEN	CH1FBOEN	CH2OVEN	CH1OVEN	CH2UVEN	CH1UVEN	00111100

- Ramp Fault Enable, CHxRFEN:

  0: Disables the CHxUV fault from affecting channel operation before or during the Soft-start ramp. In CV mode, CHx ILIM neither triggers the IFT, nor turns off the channel before or during the Soft-start ramp. Note that the cycle-by-cycle current limit is still active.

  1: All the enabled faults are active before or during the Soft-start ramp.
- CHxFBOEN: if set to '1', FB pin open fault is enabled. There are no associated fault read bits for this fault.
- CHxOVEN: if set to '1', output overvoltage fault is enabled. CH2OV fault is disabled if 2PH bit is set to '1'.
- CHxUVEN: if set to '1', output undervoltage fault is enabled. CH2UV fault is disabled if 2PH bit is set to '1'.

If 2PH is set to '1', only CH1 parameter is used.

7.6.21 FEN2 Register

Fault Enable-2 register, FEN2, determines which of the faults shown in 表 7-23 are enabled. If a fault enable is set to '1', it is enabled and it will affect the operation of the associated channel. The faults that are disabled will not affect the CHx fault pin output.

表 7-23. FEN2 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
14h	FEN2	OVOPT	RSVD	CH2OCEN	CH1OCEN	CH2ILIMEN	CH1ILIMEN	CH2ISOEN	CH1ISOEN	00001111

- OVOPT: if set to '1', the OV fault is only captured by the analog block and the digital state machine is not affected by the overvoltage fault.
- CHxOCEN: if set to '1', output overcurrent fault is enabled.
- CHxILIMEN: if set to '1', ILIM fault is enabled.
- CHxISOEN: if set to '1', ISN open pin fault is enabled.

If 2PH is set to '1', only CH1 parameter is used.

7.6.22 FLATEN Register

Fault Latch Enable register, FLATEN, determines which of the faults shown in 表 7-24 are latched faults. A latched fault turns off the channel. In this case, to turn the channel back on, the CHxEN should be set to '1' in 表 7-3 through a SPI write command.

表 7-24. FLATEN Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
15h	FLATEN	CH2ILIMFL	CH1ILIMFL	CH2OCFL	CH1OCFL	CH2OVFL	CH1OVFL	CH2UVFL	CH1UVFL	00000000

- CHxILIMFL: if set to '1', ILIM fault is set to a latched fault.
- CHxOCFL: if set to '1', output overcurrent fault is set to a latched fault.
- CHxOVFL: if set to '1', output overvoltage fault is set to a latched fault.
- CHxUVFL: if set to '1', output undervoltage fault is set to a latched fault.

If 2PH is set to '1', only CH1 parameter is used.

7.6.23 OV Register

CHxOV programs a 3-bit DAC to set the OV threshold relative to the VFB_{REF}.

表 7-25. OV Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
16h	OV	RSVD	CH2OV2:0			RSVD	CH1OV2:0			00100010

- CHxOV:

  000: $OV_{THR} = VFB_{REF} \times (1.000)$

  001: $OV_{THR} = VFB_{REF} \times (1.025)$

  010: $OV_{THR} = VFB_{REF} \times (1.050)$

  011: $OV_{THR} = VFB_{REF} \times (1.075)$

  100: $OV_{THR} = VFB_{REF} \times (1.100)$

  101: $OV_{THR} = VFB_{REF} \times (1.125)$

  110: $OV_{THR} = VFB_{REF} \times (1.150)$

  111: $OV_{THR} = VFB_{REF} \times (1.200)$

If 2PH is set to '1', only CH1 parameter is used.

7.6.24 LHCFG Register

LHCFG is the Limp-Home Configuration register. The settings in this register are applied when LH pin is set high.

表 7-26. LHCFG Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
17h	LHCFG	LHPWMPH	LHINTPWM	LHCH2MAXDEN	LHCH1MAXDEN	LHCH2PDRVEN	LHCH1PDRVEN	LHCH2EN	LHCH1EN	00111100

- LHPWMPH:

  0: Phase shift of 180° between internal PWM signals

  1: Zero phase shift between internal PWM signals

- LHINTPWM:

  0: External PWM inputs are used.

  1: Internal PWM inputs are used.

- LHCHxMAXDEN:

  0: Maximum duty cycle for the associated channel is disabled.

  1: Maximum duty cycle for the associated channel is enabled.

- LHCHxPDRVEN:

  0: The associated channel PFET driver is disabled.

  1: The associated channel PFET driver is enabled.

- LHCHxEN:

  0: The associated channel is disabled.

  1: The associated channel is enabled.

If 2PH is set to '1', only CH1 parameter is used.

7.6.25 LHCH1IADJ Register

LHCH1IADJ register programs the 8-bit IADJ DAC for channel-1. The settings in this register are applied when LH pin is set high. If LHCH1IADJ ⩽ 8, the channel-1 is turned off. The DAC output can be set from 85 mV (code 9) to 2.4 V (code 255).

表 7-27. LHCH1IADJ Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
18h	LHCH1IADJ	LHCH1IADJ7:0								00000000

7.6.26 LHCH2IADJ Register

LHCH2IADJ register programs the 8-bit IADJ DAC for channel-2. The settings in this register are applied when LH pin is set high. If LHCH2IADJ ⩽ 8, the channel-2 is turned off. The DAC output can be set from 85 mV (code 9) to 2.4 V (code 255).

表 7-28. LHCH2IADJ Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
19h	LHCH2IADJ	LHCH2IADJ7:0								00000000

If 2PH is set to '1', only CH1 parameter is used.

7.6.27 LHCH1PWML Register

LHCH1PWML register sets the eight LSBs of the PWM-width on a 10-bit counter for channel-1. The settings in this register are applied when LH pin is set high.

表 7-29. LHCH1PWML Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
1Ah	LHCH1PWML	LHCH1PWM7:0								00000000

7.6.28 LHCH1PWMH Register

LHCH1PWMH register sets the two MSBs of the PWM-width on a 10-bit counter for channel-1. The settings in this register are applied when LH pin is set high.

表 7-30. LHCH1PWMH Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
1Bh	LHCH1PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LHCH1PWM9:8		00000000

7.6.29 LHCH2PWML Register

LHCH2PWML register sets the eight LSBs of the PWM-width on a 10-bit counter for channel-2. The settings in this register are applied when LH pin is set high.

表 7-31. LHCH2PWML Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
1Ch	LHCH2PWML	LHCH2PWM7:0								00000000

If 2PH is set to '1', only CH1 parameter is used.

7.6.30 LHCH2PWMH Register

LHCH2PWMH register sets the two MSBs of the PWM-width on a 10-bit counter for channel-2. The settings in this register are applied when LH pin is set high.

表 7-32. LHCH2PWMH Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
1Dh	LHCH2PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LHCH2PWM9:8		00000000

If 2PH is set to '1', only CH1 parameter is used.

7.6.31 LHILIM Register

LHILIM register configures the ILIM event counter and the $V_{ILIM(THR)}$ of channel-1 and channel-2. The settings in this register are applied when LH pin is set high.

表 7-33. LHILIM Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
1Eh	LHILIM	LHCH2ILIMCNT1:0		LHCH1ILIMCNT1:0		LHCH2ILIM1:0		LHCH1ILIM1:0		00001111

LHILIM-counter counts the number of ILIM fault events before disabling the associated channel completely or initiating the ILIM Fault Timer.

- LHCHxILIMCNT:

  00: ILIM event counter threshold = 1

  01: ILIM event counter threshold = 4

  10: ILIM event counter threshold = 16

  11: ILIM event counter threshold = 32

- The current limit threshold voltage of the associated channel is set by LHCHxILIM:

  00: $V_{ILIM(THR)}$ = 75 mV

  01: $V_{ILIM(THR)}$ = 100 mV

  10: $V_{ILIM(THR)}$ = 150 mV

  11: $V_{ILIM(THR)}$ = 250 mV

7.6.32 LHIFT Register

LHIFT register determines the maximum count value of a 6-bit counter used for the ILIM Fault Timer. The clock for the ILIM Fault Timer is the CHx_{CLK}. The settings in this register are applied when LH pin is set high.

表 7-34. LHIFT Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
1Fh	LHIFT	RSVD	RSVD	RSVD	RSVD	LHCH2IFT1:0		LHCH1IFT1:0		00001010

- LHCHxIFT:

  00: ILIM Fault Timer maximum count = 4

  01: ILIM Fault Timer maximum count = 8

  10: ILIM Fault Timer maximum count = 16

  11: ILIM Fault Timer maximum count = 32

If 2PH is set to '1', only CH1 parameters are used and only ILIM Fault Timer 1 is active. In this case, ILIM Fault Timer-1 affects both channels.

7.6.33 LHMFT Register

LHMFT register determines the maximum count value of a 14-bit counter, used for the Main Fault Timer. The clock for the MFT is the CHx_{CLK}. The settings in this register are applied when LH pin is set high.

表 7-35. LHMFT Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
20h	LHMFT	LHCH2MFT3:0				LHCH1MFT3:0				10011001

- LHCHxMFT:

  0000: Main Fault Timer maximum count = 0 (Main Fault Timer is disabled)

  0001: Main Fault Timer maximum count = 1000

  0010: Main Fault Timer maximum count = 1500

  0011: Main Fault Timer maximum count = 2000

  0100: Main Fault Timer maximum count = 2500

  0101: Main Fault Timer maximum count = 3000

  0110: Main Fault Timer maximum count = 3500

  0111: Main Fault Timer maximum count = 4000

  1000: Main Fault Timer maximum count = 5000

  1001: Main Fault Timer maximum count = 6000

  1010: Main Fault Timer maximum count = 7000

  1011: Main Fault Timer maximum count = 8000

  1100: Main Fault Timer maximum count = 10000

  1101: Main Fault Timer maximum count = 12000

  1110: Main Fault Timer maximum count = 14000

  1111: Main Fault Timer maximum count = 16383

If 2PH is set to '1', only CH1 parameters are used and only Fault Timer 1 is active. In this case, Fault Timer 1 affects both channels.

7.6.34 LHFEN1 Register

LHFEN1 register determines which of the faults shown in 表 7-36 are enabled. If a fault enable is set to '1', it is enabled and it will affect the operation of the associated channel. The faults that are disabled will not affect the CHx fault pin output. The settings in this register are applied when LH pin is set high.

表 7-36. LHFEN1 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
21h	LHFEN1	LHCH2RFEN	LHCH1RFEN	LHCH2FBOEN	LHCH1FBOEN	LHCH2OVEN	LHCH1OVEN	LHCH2UVEN	LHCH1UVEN	00111100

- LHCHxRFEN:

  0: Disables the CHxUV fault from affecting channel operation before or during the Soft-start ramp. In CV mode, CHx ILIM neither triggers the IFT, nor turns off the channel before or during the Soft-start ramp. Note that the cycle-by-cycle current limit is still active.

  1: All the enabled faults are active before or during the Soft-start ramp.
- LHCHxFBOEN: if set to '1', FB pin open fault is enabled. There are no associated fault read bits for these faults.
- LHCHxOVEN: if set to '1', output overvoltage fault is enabled. CH2OV fault is disabled if 2PH bit is set to '1'.
- LHCHxUVEN: if set to '1', output undervoltage fault is enabled. CH2UV fault is disabled if 2PH bit is set to '1'.

If 2PH is set to '1', only CH1 parameter is used.

7.6.35 LHFEN2 Register

LHFEN2 register determines which of the faults shown in 表 7-37 are enabled. If a fault enable is set to '1', it is enabled and it will affect the operation of the associated channel. The faults that are disabled will not affect the CHx fault pin output. The settings in this register are applied when LH pin is set high.

表 7-37. LHFEN2 Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
22h	**LHFEN2**	RSVD	RSVD	LHCH2OCEN	LHCH1OCEN	LHCH2ILIMEN	LHCH1ILIMEN	LHCH2ISOEN	LHCH1ISOEN	00001111

- LHCHxOCEN: if set to '1', output overcurrent fault is enabled.
- LHCHxILIMEN: if set to '1', ILIM fault is enabled.
- LHCHxISOEN: if set to '1', ISN open pin fault is enabled.

If 2PH is set to '1', only CH1 parameter is used.

7.6.36 LHFLATEN Register

LHFLATEN register determines which of the faults shown in 表 7-38 are latched faults. A latched fault turns off the channel. In this case, to turn on the channel back on, the CHxEN should be set to '1' in 表 7-3 through a SPI write command. The settings in this register are applied when LH pin is set high.

表 7-38. LHFLATEN Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
23h	**LHFLATEN**	LHCH2ILIMFL	LHCH1ILIMFL	LHCH2OCFL	LHCH1OCFL	LHCH2OVFL	LHCH1OVFL	LHCH2UVFL	LHCH1UVFL	00000000

- LHCHxILIMFL: if set to '1', ILIM fault is set to a latched fault.
- LHCHxOCFL: if set to '1', output overcurrent fault is set to a latched fault.
- LHCHxOVFL: if set to '1', output overvoltage fault is set to a latched fault.
- LHCHxUVFL: if set to '1', output undervoltage fault is set to a latched fault.

If 2PH is set to '1', only CH1 parameter is used.

7.6.37 LHOV Register

LHCHxOV register programs a 3-bit DAC to set the OV threshold relative to the VFB_{REF}. The settings in this register are applied when LH pin is set high.

表 7-39. LHOV Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
24h	**LHOV**	RSVD	LHCH2OV2:0			RSVD	LHCH1OV2:0			00100010

- LHCHxOV:

  000: $OV_{THR} = VFB_{REF} \times (1.000)$

  001: $OV_{THR} = VFB_{REF} \times (1.025)$

  010: $OV_{THR} = VFB_{REF} \times (1.050)$

  011: $OV_{THR} = VFB_{REF} \times (1.075)$

  100: $OV_{THR} = VFB_{REF} \times (1.100)$

  101: $OV_{THR} = VFB_{REF} \times (1.125)$

  110: $OV_{THR} = VFB_{REF} \times (1.150)$

  111: $OV_{THR} = VFB_{REF} \times (1.200)$

If 2PH is set to '1', only CH1 parameter is used.

7.6.38 CAL Register

The CAL register includes calibration bits for the switch current sense circuitry.

表 7-40. CAL Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
25h	CAL	CH2CAL2:0			CH2GOFF	CH1CAL2:0			CH1GOFF	00000000

CHxCAL: Each channel has three calibration bits, which adds 2.5 mV of offset per bit (2.5 mV to 17.5 mV) to the switch current sense voltage threshold. The calibration bits can decrease the offset mismatch between the switch current sense of the two channels and improve the current sharing in two phase applications.

CHxGOFF: This bit turns off the associated channel, when set to "1".

•

7.6.39 RESET Register

Writing 0xC3 to the RESET register resets all writable registers to their default values. This register is write-only and reads from this register return 0. Note that a RESET command does not reset the PC bit in 表 7-20 to its power-on default value of '1'.

表 7-41. RESET Register

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
26h	RESET	RESET7:0								00000000

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information General Design Considerations

The TPS92682-Q1 can be configured both in CC and CV mode. In both cases, the following general design procedures are applicable.

8.1.1 Switching Frequency, f_{SW}

To set the switching frequency for each channel, refer to the *Oscillator* section.

8.1.2 Duty Cycle Considerations

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is derived using the expression:

Boost:

$$D = \frac{V_O - V_{IN}}{V_O} \tag{9}$$

Buck-Boost:

$$D = \frac{V_O}{V_O + V_{IN}} \tag{10}$$

The minimum duty cycle, D_{MIN}, and maximum duty cycle, D_{MAX}, are calculated by substituting maximum input voltage, $V_{IN(MAX)}$, and the minimum input voltage, $V_{IN(MIN)}$, respectively in the previous expressions. The minimum duty cycle achievable by the device is determined by the leading edge blanking period and the switching frequency. The maximum duty cycle is limited by the internal oscillator to 90% (typ) to allow for minimum off-time. It is necessary for the operating duty cycle to be within the operating limits of the device to ensure closed-loop regulation over the specified input and output voltage range.

8.1.3 Main Power MOSFET Selection

The power MOSFET is required to sustain the maximum switch node voltage, V_{SW}, and switch RMS current derived based on the converter topology. TI recommends a drain voltage V_{DS} rating of at least 10% greater than the maximum switch node voltage to ensure safe operation.

The worst case MOSFET RMS current for Boost and Buck-Boost topology depends on the maximum output power, $P_{O(MAX)}$, and is calculated for Boost in 方程式 11 and for Buck-Boost in 方程式 12.

$$I_{Q(RMS)} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} \times \sqrt{\left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right)} \tag{11}$$

$$I_{Q(RMS)} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} \times \sqrt{\left(1 + \frac{V_{IN(MIN)}}{V_{O(MIN)}}\right)} \tag{12}$$

Select a MOSFET with low total gate charge, Q_g, to minimize gate drive and switching losses.

8.1.4 Rectifier Diode Selection

A Schottky diode (when used as a rectifier) provides the best efficiency due to its low forward voltage drop and near-zero reverse recovery time. TI recommends a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance. It is important to understand the leakage current characteristics of the Schottky diode, especially at high operating temperatures as it impacts the overall converter operation and efficiency.

The diode power rating and package is selected based on the calculated current, the ambient temperature and the maximum allowable temperature rise.

8.1.5 Switch Current Sense Resistor

The switch current sense resistor, R_{IS}, is used to implement peak current mode control and to set the peak switch current limit. The value of R_{IS} is selected to protect the main switching MOSFET under fault conditions. R_{IS} can be calculated based on peak inductor current, $I_{L(PK)}$, and switch current limit threshold, $V_{ILIM(THR)}$.

$$R_{IS} = \frac{V_{ILIM(THR)}}{1.2 \times I_{L(PK)}} \tag{13}$$

In 方程式 13, 20% margin is considered for transient conditions.

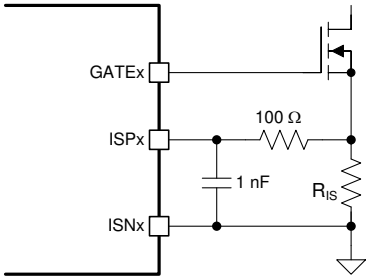


图 8-1. IS Input Filter

The use of a 1-nF and 100-Ω low-pass filter is optional. The recommended filter resistor value is less than 500 Ω to limit its influence on the internal slope compensation signal.

8.1.6 Slope Compensation

The magnitude of internal artificial ramp, V_{SLP}, is set by the ISLOPE register shown in 表 7-7. The slope of the artificial ramp is V_{SLP} / T_{SW}, where T_{SW} is the switching period. 方程式 14 shows a choice of V_{SLP}, which is sufficient for the stability of the Boost or Buck-Boost topologies over the entire range of duty-cycle D. In practice, slightly smaller V_{SLP} can be selected for a given application. The value of V_{SLP} in 方程式 14 is determined by the inductor, L, the switch current sense resistor, R_{IS}, output voltage, V_O, and the switching period, T_{SW}.

$$V_{SLP} \geq \frac{V_O}{2 \times L} \times R_{IS} \times T_{SW} \tag{14}$$

8.1.7 Soft Start

As described in the *Soft Start* section, the ramp can be programmed using *SOFTSTART Register*. The soft-start time, t_{SS}, is the time for the internal digital ramp to complete the 256 counts (from 0-V to 2.8-V typ). Program the *SOFTSTART Register* with a SSx_{DIV} that is found using 方程式 15. The maximum time, t_{SS}, for each channel is related to the maximum value of SSx_{DIV} in *SOFTSTART Register*.

$$SSx_{DIV} \geq \frac{t_{SS} \times f_{SW}}{256} \tag{15}$$

8.2 Application Information CC Mode

The TPS92682-Q1 controller, when configured in CC mode, is suitable for implementing step-up or step-down LED driver topologies including BOOST, BUCK-BOOST, SEPIC, and so forth. This section presents the design process for the BOOST and BUCK-BOOST converters. The expressions derived for the BUCK-BOOST topology can be altered to select components for a 1:1 coupled-inductor SEPIC converter. The design procedure can be easily adapted for FLYBACK and similar converter topologies.

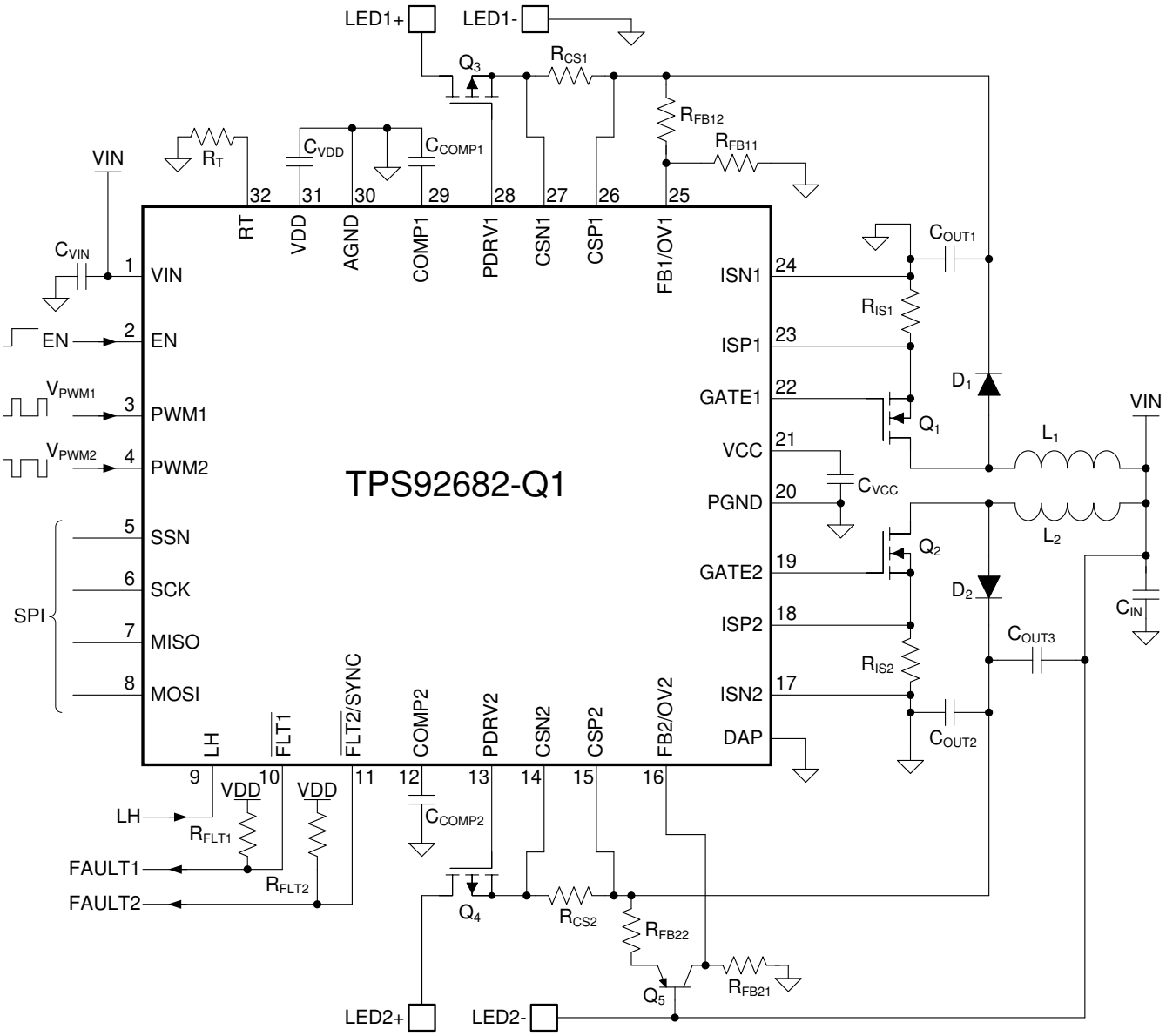


图 8-2. Two-Channel LED Driver, BOOST, and BUCK-BOOST Topology (CC mode)

8.2.1 Inductor Selection

The choice of inductor sets the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) boundary condition. Therefore, one approach of selecting the inductor value is by deriving the relationship between the output power corresponding to CCM-DCM boundary condition, $P_{O(BDRY)}$, and inductance, L. This approach ensures CCM operation in battery-powered LED driver applications that are required to support different LED string configurations with a wide range of programmable LED current set points. The CCM-DCM boundary condition can be estimated either based on the lowest LED current and the lowest output voltage requirements for a given application or as a fraction of maximum output power, $P_{O(MAX)}$.

$$P_{O(BDRY)} \le I_{LED(MIN)} \times V_{O(MIN)} \quad (16)$$

$$\frac{P_{O(MAX)}}{4} \le P_{O(BDRY)} \le \frac{P_{O(MAX)}}{2} \quad (17)$$

Boost:

$$L = \frac{V_{IN}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_O}\right) \quad (18)$$

Buck-Boost:

$$L = \frac{1}{2 \times P_{O(BDRY)} \times f_{SW} \times \left(\frac{1}{V_O} + \frac{1}{V_{IN}}\right)^2} \quad (19)$$

Select an inductor with a saturation current rating greater than the peak inductor current, $I_{L(PK)}$, at the maximum operating temperature.

Boost:

$$I_{L(PK)} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} + \frac{V_{IN(MIN)}}{2 \times L \times f_{SW}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \quad (20)$$

Buck-Boost:

$$I_{L(PK)} = P_{O(MAX)} \times \left(\frac{1}{V_{O(MIN)}} + \frac{1}{V_{IN(MIN)}}\right) + \frac{V_{O(MIN)} \times V_{IN(MIN)}}{2 \times L \times f_{SW} \times \left(V_{O(MIN)} + V_{IN(MIN)}\right)} \quad (21)$$

8.2.2 Output Capacitor Selection

The output capacitors are required to attenuate the discontinuous or large ripple output current, and achieve the desired peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, r_D, and the switching frequency, f_{SW}.The capacitance required for the target LED ripple current can be calculated based on following equations.

Boost:

$$C_{OUT} = \frac{I_{LED(MAX)}}{\Delta i_{LED(PP)} \times f_{SW} \times r_D} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \quad (22)$$

Buck-Boost:

$$C_{OUT} = \frac{I_{LED(MAX)} \times V_{O(MIN)}}{\Delta i_{LED(PP)} \times f_{SW} \times r_{D(MIN)} \times \left(V_{O(MIN)} + V_{IN(MIN)}\right)} \quad (23)$$

When choosing the output capacitors, it is important to consider the ESR and the ESL characteristics as they directly impact the LED current ripple. Ceramic capacitors are the best choice due to their low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and the DC bias operating conditions. TI recommends an X7R dielectric with voltage rating greater than maximum LED stack voltage. An aluminum electrolytic capacitor can be used in parallel with ceramic capacitors to provide bulk energy storage.

The aluminum capacitors must have necessary RMS current and temperature ratings to ensure prolonged operating lifetime. The minimum allowable RMS output capacitor current rating, $I_{COUT(RMS)}$, can be approximated as:

Boost and Buck-Boost:

$$I_{COUT(RMS)} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (24)$$

8.2.3 Input Capacitor Selection

The input capacitor, C_{IN}, reduces the input voltage ripple and stores energy to supply input current during input voltage or PWM dimming transients. The series inductor in the Boost and SEPIC topologies provides continuous input current and requires a smaller input capacitor to achieve desired input voltage ripple, $\Delta v_{IN(PP)}$. The Buck-Boost and Flyback topologies have discontinuous input current and require a larger capacitor to achieve the same input voltage ripple. Based on the switching frequency, f_{SW}, and the maximum duty cycle, D_{MAX}, the input capacitor value can be calculated for each channel as follows:

Boost:

$$C_{IN} = \frac{V_{IN(MIN)}}{8 \times L \times f_{SW}^2 \times \Delta v_{IN(PP)}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \quad (25)$$

Buck-Boost:

$$C_{IN} = \frac{P_{O(MAX)}}{f_{SW} \times \Delta v_{IN(PP)} \times V_{IN(MIN)}} \quad (26)$$

X7R dielectric-based ceramic capacitors are the best choice due to their low ESR, high ripple current rating, and good temperature performance. For applications using PWM dimming, TI recommends large bulk capacitors in addition and in parallel to the ceramic capacitors to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

Decouple the VIN pin with a 0.1-µF ceramic capacitor, placed as close as possible to the device, and optionally in series with a 10-Ω resistor to create a 160-kHz low-pass filter.

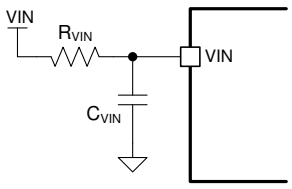


图 8-3. VIN Filter

8.2.4 Programming LED Current

The LED current can be programmed to match the LED string configuration by writing an 8-bit value to the *CH1IADJ Register* and the *CH2IADJ Register*. 方程式 27 shows the relation between the programmed LED current I_{LED}, the register CHxIADJ, and the LED current sense resistor, R_{CS}.

$$I_{LED} = \frac{CHxIADJ \times 2.4}{14 \times R_{CSx} \times 255} \quad (27)$$

8.2.5 Feedback Compensation

The loop gain T(s) is the product of the converter transfer function $G_{ivc}(s)$ (方程式 28) and the feedback transfer function $G_c(s)$.

Using a first-order approximation, the converter transfer function can be modeled as a single pole created by the output capacitor and the LED string dynamic resistance, r_D. In the boost and buck-boost topologies, the transfer function has a right half-plane zero created by the inductor, and the DC output current I_{LED}. The ESR of the output capacitor is neglected in this analysis.

$$G_{ivc}(s) = \frac{\hat{i}_{LED}}{\hat{v}_{COMP}} = G_o \times \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \tag{28}$$

表 8-1 summarizes the expression for the small-signal model parameters.

表 8-1. Small-Signal Model Parameters for CC Operation

	DC GAIN (G_0)	POLE FREQUENCY (ω_P)	ZERO FREQUENCY (ω_Z)
Boost	$\frac{(1-D)\times V_O}{R_{IS}\times(V_O + (r_D \times I_{LED}))}$	$\frac{V_O + (r_D \times I_{LED})}{V_O \times r_D \times C_{OUT}}$	$\frac{V_O \times (1-D)^2}{L \times I_{LED}}$
Buck-Boost	$\frac{(1-D)\times V_O}{R_{IS}\times(V_O + (D \times r_D \times I_{LED}))}$	$\frac{V_O + (D \times r_D \times I_{LED})}{V_O \times r_D \times C_{OUT}}$	$\frac{V_O \times (1-D)^2}{D \times L \times I_{LED}}$

The feedback transfer function includes the current sense resistor and the loop compensation of the transconductance amplifier. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. A simple capacitor, C_{COMP}, from COMPx to GND (as shown in 图 8-4) provides integral compensation and creates a pole at the origin. Alternatively, a network of R_{COMP}, C_{COMP}, and C_{HF}, shown in 图 8-5, can be used to implement Proportional-Integral (PI) compensation to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

The feedback transfer function is defined as follows.

Feedback transfer function with integral compensation:

$$G_C(s) = -\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14 \times g_M \times R_{CS}}{s \times C_{COMP}} \tag{29}$$

Feedback transfer function with proportional integral compensation:

$$G_C(s) = -\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14 \times g_M \times R_{CS}}{s \times (C_{COMP} + C_{HF})} \times \frac{(1 + s \times R_{COMP} \times C_{COMP})}{\left(1 + s \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)\right)} \tag{30}$$

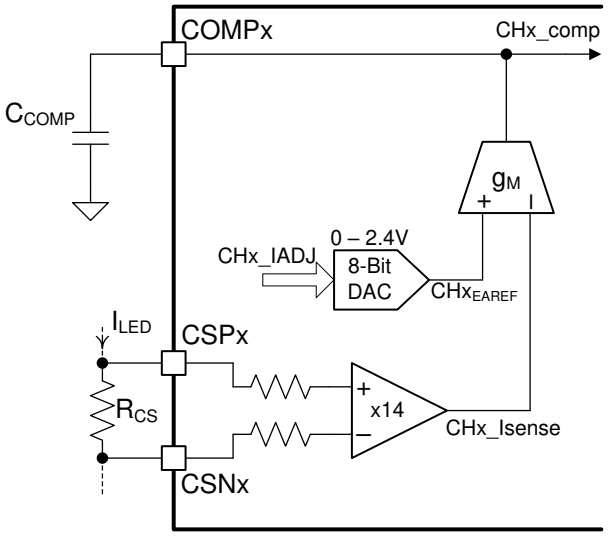


图 8-4. Integral Compensator

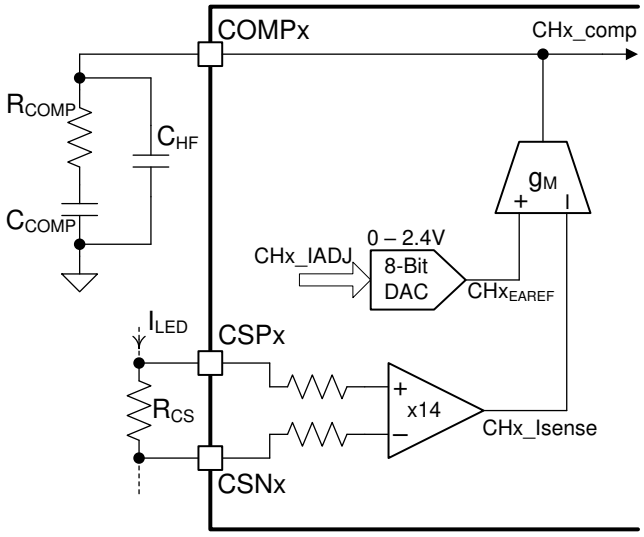


图 8-5. Proportional Integral Compensator

The pole at the origin minimizes output steady-state error. High bandwidth is achieved with the PI compensator by introducing a phase lead using a low-frequency zero. Use the following expressions to calculate the compensation network.

- BOOST and BUCK-BOOST with an Integral Compensator:

$$C_{COMP} = \frac{20 \times g_M \times R_{CS} \times G_0}{\omega_P} \quad (31)$$

- BOOST and BUCK-BOOST with a Proportional-Integral Compensator:

$$C_{COMP} = \frac{14 \times g_M \times R_{CS} \times G_0}{\sqrt{\omega_P \times \omega_Z}} \quad (32)$$

$$C_{HF} < \frac{C_{COMP}}{100} \quad (33)$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}} \quad (34)$$

The above compensation values are calculated to provide reasonable phase margin (> 45°) and bandwidth. In practice, the above values can be modified for desired dynamic performance (for example: PWM dimming rise/fall-time or overshoot/undershoot).

8.2.6 Overvoltage and Undervoltage Protection

In BOOST and SEPIC topologies, the Overvoltage threshold is programmed using a resistor divider, R_{FBx1} and R_{FBx2}, from the output voltage V_O to GND. If the LEDs are referenced to a potential other than GND, as in the BUCK-BOOST, the output voltage is sensed and translated to ground by using a PNP transistor and level-shift resistors, as shown in 图 8-2 for the channel-2. The Overvoltage turnoff threshold, $V_{O(OV)}$, is:

Boost:

$$V_{O(OV)} = V_{OV(THR)} \times \left(\frac{R_{FB1} + R_{FB2}}{R_{FB1}} \right) \quad (35)$$

Buck and Buck-Boost:

$$V_{O(OV)} = V_{OV(THR)} \times \frac{R_{FB2}}{R_{FB1}} + 0.7 \quad (36)$$

In CC mode, $V_{OV(THR)}$ = 1.24 V (typ), when CHxOV register is set to 000.

The Overvoltage hysteresis, $V_{OV(HYS)}$, is:

$$V_{OV(HYS)} = I_{OV(HYS)} \times R_{FB2} \quad (37)$$

where

- $I_{OV(HYS)}$ is 20 µA (typ.)

The corresponding undervoltage fault threshold, $V_{O(UV)}$, is:

$$V_{O(UV)} = 0.05 \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \quad (38)$$

8.2.7 Series P-Channel MOSFET Selection

In the applications with PWM dimming, the device requires a P-channel MOSFET placed in series with the LED load. Select a P-channel MOSFET with gate-to-source voltage rating of 10 V or higher and with a drain-to-source breakdown voltage rating greater than the output voltage. Ensure that the drain current rating of the P-channel MOSFET exceeds the programmed LED current by at least 10%.

It is important to consider the FET input capacitance and on-resistance as it impacts the accuracy and efficiency of the LED driver. TI recommends a FET with lower input capacitance and gate charge to minimize the errors caused by rise and fall times when PWM dimming at low duty cycles is applied.

8.2.8 Programming Example for Two-Channel CC Mode

图 8-6 shows an example for initialization of the TPS92682 registers for the two-channel CC BOOST application.

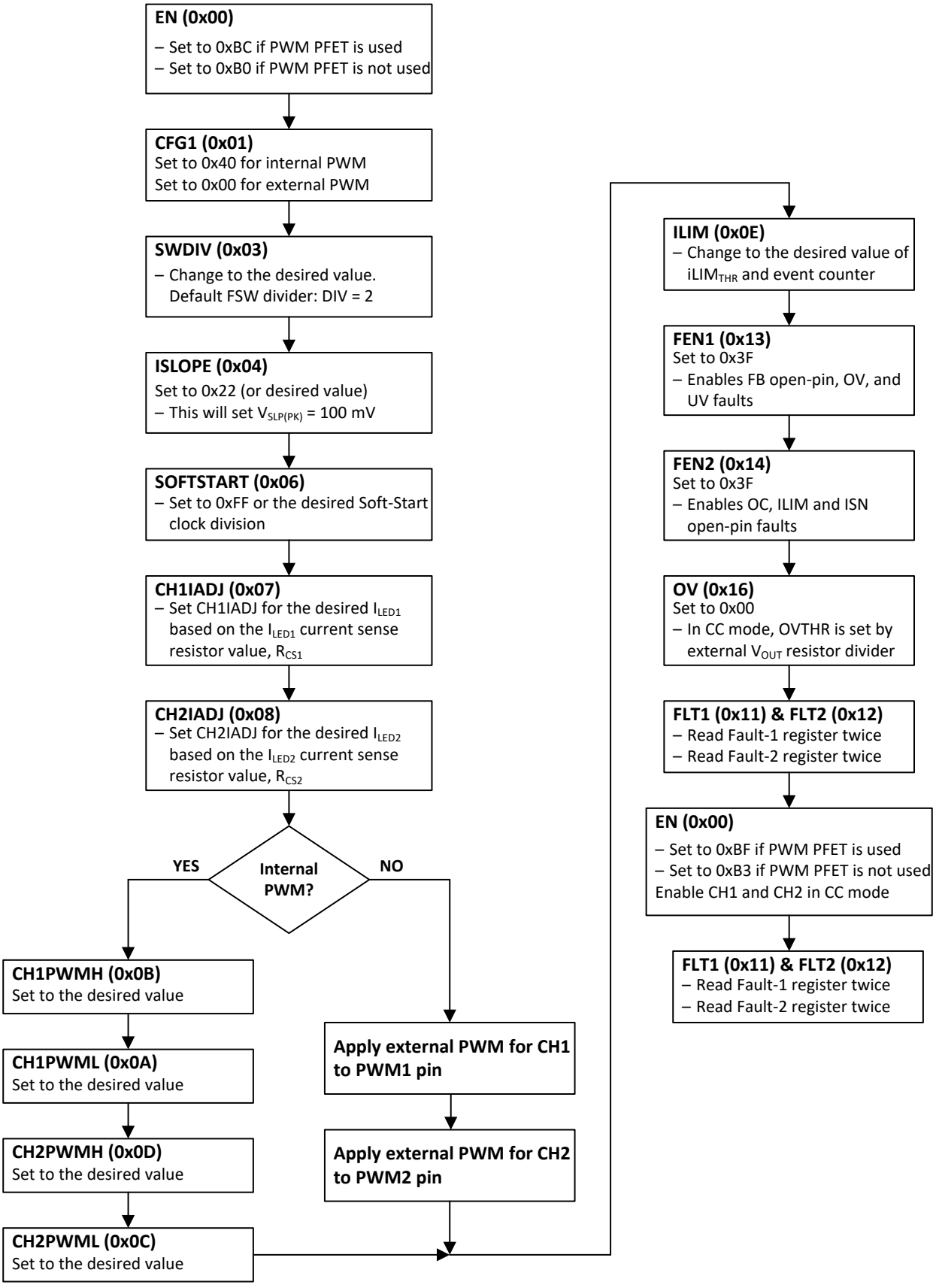


图 8-6. Register Programing for Two-Channel CC BOOST

8.3 Typical Application CV Mode

The TPS92682-Q1 controller, when configured in CV mode, is suitable for implementing step-up voltage regulator topologies including BOOST, SEPIC, and so forth. The device can also be configured in two-phase mode for efficiency optimization and reduced input and output current ripple. This section presents the design process for the BOOST voltage regulator. The design procedure can be easily adapted for other converter topologies, like 1:1 coupled-inductor SEPIC converter.

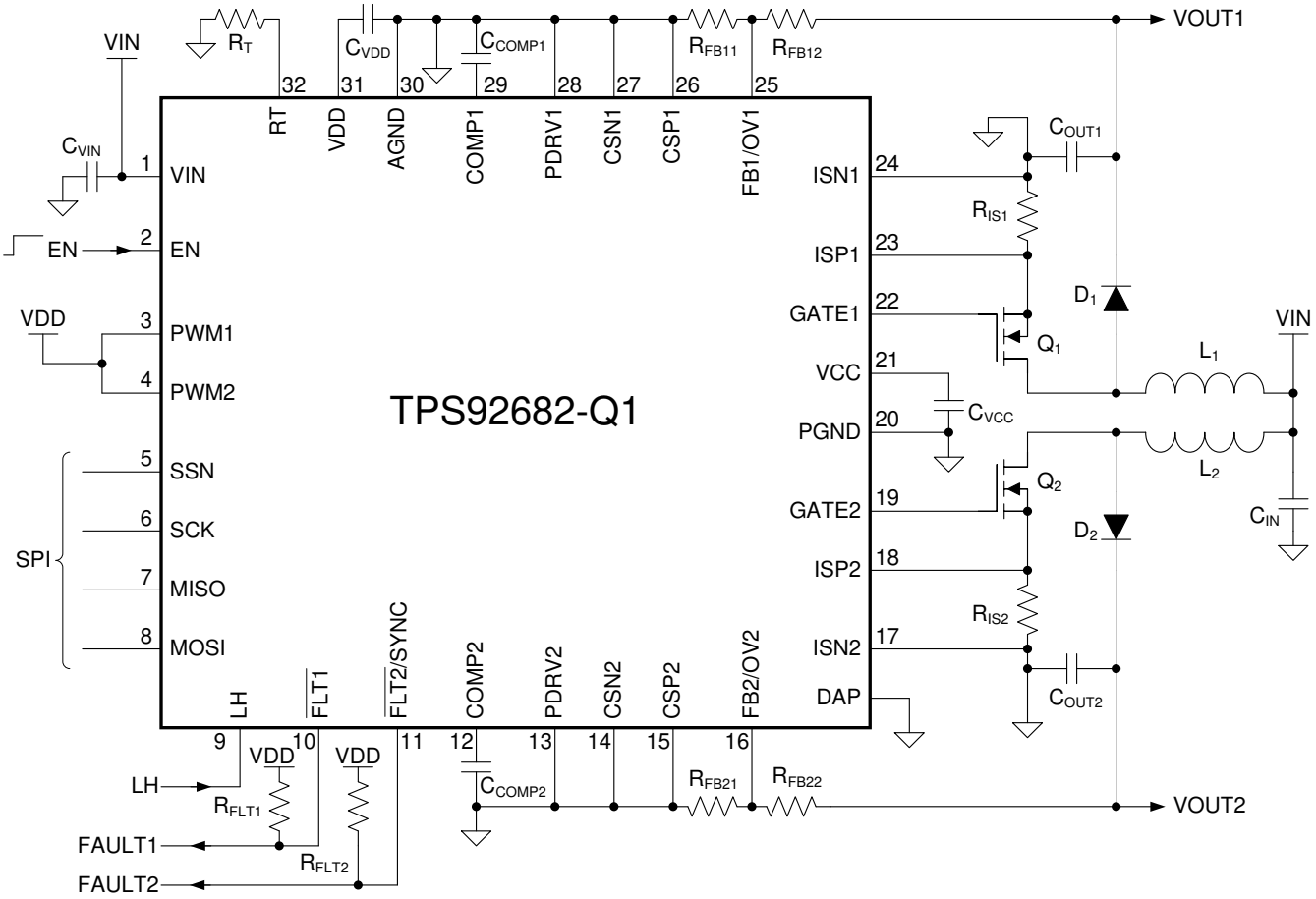


图 8-7. Two-Channel BOOST Voltage Regulator (CV mode)

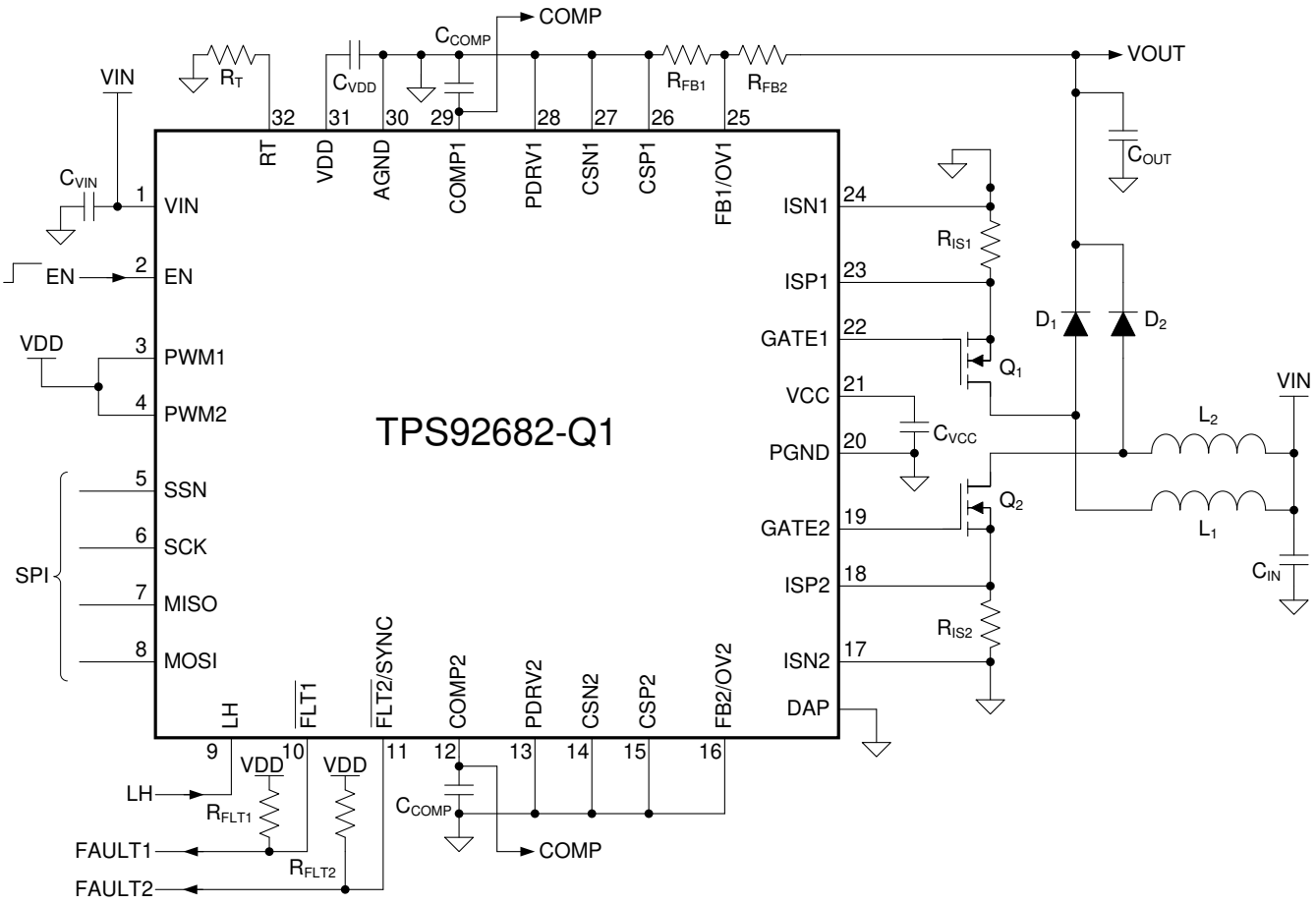


图 8-8. Two-Phase BOOST Voltage Regulator (CV mode)

8.3.1 Inductor Selection

The choice of the inductors in CV BOOST is highly dependent on the efficiency and the form-factor targets. One parameter that affects these specifications is the desired inductor current ripple. A common first choice for the inductor current ripple, Δi_{L-PP}, is 50% of the nominal inductor current I_L.

$$L = \frac{V_{IN} \times (V_O - V_{IN})}{\Delta i_{L-PP} \times V_O \times f_{SW}} \tag{39}$$

where

- $M = V_O / V_{IN}$

BOOST voltage regulators can be configured to operate in Discontinuous Conduction Mode (DCM) to achieve higher efficiency at light load. The condition to operate in DCM versus CCM are shown in 方程式 40 and 方程式 41:

CCM Operation:

$$P_O > \frac{V_{IN}^2 \times (V_O - V_{IN})}{2 \times V_O \times L \times f_{SW}} \tag{40}$$

DCM Operation:

$$P_O \le \frac{V_{IN}^2 \times (V_O - V_{IN})}{2 \times V_O \times L \times f_{SW}} \quad (41)$$

8.3.2 Output Capacitor Selection

The output capacitors are required to attenuate the discontinuous output current of the BOOST converter, as well as decreasing the output voltage undershoot and overshoot during load transient. The capacitance required for the target output peak-to-peak ripple is provided in the following equations:

For one-phase operation:

$$C_{OUT} = \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \times \frac{I_{OUT(MAX)}}{\Delta v_{O-PP} \times f_{SW}} \quad (42)$$

For two-phase operation, f_{SW} in 方程式 42 must be substituted with twice of the switching frequency.

When choosing the output capacitors, it is important to consider the ESR and the ESL characteristics as they directly impact the output voltage ripple. Ceramic capacitors are the best choice due to their low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and the DC bias operating conditions. TI recommends an X7R dielectric with voltage rating greater than maximum output voltage, V_{OUT}. An aluminum electrolytic capacitor can be used in parallel with ceramic capacitors to provide bulk energy storage. The aluminum capacitors must have necessary RMS current and temperature ratings to ensure prolonged operating lifetime. The minimum allowable RMS output capacitor current rating, $I_{COUT(RMS)}$, can be approximated as:

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (43)$$

8.3.3 Input Capacitor Selection

The input capacitors for one-phase CV BOOST can be obtained in the same way found in 方程式 25 for CC mode.

For two-phase operation, the input capacitor can be obtained as shown in 方程式 44.

$$C_{IN} = \frac{V_{IN(MIN)}}{8 \times (L/2) \times (2 x f_{SW})^2 \times \Delta v_{IN(PP)}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \quad (44)$$

8.3.4 Programming Output Voltage V_{OUT}

The output voltage V_{OUT} can be programmed using the feedback resistors and by writing an 8-bit value to the *CH1IADJ Register* and the *CH2IADJ Register*. 方程式 45 shows the relationship between the programmed V_{OUT}, the register CHxIADJ, and the feedback resistors.

$$V_{OUT} = \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \times \frac{CHxIADJ \times 2.4}{255} \quad (45)$$

8.3.5 Feedback Compensation

The loop gain T(s) is the product of the converter transfer function $G_{VVC}(s)$ and the feedback transfer function $G_C(s)$. The TPS92682-Q1 device, when configured as a BOOST voltage regulator, is normally followed by a second stage switching converter, which acts as a power sink load. In this case, the converter transfer function, $G_{VVC}(s)$, can be approximated as shown in 方程式 46. The $G_{VVC}(s)$ has a low frequency pole, ω_{P1}, and a high

frequency pole, ω_{P2}, when the converter operates in CCM. In DCM, ω_{P2} can be ignored. In a BOOST topology, the transfer function has a right half-plane zero.

$$G_{vvc}(s) = \frac{\hat{v}_o}{\hat{v}_{COMP}} = G_o \times \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right)} \quad (46)$$

表 8-2 summarizes the expressions for the small-signal model parameters of a BOOST converter operating in CCM or DCM.

表 8-2. Small-Signal Model Parameters for CV BOOST

BOOST TOPOLOGY	G_0	ω_{P1}	ω_{P2}	ω_Z
CCM	$\frac{F_m \times V_O^2}{R_{IS} \times \left(V_{IN} + F_m \times F_v \times V_O^2\right)}$	$\frac{V_{IN}}{V_O \times C_{OUT}} \times \left(\frac{V_{IN}}{F_m \times V_O^2} + F_v\right)$	$\frac{F_m \times V_O}{L}$	$\frac{V_{IN}^2}{P_O \times L}$
DCM	$\frac{2 \times (V_O - V_{IN}) \times V_O}{V_{IN} \times V_C}$	$\frac{V_{IN} \times I_O}{V_O \times (V_O - V_{IN}) \times C_{OUT}}$	∞	$\pi \times f_{SW}$

In 表 8-2, F_m is the compensation ramp gain, F_v is the V_O feedback gain, I_O is the DC output current, and V_C is the DC compensation voltage. In a BOOST topology:

$$F_m = \frac{R_{IS}}{V_{SLP}} \quad (47)$$

$$F_v = \frac{V_{IN}^2}{2 \times L \times f_{SW} \times V_O^2} \quad (48)$$

$$V_C = R_{IS} \times \sqrt{\frac{2 \times I_O \times (V_O - V_{IN})}{L \times f_{SW}}} \times \left(\frac{L \times f_{SW}}{F_m \times V_{IN}} + 1\right) \quad (49)$$

The feedback transfer function includes the voltage divider gain (H_{FB} = R_{FB1} / (R_{FB1} + R_{FB2})) and the transconductance amplifier gain. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. In CV BOOST application, a Proportional-Integral (PI) compensation is recommended. A network of R_{COMP}, C_{COMP}, and C_{HF}, shown in 图 8-9, can be used to implement PI compensation to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

The feedback transfer function is defined as follows.

Feedback transfer function with proportional integral compensation:

$$G_C(s) = -\frac{\hat{v}_{COMP}}{\hat{v}_O} = \frac{g_M \times H_{FB}}{s \times (C_{COMP} + C_{HF})} \times \frac{(1 + s \times R_{COMP} \times C_{COMP})}{\left(1 + s \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)\right)} \quad (50)$$

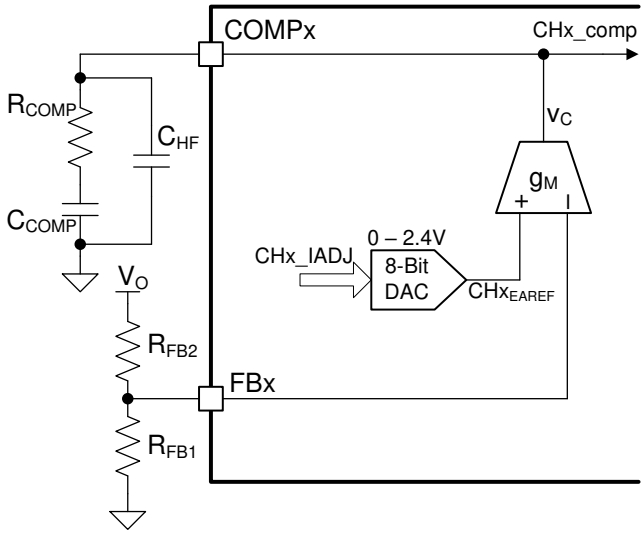


图 8-9. Proportional Integral Compensator

The pole at the origin minimizes output steady-state error. High bandwidth is achieved with the PI compensator by introducing a phase lead using a low-frequency zero.

PI compensator component values can be found by selecting a reasonable bandwidth and phase-margin. It is recommended to select a bandwidth of ω_C smaller than the RHP zero ω_Z by a factor of K_C in the range of 5 to 10. Assuming $\omega_C = \omega_Z / K_C$ and $\omega_C >> \omega_{P1}$:

$$R_{COMP} = \frac{\omega_Z}{K_C \times g_M \times G_0 \times H_{FB} \times \omega_{P1}} \tag{51}$$

The compensator zero, generated by the R_{COMP} and C_{COMP} is recommended to be placed far below the bandwidth ω_C and above ω_{P1} to provide adequate phase-margin. It is recommended to set the low-frequency zero of the compensator as follows:

$$\frac{1}{C_{COMP} \times R_{COMP}} = K_P \times \omega_{P1} \tag{52}$$

where

- K_P is a factor in the range of 1 to 5

From 方程式 51 and 方程式 52, C_{COMP} can be found.

$$C_{HF} < \frac{C_{COMP}}{100} \tag{53}$$

8.3.6 Overvoltage and Undervoltage Protection

In CV mode, the output Overvoltage level is set in *OV Register* as a percentage above the programmed regulated value of V_{OUT}.

The Overvoltage hysteresis, $V_{OV(HYS)}$, is:

$$V_{OV(HYS)} = I_{OV(HYS)} \times R_{FB2} \tag{54}$$

where

- $I_{OV(HYS)}$ is 20 µA (typ.)

The corresponding undervoltage fault threshold, $V_{O(UV)}$, is:

$$V_{O(UV)} = 0.05 \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \quad (55)$$

8.3.7 Programing Example for Two-Phase CV BOOST

图 8-10 shows an example for initialization of the TPS92682 registers for the two-phase CV BOOST application.

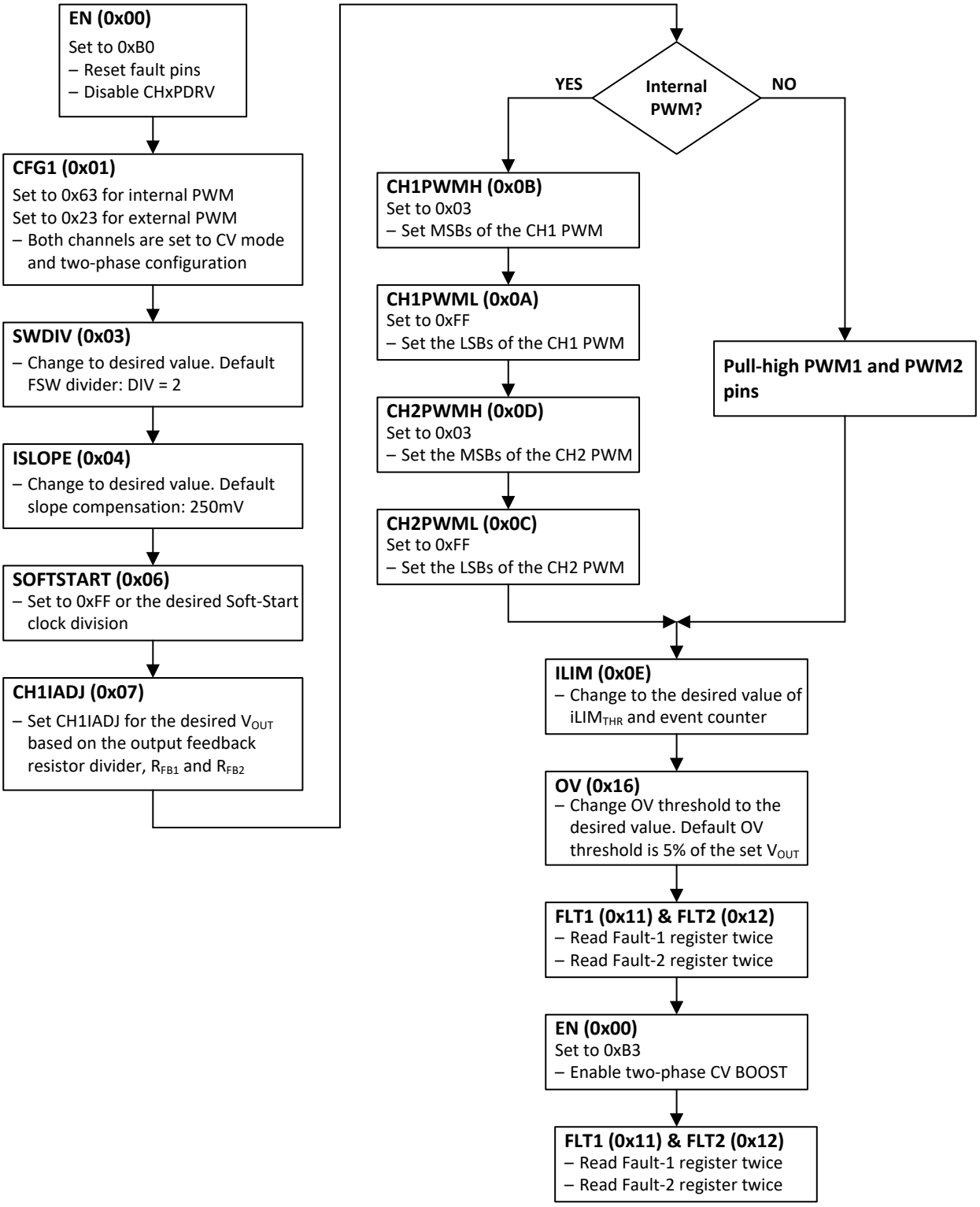


图 8-10. Register Programing for Two-Phase CV BOOST

8.4 Typical Application CC Mode

图 8-11 shows the schematic for a dual channel, high-side current sense, Boost and Buck-Boost LED driver with PFET dimming. In this application, the Channel-1 of the device is configured as Boost and the Channel-2 as Buck-Boost.

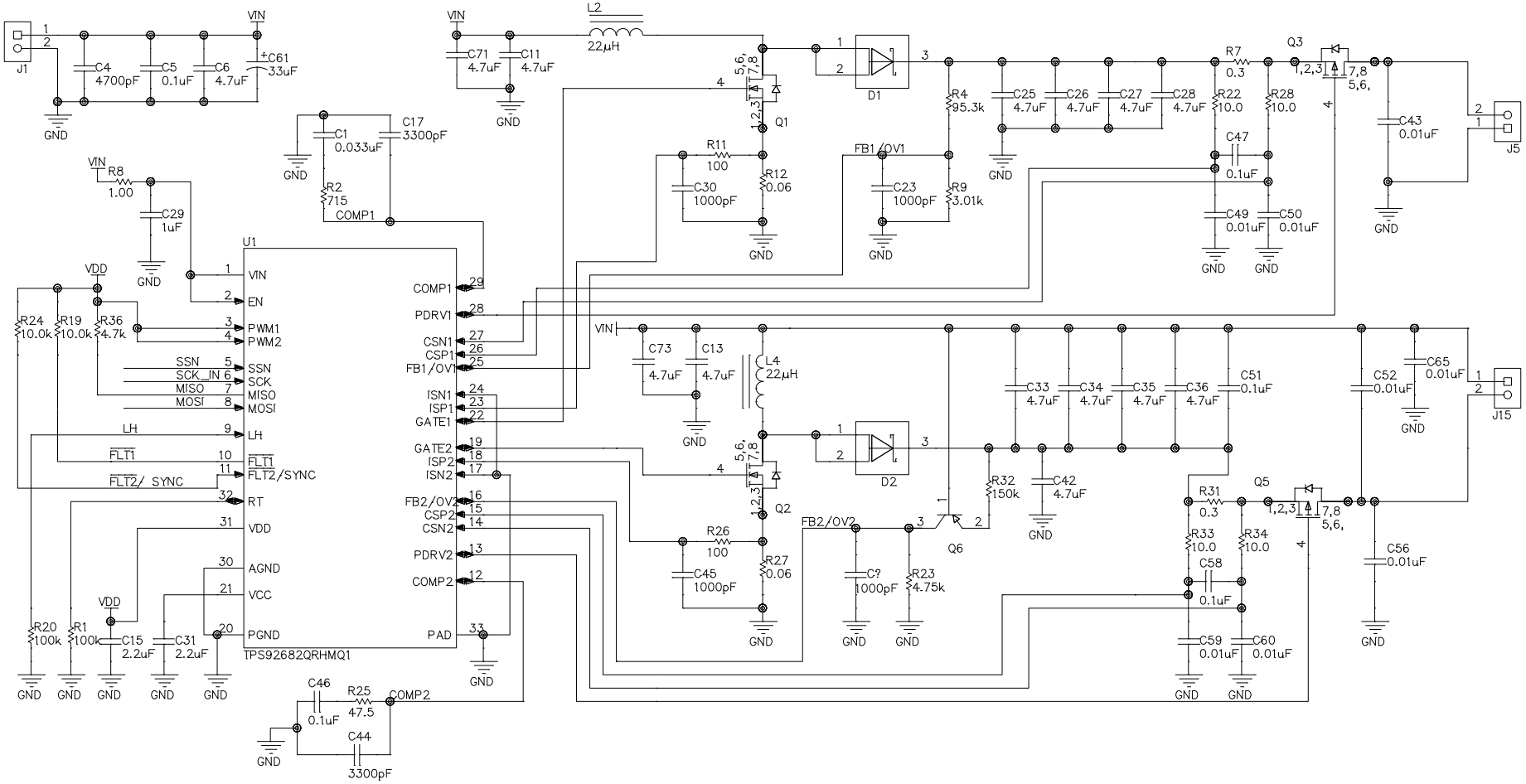


图 8-11. CC Mode LED Driver, BOOST, and Buck-Boost

8.4.1 CC Boost Design Requirements

表 8-3 shows the design parameters for the boost LED driver application.

表 8-3. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		7	14	18	V
OUTPUT CHARACTERISTICS						
$V_{F(LED)}$	LED forward voltage		2.8	3.2	3.6	V
N_{LED}	Number of LEDs in series			12		
V_O	Output voltage	LED+ to LED –	33.6	38.4	43.2	V
I_{LED}	Output current			350	550	mA
RR_{ilED}	LED current ripple ratio			4%		
r_D	LED string resistance			3		Ω
$P_{O(MAX)}$	Maximum output power				25	W
f_{PWM}	PWM dimming frequency			400		Hz
SYSTEMS CHARACTERISTICS						
$P_{O(BDRY)}$	Output power at CCM-DCM boundary condition			8		W
$\Delta v_{IN(PP)}$	Input voltage ripple			20		mV
$V_{O(OV)}$	Output Overvoltage protection threshold			50		V
$V_{OV(HYS)}$	Output Overvoltage protection hysteresis			2.4		V
f_{DM}	Dither Modulation Frequency		400		600	Hz
f_{SW}	Switching frequency			400		kHz

8.4.2 CC Boost Detailed Design Procedure

In the following section, the detailed design procedure for the CC BOOST LED driver is provided.

8.4.2.1 Calculating Duty Cycle

From 方程式 9 and the input and output characteristics in 表 8-3, you can solve for D_{TYP}, D_{MAX}, and D_{MIN}.

- D_{TYP} = 0.64
- D_{MAX} = 0.84
- D_{MIN} = 0.46

8.4.2.2 Setting Switching Frequency

For the default division factor of 2 in the *SWDIV Register* and from 方程式 1, the R_T value for f_{SW} = 400 kHz can be obtained:

$$R_T = \frac{10^{12}}{12.5 \times SW_{DIV} \times f_{SW}} \tag{56}$$

R_T = 100 kΩ

8.4.2.3 Setting Dither Modulation Frequency

The dither modulation frequency can be set using the the *FM Register* in Equation 2. For the dither modulation frequency of less than 600 Hz, the FM_{FREQ} must be set to 0101, which corresponds to a division factor of 1536 and sets FM = 521 Hz.

8.4.2.4 Inductor Selection

The inductor is selected to meet the CCM-DCM boundary power requirement, $P_{O(BDRY)}$. In most applications, $P_{O(BDRY)}$ is set to be 1/3 of the maximum output power, $P_{O(MAX)}$. The inductor value is calculated for typical input voltage, $V_{IN(TYP)}$, and output voltage, $V_{O(TYP)}$. From 方程式 18, the inductor L is calculated to be:

$L \geqslant 19.5\ \mu H$

The value of L = 22 µH is selected for this application.

Ensure that the inductor saturation current rating is greater than 1.2 × $I_{L(PK)}$ found from 方程式 20:

$I_{L(PK)} = 3.9\ A$

8.4.2.5 Output Capacitor Selection

The specified peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$, is:

$\Delta i_{LED(PP)} = RR_{iLED} \times I_{LED(MAX)} = 22\ mA$

The output capacitance required to achieve the target LED current ripple can be obtained from 方程式 22. The resulting capacitance value is calculated to be: $C_{OUT} \geqslant 17.5\ \mu F$.

Four 4.7-µF 100-V ceramic capacitors are used in parallel to achieve a combined required output capacitance.

8.4.2.6 Input Capacitor Selection

The input capacitor is required to reduce switching noise conducted through the input terminal and to reduce the input impedance of the LED driver. 方程式 25 is used to calculate the required capacitance of $C_{IN} \geqslant 10\ \mu F$ to limit peak-to-peak input voltage ripple, $\Delta v_{IN(PP)}$, to 20 mV.

Two 4.7-µF, 50-V ceramic capacitors are used in parallel to achieve the combined input capacitance of 9.4 µF. As shown in 图 8-11, an additional 33-µF 50-V electrolytic capacitor and more ceramic capacitors are also used at the input terminal to further decrease the overshoot and undershoot of V_{IN} during PWM dimming.

8.4.2.7 Main N-Channel MOSFET Selection

Ensure that the MOSFET ratings exceed the maximum output voltage and RMS switch current.

$V_{DS} = V_{O(OV)} \times 1.1 = 55\ V$

The maximum RMS switch current can be found from Equation 11 to be 3.3 A.

An N-channel MOSFET with a voltage rating of 100 V and a current rating of more than 4 A is required for this design.

8.4.2.8 Rectifier Diode Selection

Select a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance.

The DC current rating of the diode rectifier for the Boost LED driver must be greater than $I_{LED(MAX)}$.

8.4.2.9 Setting I_{LED} and Selecting R_{CS}

The LED current can be programmed by writing an 8-bit value to the *CH1IADJ Register*, and as described in the *Programming LED Current* section.

The value of the current sense resistor, R_{CS}, can be selected to result in the $I_{LED(MAX)}$ for the maximum programmed value of 255 in the CHxIADJ register.

$$R_{CS} = \frac{2.4}{14 \times I_{LED(MAX)}} \tag{57}$$

Substituting $I_{LED(MAX)}$ = 0.55 A in 方程式 57 results in R_{CS} = 0.31 Ω. A current sense value of 0.3 Ω is selected for this design.

8.4.2.10 Setting Switch Current Limit

As shown in 方程式 13, the switch current limit is determined by the switch current sense resistor, R_{IS}, and the switch current threshold. For $V_{ILIM(THR)}$ = 250 mV and 1.2 × $I_{L(PK)}$ = 4.7 A, $R_{IS} \leqslant 53\ m\Omega$. A standard sense resistor of R_{IS} = 40 mΩ is selected for this application.

8.4.2.11 Slope Compensation

The recommended slope compensation magnitude can be obtained from 方程式 14, $V_{SLP} \geqslant 100$ mV.

The V_{SLP} can be programmed in the *ISLOP Register*. The ISLOPE =011 is selected, which corresponds with V_{SLP} = 150 mV.

8.4.2.12 Compensator Parameters

Proportional-Integral Compensator is selected for this design. The initial compensator component values can be obtained from 方程式 32, 方程式 33, and 方程式 34 The final values are tuned to get the best overall dynamic performance.

C_{COMP} = 33 nF

C_{HF} = 3.3 nF

R_{COMP} = 715 Ω

It is be noted that the above compensator components are fine-tuned to provide improved transient performance in PWM dimming.

8.4.2.13 Overvoltage Protection

The output Overvoltage level is programmed using a resistor divider, R_{FB2} and R_{FB1}, from the output voltage, V_O, to GND. R_{FB2} can be calculated from the $V_{OV(HYS)}$ = 2.4 V and 方程式 37:

R_{FB2} = 120 kΩ

R_{FB1} can be calculated from 方程式 35 and the required value of $V_{O(OV)}$ = 50 V:

R_{FB1} = 3 kΩ

8.4.2.14 Series P-Channel MOSFET Selection

In applications with PWM dimming, the device requires a P-channel MOSFET placed in series with the LED load. Select a P-channel MOSFET with a gate-to-source voltage rating of 10 V or higher and with a drain-to-source breakdown voltage rating greater than the output voltage. Ensure that the drain current rating of the P-channel MOSFET exceeds the programmed LED current by at least 10%. It is important to consider the FET input capacitance and on-resistance as it impacts the accuracy and efficiency of the LED driver. TI recommends a FET with lower input capacitance and gate charge to minimize the errors caused by rise and fall times when PWM dimming at low duty cycles is applied.

8.4.3 CC Buck-Boost Design Requirements

Buck-Boost LED drivers provide the flexibility needed in applications, where the load voltage (LED string voltage) maybe less or more than the input battery voltage or the application supports multiple LED load configurations. For such applications, it is necessary to modify the design procedure presented to account for the wider range of output voltage and LED current specifications. 表 8-4 shows the design parameters for the Buck-Boost (BtB) LED driver application.

表 8-4. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		7	14	18	V
OUTPUT CHARACTERISTICS						
$V_{F(LED)}$	LED forward voltage		2.8	3.2	3.6	V

表 8-4. Design Parameters (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N_{LED}	Number of LEDs in series		3	6	9	
V_O	Output voltage	LED+ to LED –	8.4	19.2	32.4	V
I_{LED}	Output current		200	500	1200	mA
RR_{iLED}	LED current ripple ratio			7.5%		
r_D	LED string resistance		0.8	1.5	2.3	Ω
$P_{O(MAX)}$	Maximum output power				12	W
f_{PWM}	PWM dimming frequency			400		Hz
SYSTEMS CHARACTERISTICS						
$P_{O(BDRY)}$	Output power at CCM-DCM boundary condition			3.5		W
$\Delta v_{IN(PP)}$	Input voltage ripple			100		mV
$V_{O(OV)}$	Output Overvoltage protection threshold			40		V
$V_{OV(HYS)}$	Output Overvoltage protection hysteresis			3		V
f_{DM}	Dither Modulation Frequency		400		600	Hz
f_{SW}	Switching frequency			400		kHz

8.4.4 CC Buck-Boost Detailed Design Procedure

In the following section, the detailed design procedure for the CC Buck-Boost LED driver is provided.

8.4.4.1 Calculating Duty Cycle

From Equation 10 and the input and output characteristics in 表 8-4, you can solve for D_{TYP}, D_{MAX}, and D_{MIN}.

$D_{TYP} = 0.58$

$D_{MAX} = 0.82$

$D_{MIN} = 0.32$

8.4.4.2 Setting Switching Frequency

The R_T value that sets the internal clock is calculated from 方程式 56 in the *CC Boost Detailed Design Procedure* section. For the default division factor of 2 in the *SWDIV Register*, the value for f_{SW} = 400 kHz can be obtained.

8.4.4.3 Setting Dither Modulation Frequency

Frequency modulation is shared between both channels of the TPS92682-Q1. As a result, the same frequency modulation is applied to both Boost and Buck-Boost LED drivers.

8.4.4.4 Inductor Selection

The inductor is selected to meet the CCM-DCM boundary power requirement, $P_{O(BDRY)}$. Typically, the boundary condition is set to enable CCM operation at the lowest possible operating power. The inductor value is calculated for typical input voltage, $V_{IN(TYP)}$, and output voltage, $V_{O(TYP)}$. From 方程式 19, the inductor L is calculated to be:

$L = 23.4\ \mu H$

The value of L = 22 µH is selected for this application.

Ensure that the inductor saturation current rating is greater than the $1.2 \times I_{L(PK)}$ found from 方程式 21:

$I_{L(PK)} = 3.4\ A$

8.4.4.5 Output Capacitor Selection

The specified peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$, is:

$\Delta i_{LED(PP)} = RR_{iLED} \times I_{LED(MAX)} = 90\ mA$

The output capacitance required to achieve the target LED current ripple can be obtained from 方程式 23. The resulting capacitance value is calculated to be $C_{OUT} \geqslant 23$ µF.

Five 4.7-µF 100-V ceramic capacitors are used in parallel to achieve a combined required output capacitance.

8.4.4.6 Input Capacitor Selection

The input capacitor is required to reduce switching noise conducted through the input terminal and to reduce the input impedance of the LED driver. 方程式 26 is used to calculate the required capacitance of $C_{IN} \geqslant 43$ µF to limit peak-to-peak input voltage ripple, $\Delta v_{IN(PP)}$, to 100 mV.

Four 10-µF, 50-V ceramic capacitors are used in parallel to achieve a combined input capacitance of 40 µF. As shown in 图 8-11, an additional 33-µF 50-V electrolytic capacitor and more ceramic capacitors are also used at the input terminal to further decrease the overshoot and undershoot of V_{IN} during PWM dimming.

8.4.4.7 Main N-Channel MOSFET Selection

Maximum transistor voltage rating must exceed the following:

$V_{DS} = 1.2 \times (V_{O(OV)} + V_{IN(MAX)}) = 70$ V

The maximum RMS switch current can be found from 方程式 12 to be 2.3 A.

An N-channel MOSFET with a voltage rating of 100 V and a current rating of more than 3 A is required for this design.

8.4.4.8 Rectifier Diode Selection

Select a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance.

The DC current rating of the diode rectifier for the Buck-Boost LED driver must be greater than $I_{LED(MAX)}$.

8.4.4.9 Setting I_{LED} and Selecting R_{CS}

The LED current can be programmed by writing an 8-bit value to *CH2IADJ Register*, and as described in the *Programming LED Current* section.

The value of the current sense resistor, R_{CS}, can be selected to result in the $I_{LED(MAX)}$ for the maximum programmed value of 255 in the CHxIADJ register.

Substituting $I_{LED(MAX)} = 1.2$ A in 方程式 57 results in $R_{CS} = 0.14$ Ω. A current sense value of 0.1 Ω is selected for this design.

8.4.4.10 Setting Switch Current Limit

As shown in 方程式 13, the switch current limit is determined by the switch current sense resistor, R_{IS}, and the switch current threshold. For $V_{ILIM(THR)} = 250$ mV and $1.2 \times I_{L(PK)} = 4$ A, $R_{IS} \leqslant 62$ mΩ. A standard sense resistor of $R_{IS} = 60$ mΩ is selected in this design.

8.4.4.11 Slope Compensation

The recommended slope compensation magnitude can be obtained from 方程式 14, $V_{SLP} \geqslant 110$ mV.

The V_{SLP} can be programmed in the *ISLOPE Register*. The ISLOPE =011 is selected, which corresponds with $V_{SLP} = 150$ mV.

8.4.4.12 Compensator Parameters

An integral compensator can be selected for this design. The C_{COMP} can be calculated from 方程式 31 . A standard capacitor value is selected for this design:

$C_{COMP} = 100$ nF

A proportional integral compensator can be used to achieve higher bandwidth and improved transient performance. However, it is necessary to experimentally tune the compensator parameters over the entire operating range to ensure stable operation.

8.4.4.13 Overvoltage Protection

The output Overvoltage level is programmed using R_{FB2} and R_{FB1}. R_{FB2} can be calculated from the $V_{OV(HYS)}$ = 3 V and 方程式 37:

R_{FB2} = 150 kΩ

R_{FB1} can be calculated from 方程式 36 and the required value of $V_{O(OV)}$ = 40 V:

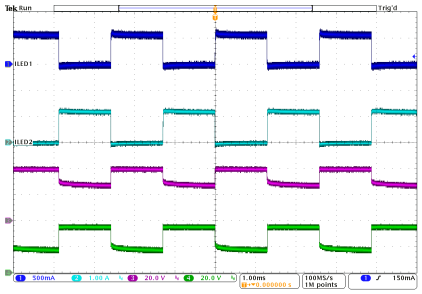
R_{FB1} = 4.75 kΩ

8.4.5 PWM Dimming Consideration

A 60-V, 2-A P-channel FET is used to achieve series FET PWM dimming.

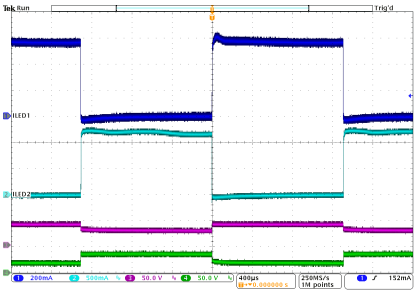
8.4.6 Application Curves

The following waveform curves are for the Boost and the Buck-Boost LED drivers. Channel-1 of the TPS92682-Q1 is configured as a Boost LED driver and the Channel-2 as a Buck-Boost.



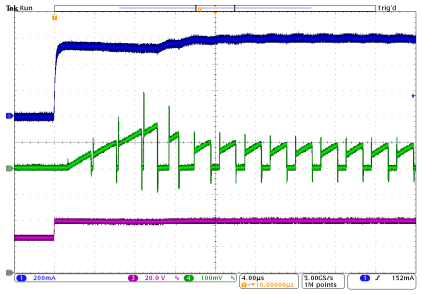
CH1: Boost I_{LED} current | CH2: Buck-Boost I_{LED} current | CH3: Boost LED+ voltage (12×LED) | CH4: Buck-Boost LED+ voltage (3×LED)

图 8-12. PWM Dimming Transient



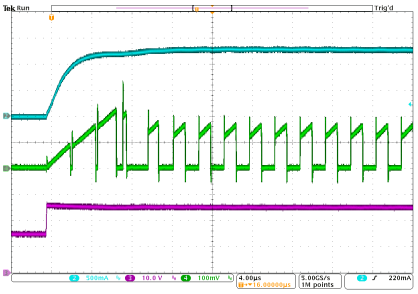
CH1: Boost I_{LED} current | CH2: Buck-Boost I_{LED} current | CH3: Boost LED+ voltage (12×LED) | CH4: Buck-Boost LED+ voltage (3×LED)

图 8-13. PWM Dimming Transient with FM



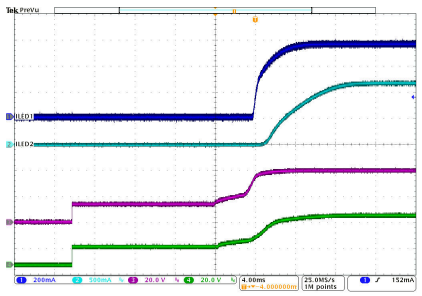
CH1: Boost I_{LED} current | CH2: Boost switch current sense voltage | CH3: Boost LED+ voltage (12xLED)

图 8-14. Boost PWM Dimming, Switch Current



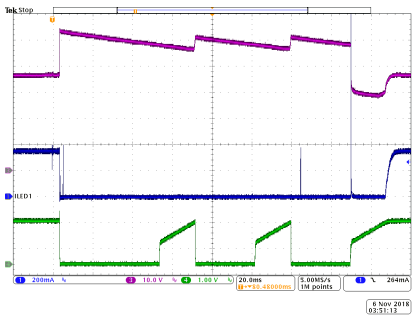
CH2: Buck-Boost I_{LED} current | CH4: Buck-Boost switch current sense voltage | CH3: Buck-Boost LED+ voltage (3×LED)

图 8-15. Buck-Boost PWM Dimming, Switch Current



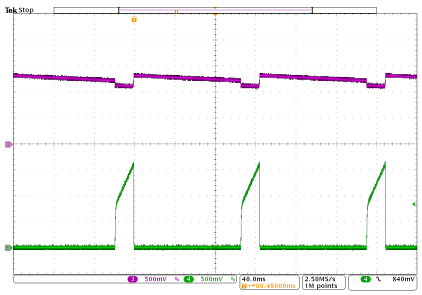
CH1: Boost I_{LED} current | CH2: Buck-Boost I_{LED} current | CH3: Boost LED+ voltage (12×LED) | CH4: Buck-Boost LED+ voltage (6×LED)

图 8-16. Buck-Boost PWM Dimming, Switch Current



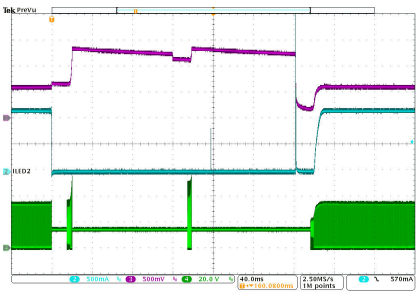
CH1: Boost I_{LED} current | CH3: Boost LED+ voltage (12×LED) | CH4: COMP1-PIN voltage

图 8-17. Boost LED Open Fault



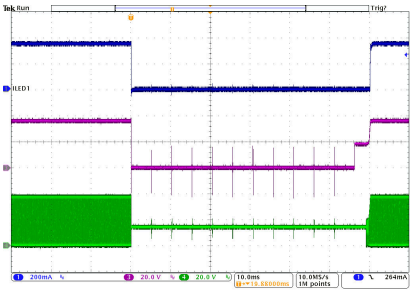
CH3: FB2/OV2 PIN voltage CH4: COMP2 PIN voltage

图 8-18. Buck-Boost LED Open Fault



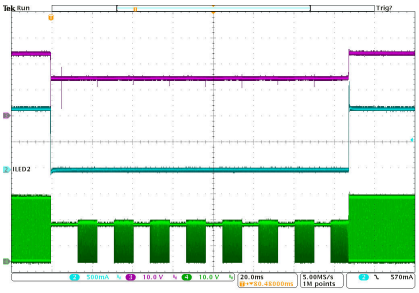
CH2: Buck-Boost I_{LED} current CH3: FB2/OV2 PIN voltage CH4: Buck-Boost V_{SW} voltage

图 8-19. Buck-Boost LED Open Fault



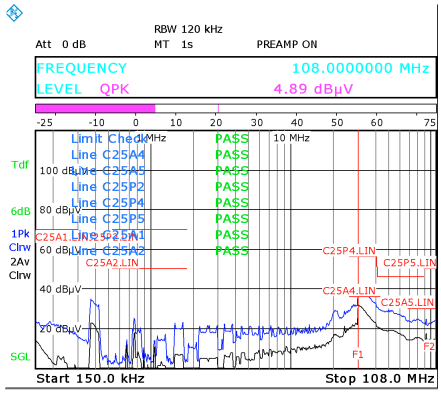
CH1: Boost I_{LED} current CH3: Boost LED+ voltage CH4: Boost V_{SW} voltage

图 8-20. Boost Output Short Fault



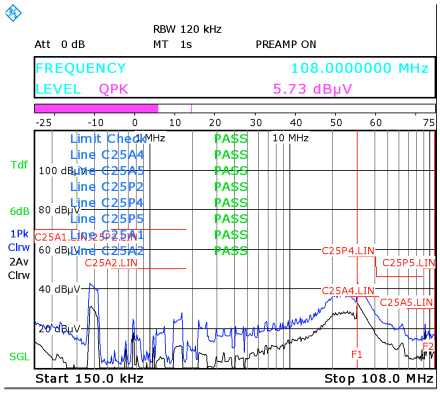
CH2: Buck-Boost I_{LED} current CH3: Buck-Boost LED+ voltage CH4: Buck-Boost V_{SW} voltage

图 8-21. Buck-Boost Output Short Fault



12×LED, I_{LED} = 560 mA

图 8-22. Boost Conducted EMI Scan with FM



6×LED, I_{LED} = 700 mA

图 8-23. Buck-Boost Conducted EMI Scan with FM

8.5 Typical Application CV Mode

图 8-24 shows the schematic for a two-phase Boost Constant Voltage (CV) regulator.

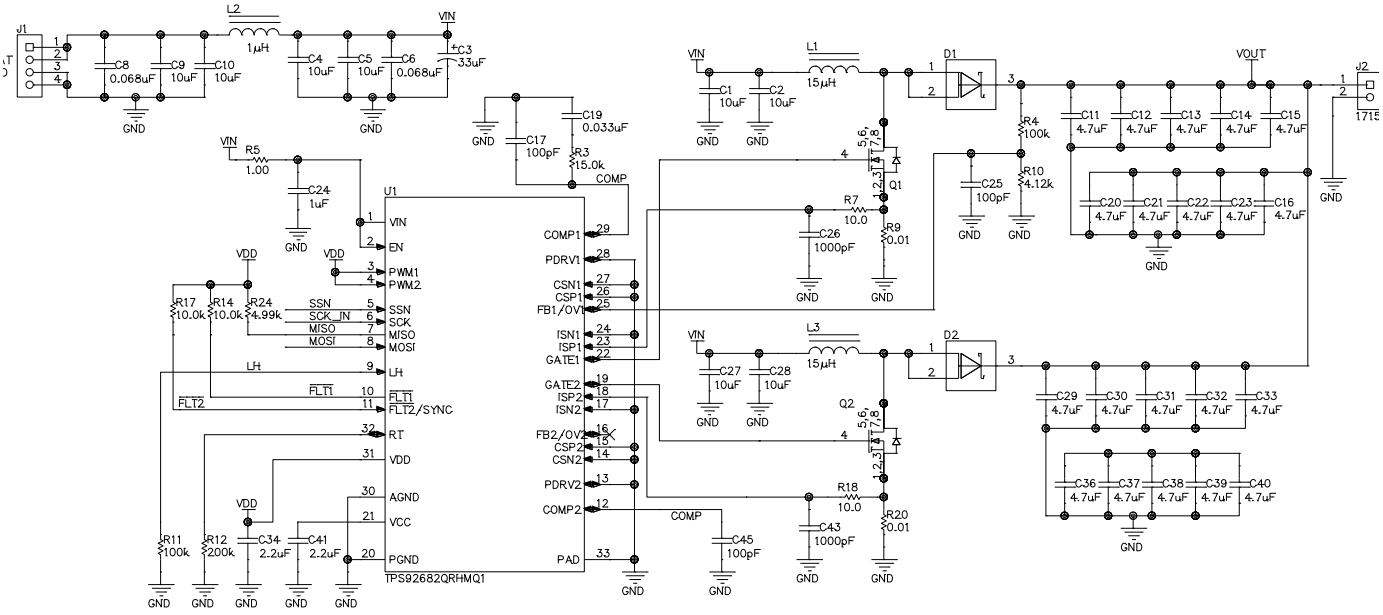


图 8-24. CV Mode Two-Phase BOOST

8.5.1 CV Design Requirements

表 8-5 shows the design parameters for the CV two-phase boost.

表 8-5. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		8	14	28	V
$I_{IN(MAX)}$	Maximum input current				10	A
OUTPUT CHARACTERISTICS						
V_O	Output voltage			50		V
$I_{O(MAX)}$	Maximum output current				2	A
$P_{O(MAX)}$	Maximum output power				100	W
SYSTEMS CHARACTERISTICS						
PR	Peak Ratio: peak to average inductor current at $P_{OUT(MAX)}$, $I_{L(PK)}/I_L$			1.4		
$\Delta v_{IN(PP)}$	Input voltage ripple			10		mV
$\Delta v_{OUT(PP)}$	Output voltage ripple			50		mV
$V_{O(OV)}$	Output Overvoltage protection threshold			55		V
$V_{OV(HYS)}$	Output Overvoltage protection hysteresis			2.0		V
f_{DM}	Dither Modulation Frequency		400		600	Hz
f_{SW}	Switching frequency			200		kHz

8.5.2 Detailed Design Procedure

In the following section, the detailed design procedure for the two-phase CV Boost is provided.

8.5.2.1 Calculating Duty Cycle

From Equation 9 and the input and output characteristics in 表 8-5, you can solve for D_{TYP}, D_{MAX}, and D_{MIN}.

$D_{TYP} = 0.72$

$D_{MAX} = 0.84$

D_{MIN} = 0.44

8.5.2.2 Setting Switching Frequency

Assuming the division factor of 4 in *SWDIV Register* and from 方程式 1, the R_T value for the f_{SW} = 200 kHz can be obtained:

$$R_T = \frac{10^{12}}{12.5 \times SW_{DIV} \times f_{SW}} \quad (58)$$

R_T = 100 kΩ

8.5.2.3 Setting Dither Modulation Frequency

The dither modulation frequency can be set using the *FM Register* in 方程式 2. For the dither modulation frequency of less than 600 Hz, the FM_{FREQ} must be set to 0101, which corresponds to a division factor of 1536 and sets FM = 521 Hz.

8.5.2.4 Inductor Selection

The inductor is selected to meet the peak-to-peak inductor current ripple at $P_{OUT(MAX)}$. The inductor current ripple, Δi_{L-PP}, can be obtained from the PR = $I_{L(PK)}$ / I_L at $P_{OUT(MAX)}$:

$$\Delta i_{L-PP} = 2 \times (PR - 1) \times \frac{P_{O(MAX)}}{V_{IN}} \quad (59)$$

In 方程式 59, it is important to note that the $P_{OUT(MAX)}$ is the maximum output power per phase, 50 W in this design.

The value of Δi_{L-PP} is calculated for typical input voltage, $V_{IN(TYP)}$. From 方程式 39, the inductor L is calculated to be:

L ⩾ 17 µH

The value of L = 15 µH is selected for this application.

Ensure that the inductor saturation current rating is greater than 1.1 × $I_{L(PK)}$ = 6.5 A ($I_{L(PK)}$ is calculated with 90% CV BOOST efficiency assumption).

8.5.2.5 Output Capacitor Selection

The output capacitors are required to attenuate the discontinuous output current of the BOOST converter, as well as decreasing the output voltage undershoot and overshoot during load transient. The total required output capacitor, C_{OUT}, can be found from 方程式 42, where f_{SW} is replaced with 2 × 200 kHz = 400 kHz for two-phase operation.

C_{OUT} ⩾ 84 µF

10 × 4.7-µF, 100-V ceramic capacitors are used in parallel, at the output of each phase, to achieve a combined required output capacitance. It is important to note that the CV Boost output capacitor also plays an important role in decreasing the output undershoot and overshoot voltage during load transient.

8.5.2.6 Input Capacitor Selection

The input capacitor is required to reduce switching noise conducted through the input terminal and to reduce the input impedance of the CV Boost. 方程式 44 is used to calculate the required capacitance of C_{IN} ⩾ 70 µF to limit peak-to-peak input voltage ripple, $\Delta v_{IN(PP)}$, to 10 mV.

Eight 10-µF, 50-V ceramic capacitors are used in parallel to achieve a combined input capacitance of 80 µF. As shown in 图 8-24, an additional 33-µF, 50-V electrolytic capacitor and a 1-µH inductor are also used at the input terminal. The electrolytic capacitor is used to further decrease overshoot and undershoot during load transient. The input inductor is used to decrease the switching noise and improve EMI performance.

8.5.2.7 Main N-Channel MOSFET Selection

Ensure that the MOSFET ratings exceed the maximum output voltage and RMS switch current.

$V_{DS} = V_{O(OV)} \times 1.1 = 61$ V

The maximum RMS switch current can be found from 方程式 11, where $P_{O(MAX)}$ is replaced by half of the total maximum output power for two-phase operation.

An N-channel MOSFET with a voltage rating of 100 V and a current rating of more than 7 A is required for this design.

8.5.2.8 Rectifier Diode Selection

Select a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance.

The DC current rating of the diode rectifier for the Boost LED driver must be greater than half of the total output current, $I_{O(MAX)} = 2$ A.

8.5.2.9 Programming V_{OUT}

The output voltage V_{OUT} can be programmed using the feedback resistors and by writing an 8-bit value to *CH1IADJ Register* and *CH2IADJ Register*. 方程式 45 shows the relation between the programmed V_{OUT}, the register CHxIADJ, and the feedback resistors.

It is recommended to set the ratio of the feedback resistors R_{FB2} / R_{FB1} such that for the maximum CHxIADJ = 255, V_{OUT} does not increase above the maximum desired limit (for example, $V_{O(LIM)} = 60$ V).

In this design for $V_{O(LIM)} = 60$ V, R_{FB2} / $R_{FB1} = 24$.

In this design, CHxIADJ is set to the value of 212 to achieve $V_O = 50$ V, for the R_{FB2} / $R_{FB1} = 24$.

8.5.2.10 Setting Switch Current Limit

As shown in 方程式 13, the switch current limit is determined by the switch current sense resistor, R_{IS}, and the switch current threshold. For $V_{ILIM(THR)} = 100$ mV and $I_{L(PK)} = 6$ A, $R_{IS} \leqslant 16$ mΩ. A standard sense resistor of $R_{IS} = 10$ mΩ is selected for this application.

The maximum power loss introduced by R_{IS} can be found from 方程式 60, to be 0.45 W.

$$P_{RIS-Loss} = R_{IS} \times \left(I_{Q(RMS)}\right)^2 \quad (60)$$

8.5.2.11 Slope Compensation

The recommended slope compensation magnitude can be obtained from 方程式 14, $V_{SLP} \geqslant 100$ mV.

In CV mode for R_{IS} values smaller than 20 mΩ, it is recommended to use $V_{SLP} \geqslant 250$ mV for better noise immunity.

The V_{SLP} can be programmed in the *ISLOPE Register*. The ISLOPE =101 is selected, which corresponds with $V_{SLP} = 250$ mV.

8.5.2.12 Compensator Parameters

Proportional-Integral Compensator is selected for this design. The compensator component can be obtained from 方程式 51, 方程式 52 and 方程式 53:

$C_{COMP} = 33$ nF

$C_{HF} = 100$ pF

$R_{COMP} = 15$ kΩ

It is noted that the above compensator components are fine-tuned to provide improved load transient performance.

8.5.2.13 Overvoltage Protection

In CV mode, the output Overvoltage level is set in the *OV Register* as a percentage above the programmed regulated value of V_{OUT}. For $V_{O(OV)}$ = 55 V, *OV Register* is set to 10%, which corresponds with CHxOV = 100.

R_{FB2} can be calculated from the $V_{OV(HYS)}$ = 2 V and from 方程式 54:

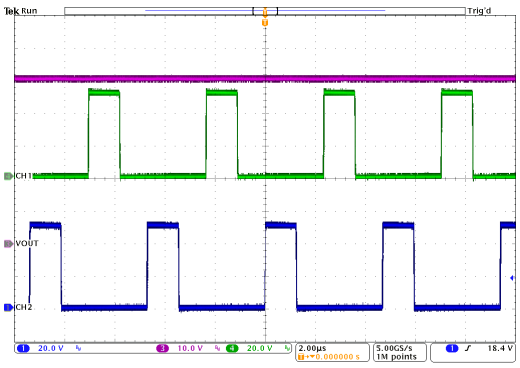
R_{FB2} = 100 kΩ

R_{FB1} can be calculated from the ratio of R_{FB2} / R_{FB1} = 24, found in the *VOUT setting*.

R_{FB1} = 4.12 kΩ

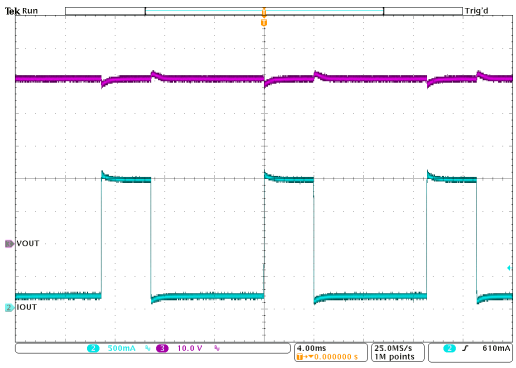
8.5.3 Application Curves

The following waveform curves are for the two-phase CV Boost.



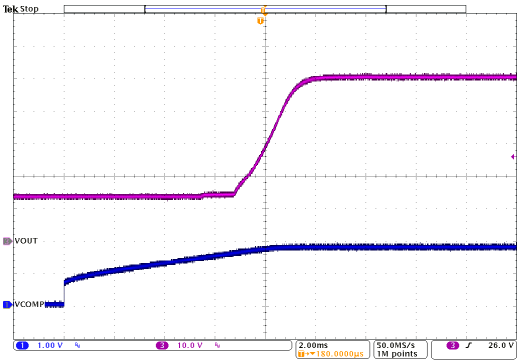
CH1: Phase-1 V_{SW} voltage CH2: Phase-2 V_{SW} voltage CH3: CV Boost V_{OUT}

图 8-25. Normal Operation, P_{OUT} = 50 W



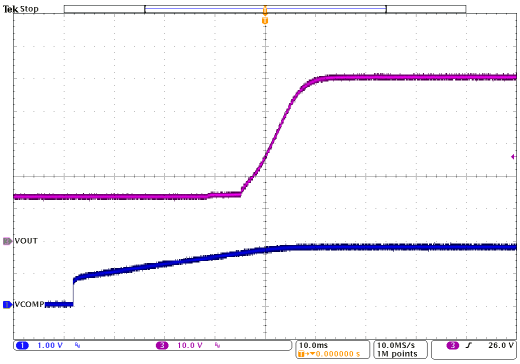
CH2: I_{OUT}, 0.2 A to 2 A transient CH3: CV Boost V_{OUT}

图 8-26. Load Transient



CH1: V_{COMP1} pin CH3: CV Boost V_{OUT}

图 8-27. Start-up, SOFTSTART = 0111



CH1: V_{COMP1} pin CH3: CV Boost V_{OUT}

图 8-28. Start-up, SOFTSTART = 1111

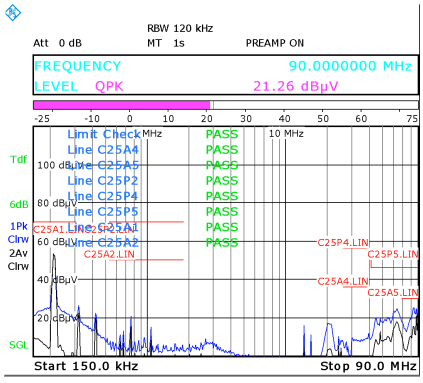


图 8-29. CV Conducted EMI Scan, f_{SW} = 100 kHz

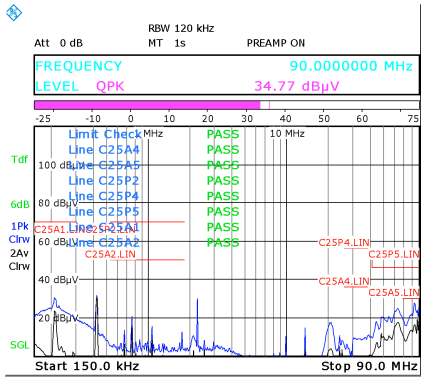


图 8-30. CV Conducted EMI Scan, f_{SW} = 200 kHz

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 4.5 V and 65 V. The input can be a car battery or another pre-regulated power supply. If the input supply is located more than a few inches from the TPS92682-Q1 device, additional bulk capacitance or an input filter can be required in addition to the ceramic bypass capacitors to address noise and EMI concerns.

10 Layout

10.1 Layout Guidelines

- The performance of the switching regulator depends as much on the layout of the PCB as the component selection. Following a few simple guidelines maximizes noise rejection and minimizes the generation of EMI within the circuit.
- Discontinuous currents are the most likely to generate EMI. Therefore, take care when routing these paths. The main path for discontinuous current in the device using a buck regulator topology contains the input capacitor, C_{IN}, the recirculating diode, D, the N-channel MOSFET, Q1, and the sense resistor, R_{IS}. In the TPS92682-Q1 device using a boost regulator topology, the discontinuous current flows through the output capacitor C_{OUT}, diode, D, N-channel MOSFET, Q1, and the current sense resistor, R_{IS}. When using a buck-boost regulator topology, implement the layout of both input and output loops carefully. Make sure that these loops are as small as possible. In order to minimize parasitic inductance, ensure that the connection between all the components are short and thick. In particular, make the switch node (where L, D, and Q1 connect) just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.
- Route the CSP and CSN together with kelvin connections to the current sense resistor with traces as short as possible. If needed, use common mode and differential mode noise filters to attenuate switching and diode reverse recovery noise from affecting the internal current sense amplifier.
- Because the COMPx, ISPx, ISNx, and FBx pins are all high-impedance inputs that may couple external noise, ensure that the loops containing these nodes are minimized whenever possible.
- In some applications, the LED or LED array can be far away from the TPS92682-Q1 device, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, place the output capacitor close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.
- The TPS92682-Q1 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction-to-ambient thermal resistance varies with application. The most significant variables are the area of copper in the PCB and the number of vias under the exposed pad. The integrity of the solder connection from the device exposed pad to the PCB is critical. Excessive voids greatly decrease the thermal dissipation capacity.

10.2 Layout Example

图 10-1 shows a layout example for a CC boost LED driver, which is connected to the channel-1 of the TPS92682-Q1.

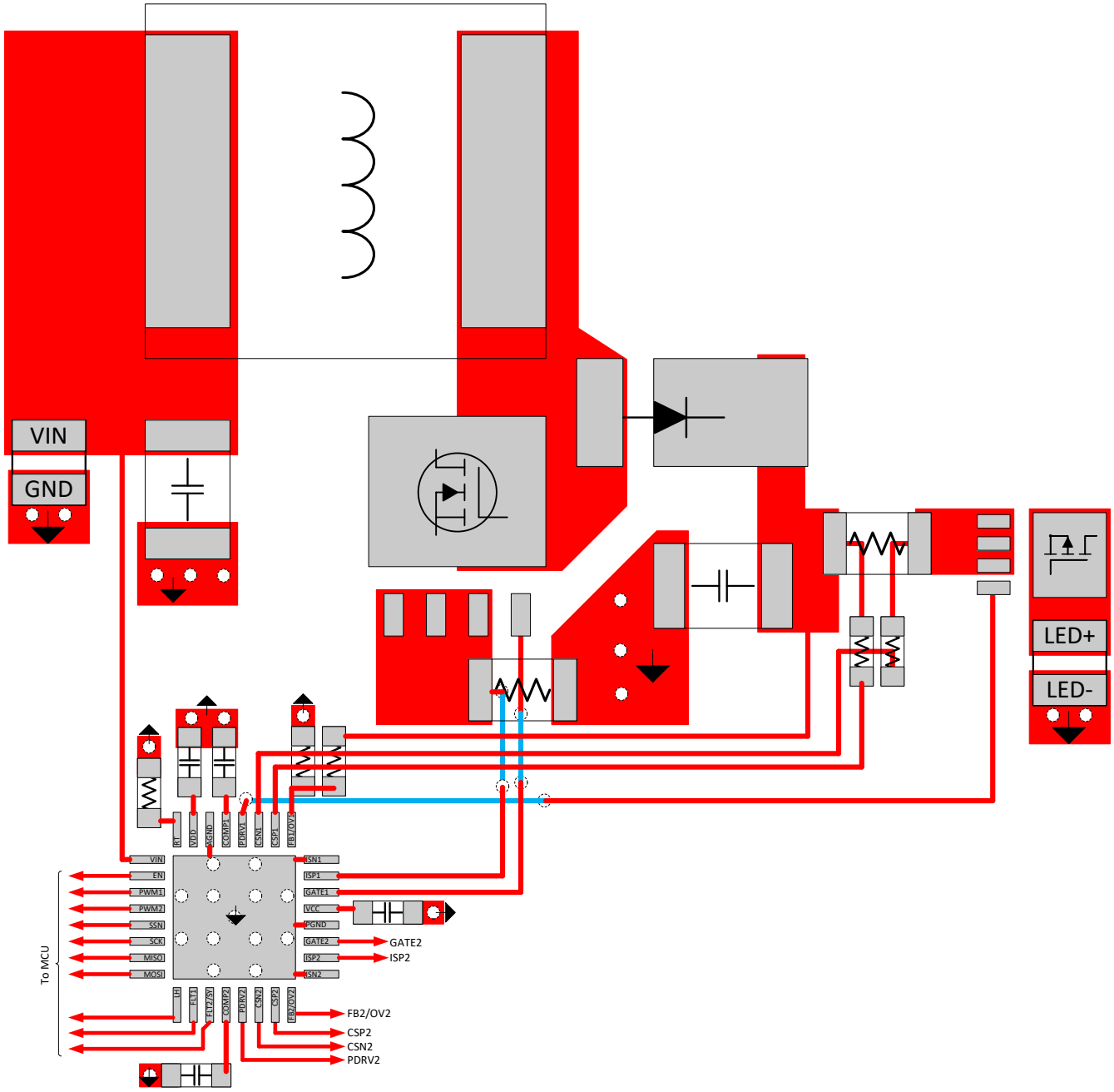


图 10-1. CC Boost Layout Example

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92682QDAPRQ1	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92682Q	Samples
TPS92682QRHBRQ1	ACTIVE	VQFN	RHB	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92682Q	Samples
TPS92682QRHMRQ1	ACTIVE	VQFN	RHM	32	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS 92682Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

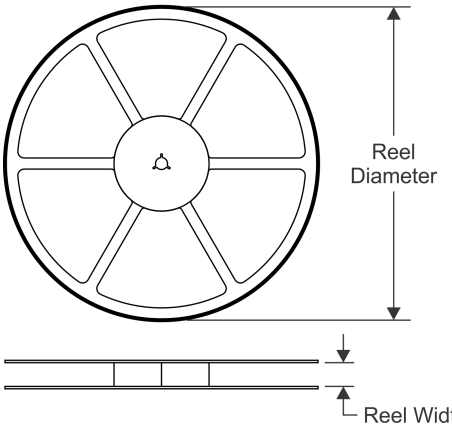
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

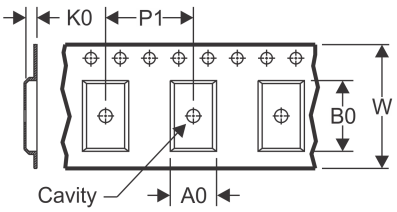
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

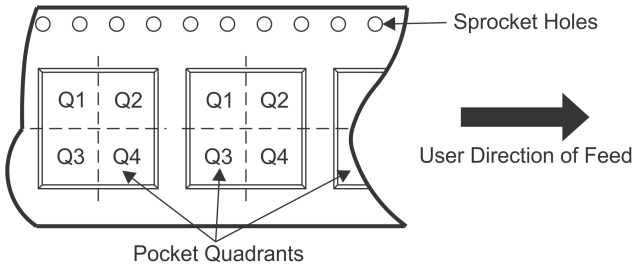


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

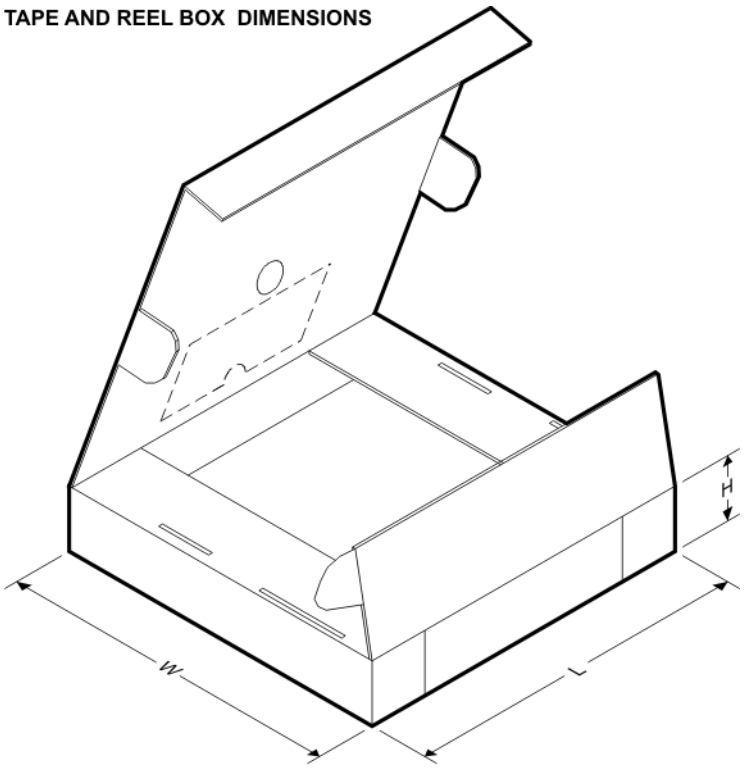
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92682QDAPRQ1	HTSSOP	DAP	32	2000	330.0	24.4	8.8	11.8	1.8	12.0	24.0	Q1
TPS92682QRHBRQ1	VQFN	RHB	32	2000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS92682QRHMRQ1	VQFN	RHM	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



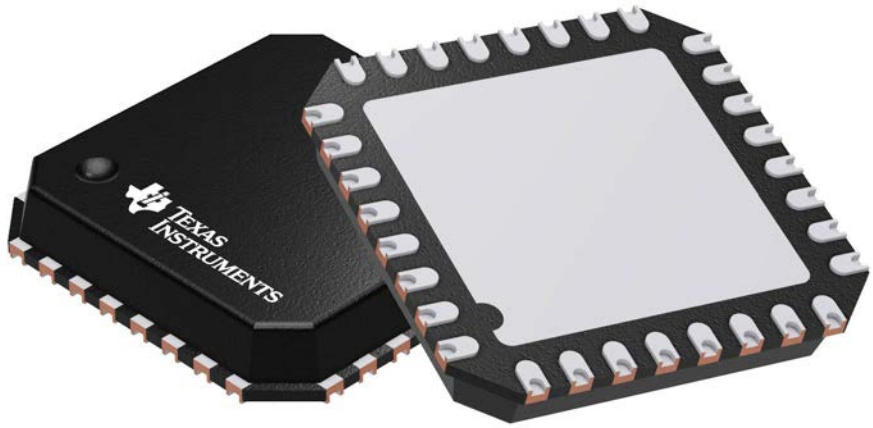
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92682QDAPRQ1	HTSSOP	DAP	32	2000	367.0	367.0	45.0
TPS92682QRHBRQ1	VQFN	RHB	32	2000	367.0	367.0	35.0
TPS92682QRHMRQ1	VQFN	RHM	32	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RHM 32 VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

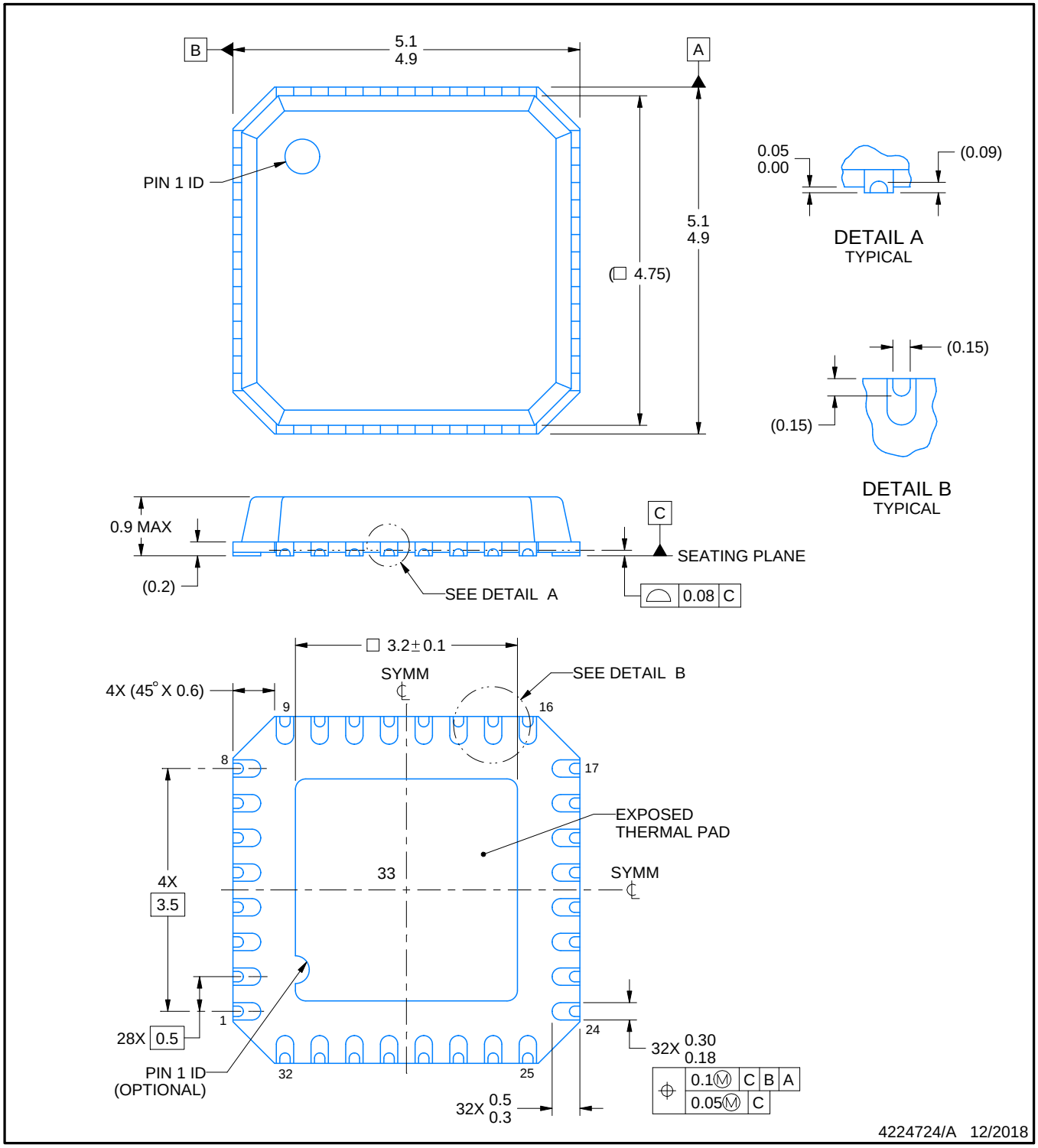
4205347/C

PACKAGE OUTLINE

RHM0032C

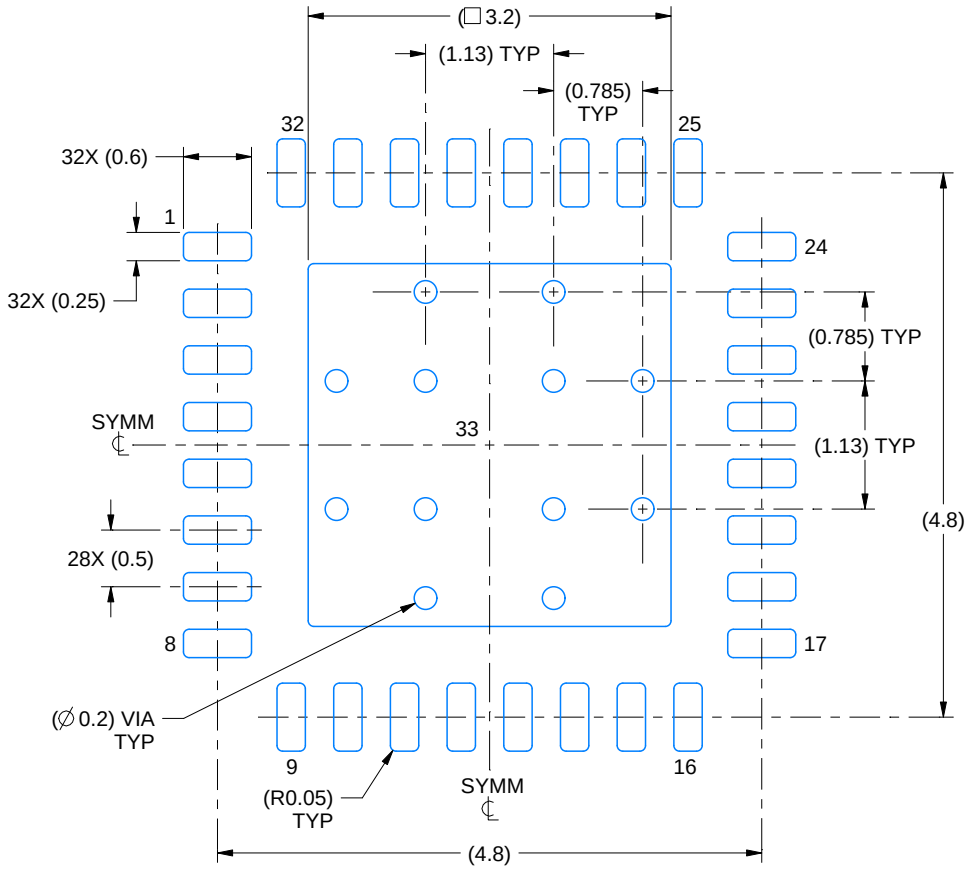
VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

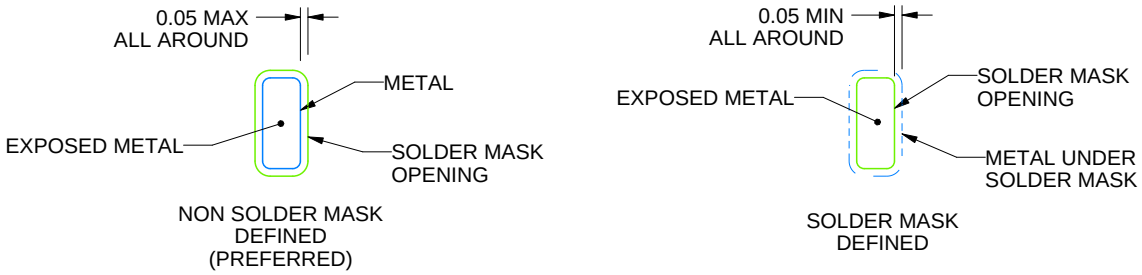


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

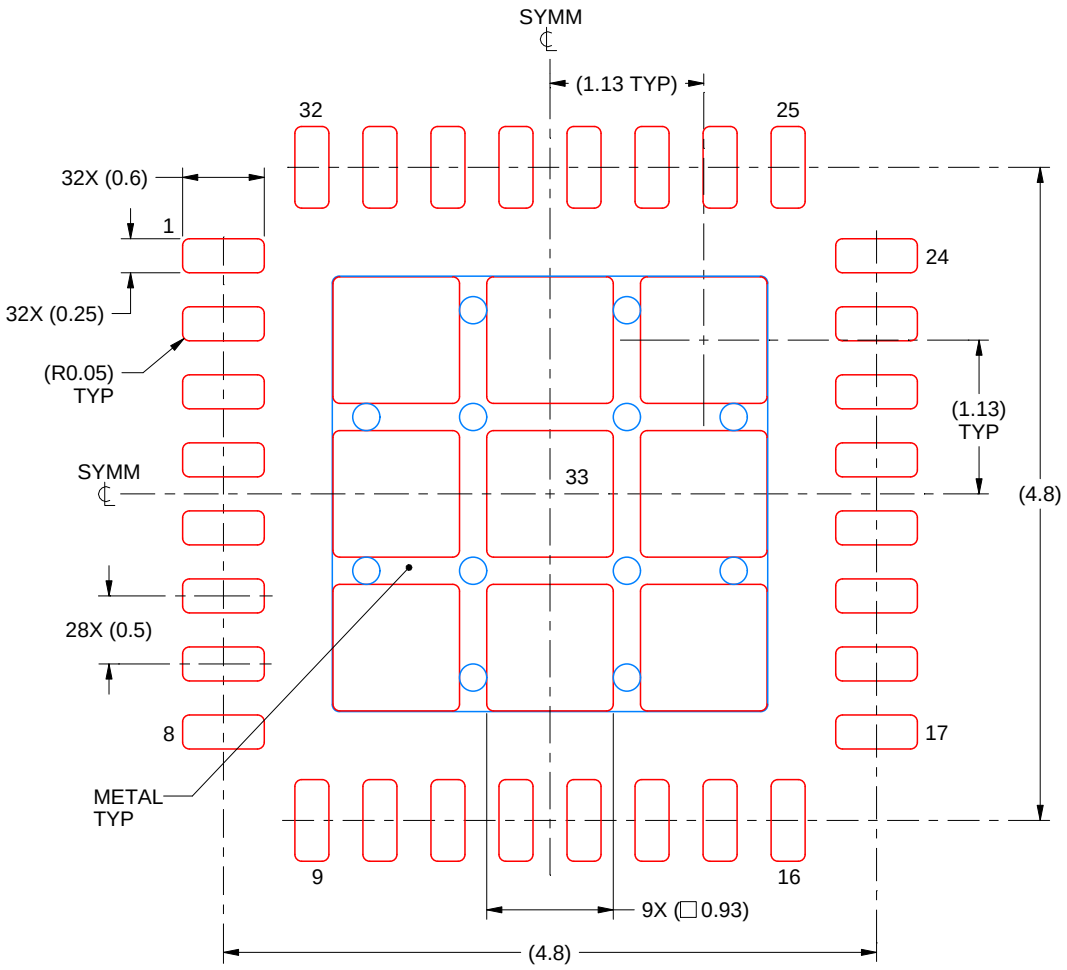


SOLDER MASK DETAILS

4224724/A 12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:18X

4224724/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

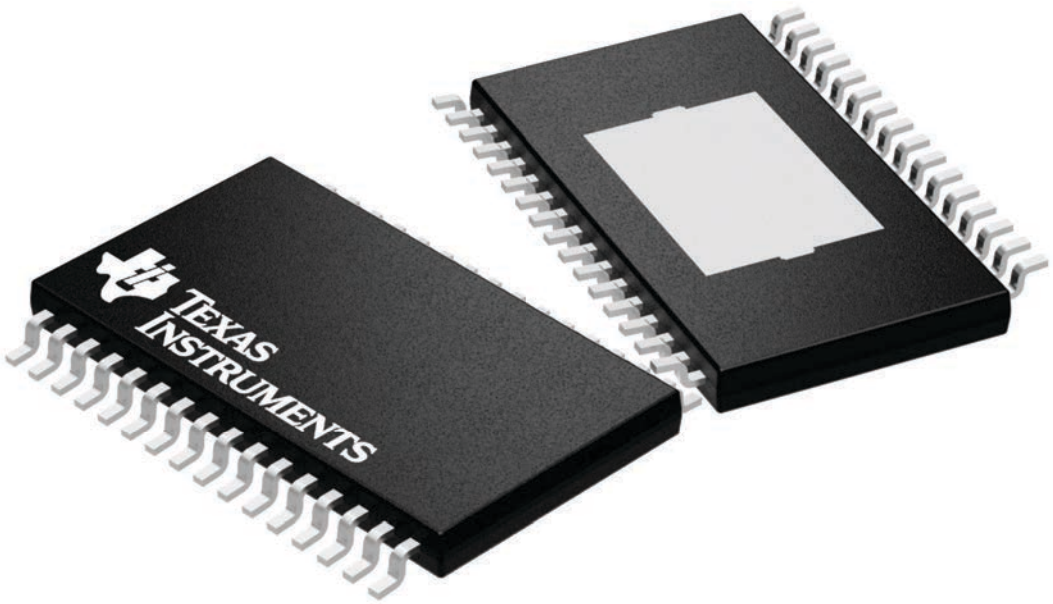
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

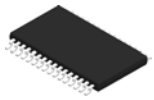
8.1 x 11, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

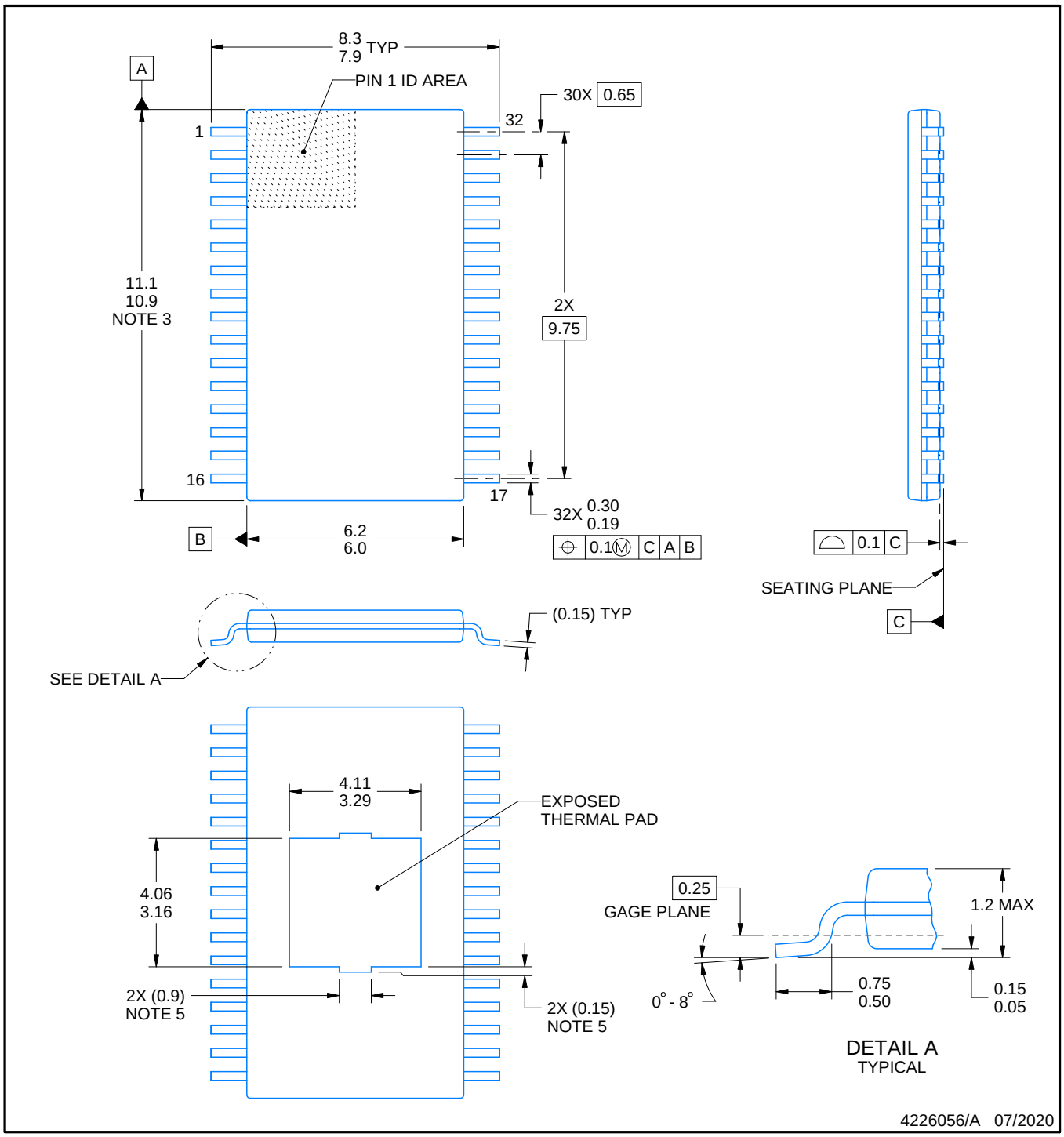


PACKAGE OUTLINE

DAP0032F

PowerPAD™ TSSOP - 1.2 mm max height

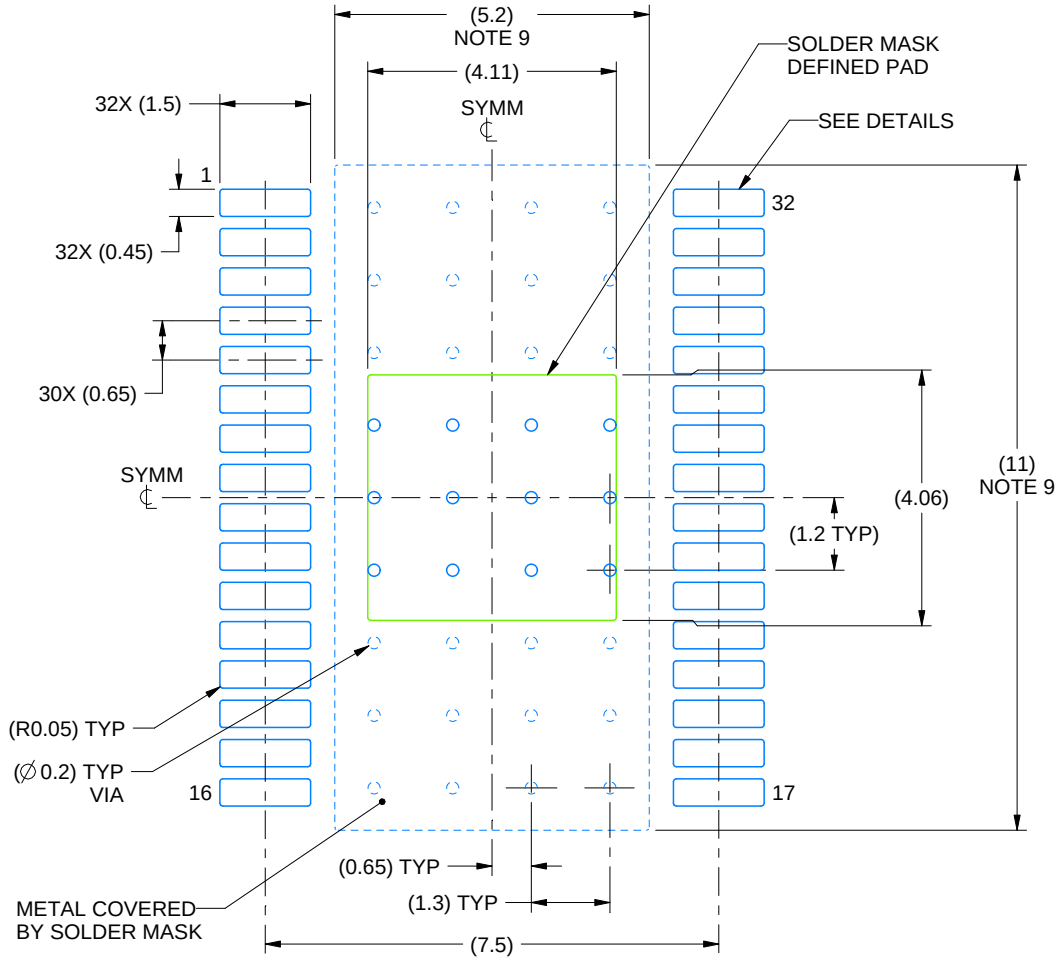
PLASTIC SMALL OUTLINE



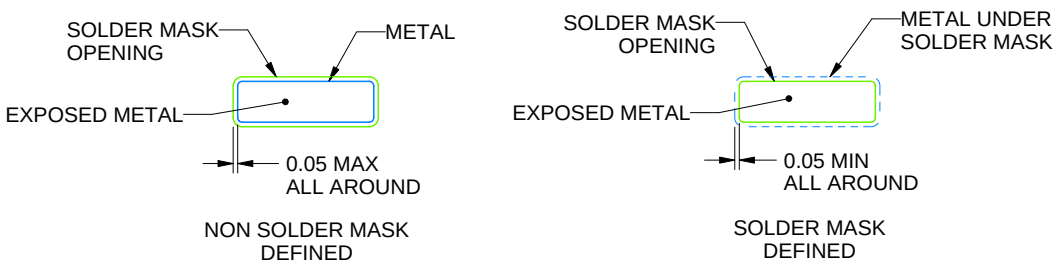
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

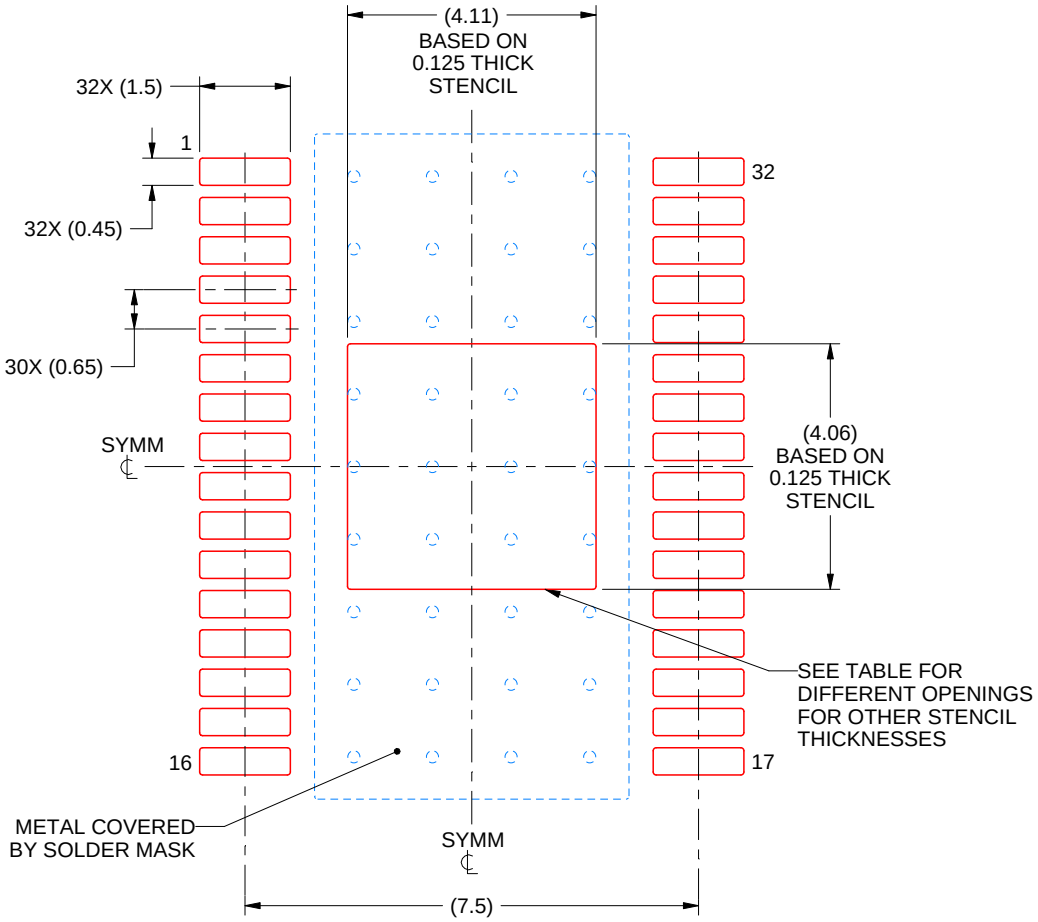


SOLDER MASK DETAILS
NOT TO SCALE

4226056/A 07/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.60 X 4.54
0.125	4.11 X 4.06 (SHOWN)
0.15	3.75 X 3.71
0.175	3.47 X 3.43

4226056/A 07/2020

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

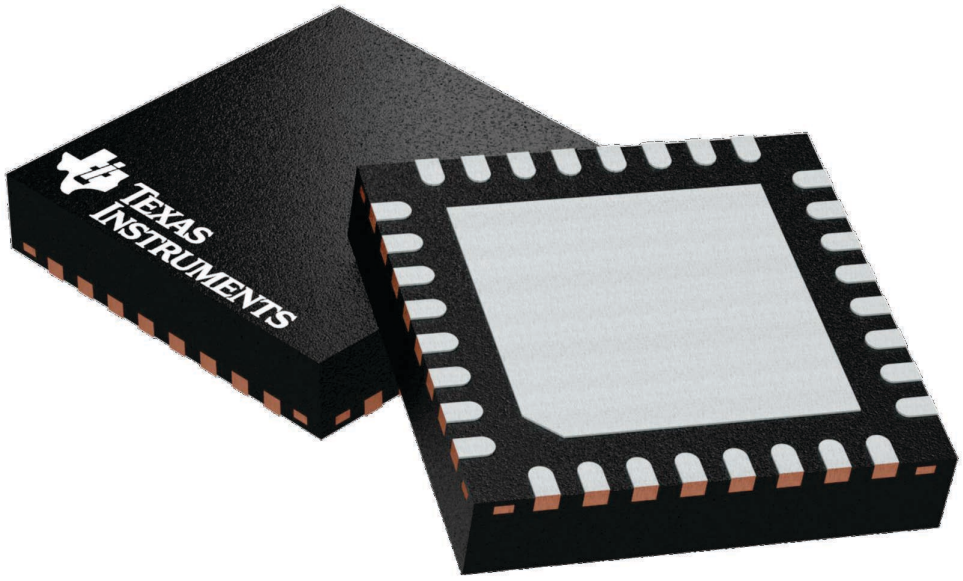
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

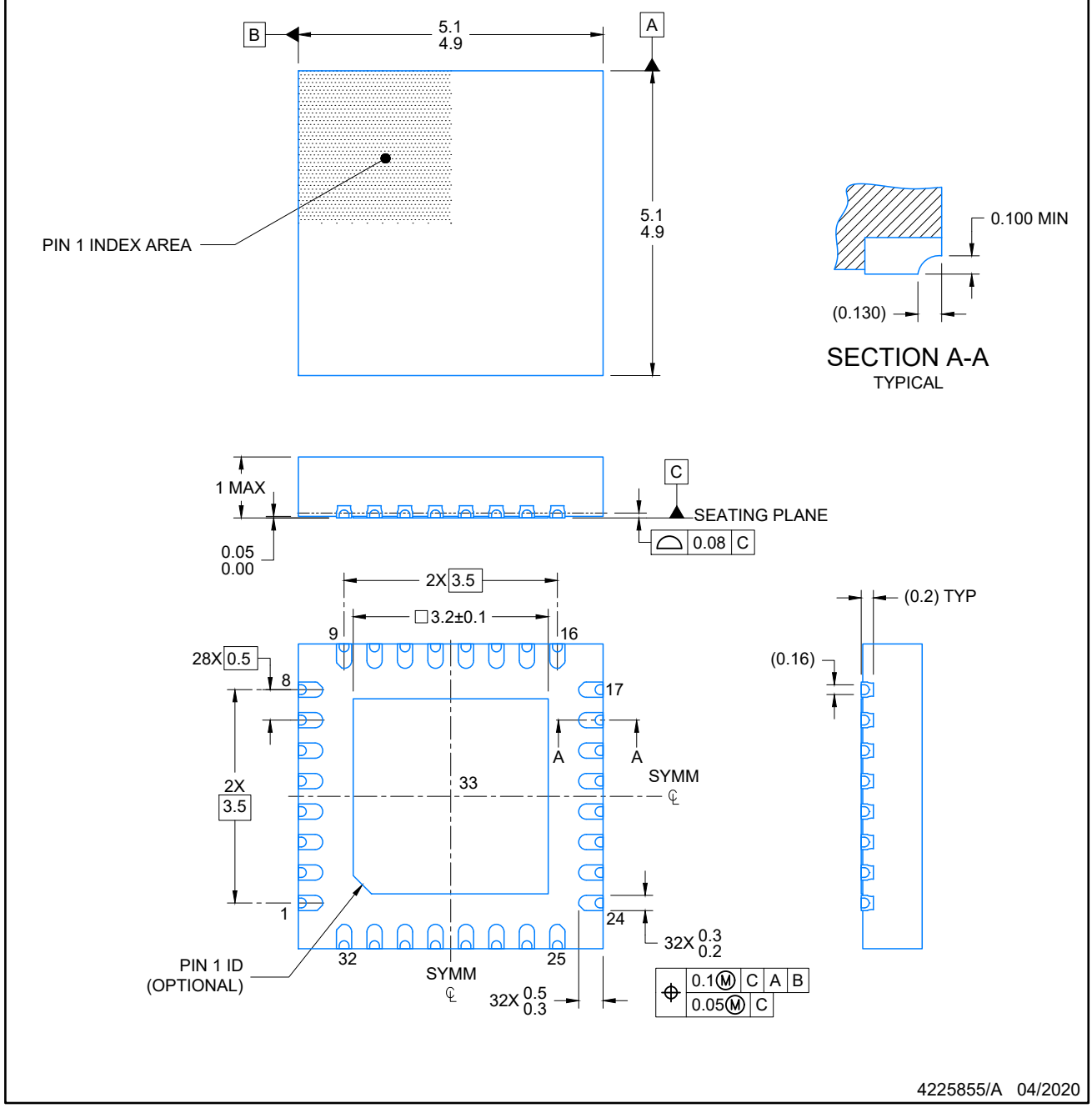
4224745/A

PACKAGE OUTLINE

RHB0032V

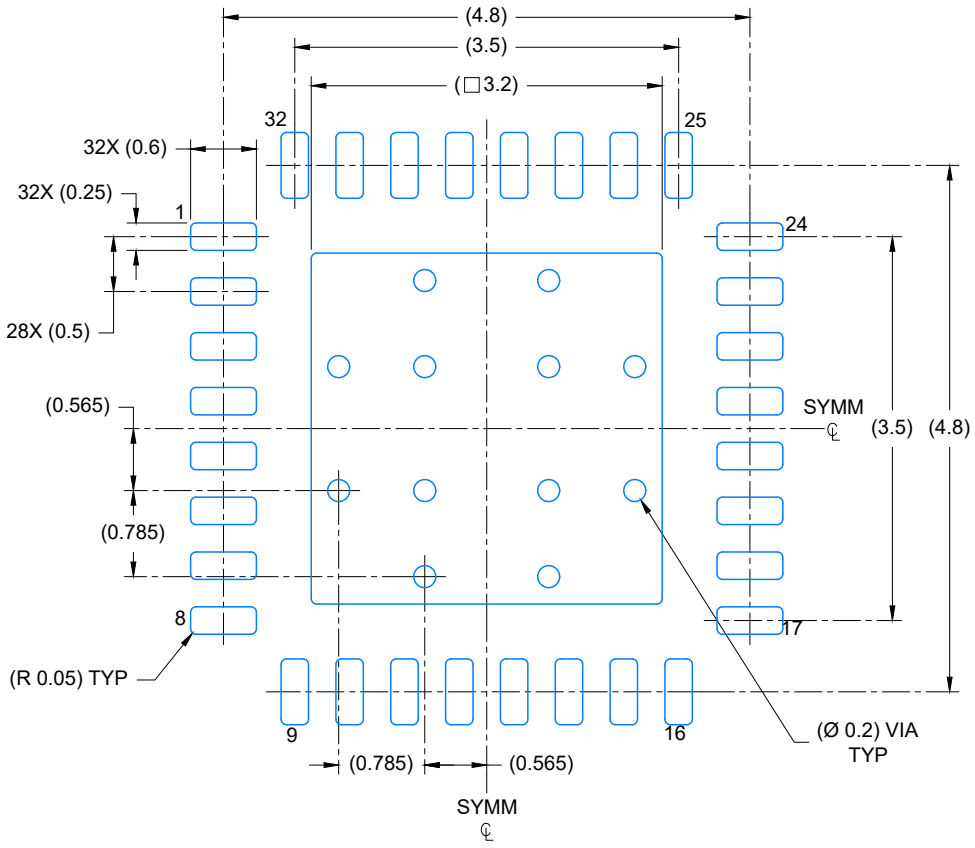
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

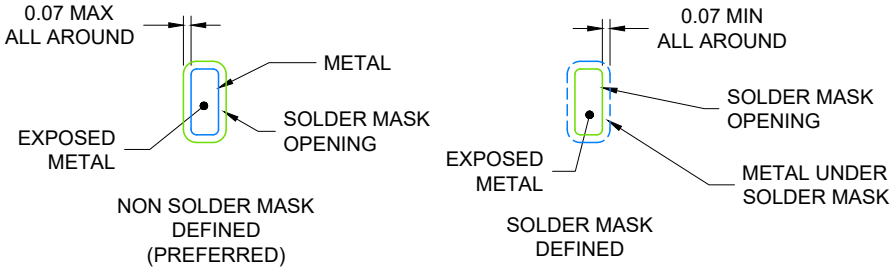


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

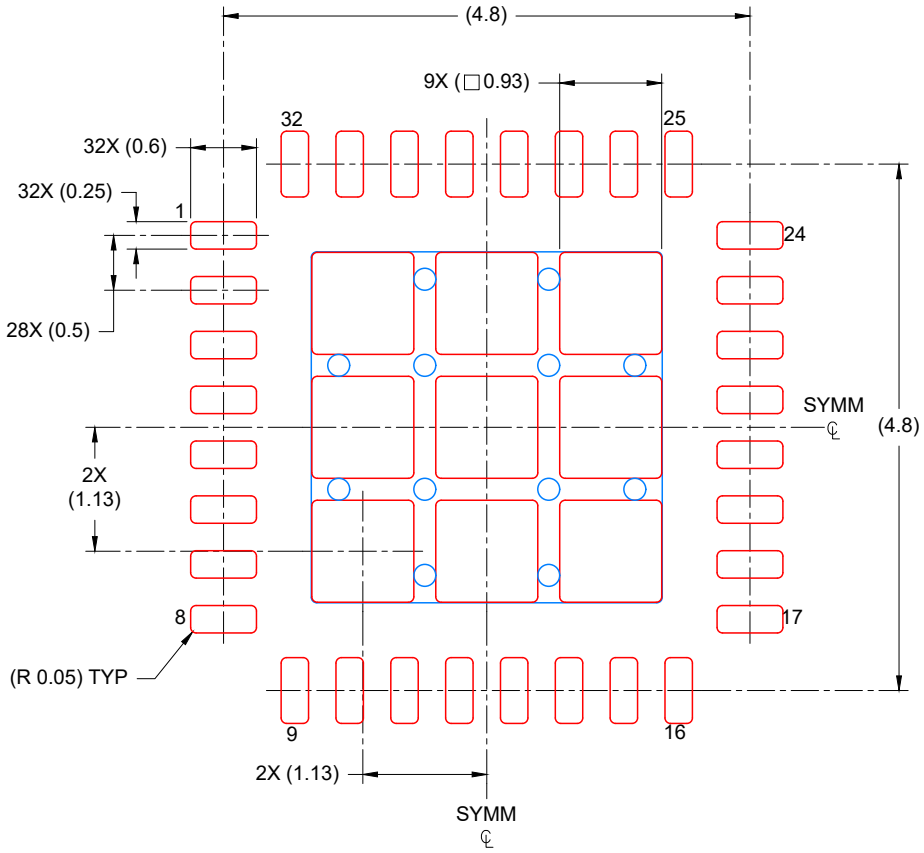


SOLDER MASK DETAILS

4225855/A 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4225855/A 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122