- 2-V to 5.5-V $V_{CC}$ Operation
- Max $t_{pd}$ of 7 ns at 5 V
- Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**SN54LV27A . . . J OR W PACKAGE**
**SN74LV27A . . . D, DB, DGV, NS, OR PW PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| 1A | 1 | 14 | $V_{CC}$ |
| 1B | 2 | 13 | 1C |
| 2A | 3 | 12 | 1Y |
| 2B | 4 | 11 | 3C |
| 2C | 5 | 10 | 3B |
| 2Y | 6 | 9 | 3A |
| GND | 7 | 8 | 3Y |
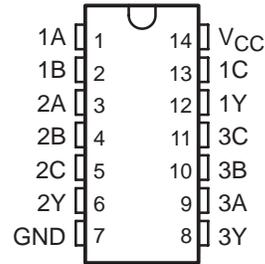
**SN54LV27A . . . FK PACKAGE**
**(TOP VIEW)**

Top pins: 1B, 1A, NC, $V_{CC}$, 1C (pins 3, 2, 1, 20, 19)

| | | |
|---|---|---|
| 2A | 4 | 18 1Y |
| NC | 5 | 17 NC |
| 2B | 6 | 16 3C |
| NC | 7 | 15 NC |
| 2C | 8 | 14 3B |

Bottom pins: 2Y, GND, NC, 3Y, 3A (pins 9, 10, 11, 12, 13)

NC – No internal connection

## description/ordering information

These triple 3-input positive-NOR gates are designed for 2-V to 5.5-V $V_{CC}$ operation.

The 'LV27A devices perform the Boolean function $Y = \overline{A + B + C}$ or $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ in positive logic.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### ORDERING INFORMATION

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SOIC – D | Tube of 50 | SN74LV27AD | LV27A |
| | | Reel of 2500 | SN74LV27ADR | |
| | SOP – NS | Reel of 2000 | SN74LV27ANSR | 74LV27A |
| | SSOP – DB | Reel of 2000 | SN74LV27ADBR | LV27A |
| | TSSOP – PW | Tube of 90 | SN74LV27APW | LV27A |
| | | Reel of 2000 | SN74LV27APWR | |
| | | Reel of 250 | SN74LV27APWT | |
| | TVSOP – DGV | Reel of 2000 | SN74LV27ADGVR | LV27A |
| −55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LV27AJ | SNJ54LV27AJ |
| | CFP – W | Tube of 150 | SNJ54LV27AW | SNJ54LV27AW |
| | LCCC – FK | Tube of 55 | SNJ54LV27AFK | SNJ54LV27AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**TEXAS INSTRUMENTS**

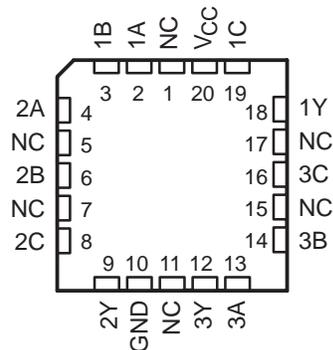POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LV27A, SN74LV27A
# TRIPLE 3-INPUT POSITIVE-NOR GATE

SCES341E – SEPTEMBER 2000 – REVISED APRIL 2005

**FUNCTION TABLE**
(each gate)

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | X | X | L |
| X | H | X | L |
| X | X | H | L |
| L | L | L | H |

**logic diagram, each gate (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 7 V
Output voltage range applied in high or low state, $V_O$ (see Notes 1 and 2) . . . . . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Output voltage range applied in power-off state, $V_O$ (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 86°C/W
DB package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 96°C/W
DGV package . . . . . . . . . . . . . . . . . . . . . . . . . . . . 127°C/W
NS package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 76°C/W
PW package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 113°C/W
Storage temperature range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
        2. This value is limited to 5.5 V maximum.
        3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | SN54LV27A | | SN74LV27A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | −50 | | −50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | −2 | | −2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | −6 | | −6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | −12 | | −12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN54LV27A | | | SN74LV27A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 µA | 2 V to 5.5 V | $V_{CC}$−0.1 | | | $V_{CC}$−0.1 | | | V |
| | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | 2 | | | |
| | $I_{OH}$ = −6 mA | 3 V | 2.48 | | | 2.48 | | | |
| | $I_{OH}$ = −12 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.44 | |
| | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND,   $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | | | 5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 1.9 | | | 1.9 | | pF |

**TEXAS INSTRUMENTS**

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3

# SN54LV27A, SN74LV27A
## TRIPLE 3-INPUT POSITIVE-NOR GATE

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV27A | | SN74LV27A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | $C_L$ = 15 pF | | 6.7* | 13.8* | 1* | 16* | 1 | 16 | ns |
| $t_{pd}$ | A, B, or C | Y | $C_L$ = 50 pF | | 9.5 | 17.5 | 1 | 21 | 1 | 21 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV27A | | SN74LV27A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | $C_L$ = 15 pF | | 5* | 8.8* | 1* | 10.5* | 1 | 10.5 | ns |
| $t_{pd}$ | A, B, or C | Y | $C_L$ = 50 pF | | 6.9 | 12.3 | 1 | 14 | 1 | 14 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV27A | | SN74LV27A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A, B, or C | Y | $C_L$ = 15 pF | | 3.9* | 5.9* | 1* | 7* | 1 | 7 | ns |
| $t_{pd}$ | A, B, or C | Y | $C_L$ = 50 pF | | 5.2 | 7.9 | 1 | 9 | 1 | 9 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

## noise characteristics, $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

| PARAMETER | | SN74LV27A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.2 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | 0 | −0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3.2 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

NOTE 5: Characteristics are for surface-mount packages only.
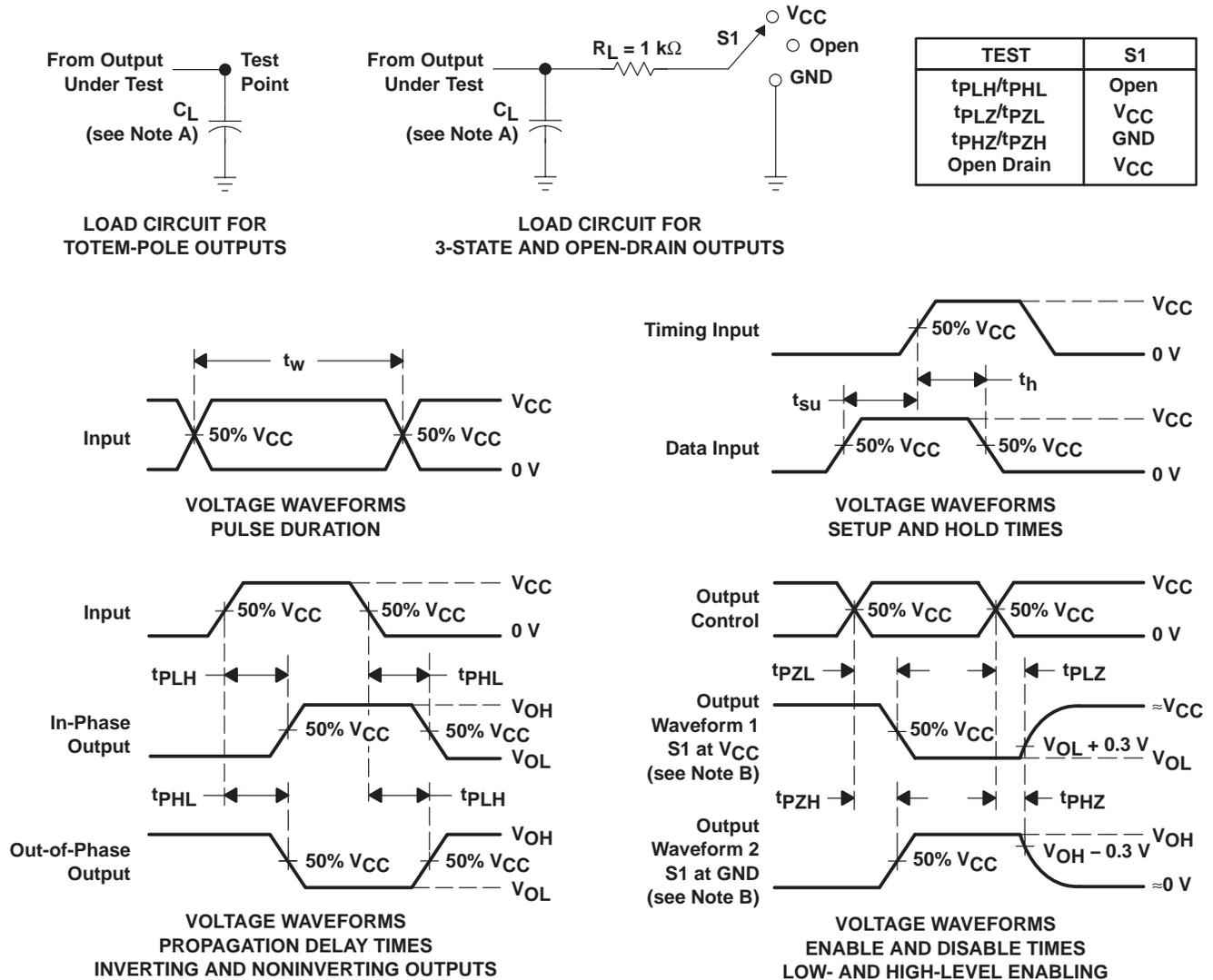
## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF,　f = 10 MHz | 3.3 V | 13.7 | pF |
| | | | 5 V | 15 | |

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## PARAMETER MEASUREMENT INFORMATION

| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

**LOAD CIRCUIT FOR**
**TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR**
**3-STATE AND OPEN-DRAIN OUTPUTS**

**VOLTAGE WAVEFORMS**
**PULSE DURATION**

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
        Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
     D. The outputs are measured one at a time, with one input transition per measurement.
     E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
     F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
     G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
     H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV27AD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27ADBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27ADG4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27ANSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV27A | Samples |
| SN74LV27APW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |
| SN74LV27APWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV27A | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
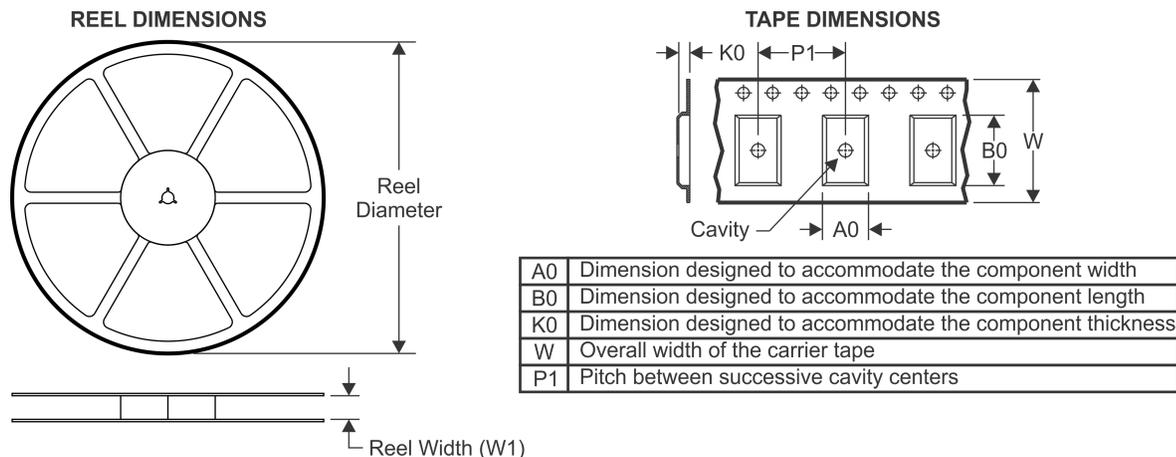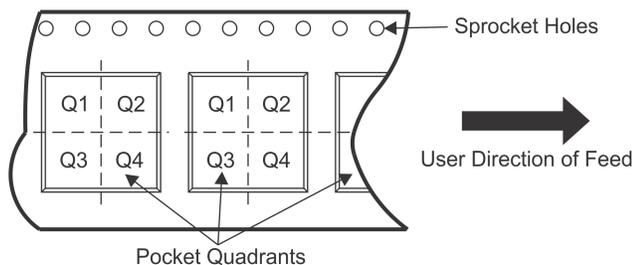
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

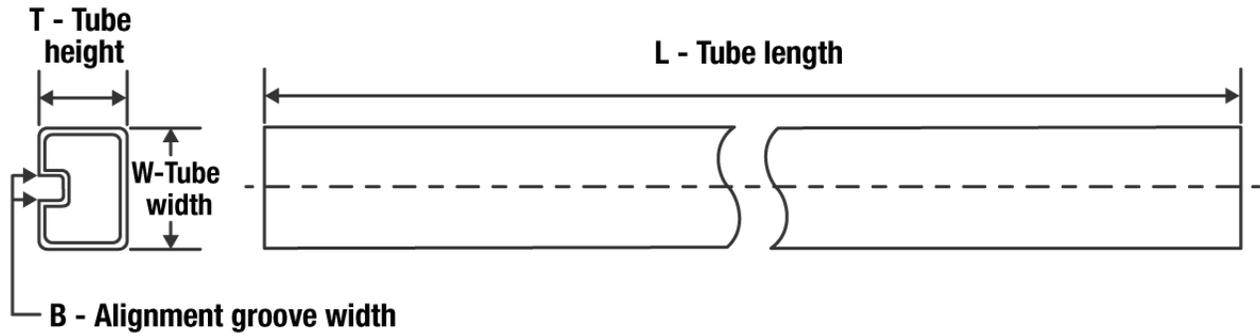**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV27ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV27ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV27ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV27ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV27APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV27APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**
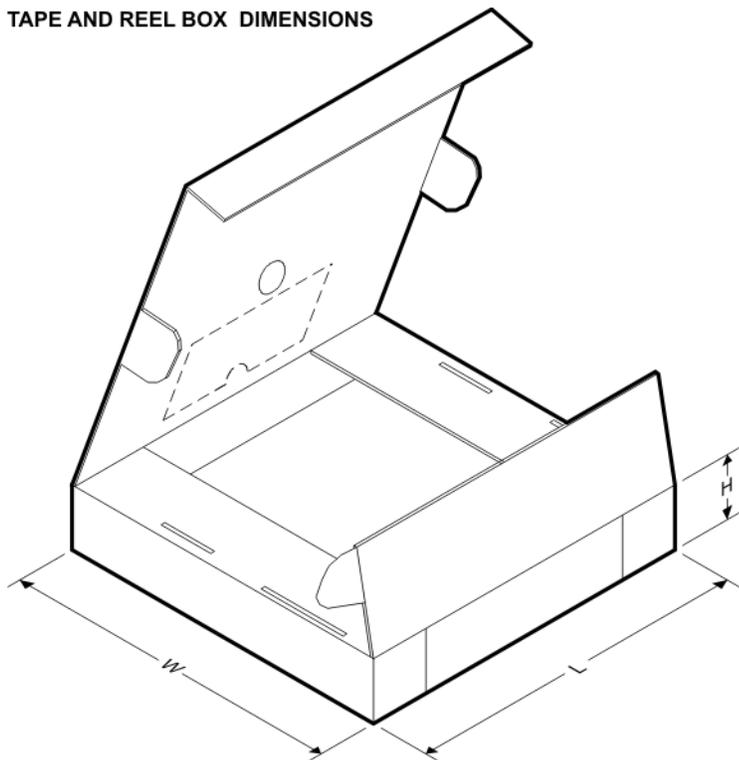


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV27ADBR | SSOP | DB | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV27ADGVR | TVSOP | DGV | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV27ADR | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| SN74LV27ANSR | SO | NS | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV27APWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LV27APWT | TSSOP | PW | 14 | 250 | 853.0 | 449.0 | 35.0 |

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

## TUBE



T - Tube height
L - Tube length
W - Tube width
B - Alignment groove width

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LV27AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LV27ADG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LV27APW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

## MECHANICAL DATA

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**
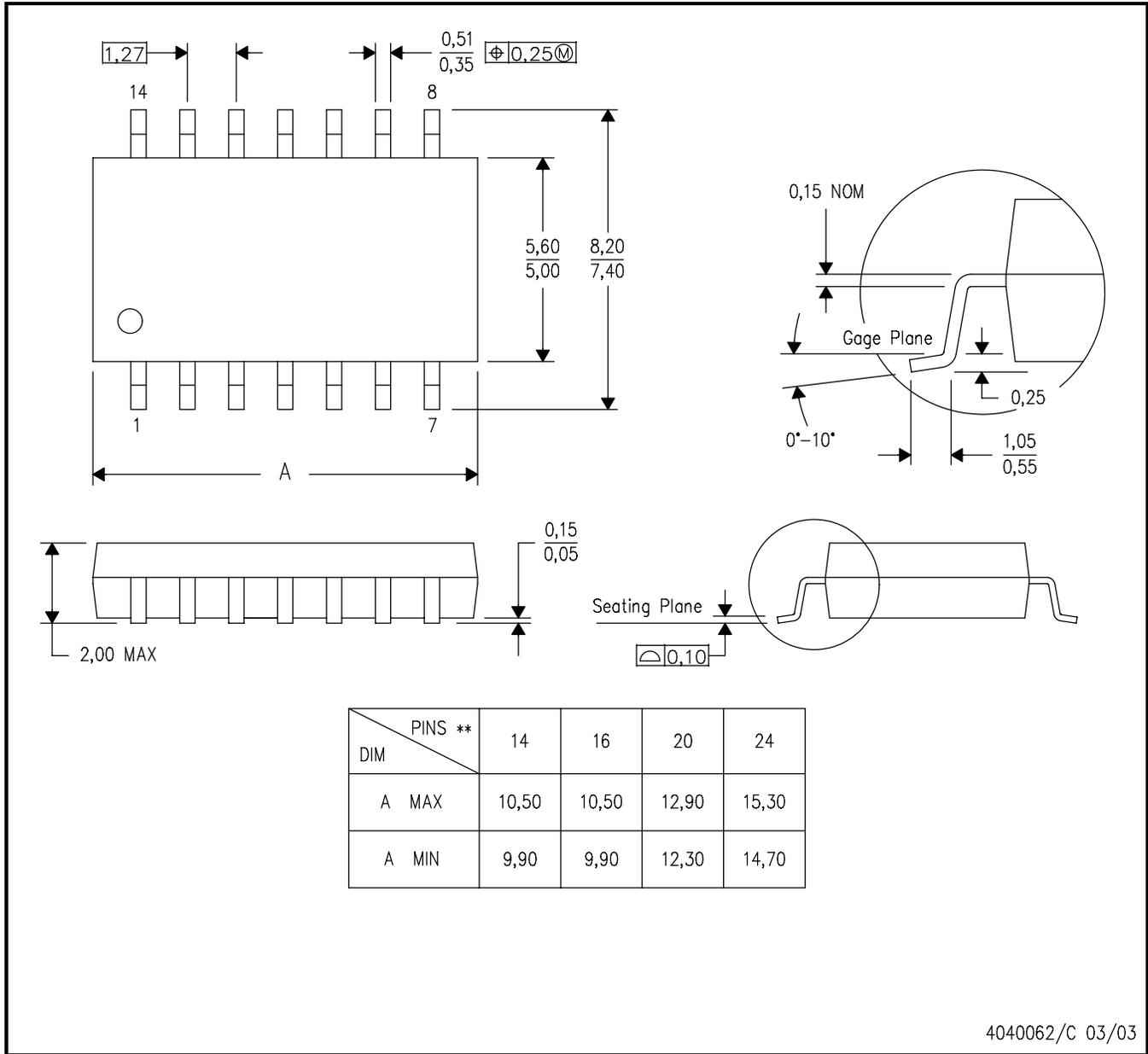


| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A   MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A   MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03
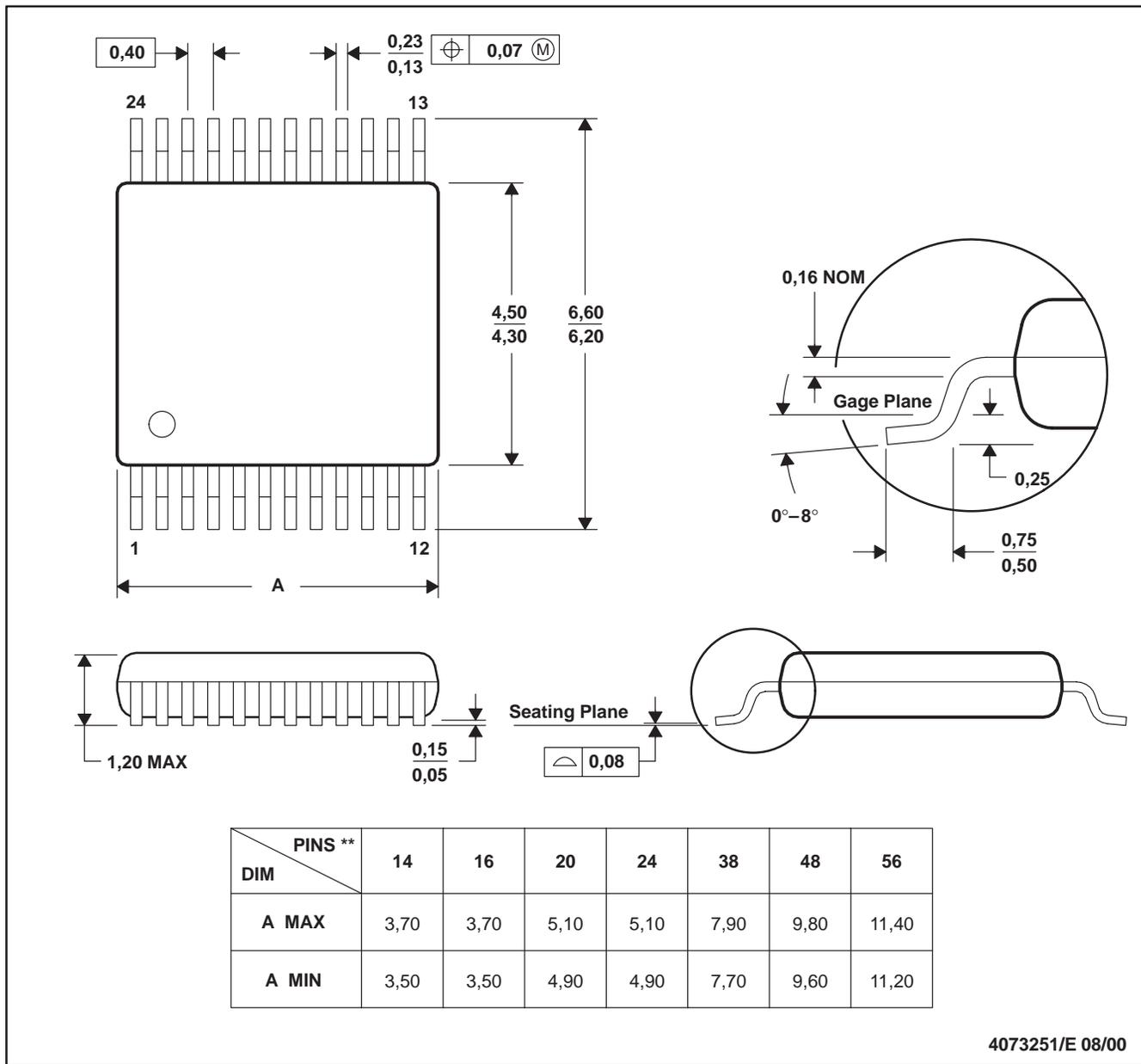
NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

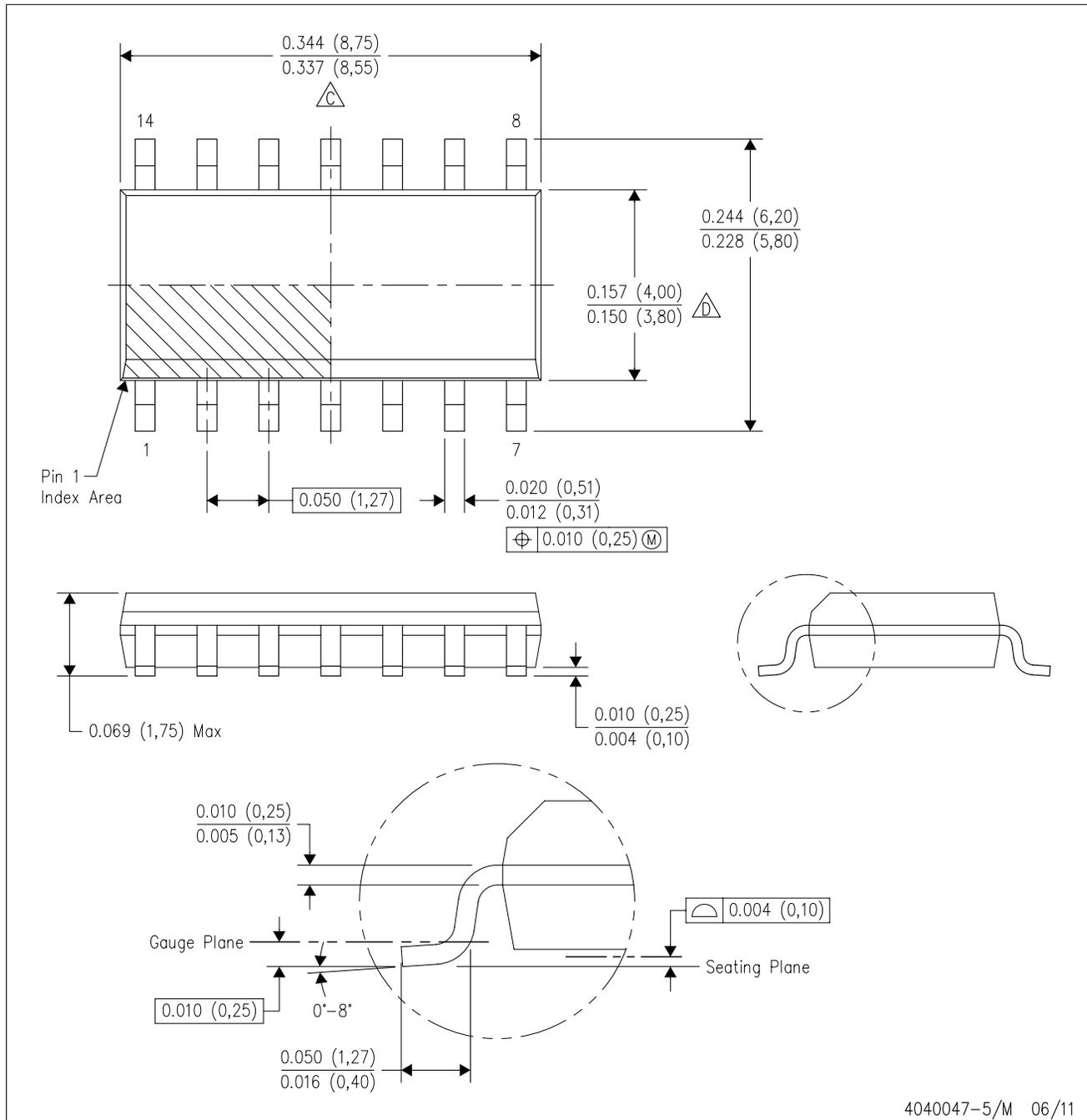**DGV (R-PDSO-G\*\*)**                      **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**



| DIM \ PINS \*\* | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
         D. Falls within JEDEC:  24/48 Pins – MO-153
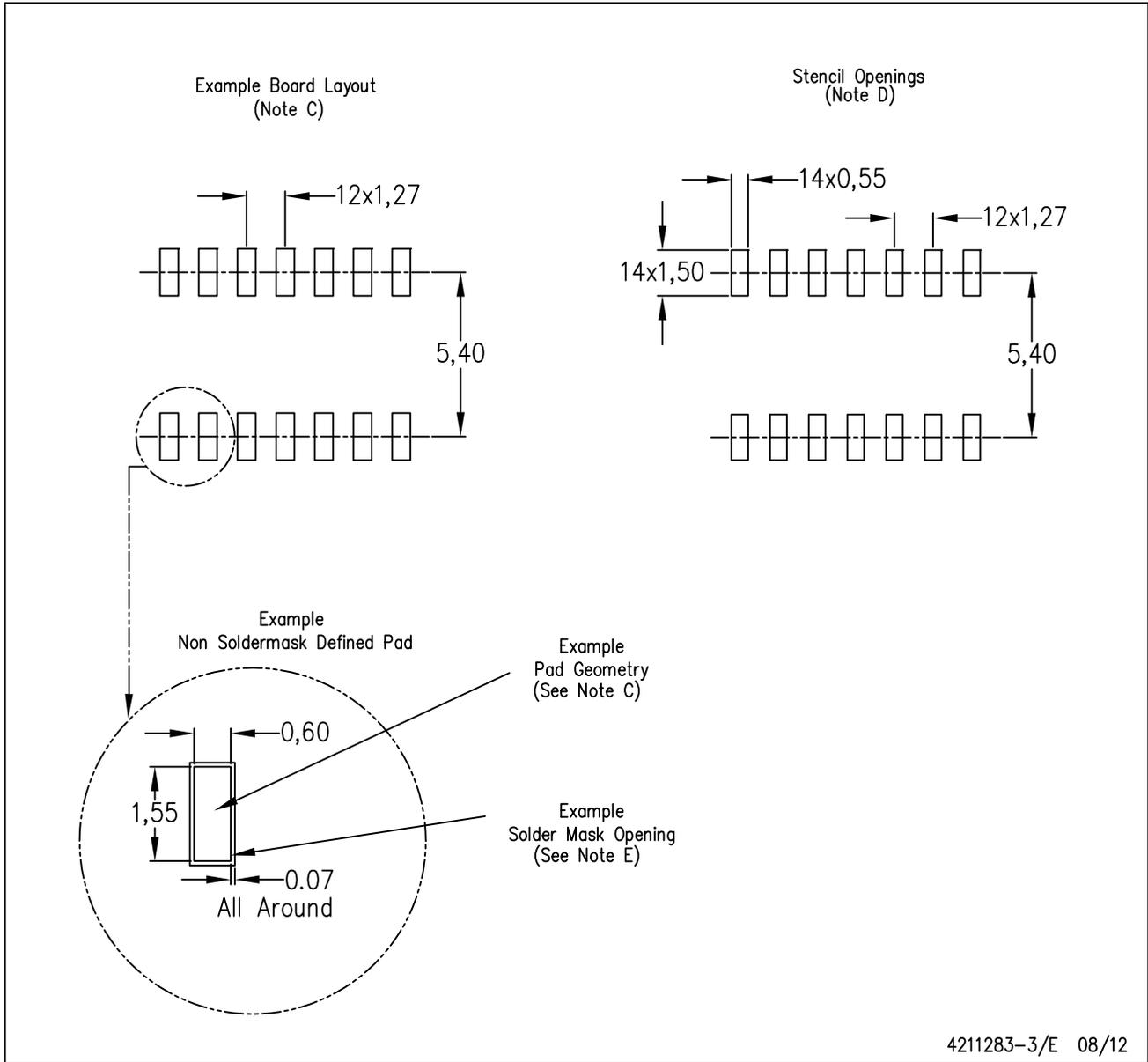                              14/16/20/56 Pins – MO-194

D (R−PDSO−G14)                                    PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
⟨C⟩

14                           8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)  ⟨D⟩

1                            7

Pin 1
Index Area

0.050 (1,27)        0.020 (0,51)
                    0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)      0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
         ⟨C⟩  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
         ⟨D⟩  Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
         E.  Reference JEDEC MS−012 variation AB.

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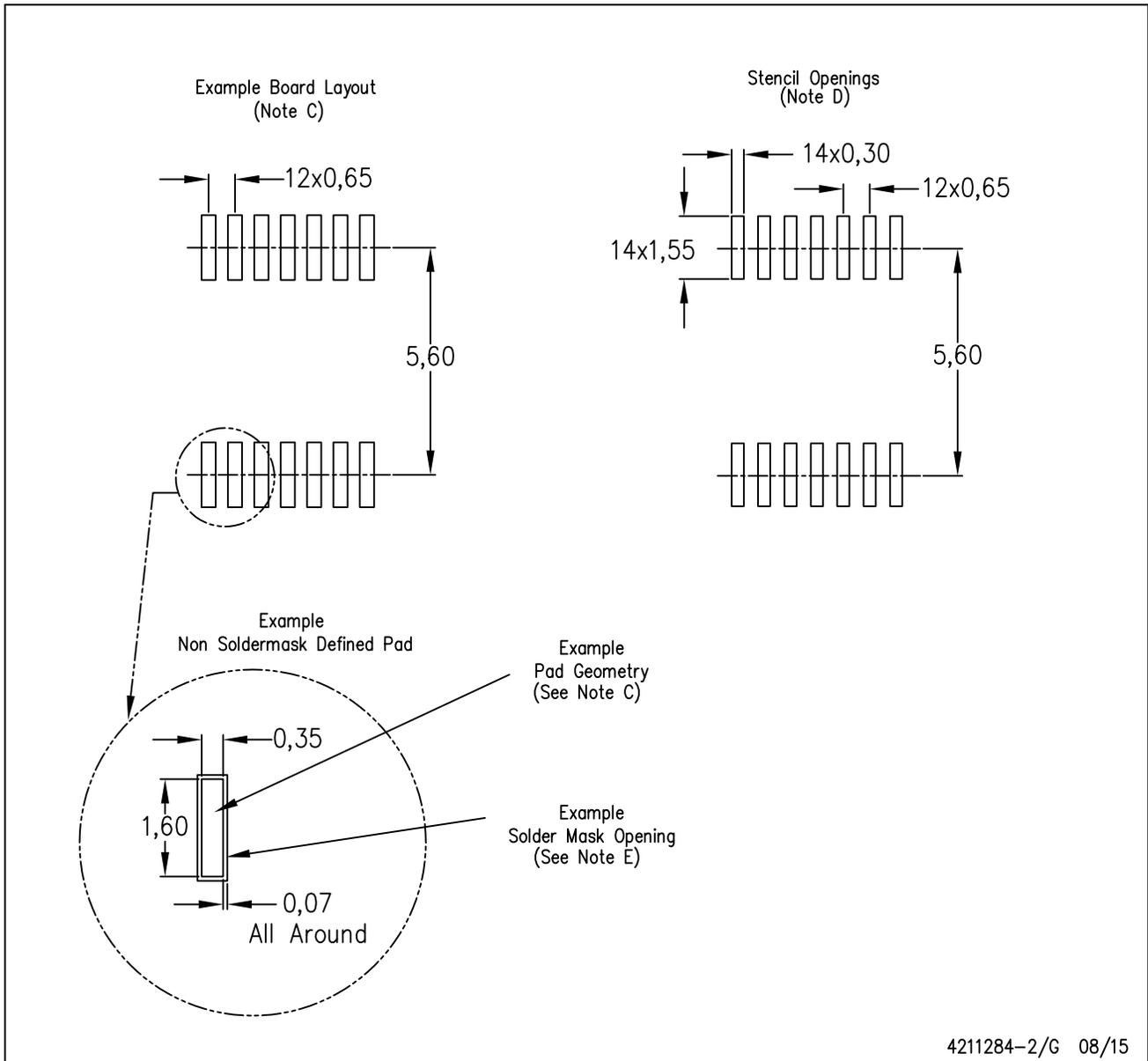
D (R−PDSO−G14)                                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x1,27

5,40

Stencil Openings
(Note D)

14x0,55

14x1,50

12x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

0,60

1,55

0.07
All Around

4211283−3/E  08/12

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

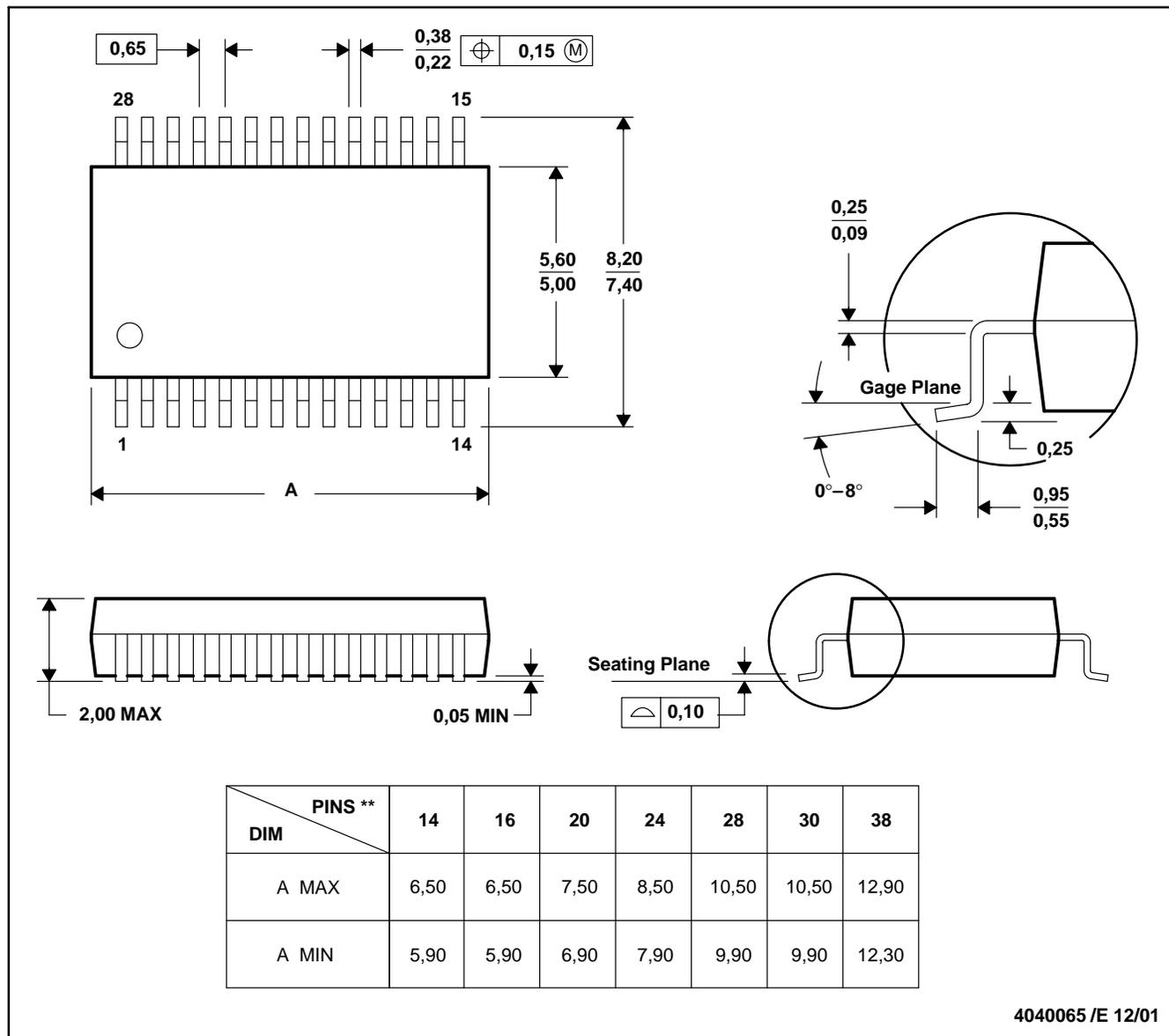PW (R−PDSO−G14)                                      PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14                    8

Ⓓ   4,50
     4,30

6,60
6,20

1                     7

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

△ 0,10

4040064−3/G  02/11

NOTES:   A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
         Ⓒ  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
         Ⓓ  Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.  Falls within JEDEC MO−153

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PW (R−PDSO−G14)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x0,65

5,60

Stencil Openings
(Note D)

14x0,30

14x1,55        12x0,65

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

0,07
All Around

Example
Solder Mask Opening
(See Note E)

4211284−2/G  08/15

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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**DB (R-PDSO-G\*\*)**                                                    **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**

| PINS \*\* DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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