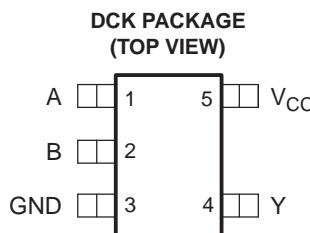


## FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of -55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree <sup>(1)</sup>**
- **Supports 5-V V<sub>CC</sub> Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t<sub>pd</sub> of 6.7 ns at 3.3 V**
- **Low Power Consumption, 15-µA Max I<sub>cc</sub>**
- **±24-mA Output Drive at 3.3 V**
- **I<sub>off</sub> Supports Partial-Power-Down Mode Operation**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over specified temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G86 performs the Boolean function  $Y = A \oplus B$  or  $Y = \bar{A}B + A\bar{B}$  in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
-55°C to 125°C	SOT (SC-70) – DCK	SN74LVC1G86MDCKREP	CJ_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) DCK: The actual top-side marking has one additional character that designates the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE**

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

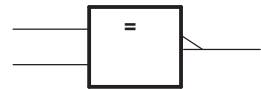
**EXCLUSIVE-OR LOGIC**

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



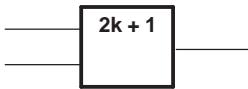
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

**EVEN-PARITY ELEMENT**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		252	$^{\circ}\text{C}/\text{W}$
$T_{stg}$	Storage temperature range	-65	150	$^{\circ}\text{C}$

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74LVC1G86-EP

## SINGLE 2-INPUT EXCLUSIVE-OR GATE

SCES679—JULY 2007

 **TEXAS  
INSTRUMENTS**  
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### Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 X V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 X V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 X V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.3 X V <sub>CC</sub>		
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		-4	mA
		V <sub>CC</sub> = 2.3 V		-8	
		V <sub>CC</sub> = 3 V		-16	
		V <sub>CC</sub> = 4.5 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
		V <sub>CC</sub> = 4.5 V		24	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V		10	
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>A</sub>	Operating free-air temperature		-55	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-55°C to 125°C		UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1		V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -4 mA	1.65 V		1.2			1.2	
	I <sub>OH</sub> = -8 mA	2.3 V		1.9			1.9	
	I <sub>OH</sub> = -16 mA	3 V		2.4			2.4	
	I <sub>OH</sub> = -24 mA			2.3			2.3	
	I <sub>OH</sub> = -32 mA	4.5 V		3.8			3.8	
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 5.5 V			0.1		0.1	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45		0.45	
	I <sub>OL</sub> = 8 mA	2.3 V			0.3		0.3	
	I <sub>OL</sub> = 16 mA	3 V			0.4		0.4	
	I <sub>OL</sub> = 24 mA				0.55		0.55	
	I <sub>OL</sub> = 32 mA	4.5 V			0.55		0.55	
I <sub>I</sub>	A or B input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±5		±5	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0		±10		±10	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10		15	µA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500		500	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			6			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Figure 2](#))

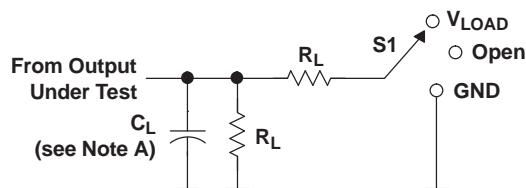
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	1.3	6.7	1	5.7	ns

## Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 3.3 V		V <sub>CC</sub> = 5 V		UNIT
		MIN	MAX	MIN	MAX	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz		22	24	pF

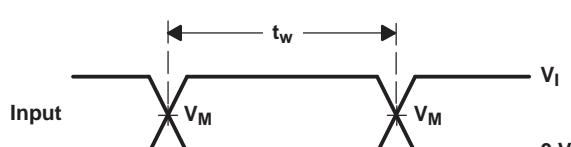
**PARAMETER MEASUREMENT INFORMATION**



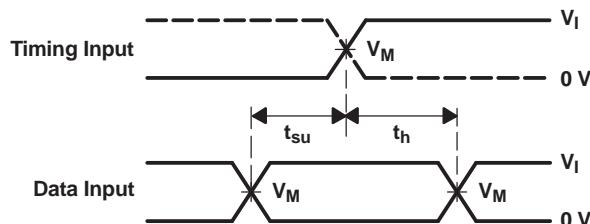
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

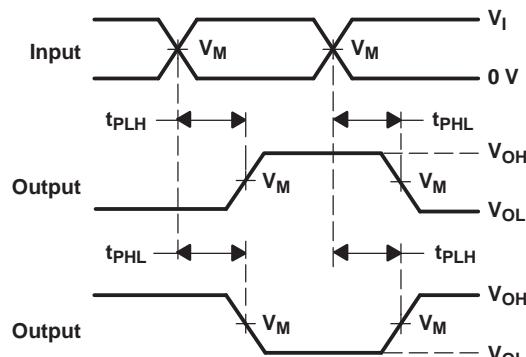
V <sub>CC</sub>	INPUTS		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
	V <sub>I</sub>	t <sub>r/t<sub>f</sub></sub>					
1.8 V $\pm$ 0.15 V	V <sub>CC</sub>	$\leq 2$ ns	V <sub>CC</sub> /2	2 $\times$ V <sub>CC</sub>	15 pF	1 M $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	V <sub>CC</sub>	$\leq 2$ ns	V <sub>CC</sub> /2	2 $\times$ V <sub>CC</sub>	15 pF	1 M $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	$\leq 2.5$ ns	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
5 V $\pm$ 0.5 V	V <sub>CC</sub>	$\leq 2.5$ ns	V <sub>CC</sub> /2	2 $\times$ V <sub>CC</sub>	15 pF	1 M $\Omega$	0.3 V



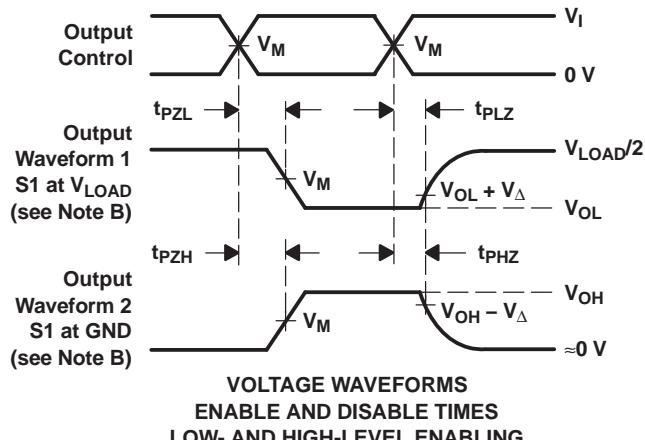
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



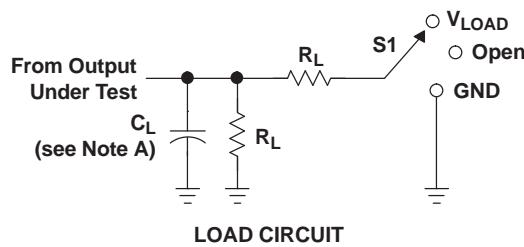
VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- H. All parameters and waveforms are not applicable to all devices.

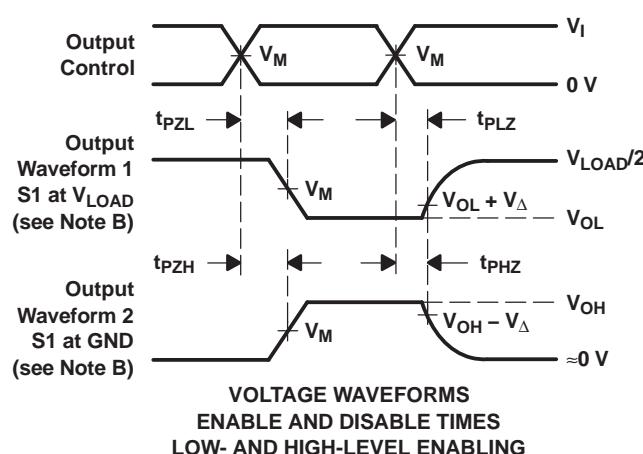
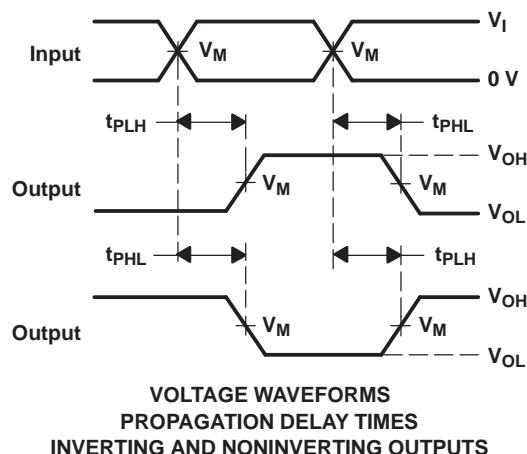
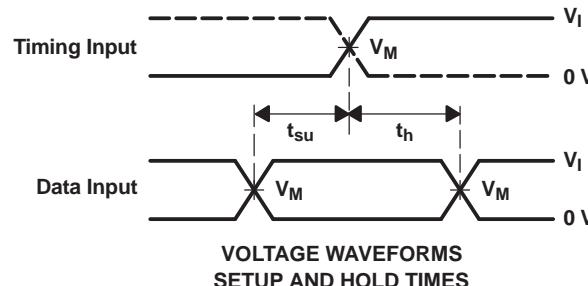
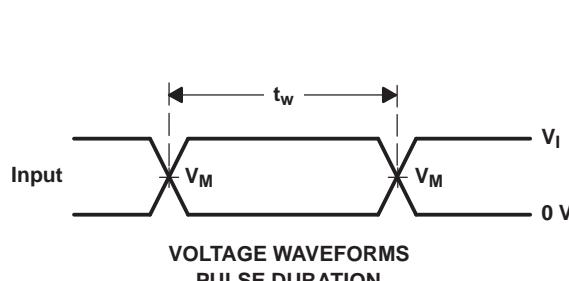
**Figure 1. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

V <sub>CC</sub>	INPUTS		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
	V <sub>I</sub>	t <sub>r/t<sub>f</sub></sub>					
1.8 V ± 0.15 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>CC</sub>	≤ 2.5 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G86MDCKREP	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CJY	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
V62/06666-01XE	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CJY	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

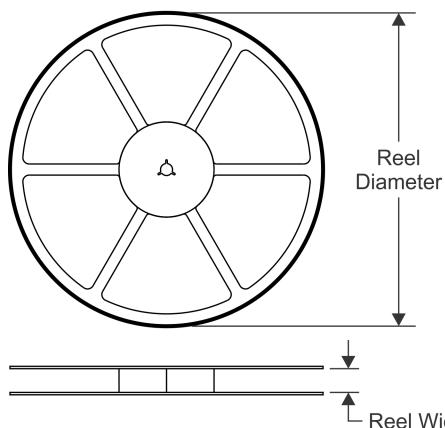
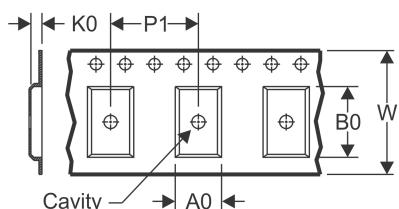
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G86-EP :**

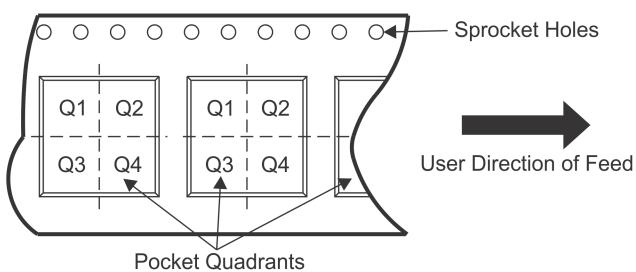
- Catalog: [SN74LVC1G86](#)
- Automotive: [SN74LVC1G86-Q1](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

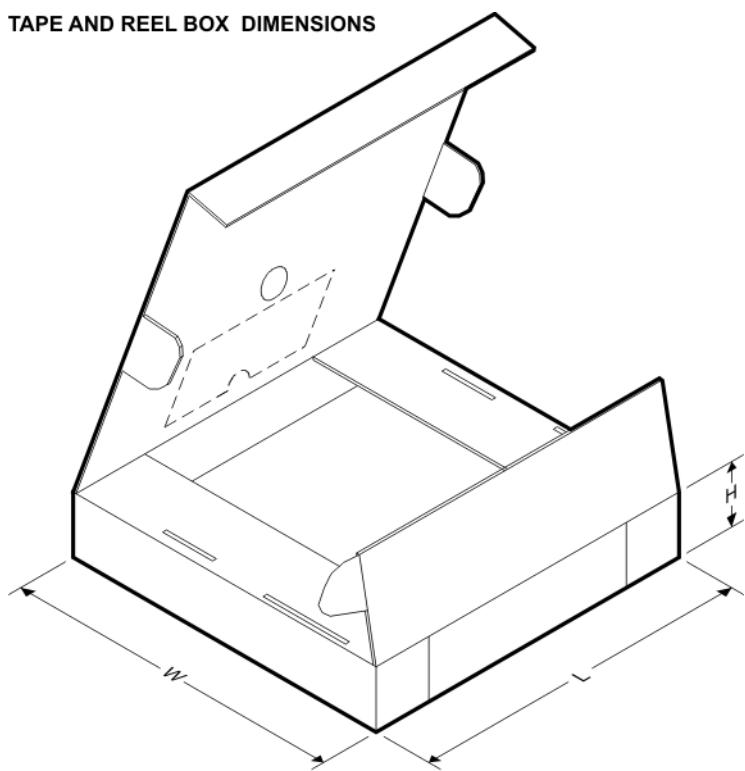
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G86MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

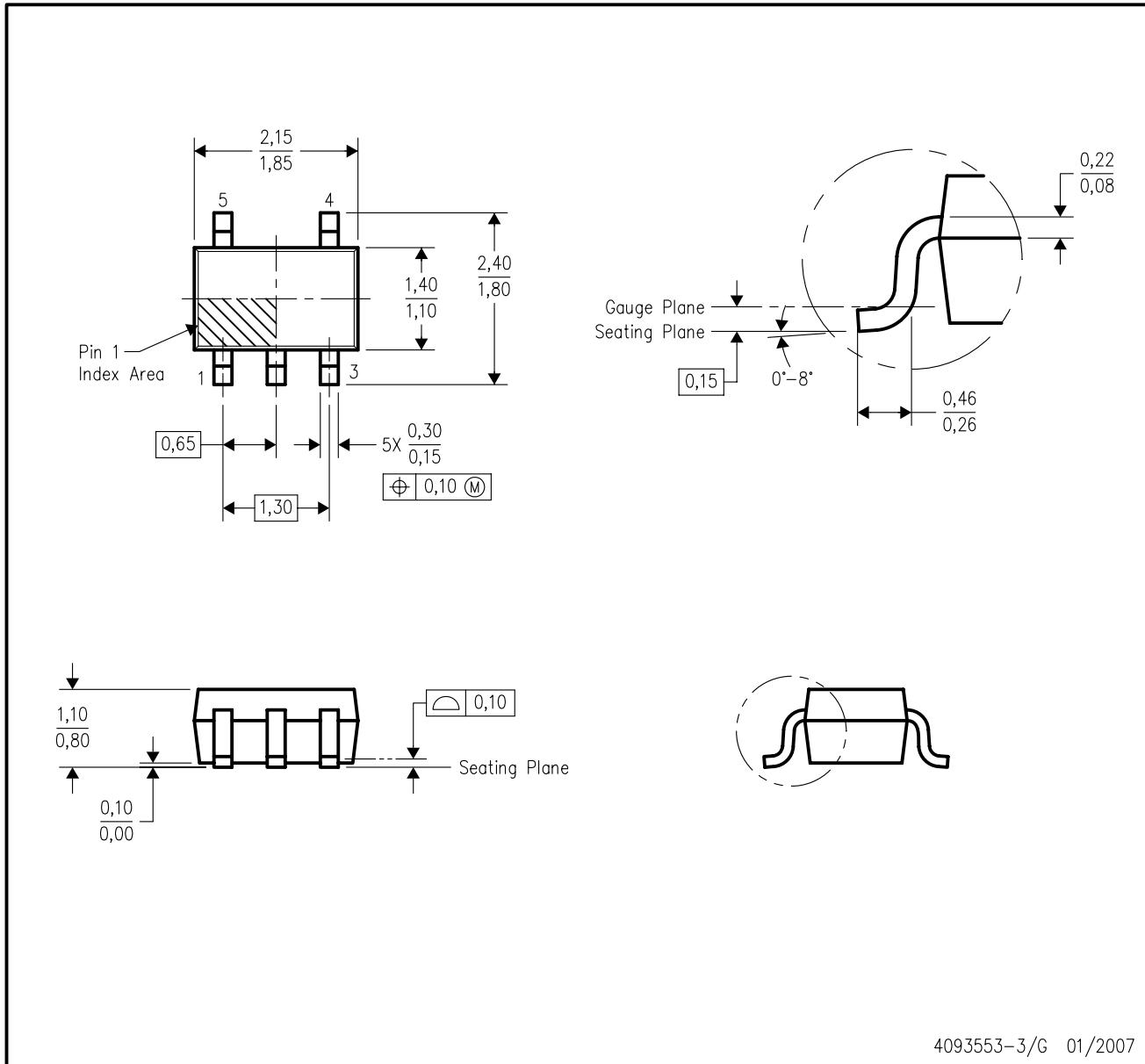
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G86MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

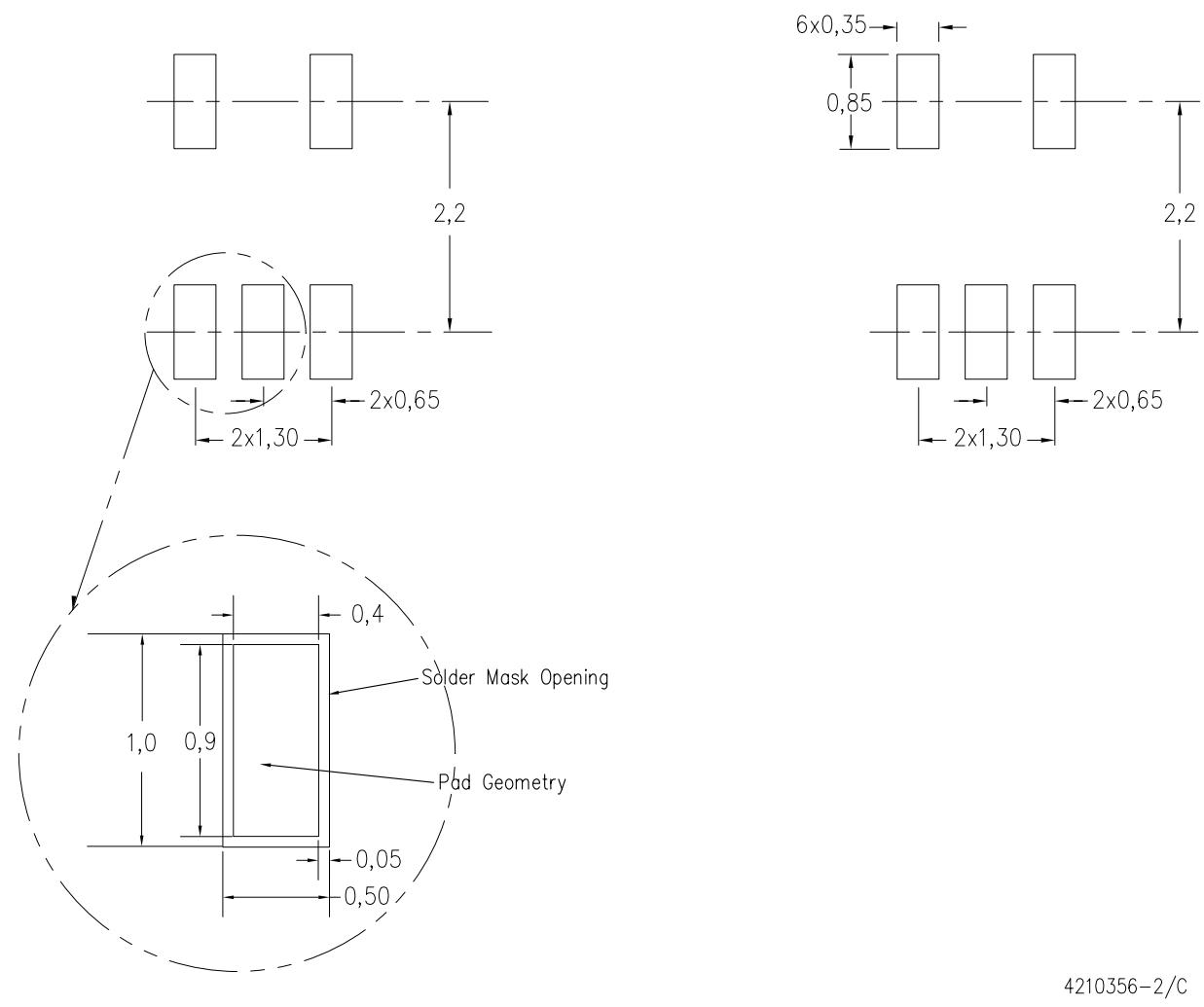
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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