- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Output Swing includes Both Supply Rails**
- **Low Noise . . . 12 nV/$\sqrt{\text{Hz}}$ Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**

- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C (TLC2262A)**
- **Macromodel Included**
- **Performance Upgrade for the TS27M2/M4 and TLC27M2/M4**

description

The TLC2262 and TLC2264 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC226x family offers a compromise between the micropower TLC225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

The TLC226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC226xA family is available and has a maximum input offset voltage of 950 µV. This family is fully characterized at 5 V and ±5 V.

The TLC2262/4 also makes great upgrades to the TLC27M2/L4 or TS27M2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.
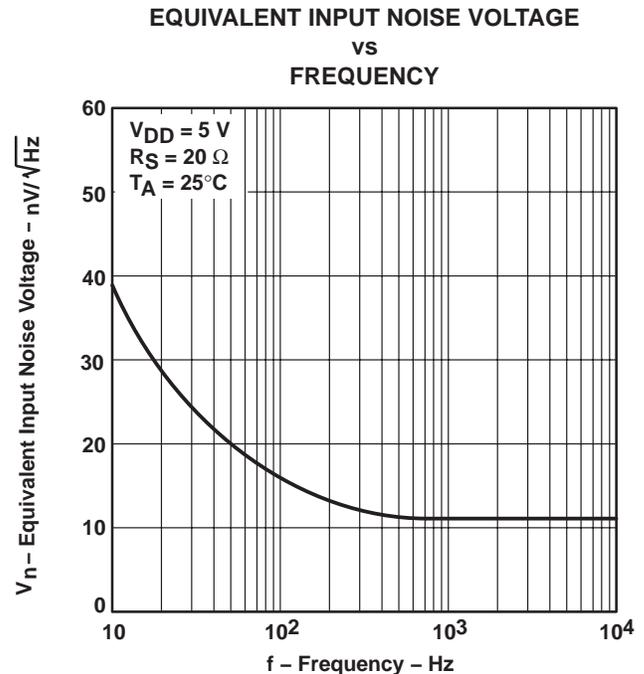
EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

Figure 1

Advanced LinCMOS is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

ORDERING INFORMATION†

T$_A$	V$_{IO}$max AT 25°C	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	950 μV	SOIC (D)	Tape and reel	TLC2262AQDRQ1§	2262AQ1
	2.5 mV	SOIC (D)	Tape and reel	TLC2262QDRQ1§	2262Q1
	950 μV	TSSOP (PW)	Tape and reel	TLC2262AQPWRQ1§	2262AQ1
	2.5 mV	TSSOP (PW)	Tape and reel	TLC2262QPWRQ1§	2262Q1
	950 μV	SOIC (D)	Tape and reel	TLC2264AQDRQ1	2264AQ1
	2.5 mV	SOIC (D)	Tape and reel	TLC2264QDRQ1	2264Q1
	950 μV	TSSOP (PW)	Tape and reel	TLC2264AQPWRQ1	2264AQ1
	2.5 mV	TSSOP (PW)	Tape and reel	TLC2264QPWRQ1	2264Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ Product Preview.

TLC2262, TLC2262A
D OR PW PACKAGE
(TOP VIEW)

```
1OUT   [ 1      8 ]  V_DD+
1IN−   [ 2      7 ]  2OUT
1IN+   [ 3      6 ]  2IN−
V_DD−/GND [ 4   5 ]  2IN+
```
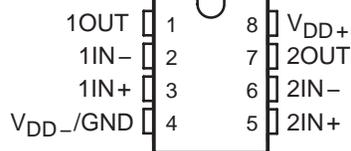
TLC2264, TLC2264A
D OR PW PACKAGE
(TOP VIEW)

```
1OUT   [ 1     14 ]  4OUT
1IN−   [ 2     13 ]  4IN−
1IN+   [ 3     12 ]  4IN+
V_DD+  [ 4     11 ]  V_DD−/GND
2IN+   [ 5     10 ]  3IN+
2IN−   [ 6      9 ]  3IN−
2OUT   [ 7      8 ]  3OUT
```

equivalent schematic (each amplifier)
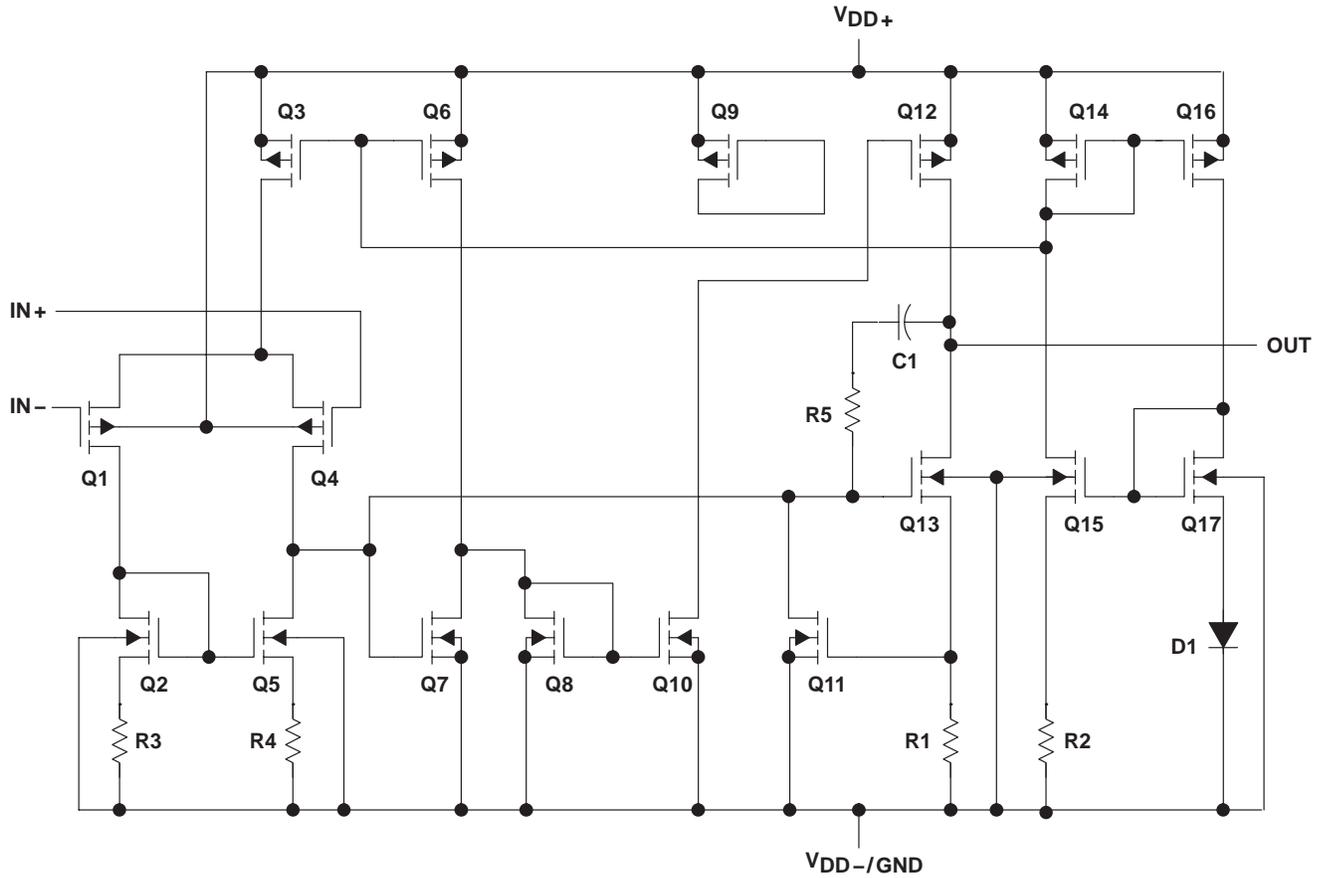
ACTUAL DEVICE COMPONENT COUNT[†]		
COMPONENT	TLC2262	TLC2264
Transistors	38	76
Resistors	28	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1) . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . −8 V
Differential input voltage, V_{ID} (see Note 2) . . . . ±16 V
Input voltage, V_I (any input, see Note 1) . . . . V_{DD-} − 0.3 V to V_{DD+}
Input current, I_I (each input) . . . . ±5 mA
Output current, I_O . . . . ±50 mA
Total current into V_{DD+} . . . . ±50 mA
Total current out of V_{DD-} . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: Q suffix . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or PW package . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
          2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if input is brought below V_{DD-} − 0.3 V.
          3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum
              dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
PW–14	750 mW	6.0 mW/°C	480 mW	389 mW	150 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} −1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −1.5	V
Operating free-air temperature, T_A	−40	125	°C

TEXAS INSTRUMENTS

TLC2262 electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262-Q1			TLC2262A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		5			5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$,	$\|V_{IO}\| \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20$ μA		25°C		4.99			4.99		V
		$I_{OH} = -100$ μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		$I_{OH} = -400$ μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50$ μA	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 500$ μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		$V_{IC} = 2.5$ V,	$I_{OL} = 4$ mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 50$ kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			$R_L = 1$ MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz,	P package	25°C		8			8		pF
z_O	Closed-loop output impedance	$f = 100$ kHz,	$A_V = 10$	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $R_S = 50\ \Omega$	$V_O = 2.5$ V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is –40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TEXAS INSTRUMENTS

TLC2262 operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262-Q1			TLC2262A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V

TEXAS INSTRUMENTS

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TLC2262 electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2262-Q1 MIN	TLC2262-Q1 TYP	TLC2262-Q1 MAX	TLC2262A-Q1 MIN	TLC2262A-Q1 TYP	TLC2262A-Q1 MAX	UNIT
V_{IO}	Input offset voltage		25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		5			5		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			800			800	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			800			800	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $|V_{IO}| \leq 5$ mV	25°C	−5 to 4	−5.3 to 4		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 50$ kΩ	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$R_L = 1$ MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	$f = 100$ kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		425	500		425	500	μA
			Full range			500			500	

† Full range is −40°C to 125°C for Q suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262 operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262-Q1			TLC2262A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		85			85		kHz
t_S	Settling time	A_V = – 1, Step = – 2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕm	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q suffix.

TLC2264 electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264-Q1 MIN	TYP	MAX	TLC2264A-Q1 MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			800			800	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, |V_{IO}| ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99			4.99		V
		I_{OH} = −100 μA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		I_{OH} = −400 μA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
			Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
			Full range	50			50			
		R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V,	25°C	80	95		80	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is −40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264 operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264-Q1			TLC2264A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_S	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V

TLC2264 electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264-Q1			TLC2264A-Q1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			800			800	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			800			800	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $|V_{IO}| \leq 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20$ μA	25°C		4.99			4.99		V
		$I_O = -100$ μA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400$ μA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50$ μA	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500$ μA	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 50$ kΩ	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$R_L = 1$ MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	$f = 100$ kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.85	1		0.85	1	mA
			Full range			1			1	

† Full range is −40°C to 125°C for Q suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264 operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264-Q1			TLC2264A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.014%			0.014%		
			$A_V = 10$			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		70			70		kHz
t_S	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q suffix.

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TYPICAL CHARACTERISTICS

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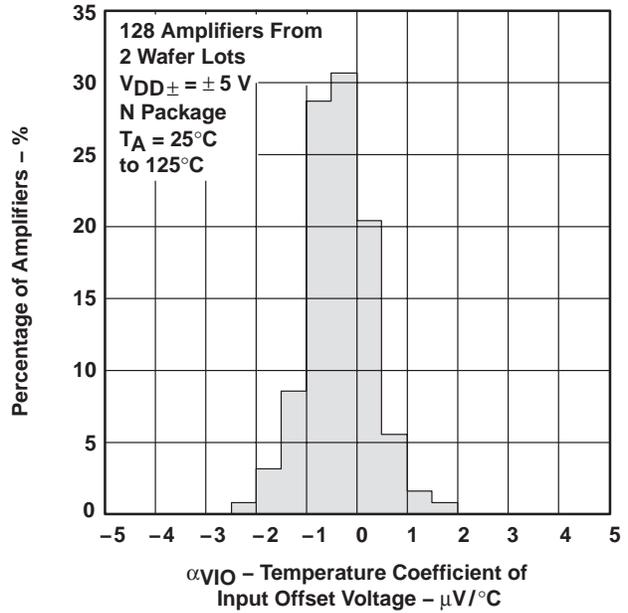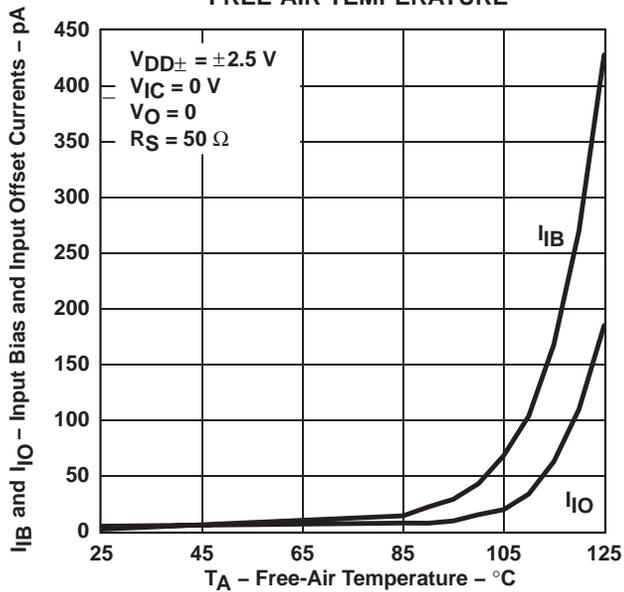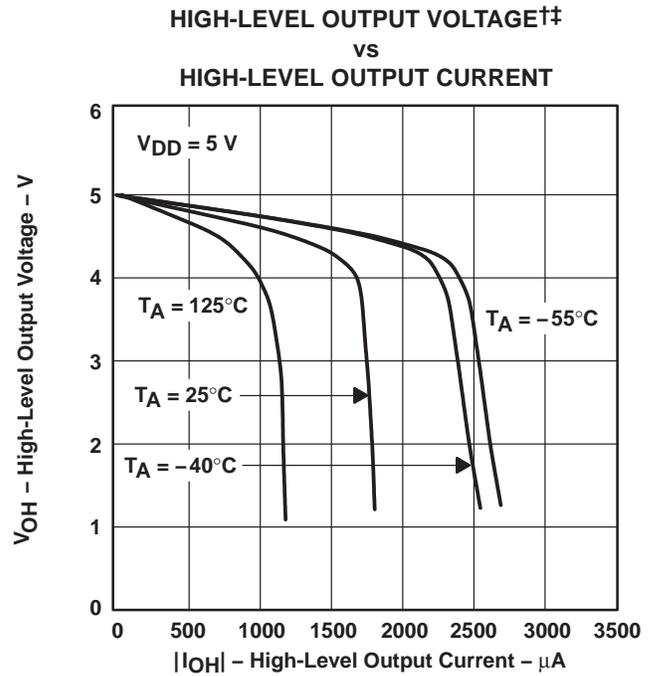|			FIGURE
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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2262
INPUT OFFSET VOLTAGE

1274 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
$T_A = 25°C$
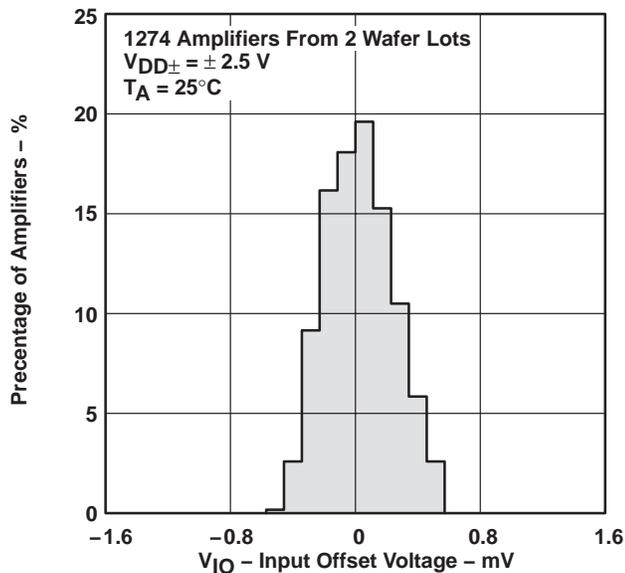
Figure 2

DISTRIBUTION OF TLC2262
INPUT OFFSET VOLTAGE

1274 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 5$ V
$T_A = 25°C$
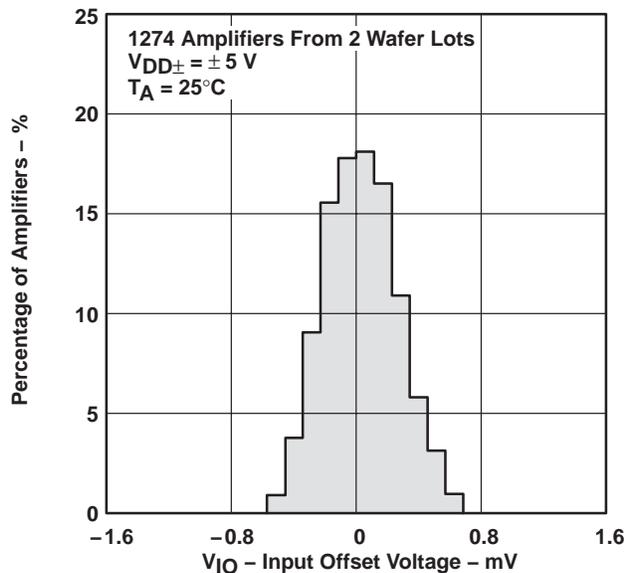
Figure 3

DISTRIBUTION OF TLC2264
INPUT OFFSET VOLTAGE

2272 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
$T_A = 25°C$
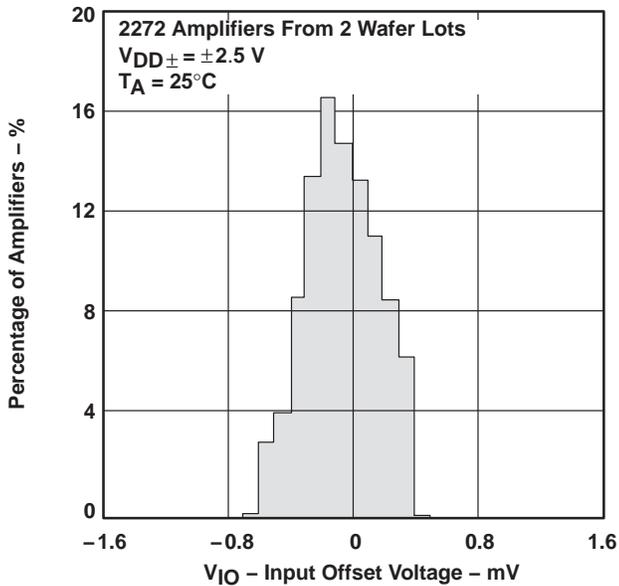
Figure 4

DISTRIBUTION OF TLC2264
INPUT OFFSET VOLTAGE

2272 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 5$ V
$T_A = 25°C$

Figure 5

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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

$V_{DD} = 5$ V
$R_S = 50$ Ω
$T_A = 25°C$

V_{IO} – Input Offset Voltage – mV

V_{IC} – Common-Mode Input Voltage – V

† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

Figure 6

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

$V_{DD\pm} = \pm 5$ V
$R_S = 50$ Ω
$T_A = 25°C$

V_{IO} – Input Offset Voltage – mV

V_{IC} – Common-Mode Input Voltage – V

Figure 7

DISTRIBUTION OF TLC2262 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

128 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
P Package
$T_A = 25°C$ to $125°C$

Percentage of Amplifiers – %

α_{VIO} – Temperature Coefficient – $\mu V/°C$

Figure 8

DISTRIBUTION OF TLC2262 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

128 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 5$ V
P Package
$T_A = 25°C$ to $125°C$

Percentage of Amplifiers – %

α_{VIO} – Temperature Coefficient – $\mu V/°C$

Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
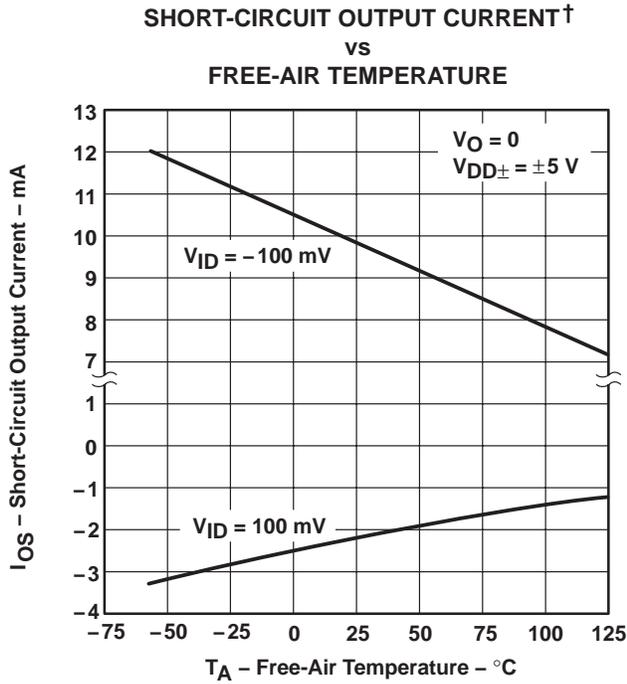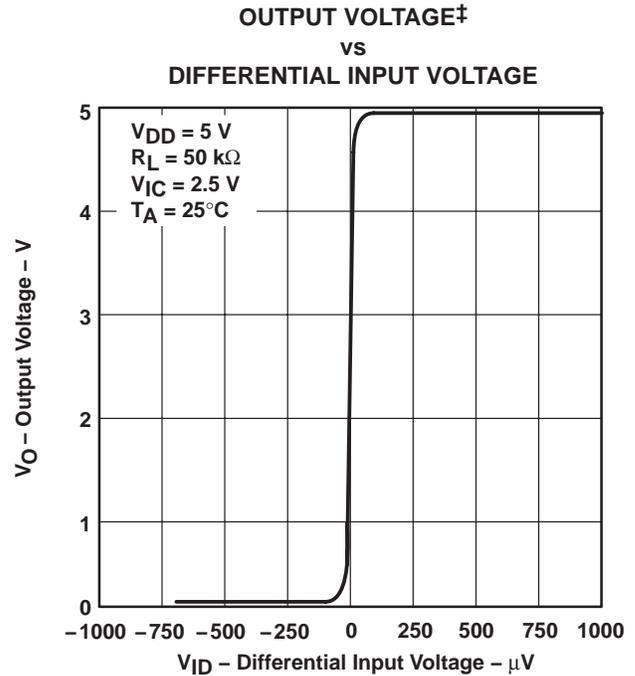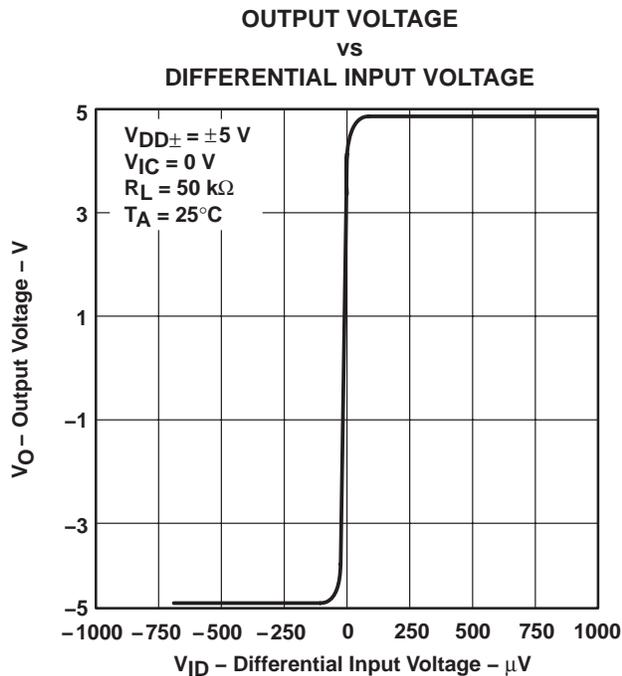
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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2264 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

128 Amplifiers From
2 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
N Package
$T_A = 25°C$ to $125°C$

α_{VIO} – Temperature Coefficient of
Input Offset Voltage – $\mu V/°C$

Figure 10

DISTRIBUTION OF TLC2264 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

128 Amplifiers From
2 Wafer Lots
$V_{DD\pm} = \pm 5$ V
N Package
$T_A = 25°C$
to $125°C$

α_{VIO} – Temperature Coefficient of
Input Offset Voltage – $\mu V/°C$

Figure 11

INPUT BIAS AND INPUT OFFSET CURRENTS†
vs
FREE-AIR TEMPERATURE

$V_{DD\pm} = \pm 2.5$ V
$V_{IC} = 0$ V
$V_O = 0$
$R_S = 50\ \Omega$

I_{IB}

I_{IO}

T_A – Free-Air Temperature – $°C$

Figure 12

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

$R_S = 50\ \Omega$
$T_A = 25°C$

$|V_{IO}| \leq 5$ mV

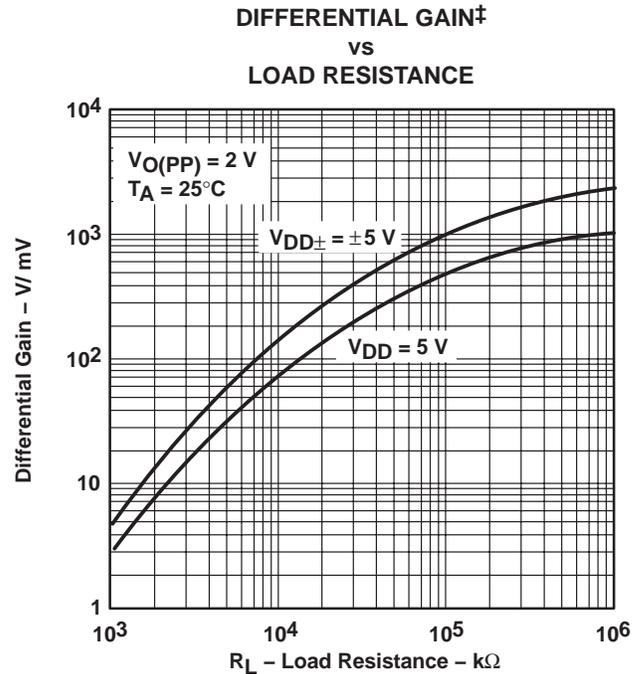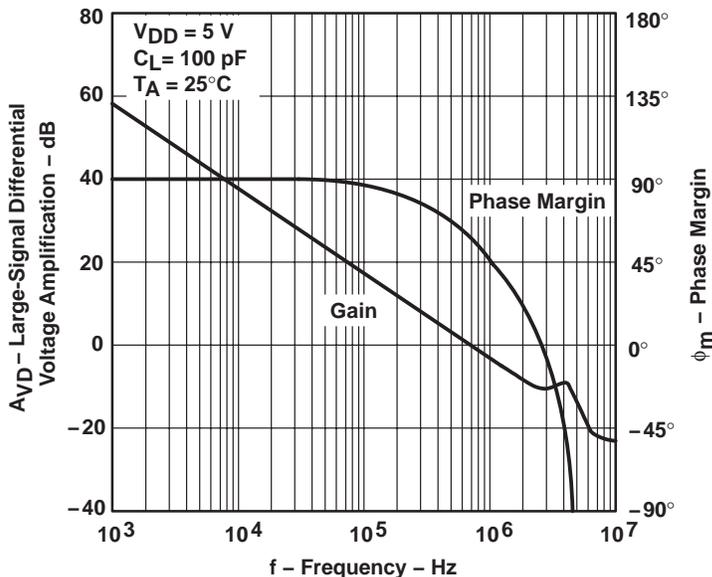$|V_{DD\pm}|$ – Supply Voltage – V
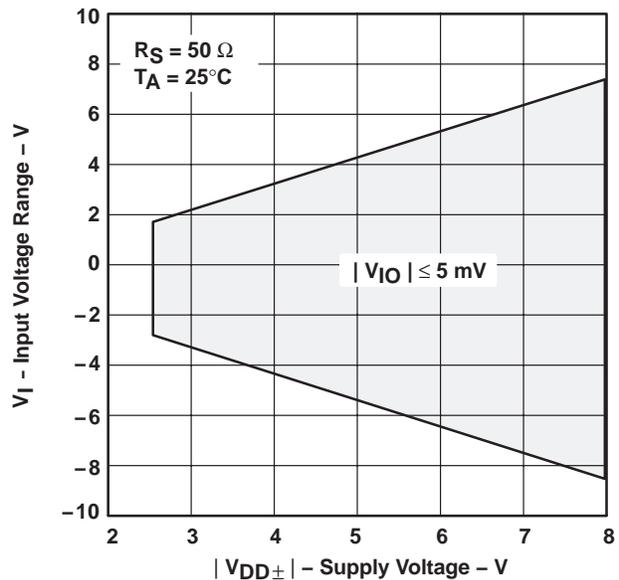
Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS
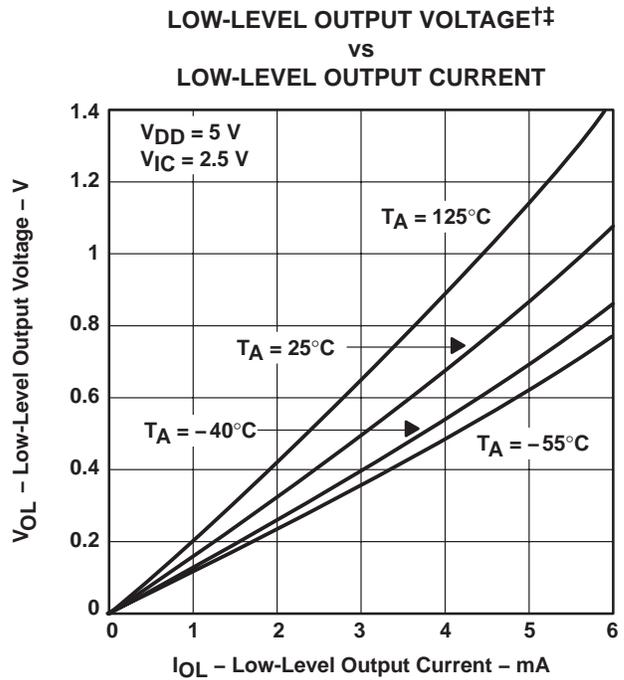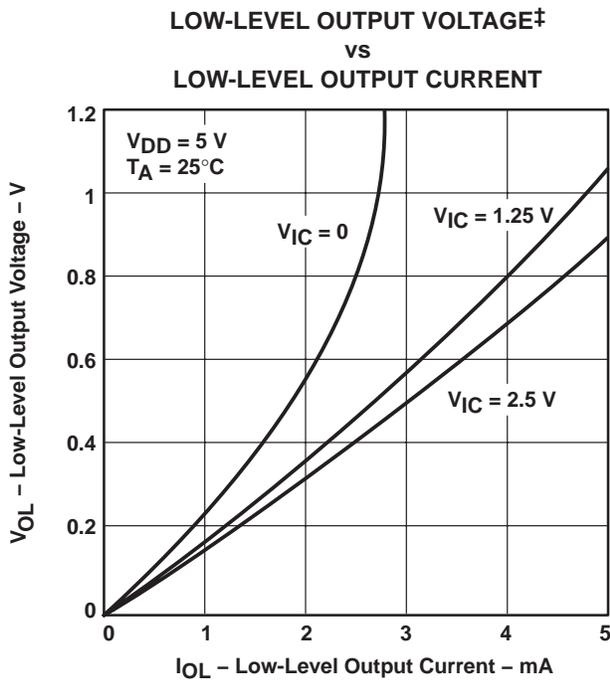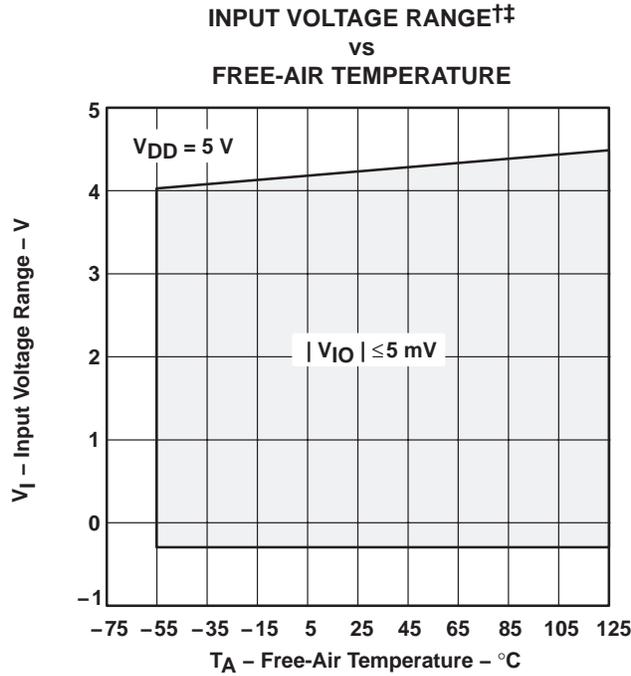
INPUT VOLTAGE RANGE†‡
vs
FREE-AIR TEMPERATURE

Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE†
vs
OUTPUT CURRENT
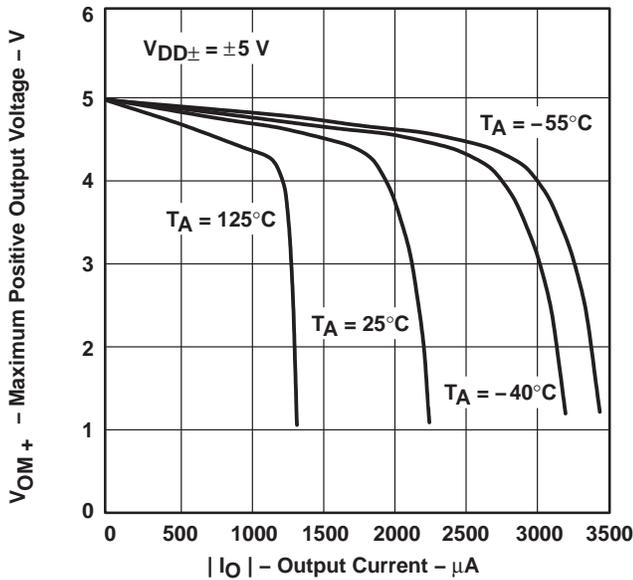
Figure 18

MAXIMUM NEGATIVE OUTPUT VOLTAGE†
vs
OUTPUT CURRENT
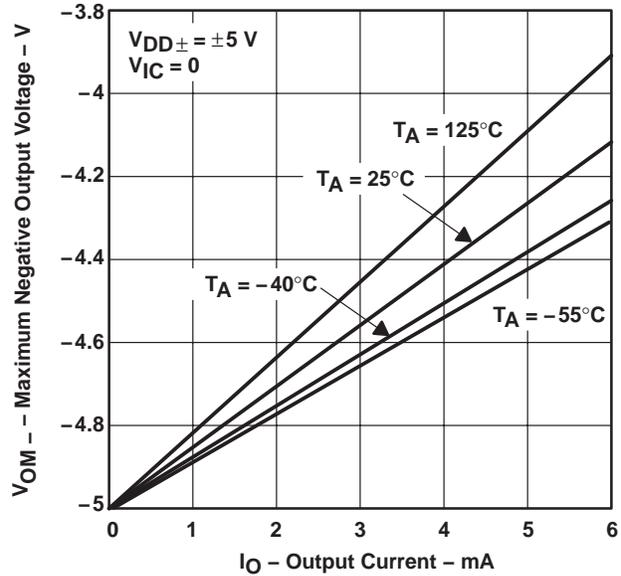
Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†‡
vs
FREQUENCY

‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
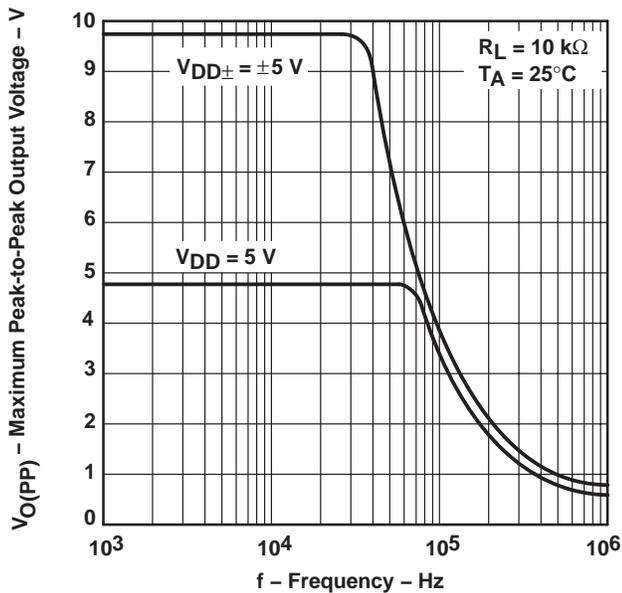
Figure 20

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

Figure 22

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 23

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 24

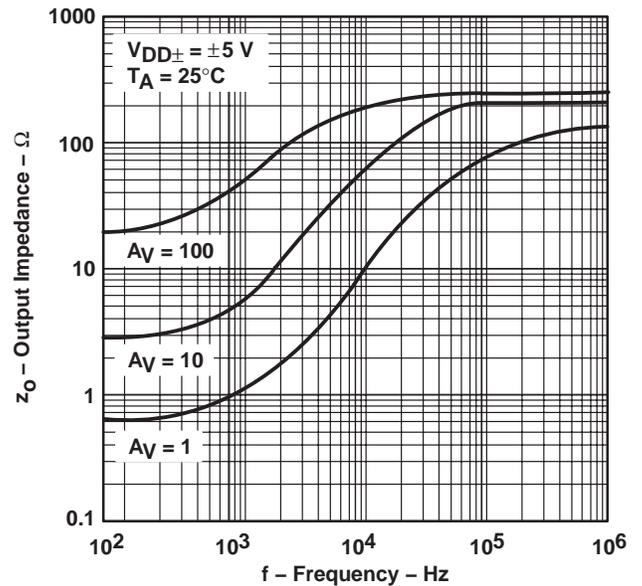DIFFERENTIAL GAIN‡
vs
LOAD RESISTANCE

Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY**

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 26

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY**
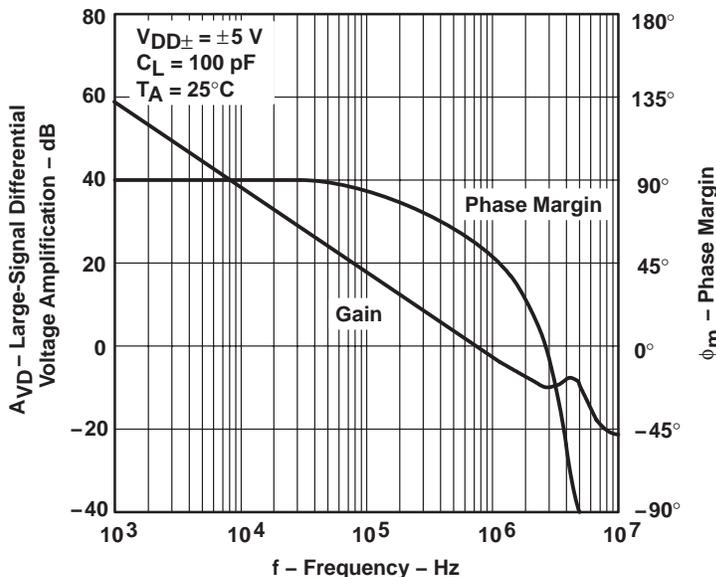
Figure 27

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE
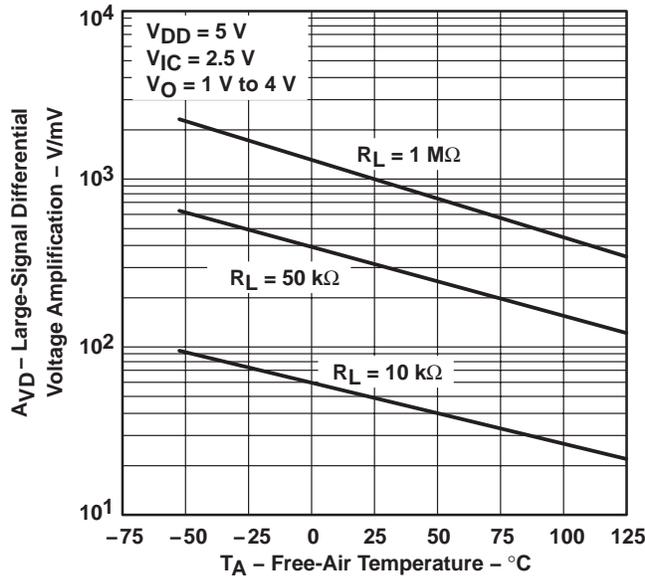
Figure 28

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE
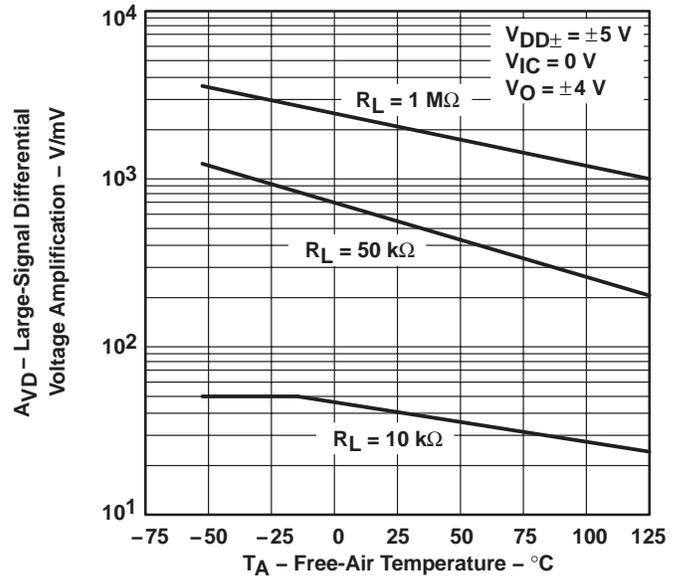
Figure 29

OUTPUT IMPEDANCE‡
vs
FREQUENCY
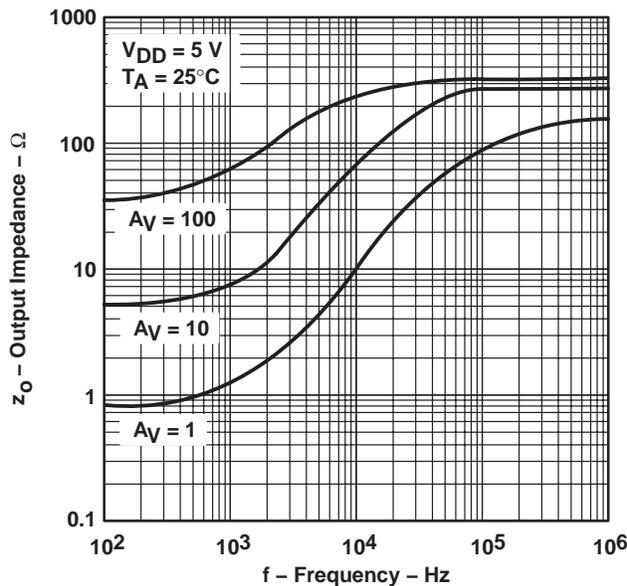
Figure 30

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

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TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO[†]
vs
FREQUENCY
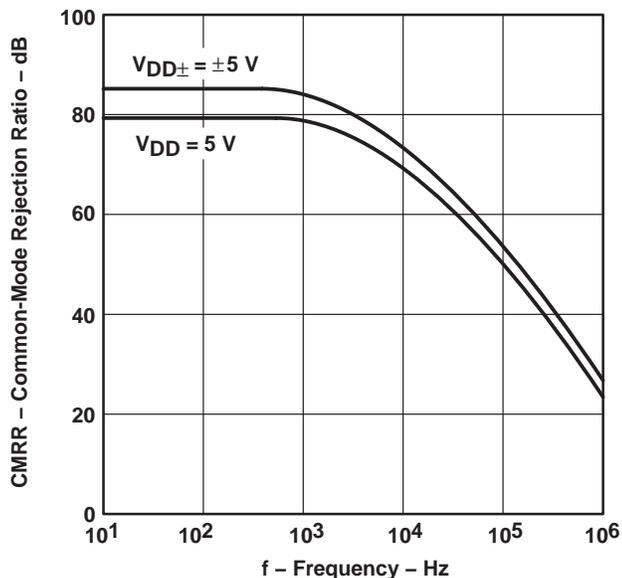
Figure 32

COMMON-MODE REJECTION RATIO[†‡]
vs
FREE-AIR TEMPERATURE
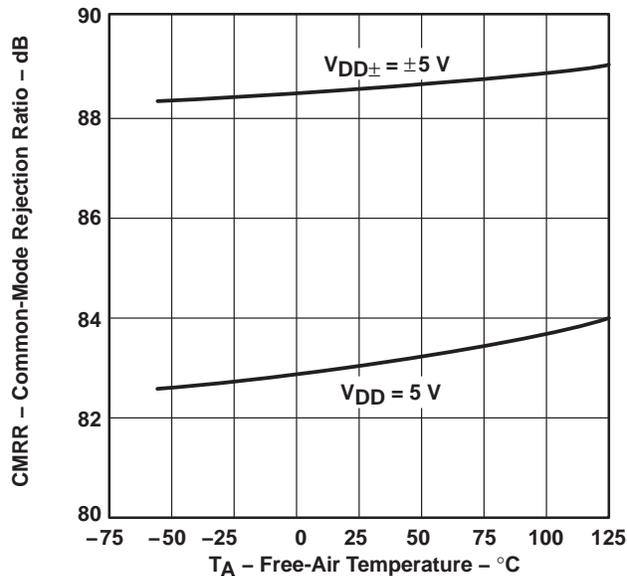
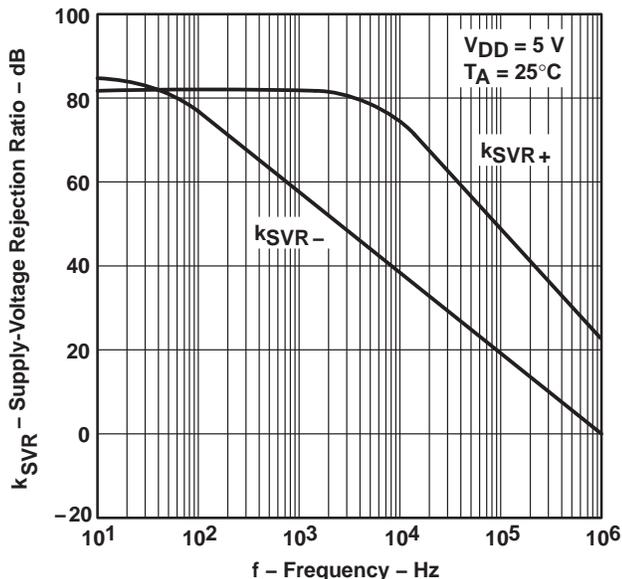**Figure 33**

SUPPLY-VOLTAGE REJECTION RATIO[†]
vs
FREQUENCY

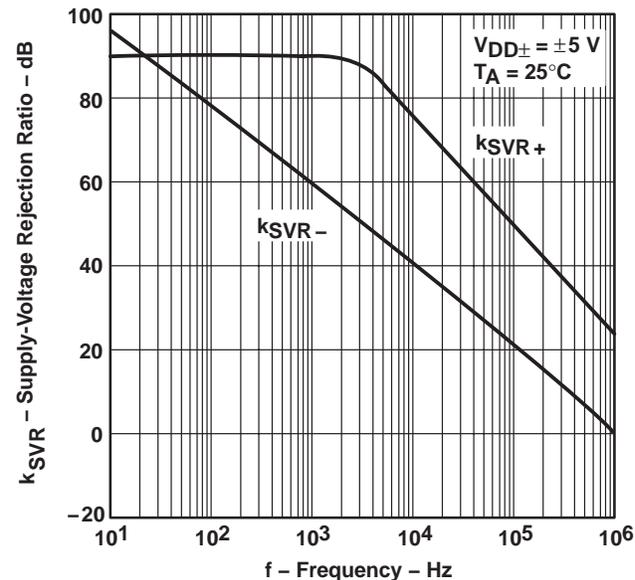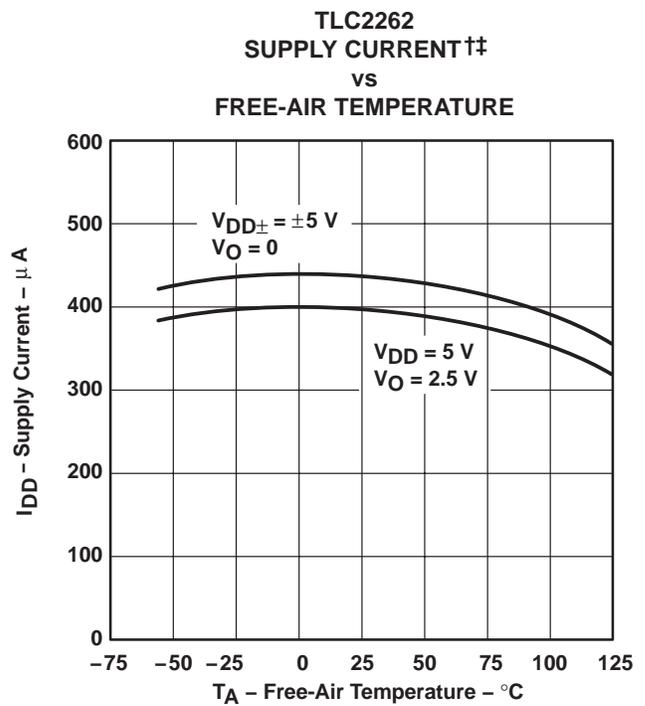

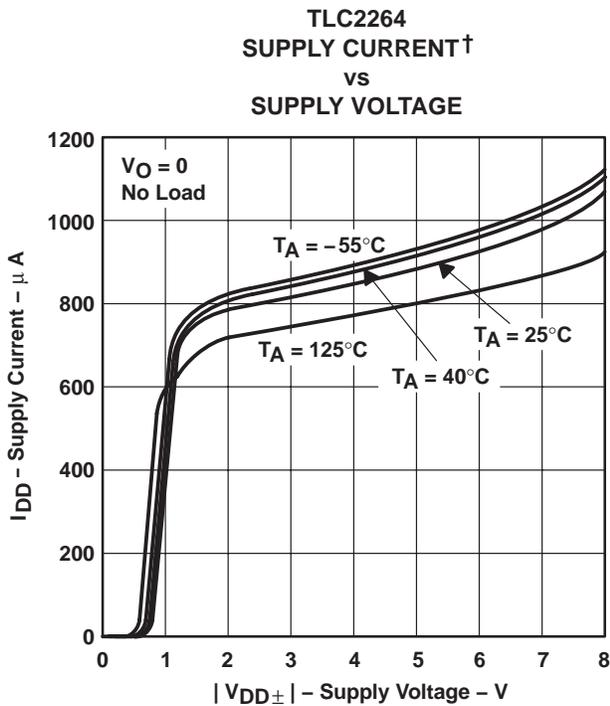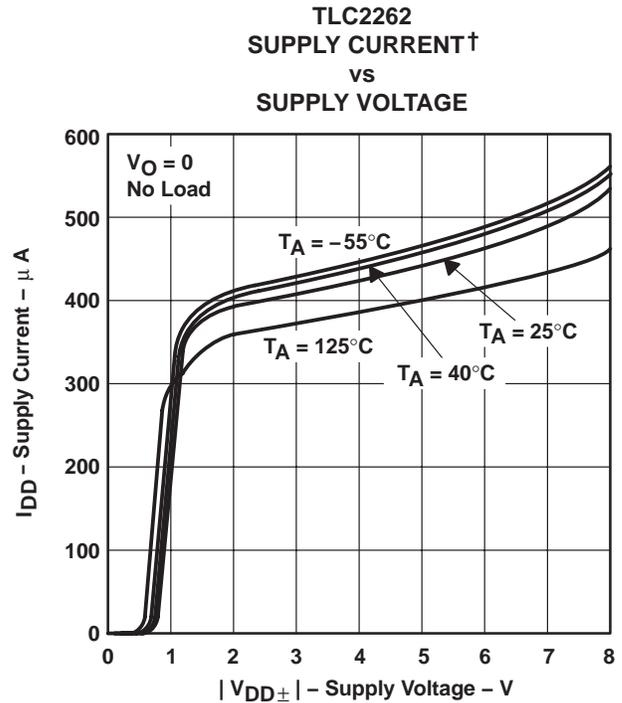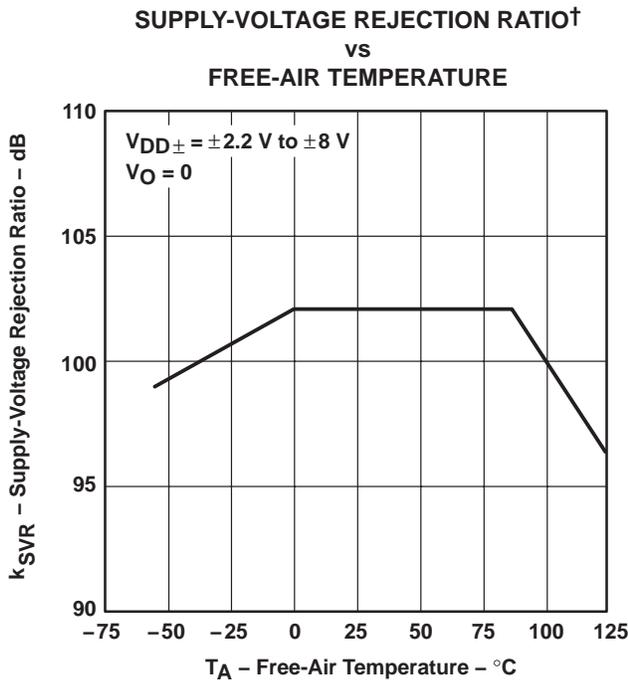**Figure 34**

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 35

[†] For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
[‡] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

$V_{DD\pm} = \pm 2.2$ V to ± 8 V
$V_O = 0$

Figure 36

TLC2262
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

$V_O = 0$
No Load

$T_A = -55°C$
$T_A = 25°C$
$T_A = 125°C$
$T_A = 40°C$

Figure 37

TLC2264
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

$V_O = 0$
No Load

$T_A = -55°C$
$T_A = 25°C$
$T_A = 125°C$
$T_A = 40°C$

Figure 38

TLC2262
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

$V_{DD\pm} = \pm 5$ V
$V_O = 0$

$V_{DD} = 5$ V
$V_O = 2.5$ V

Figure 39

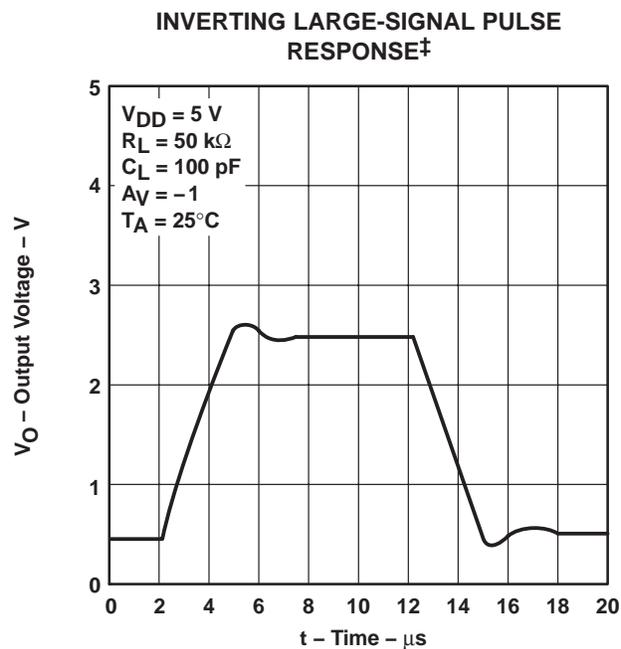† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

TLC2264
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

Figure 40

SLEW RATE‡
vs
LOAD CAPACITANCE

Figure 41

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

Figure 42

INVERTING LARGE-SIGNAL PULSE
RESPONSE‡

Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
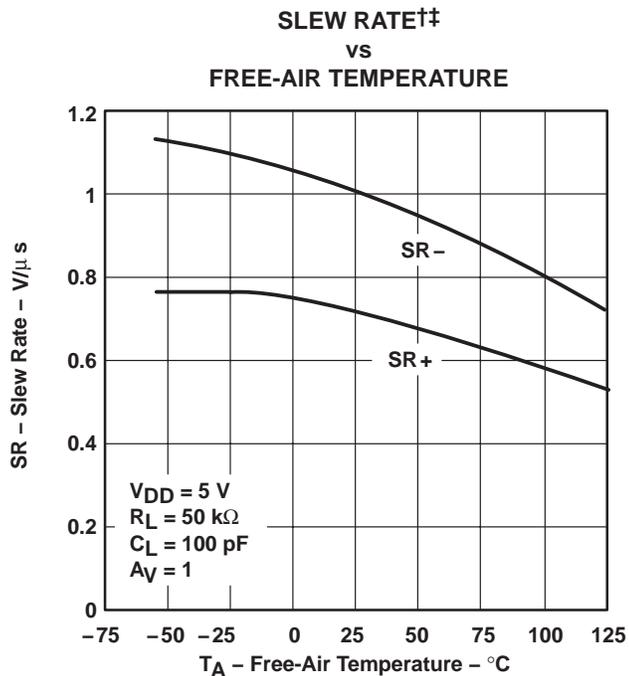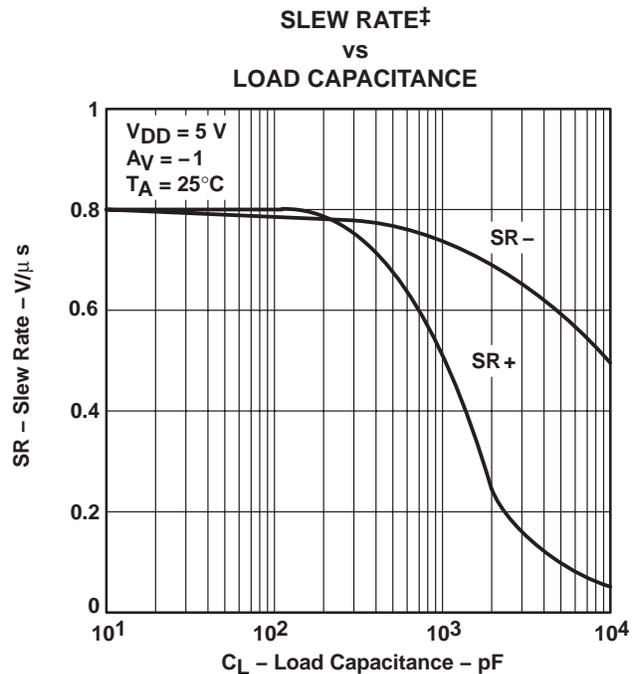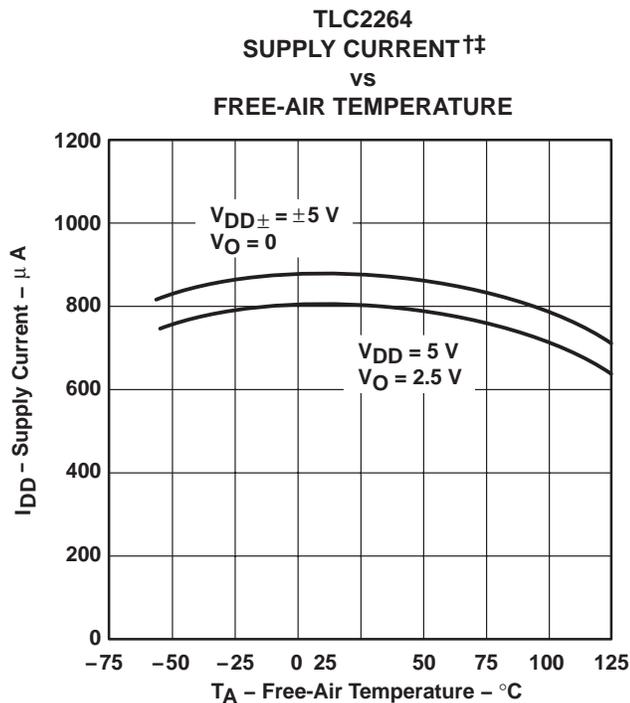‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

$V_{DD\pm} = \pm 5$ V
$R_L = 50$ kΩ
$C_L = 100$ pF
$A_V = -1$
$T_A = 25°C$

V$_O$ – Output Voltage – V

t – Time – µs

Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

$V_{DD} = 5$ V
$R_L = 50$ kΩ
$C_L = 100$ pF
$A_V = 1$
$T_A = 25°C$

V$_O$ – Output Voltage – V

t – Time – µs

Figure 45

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

$V_{DD\pm} = \pm 5$ V
$R_L = 50$ kΩ
$C_L = 100$ pF
$A_V = 1$
$T_A = 25°C$

V$_O$ – Output Voltage – V

t – Time – µs

Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†

$V_{DD} = 5$ V
$R_L = 50$ kΩ
$C_L = 100$ pF
$A_V = -1$
$T_A = 25°C$

V$_O$ – Output Voltage – V

t – Time – µs

Figure 47

† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

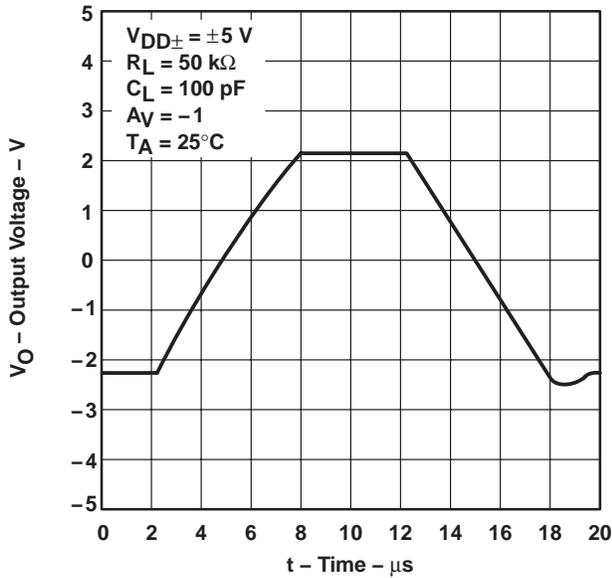## TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

$V_{DD\pm} = \pm 5$ V
$R_L = 50$ kΩ
$C_L = 100$ pF
$A_V = -1$
$T_A = 25°C$

Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

$V_{DD} = 5$ V
$R_L = 50$ kΩ
$C_L = 100$ pF
$A_V = 1$
$T_A = 25°C$

Figure 49

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

$V_{DD\pm} = \pm 5$ V
$R_L = 50$ kΩ
$C_L = 100$ pF
$A_V = 1$
$T_A = 25°C$

Figure 50

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY
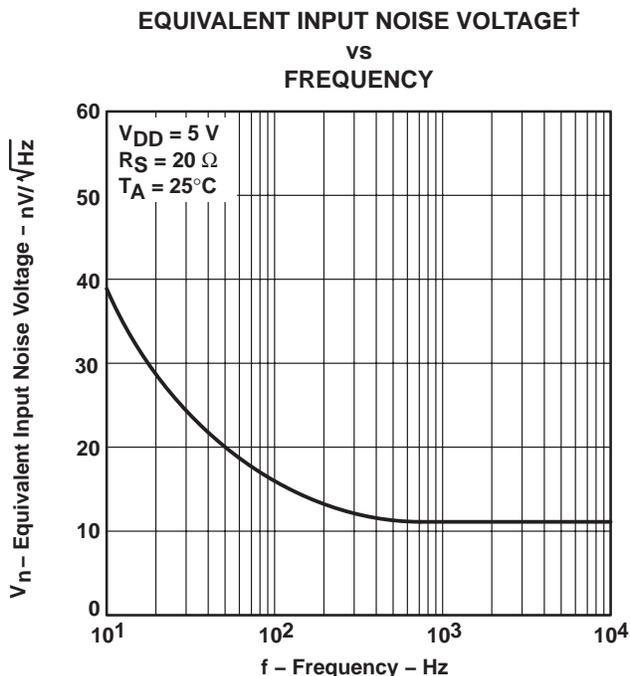
$V_{DD} = 5$ V
$R_S = 20$ Ω
$T_A = 25°C$

Figure 51

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 52

EQUIVALENT INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD†

Figure 53

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

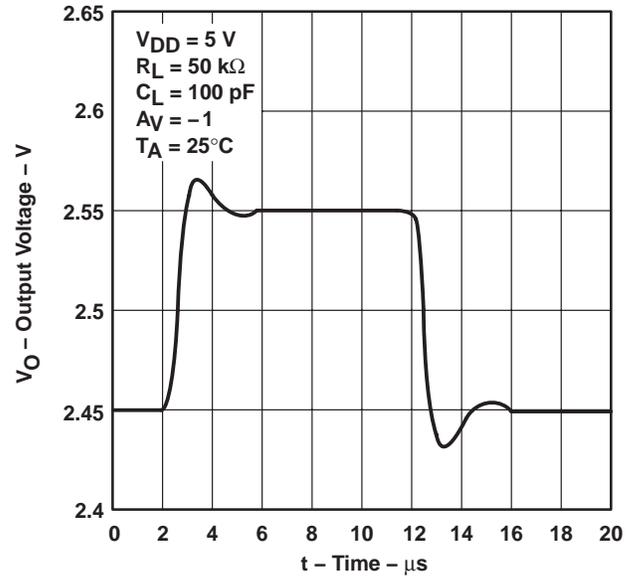**Figure 54**

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY
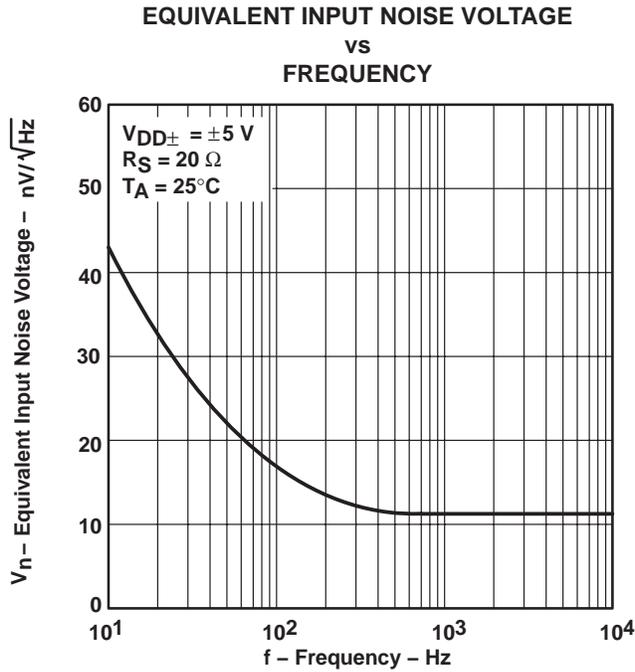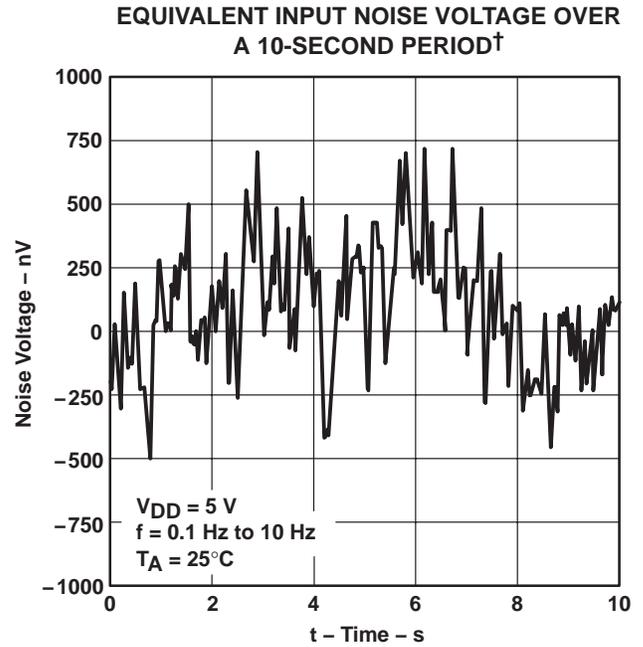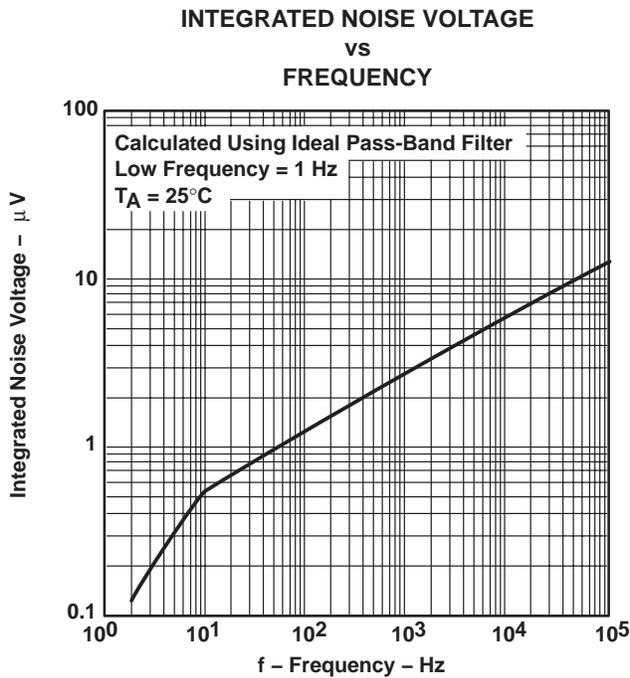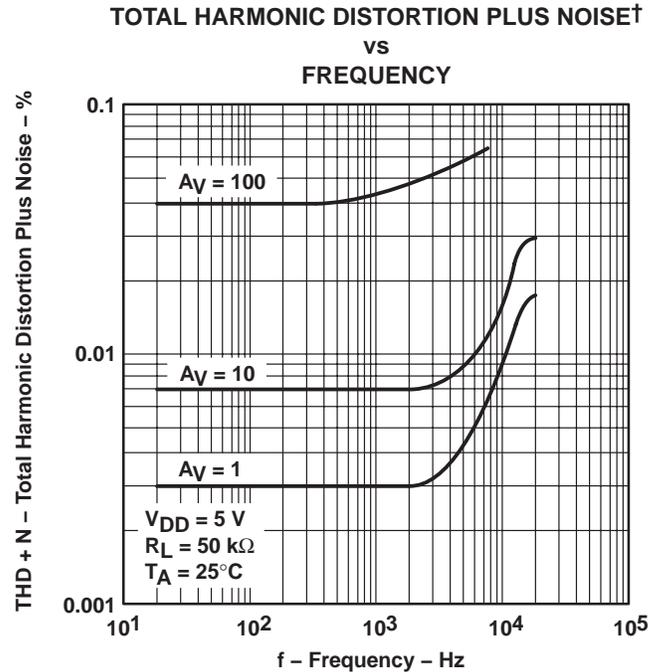
Figure 55

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
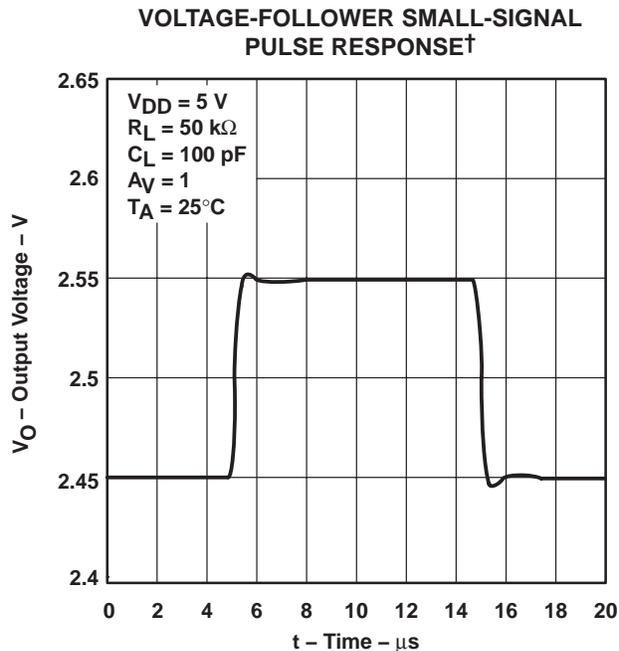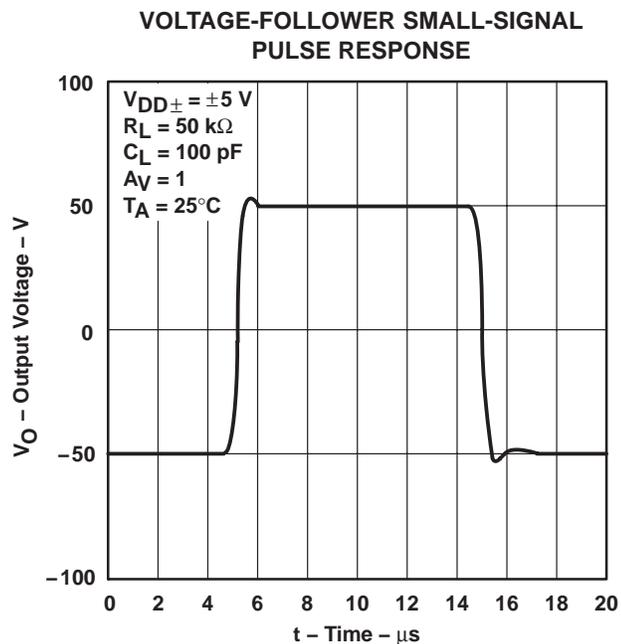
TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

f = 10 kHz
R_L = 50 kΩ
C_L = 100 pF
T_A = 25°C
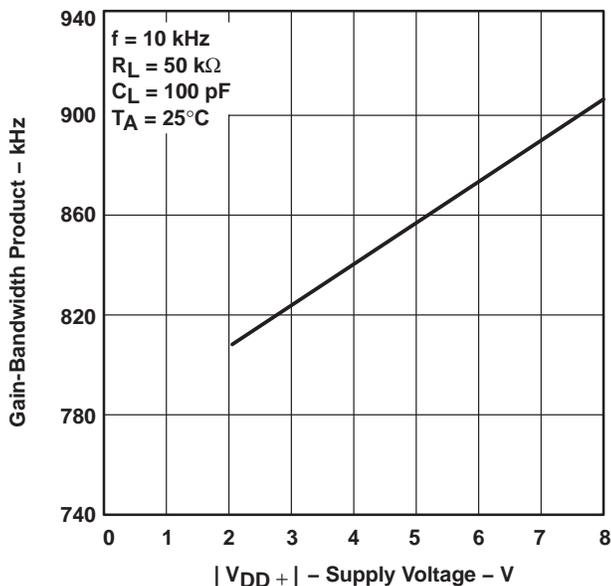
Figure 56

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

V_{DD} = 5 V
f = 10 kHz
C_L = 100 pF
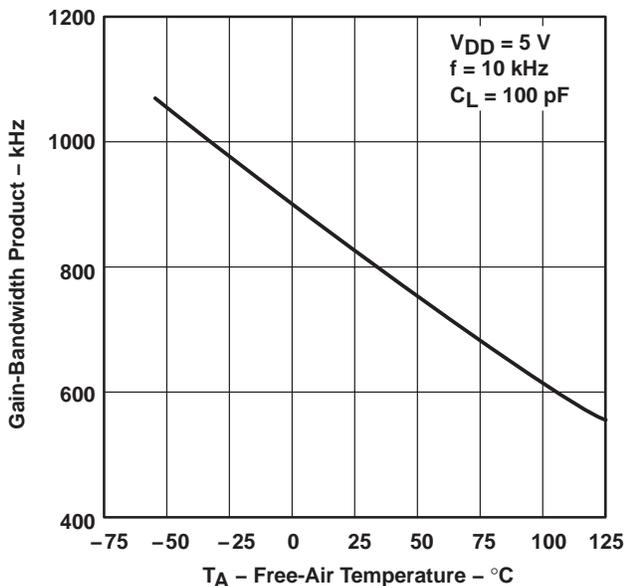
Figure 57

PHASE MARGIN
vs
LOAD CAPACITANCE

T_A = 25°C

R_{null} = 100 Ω
R_{null} = 50 Ω
R_{null} = 20 Ω
R_{null} = 10 Ω
R_{null} = 0
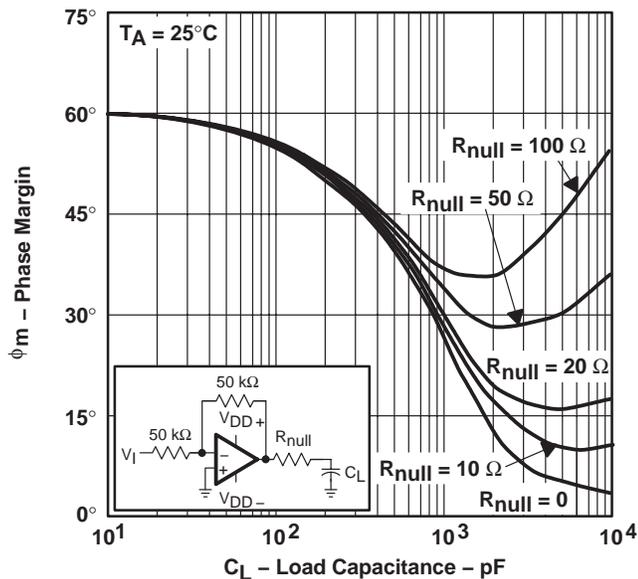
Figure 58

GAIN MARGIN
vs
LOAD CAPACITANCE

T_A = 25°C

R_{null} = 100 Ω
R_{null} = 50 Ω
R_{null} = 20 Ω
R_{null} = 10 Ω
R_{null} = 0

Figure 59

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH†
vs
LOAD CAPACITANCE

Figure 60

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE
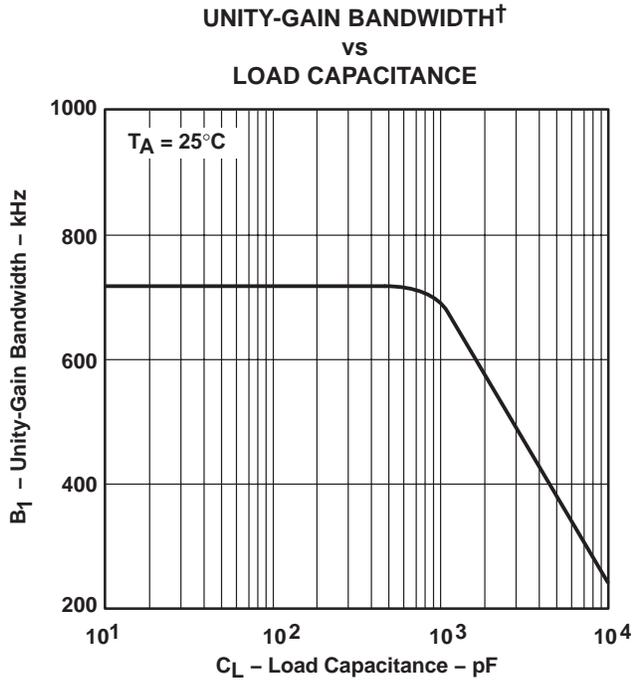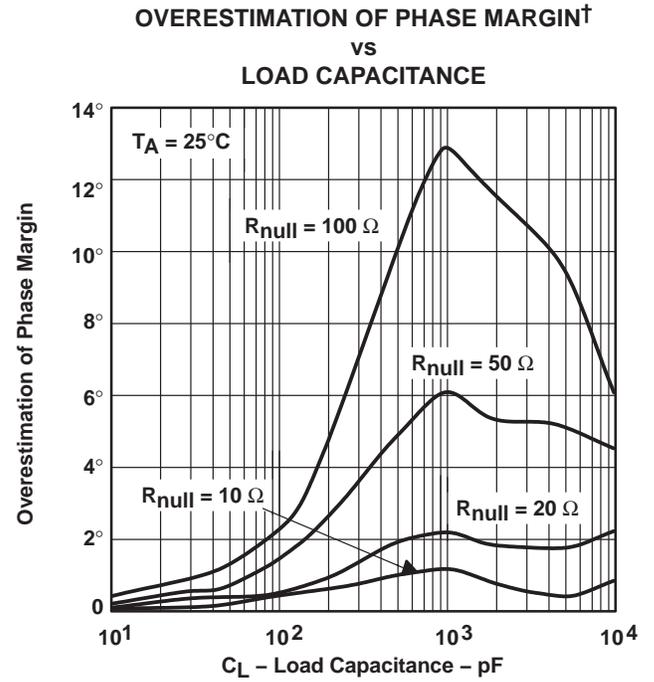
Figure 61

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 58 and Figure 59 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 62) improves the gain and phase margins when driving large capacitive loads. Figure 58 and Figure 59 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\Theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \tag{1}$$

Where :

$$\Delta\Theta_{m1} = \text{improvement in phase margin}$$
$$\text{UGBW} = \text{unity-gain bandwidth frequency}$$
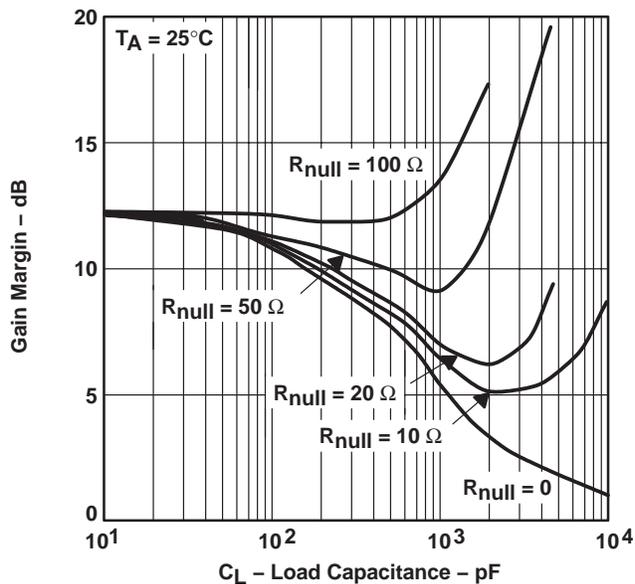$$R_{null} = \text{output series resistance}$$
$$C_L = \text{load capacitance}$$

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 60). To use equation 1, UGBW must be approximated from Figure 60.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 61. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \tag{2}$$

Where :

$$F = \text{factor reducing frequency of pole}$$
$$g_m = \text{small-signal output transconductance (typically } 4.83 \times 10^{-3} \text{ mhos)}$$
$$R_{null} = \text{output series resistance}$$

For the TLC226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 70 MHz, at C_L = 1000 pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation in equation 1 to better approximate the improvement in phase margin.

TEXAS INSTRUMENTS

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\Theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \tag{3}$$

Where :

$\Delta\Theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation 2

P_2 = unadjusted pole (70 MHz @ 10 pF, 7 MHz @ 100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.
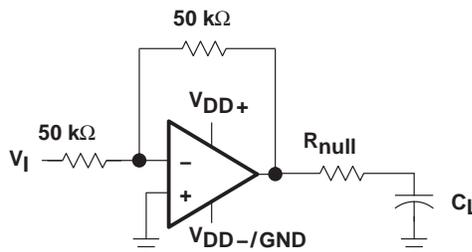

Figure 62. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 63 are generated using the TLC226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).


```
.SUBCKT TLC226x 1 2 3 4 5
        C1      11      12      3.560E−12
        C2      6       7       15.00E−12
        DC      5       53      DX
        DE      54      5       DX
        DLP     90      91      DX
        DLN     92      90      DX
        DP      4       3       DX
        EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7       99      POLY (5) VB VC VE VLP
+ VLN 0 21.04E6 −30E6 30E6 30E6 −30E6
        GA      6       0       11      12 47.12E−6
        GCM     0       6       10      99 4.9E−9
        ISS     3       10      DC 8.250E−6
        HLIM    90      0       VLIM 1K
        J1      11      2       10 JX
        J2      12      1       10 JX
        R2      6       9       100.0E3
```

```
        RD1     60      11      21.22E3
        RD2     60      12      21.22E3
        R01     8       5       120
        R02     7       99      120
        RP      3       4       26.04E3
        RSS     10      99      24.24E6
        VAD     60      4       −.6
        VB      9       0       DC 0
        VC      3       53      DC .65
        VE      54      4       DC .65
        VLIM    7       8       DC 0
        VLP     91      0       DC 1.4
        VLN     0       92      DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=500.0E−15 BETA=281E−6
+ VTO=−.065)
.ENDS
```

Figure 63. Boyle Macromodel and Subcircuit

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TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2264AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ	Samples
TLC2264AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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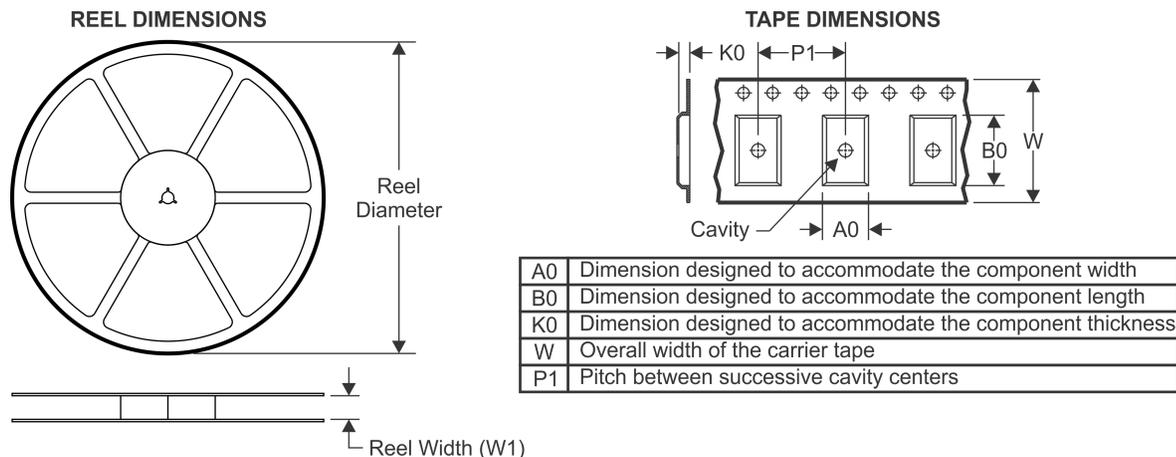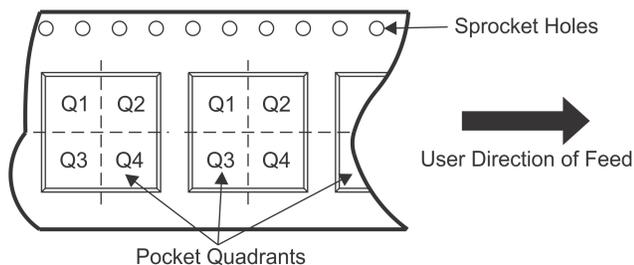In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC2264A-Q1 :

● Catalog: TLC2264A

● Military: TLC2264AM

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2264AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
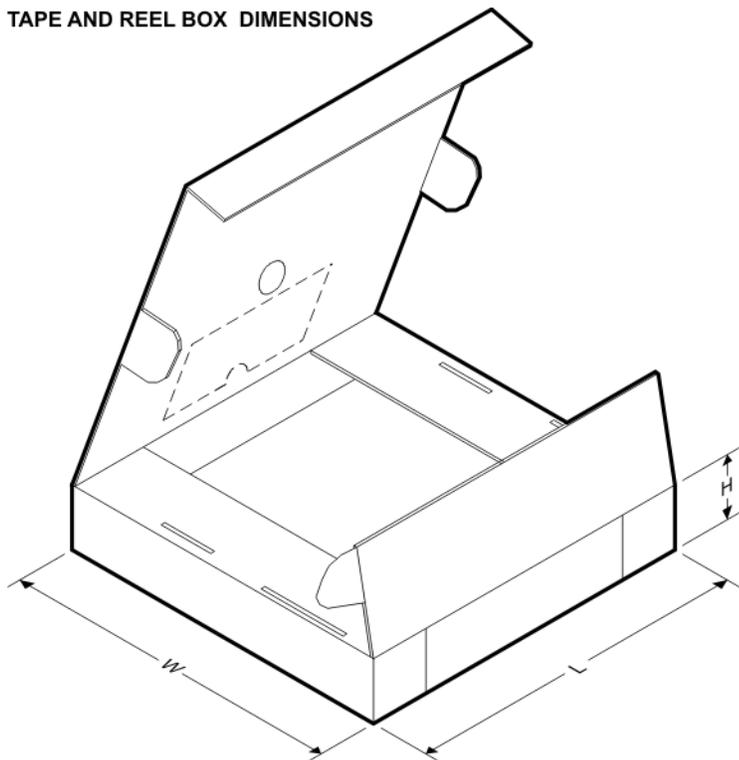
*All dimensions are nominal

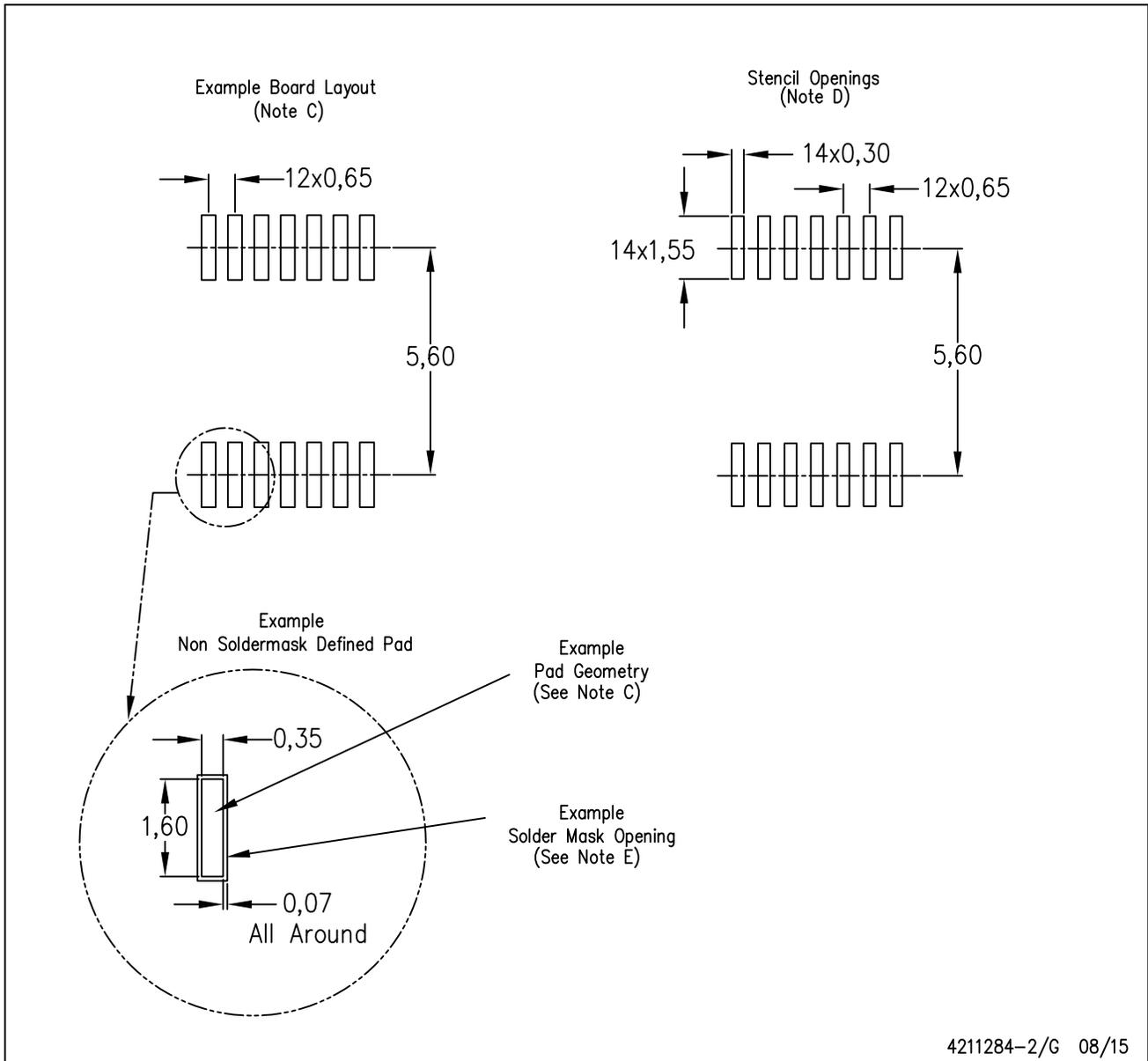| Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2264AQPWRG4Q1	TSSOP	PW	14	2000	853.0	449.0	35.0
TLC2264AQPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE

0,15 NOM

Gage Plane

0°–8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

0,10

4040064–3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
          B. This drawing is subject to change without notice.
          C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
          D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E. Falls within JEDEC MO–153

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PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

←12x0,65

5,60

Stencil Openings
(Note D)

←14x0,30

←12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284-2/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC–7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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