

# CDx4HC374 High-Speed CMOS Logic Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered

## 1 Features

- Buffered inputs
- Common three-state output enable control
- Three-state outputs
- Bus line driving capability
- Typical propagation delay (clock to Q) = 15 ns at  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range:  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2-V to 6-V operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5-V to 5.5-V Operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V}$  (max),  $V_{IH} = 2\text{ V}$  (min)
  - CMOS input compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

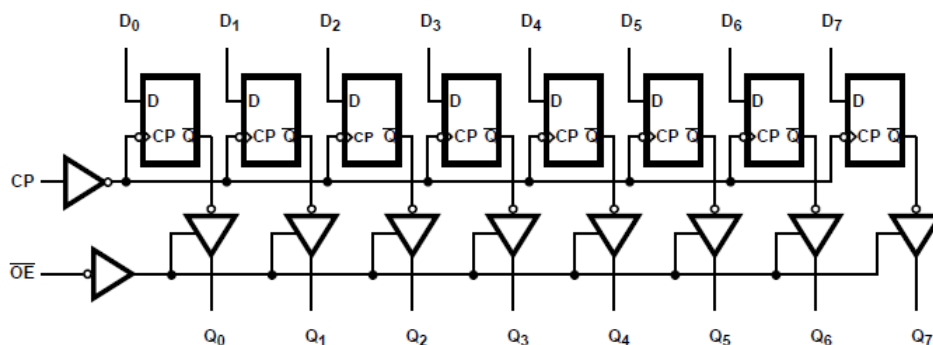
## 2 Description

The 'HC374, 'HCT374, 'HC574, and 'HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When  $\overline{OE}$  is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD54HC374F3A	CDIP (20)	26.92 mm × 6.92 mm
CD54HC574F	CDIP (20)	26.92 mm × 6.92 mm
CD54HCT374F3A	CDIP (20)	26.92 mm × 6.92 mm
CD54HCT574F	CDIP (20)	26.92 mm × 6.92 mm
CD74HC374M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC574M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT374M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT574M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC374E	PDIP (20)	25.40 mm × 6.35 mm
CD74HC574E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT374E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT574E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT574PWR	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagram



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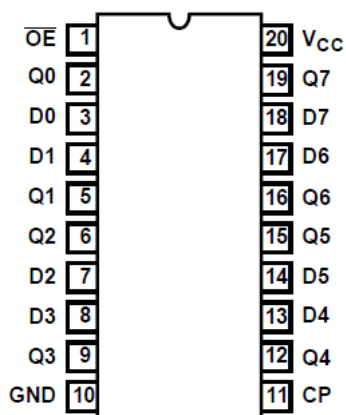
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## 3 Revision History

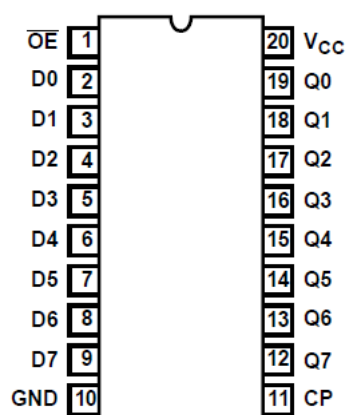
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (May 2004) to Revision D (January 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	<b>1</b>

## 4 Pin Configuration and Functions



**HC(T) 374**  
J, DW, or N package  
20-Pin CDIP, SOIC, or PDIP  
Top View



**HC(T) 574**  
J, DW, N, or PW package  
20-Pin CDIP, SOIC, PDIP, or TSSOP  
Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		– 0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < –0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>OK</sub>	Output diode current	For V <sub>O</sub> < –0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>O</sub>	Drain current, per output	For –0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±35	mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > –0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25	mA
	Continuous current through V <sub>CC</sub> or ground current			±50	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead Tips Only)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V <sub>I</sub> , V <sub>O</sub>	DC input or output voltage		0	V <sub>CC</sub>	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T <sub>A</sub>	Temperature range		–55	125	°C

### 5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	58	69	83	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V <sub>IH</sub>	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V <sub>IL</sub>	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		
			6	1.8			1.8		1.8		
V <sub>OH</sub>	High level output voltage CMOS loads	I <sub>OH</sub> = – 20 µA	2	1.9			1.9		1.9		V
		I <sub>OH</sub> = – 20 µA	4.5	4.4			4.4		4.4		
		I <sub>OH</sub> = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage TTL loads	I <sub>OH</sub> = – 6 mA	4.5	3.98			3.84		3.7		V
		I <sub>OH</sub> = –7.8 mA	6	5.48			5.34		5.2		
V <sub>OL</sub>	Low level output voltage CMOS loads	I <sub>OL</sub> = 20 µA	2	0.1			0.1		0.1		V
		I <sub>OL</sub> = 20 µA	4.5	0.1			0.1		0.1		
		I <sub>OL</sub> = 20 µA	6	0.1			0.1		0.1		
	Low level output voltage TTL loads	I <sub>OL</sub> = 6 mA	4.5	0.26			0.33		0.4		V
		I <sub>OL</sub> = 7.8 mA	6	0.26			0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	±0.1			±1		±1		µA
I <sub>CC</sub>	Quiescent device current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	8			80		160		µA
V <sub>IL</sub> or V <sub>IH</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	6	±0.5			±5.0		±10		µA
HCT TYPES											
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2			2		2		V
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V <sub>OH</sub>	High level output voltage CMOS loads	I <sub>OH</sub> = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage TTL loads	I <sub>OH</sub> = – 6 mA	4.5	3.98			3.84		3.7		
V <sub>OL</sub>	Low level output voltage CMOS loads	I <sub>OL</sub> = 20 µA	4.5	0.1			0.1		0.1		V
	Low level output voltage TTL loads	I <sub>OL</sub> = 6 mA	4.5	0.26			0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	±0.1			±1		±1		µA
I <sub>CC</sub>	Quiescent device current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	8			80		160		µA
V <sub>IL</sub> or V <sub>IH</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	6	±0.5			±5.0		±10		µA

## 5.4 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\Delta I_{CC}$ <sup>(1)</sup>	HCT374 Additional quiescent device current per input pin	D0 - D7 inputs held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	108		135		147	μA
		CP input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	324		405		441	μA
		OE input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	468		585		637	μA
	HCT574 Additional quiescent device current per input pin	D0 - D7 inputs held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	144		180		196	μA
		CP input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	270		337.5		367.5	μA
		OE input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	216		270		294	μA

(1) For dual-supply systems, theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.5 Prerequisite for Switching Characteristics

PARAMETER		V <sub>CC</sub> (V)	25°C			–40°C to 85°C			–55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
f <sub>MAX</sub>	Maximum clock frequency	2	6			5			4			MHz
		4.5	30			25			20			
		6	35			29			23			
t <sub>W</sub>	Clock pulse width	2	80			100			120			ns
		4.5	16			20			24			
		6	14			17			20			
t <sub>SU</sub>	Setup time data to clock	2	60			75			90			ns
		4.5	12			15			18			
		6	10			13			15			
t <sub>H</sub>	Hold time data to clock	2	5			5			5			ns
		4.5	5			5			5			
		6	5			5			5			
HCT TYPES												
f <sub>MAX</sub>	Maximum clock frequency	4.5	30			25			20			MHz
t <sub>W</sub>	Clock pulse width	4.5	16			20			24			ns
t <sub>SU</sub>	Setup time data to clock	4.5	12			15			18			ns
t <sub>H</sub>	Hold time data to clock	4.5	5			5			5			ns

## 5.6 Switching Characteristics

$C_L = 50$  pF, Input  $t_r$ ,  $t_f = 6$  ns

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay Clock to output	C <sub>L</sub> = 50 pF	2	165			205		250		ns
			4.5	33			41		50		
		C <sub>L</sub> = 15 pF	5	15							ns
			C <sub>L</sub> = 50 pF	6	28			35		43	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output disable to Q	C <sub>L</sub> = 50 pF	2	135			170		205		ns
			4.5	27			34		41		
		C <sub>L</sub> = 15 pF	5	11							ns
			C <sub>L</sub> = 50 pF	6	23			29		35	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output enable to Q	C <sub>L</sub> = 50 pF	2	150			190		225		ns
			4.5	30			38		45		
		C <sub>L</sub> = 15 pF	5	12							ns
			C <sub>L</sub> = 50 pF	6	26			33		38	
f <sub>MAX</sub>	Maximum clock frequency	C <sub>L</sub> = 15 pF	5	60							MHz
t <sub>THL</sub> , t <sub>TLH</sub>	Output transition time	C <sub>L</sub> = 50 pF	2	60			75		90		ns
			4.5	12			15		18		
			6	10			13		15		
C <sub>I</sub>	Input capacitance	C <sub>L</sub> = 50 pF		10			10		10		pF
C <sub>O</sub>	Three-state output capacitance			20			20		20		pF
C <sub>PD</sub>	Power dissipation capacitance <sup>(1) (2)</sup>	C <sub>L</sub> = 15 pF	5	39							pF
HCT TYPES											
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay Clock to output	C <sub>L</sub> = 50 pF	4.5	33			41		50		ns
		C <sub>L</sub> = 15 pF	5	15							
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output disable to Q	C <sub>L</sub> = 50pF	4.5	28			35		42		ns
		C <sub>L</sub> = 15 pF	5	11							
t <sub>PZL</sub> , t <sub>PZH</sub>	Output enable to Q	C <sub>L</sub> = 50 pF	4.5	30			38		45		ns
		C <sub>L</sub> = 15 pF	5	12							
f <sub>MAX</sub>	Maximum clock frequency	C <sub>L</sub> = 15 pF	5	60							MHz
t <sub>TLH</sub> , t <sub>THL</sub>	Output transition time	C <sub>L</sub> = 50 pF	4.5	12			15		18		ns
C <sub>I</sub>	Input capacitance	C <sub>L</sub> = 50 pF		10			10		10		pF
C <sub>O</sub>	Three-state output capacitance			20			20		20		pF
C <sub>PD</sub>	Power dissipation capacitance <sup>(1) (2)</sup>	C <sub>L</sub> = 15 pF	5	47							pF

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per package.

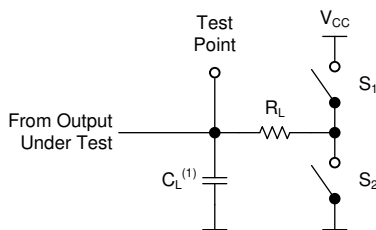
(2)  $P_D = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 f_o C_L$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_f < 6 \text{ ns}$ .

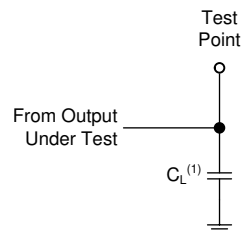
For clock inputs,  $f_{\max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



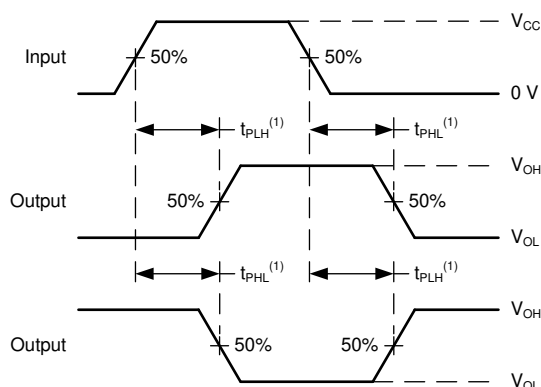
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for 3-State Outputs**



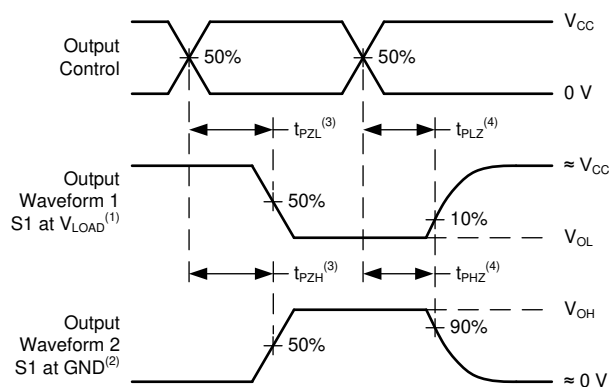
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-2. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

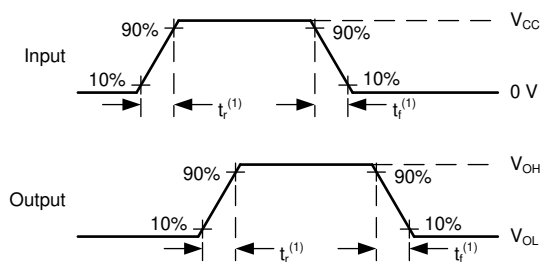
**Figure 6-3. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**



(1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

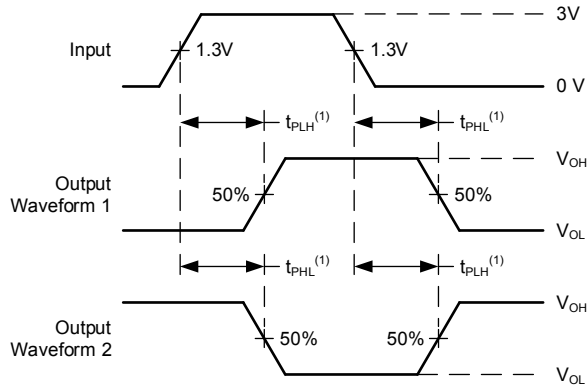
**Figure 6-4. Voltage Waveforms, Standard CMOS Inputs Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

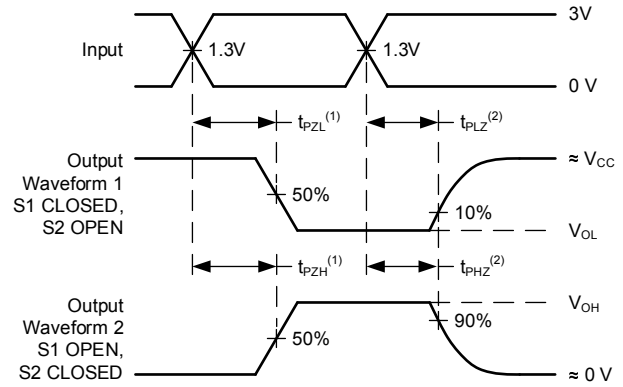
**Figure 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**





(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-6. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**



(1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

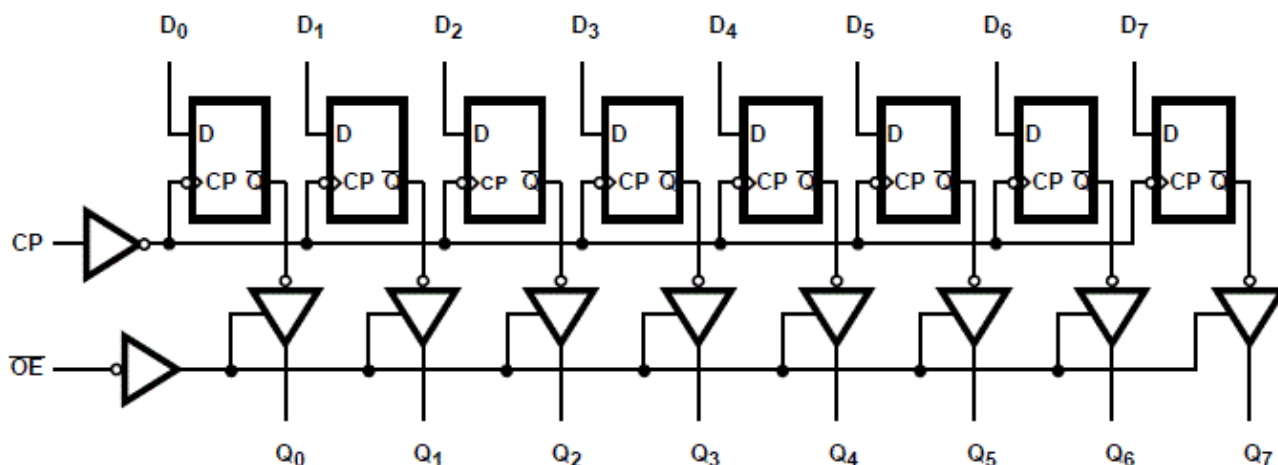
**Figure 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays**

## 7 Detailed Description

### 7.1 Overview

The 'HC374, 'HCT374, 'HC574, and 'HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When  $\overline{OE}$  is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

Table 7-1. Truth Table<sup>(1)</sup>

INPUTS			OUTPUT
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

- (1) H = high level (steady state), L = low level (steady state), X = don't care, ↑ = transition from low to high level, Q0 = the level of Q before the indicated steady-state input conditions were established, Z = high impedance state

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8974201RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8974201RA CD54HCT574F3A	<a href="#">Samples</a>
CD54HC374F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8407101RA CD54HC374F3A	<a href="#">Samples</a>
CD54HC574F	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC574F	<a href="#">Samples</a>
CD54HC574F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC574F3A	<a href="#">Samples</a>
CD54HCT374F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8550701RA CD54HCT374F3A	<a href="#">Samples</a>
CD54HCT574F	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT574F	<a href="#">Samples</a>
CD54HCT574F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8974201RA CD54HCT574F3A	<a href="#">Samples</a>
CD74HC374E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC374E	<a href="#">Samples</a>
CD74HC374M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC374M	<a href="#">Samples</a>
CD74HC374M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC374M	<a href="#">Samples</a>
CD74HC374M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC374M	<a href="#">Samples</a>
CD74HC574E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC574E	<a href="#">Samples</a>
CD74HC574M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC574M	<a href="#">Samples</a>
CD74HC574M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC574M	<a href="#">Samples</a>
CD74HC574M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC574M	<a href="#">Samples</a>
CD74HC574M96G4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC574M	<a href="#">Samples</a>
CD74HCT374E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT374E	<a href="#">Samples</a>
CD74HCT374EE4	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT374E	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT374M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT374M	<a href="#">Samples</a>
CD74HCT374M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT374M	<a href="#">Samples</a>
CD74HCT574E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT574E	<a href="#">Samples</a>
CD74HCT574M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT574M	<a href="#">Samples</a>
CD74HCT574M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT574M	<a href="#">Samples</a>
CD74HCT574M96G4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT574M	<a href="#">Samples</a>
CD74HCT574ME4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT574M	<a href="#">Samples</a>
CD74HCT574PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK574	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC374, CD54HC574, CD54HCT374, CD54HCT574, CD74HC374, CD74HC574, CD74HCT374, CD74HCT574 :**

- Catalog : [CD74HC374](#), [CD74HC574](#), [CD74HCT374](#), [CD74HCT574](#)
- Automotive : [CD74HCT574-Q1](#), [CD74HCT574-Q1](#)
- Enhanced Product : [CD74HCT574-EP](#), [CD74HCT574-EP](#)
- Military : [CD54HC374](#), [CD54HC574](#), [CD54HCT374](#), [CD54HCT574](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC374M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC574M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT374M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT574M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT574PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC374E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC374M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HC574E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC574M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT374E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT374EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT374M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT574E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT574M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT574ME4	DW	SOIC	20	25	507	12.83	5080	6.6



# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

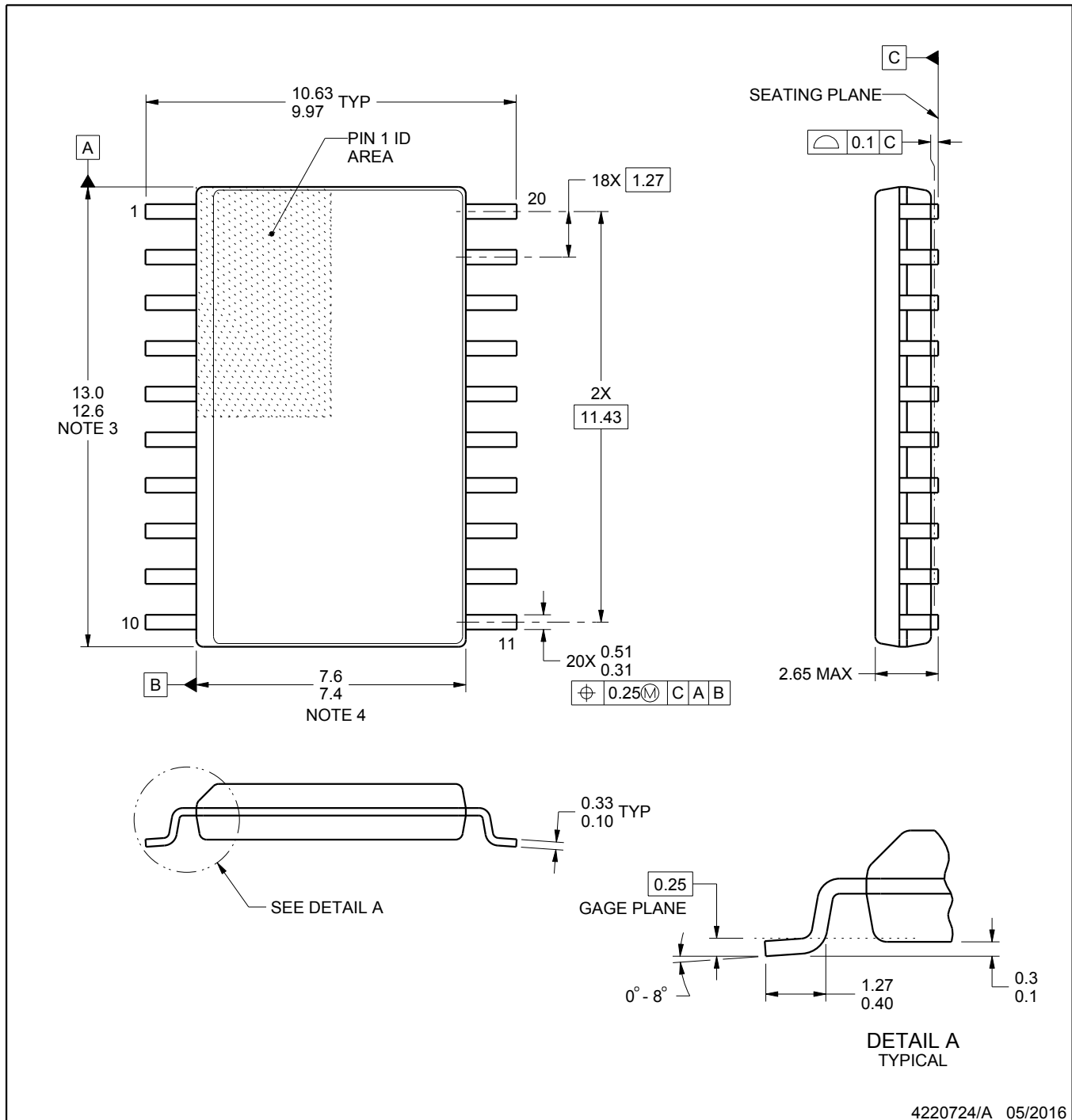


4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.





4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

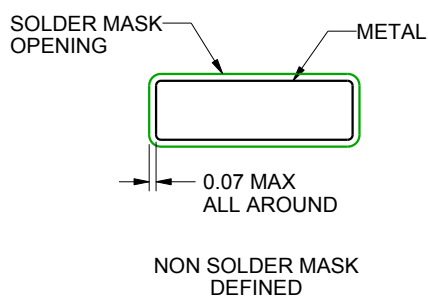
**DW0020A**

### SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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