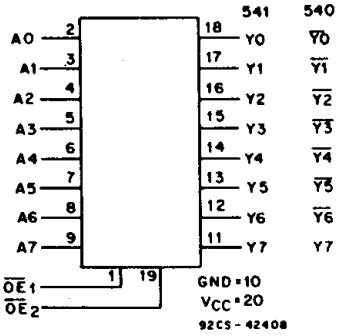
**Technical Data**

# CD54/74AC540, CD54/74AC541
# CD54/74ACT540, CD54/74ACT541

Data sheet acquired from Harris Semiconductor
SCHS285A – Revised November 1999




**FUNCTIONAL DIAGRAM**

## Octal Buffer/Line Drivers, 3-State

CD74AC/ACT540 - Inverting
CD74AC/ACT541 - Non-Inverting

**Type Features:**

- *Buffered inputs*
- *Typical propagation delay:*
  *4.5 ns @ $V_{CC}$ = 5 V, $T_A$ = 25° C, $C_L$ = 50 pF*

The CD54/74AC540, -541, and CD54/74ACT540, -541 octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT540 are inverting 3-state buffers having two active-LOW output enables. The CD54/74AC/ACT541 are non-inverting 3-state buffers having two active-LOW output enables.

The CD74AC540, -541, and CD74ACT540, -541 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Industrial (–40 to +85°C) and Extended Industrial/Military (–55 to +125°C).

The CD54AC540, -541, and CD54ACT540, -541, available in chip form (H suffix), are operable over the –55 to +125°C temperature range.

**Family Features:**

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

*®FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

**TRUTH TABLE**

| CD54/74AC/ACT540 | | |
|---|---|---|
| INPUTS | | OUTPUTS |
| $\overline{OE1}$, $\overline{OE2}$ | A | Y |
| L | L | H |
| L | H | L |
| H | X | Z |

**TRUTH TABLE**

| CD54/74AC/ACT541 | | |
|---|---|---|
| INPUTS | | OUTPUTS |
| $\overline{OE1}$, $\overline{OE2}$ | A | Y |
| L | L | L |
| L | H | H |
| H | X | Z |

H = High Voltage
L = Low Voltage
X = Immaterial
Z = High Impedance

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE ($V_{CC}$) ..... –0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC $V_{CC}$ OR GROUND CURRENT ($I_{CC}$ or $I_{GND}$) ..... ±100 mA*
PACKAGE THERMAL IMPEDANCE, $\theta_{JA}$ (see Note 1): E package ..... 69°C/W
M package ..... 58°C/W
STORAGE TEMPERATURE ($T_{stg}$) ..... –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

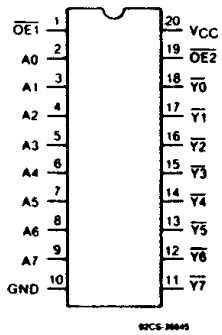
* For up to 4 outputs per device: add ±25 mA for each additional output.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:**

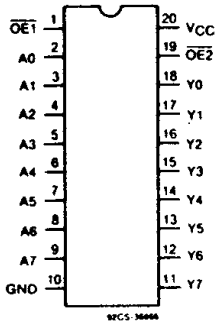
| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range, $V_{CC}$*: (For $T_A$ = Full Package-Temperature Range) | | | |
| AC Types | 1.5 | 5.5 | V |
| ACT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage, $V_I$, $V_O$ | 0 | $V_{CC}$ | V |
| Operating Temperature, $T_A$: | –55 | +125 | °C |
| Input Rise and Fall Slew Rate, dt/dv | | | |
| at 1.5 V to 3 V (AC Types) | 0 | 50 | ns/V |
| at 3.6 V to 5.5 V (AC Types) | 0 | 20 | ns/V |
| at 4.5 V to 5.5 V (ACT Types) | 0 | 10 | ns/V |

*Unless otherwise specified, all voltages are referenced to ground.

**TERMINAL ASSIGNMENT DIAGRAMS**




**CD54/74AC/ACT540**




**CD54/74AC/ACT541**

# CD54/74AC540, CD54/74AC541
# CD54/74ACT540, CD54/74ACT541

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | |
| | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | |
| Low-Level Input Voltage $V_{IL}$ | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V |
| | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | |
| | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | #, * | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | #, * | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | #, * | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | #, * | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

# CD54/74AC540, CD54/74AC541
# CD54/74ACT540, CD54/74ACT541

**STATIC ELECTRICAL CHARACTERISTICS: ACT Series**

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V |
| Low-Level Input Voltage $V_{IL}$ | | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | #, * | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | #, * | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load $\Delta I_{CC}$ | $V_{CC}$-2.1 | | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

**ACT INPUT LOADING TABLE**

| INPUT | UNIT LOAD* | |
|---|---|---|
| | 540 | 541 |
| DATA | 1.42 | 0.5 |
| $\overline{OE1}$, $\overline{OE2}$ | 1.3 | 1.3 |

*Unit load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC540, CD54/74AC541
# CD54/74ACT540, CD54/74ACT541

**SWITCHING CHARACTERISTICS: AC Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output AC540 | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 77 | — | 85 | ns |
| | | 3.3* | 2.4 | 8.6 | 2.4 | 9.5 | |
| | | 5† | 1.8 | 6.2 | 1.7 | 6.8 | |
| AC541 | $t_{PLH}$ $t_{PHL}$ | 1.5 | — | 89 | — | 98 | ns |
| | | 3.3 | 2.8 | 9.9 | 2.7 | 10.9 | |
| | | 5 | 2.1 | 7.1 | 2 | 7.8 | |
| Enable, to Output to Output | $t_{PZL}$ $t_{PZH}$ | 1.5 | — | 136 | — | 150 | ns |
| | | 3.3 | 4.6 | 16.4 | 4.5 | 18 | |
| | | 5 | 3.1 | 10.9 | 3 | 12 | |
| Disable to Output to Output | $t_{PLZ}$ $t_{PHZ}$ | 1.5 | — | 136 | — | 150 | ns |
| | | 3.3 | 3.9 | 13.6 | 3.8 | 15 | |
| | | 5 | 3.1 | 10.9 | 3 | 12 | |
| Power Dissipation Capacitance AC540 AC541 | $C_{PD}$‡ | — | 60 Typ. | | 60 Typ. | | pF |
| | | — | 60 Typ. | | 60 Typ. | | |
| Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | — | 15 | pF |

**SWITCHING CHARACTERISTICS: ACT Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to =125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output ACT540 | $t_{PLH}$ $t_{PHL}$ | 5† | 1.9 | 6.5 | 1.8 | 7.2 | ns |
| ACT541 | $t_{PLH}$ $t_{PHL}$ | 5† | 2.1 | 7.5 | 2.1 | 8.2 | ns |
| Enable to Output | $t_{PZL}$ $t_{PZH}$ | 5 | 3.5 | 12.2 | 3.4 | 13.4 | ns |
| Disable to Output | $t_{PLZ}$ $t_{PHZ}$ | 5 | 3.5 | 12.2 | 3.4 | 13.4 | ns |
| Power Dissipation Capacitance ACT540 ACT541 | $C_{PD}$§ | — | 60 Typ. | | 60 Typ. | | pF |
| | | — | 60 Typ. | | 60 Typ. | | |
| Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | — | 15 | pF |

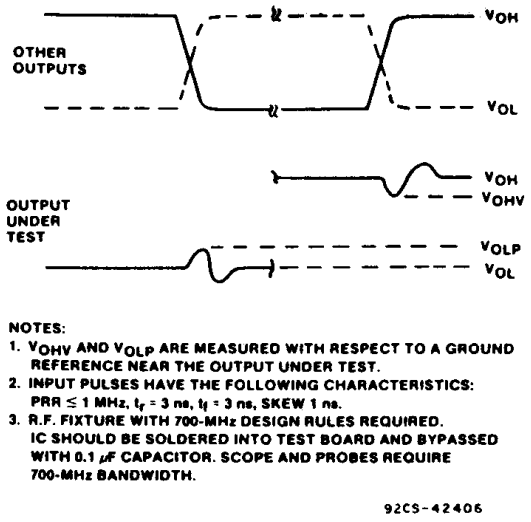
*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§$C_{PD}$ is used to determine the dynamic power consumption, per channel.
For AC series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where $f_i$ = input frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage.

# CD54/74AC540, CD54/74AC541
# CD54/74ACT540, CD54/74ACT541

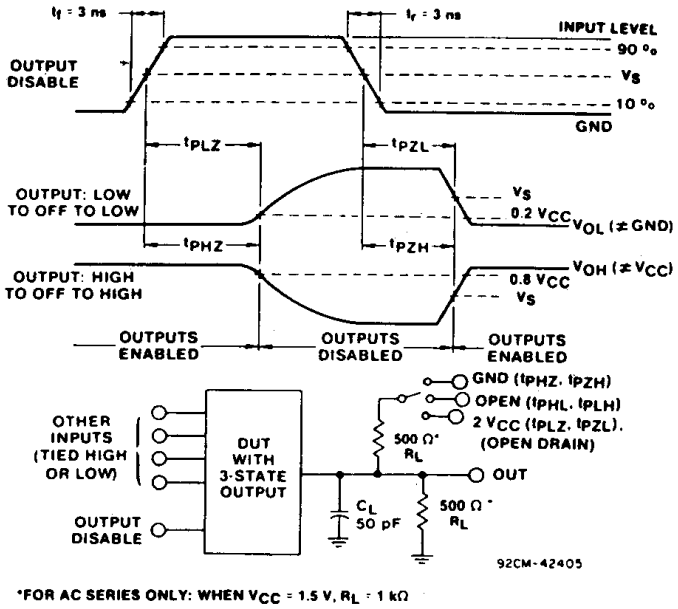
## PARAMETER MEASUREMENT INFORMATION




NOTES:
1. $V_{OHV}$ AND $V_{OLP}$ ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, $t_r$ = 3 ns, $t_f$ = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

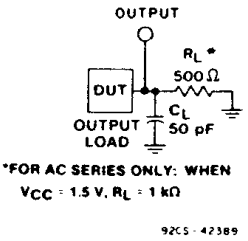
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*Fig. 1 - Simultaneous switching transient waveforms.*




*FOR AC SERIES ONLY: WHEN $V_{CC}$ = 1.5 V, $R_L$ = 1 kΩ

*Fig. 2 - Three-state propagation delay waveforms and test circuit.*




*FOR AC SERIES ONLY: WHEN $V_{CC}$ = 1.5 V, $R_L$ = 1 kΩ

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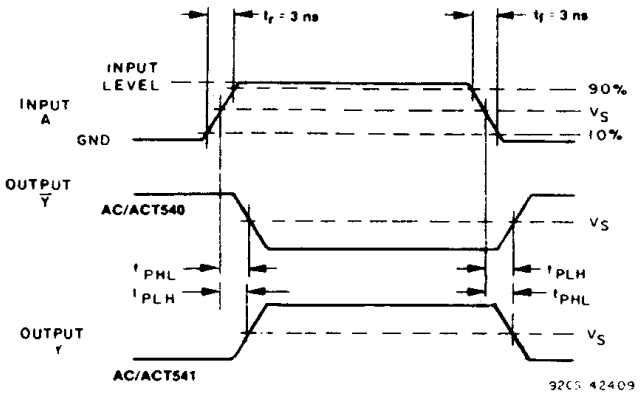



*Fig. 3 - Propagation delay times and test circuit.*

| | CD54/74AC | CD54/74ACT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| Input Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 1.5 V |
| Output Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 0.5 $V_{CC}$ |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54AC541F3A | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54AC541F3A | Samples |
| CD54ACT540F3A | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54ACT540F3A | Samples |
| CD54ACT541F3A | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54ACT541F3A | Samples |
| CD74AC540M | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC540M | Samples |
| CD74AC540M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | AC540M | Samples |
| CD74AC540ME4 | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC540M | Samples |
| CD74AC541E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC541E | Samples |
| CD74AC541EE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC541E | Samples |
| CD74AC541M | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC541M | Samples |
| CD74AC541M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC541M | Samples |
| CD74AC541M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC541M | Samples |
| CD74AC541M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC541M | Samples |
| CD74AC541SM96 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC541SM | Samples |
| CD74ACT540E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT540E | Samples |
| CD74ACT540M | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT540M | Samples |
| CD74ACT540M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT540M | Samples |
| CD74ACT540M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT540M | Samples |
| CD74ACT540MG4 | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT540M | Samples |
| CD74ACT541E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT541E | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74ACT541EE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT541E | Samples |
| CD74ACT541M | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT541M | Samples |
| CD74ACT541M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT541M | Samples |
| CD74ACT541M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT541M | Samples |
| CD74ACT541M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT541M | Samples |
| CD74ACT541MG4 | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT541M | Samples |
| CD74ACT541SM96 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT541SM | Samples |
| CD74ACT541SM96E4 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT541SM | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC541, CD54ACT540, CD54ACT541, CD74AC541, CD74ACT540, CD74ACT541 :**

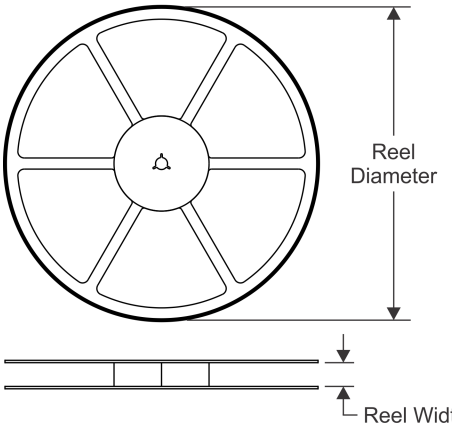
- Catalog : CD74AC541, CD74ACT540, CD74ACT541
- Military : CD54AC541, CD54ACT540, CD54ACT541

NOTE: Qualified Version Definitions:

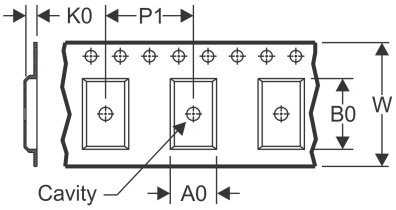
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

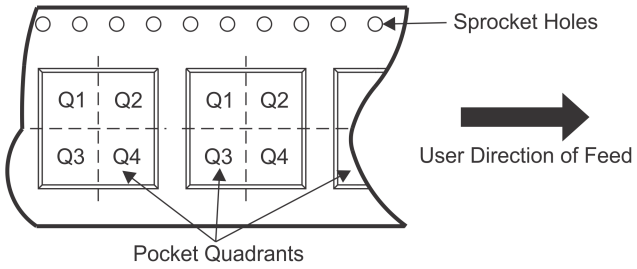



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

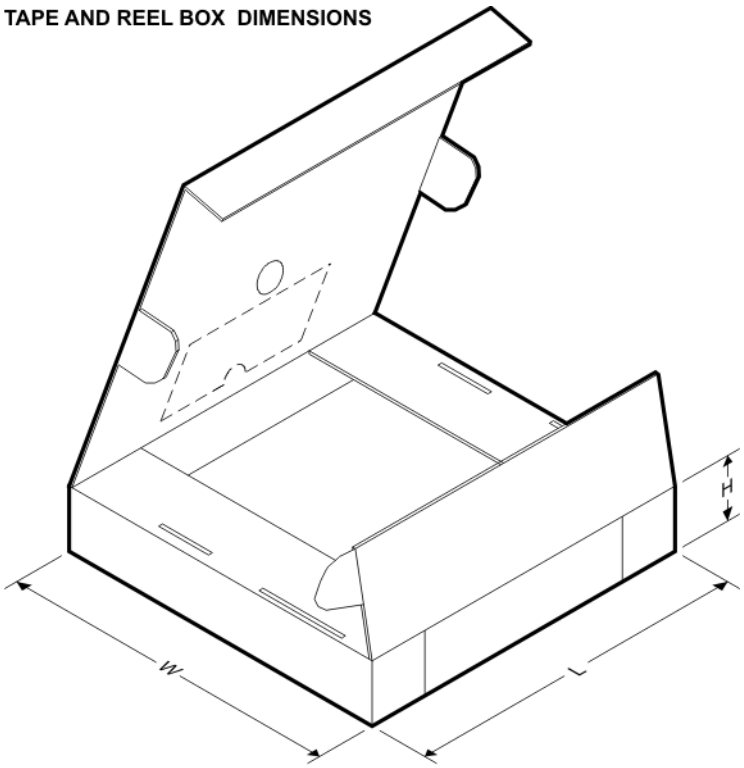
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC540M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74AC541M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74AC541SM96 | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74ACT540M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT541M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT541SM96 | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |

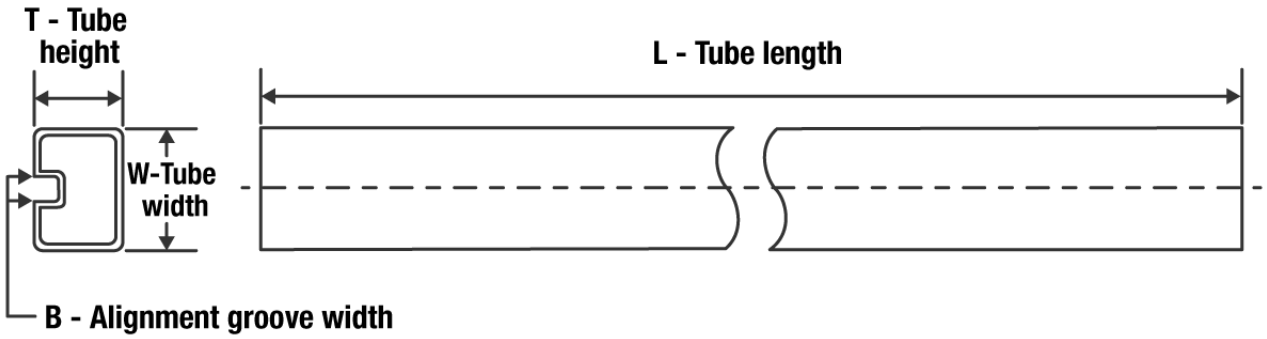
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC540M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74AC541M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74AC541SM96 | SSOP | DB | 20 | 2000 | 853.0 | 449.0 | 35.0 |
| CD74ACT540M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74ACT541M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74ACT541SM96 | SSOP | DB | 20 | 2000 | 853.0 | 449.0 | 35.0 |

## TUBE




*All dimensions are nominal

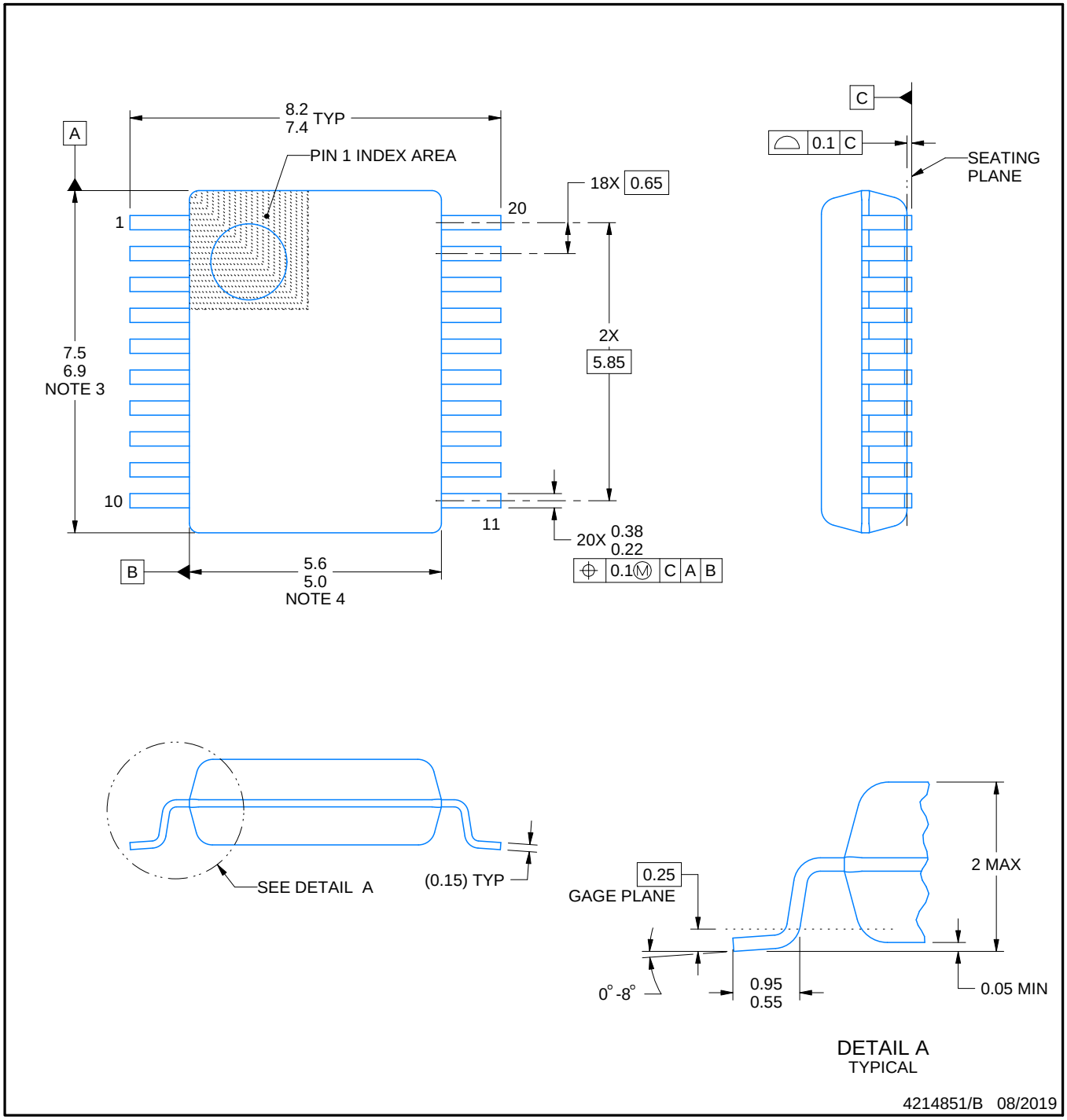
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74AC540M | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CD74AC540ME4 | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CD74AC541E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC541EE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC541M | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CD74ACT540E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT540M | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CD74ACT540MG4 | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CD74ACT541E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT541EE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT541M | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CD74ACT541MG4 | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |

# PACKAGE OUTLINE

## DB0020A

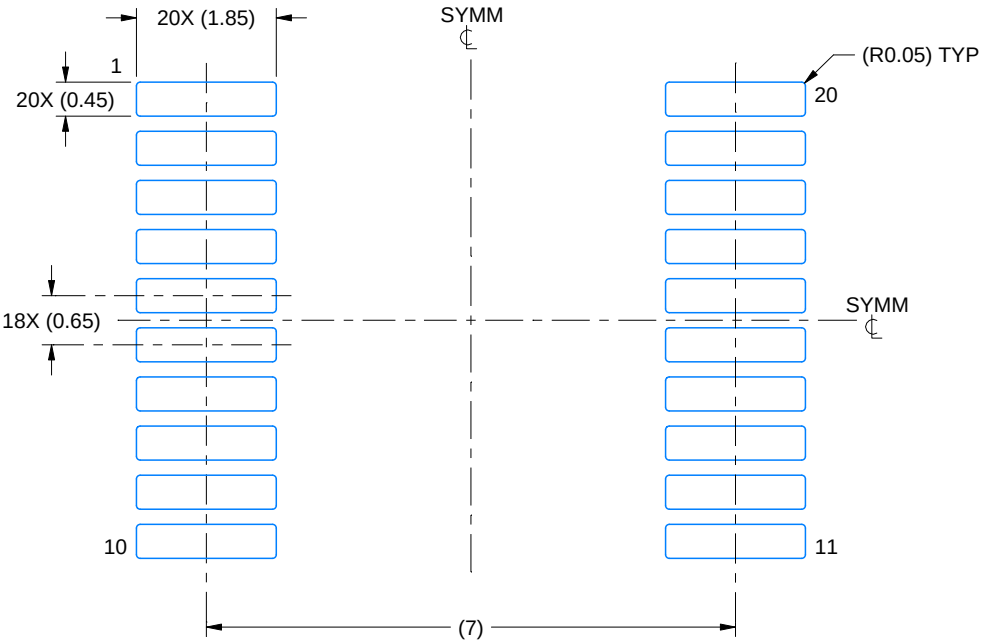
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

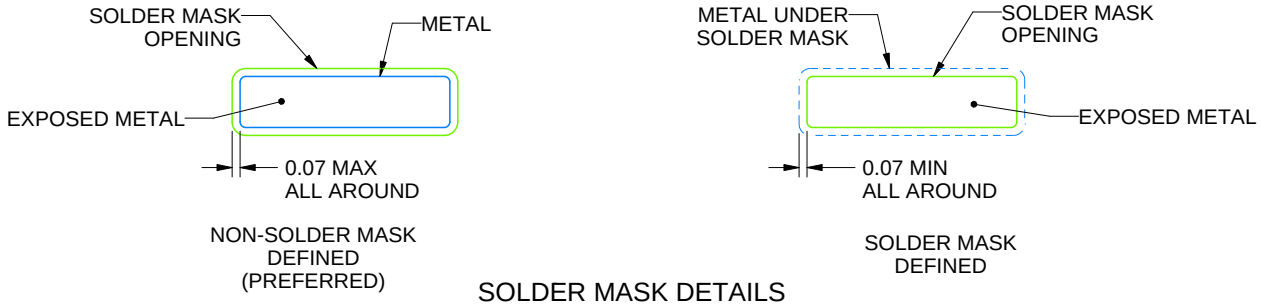



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

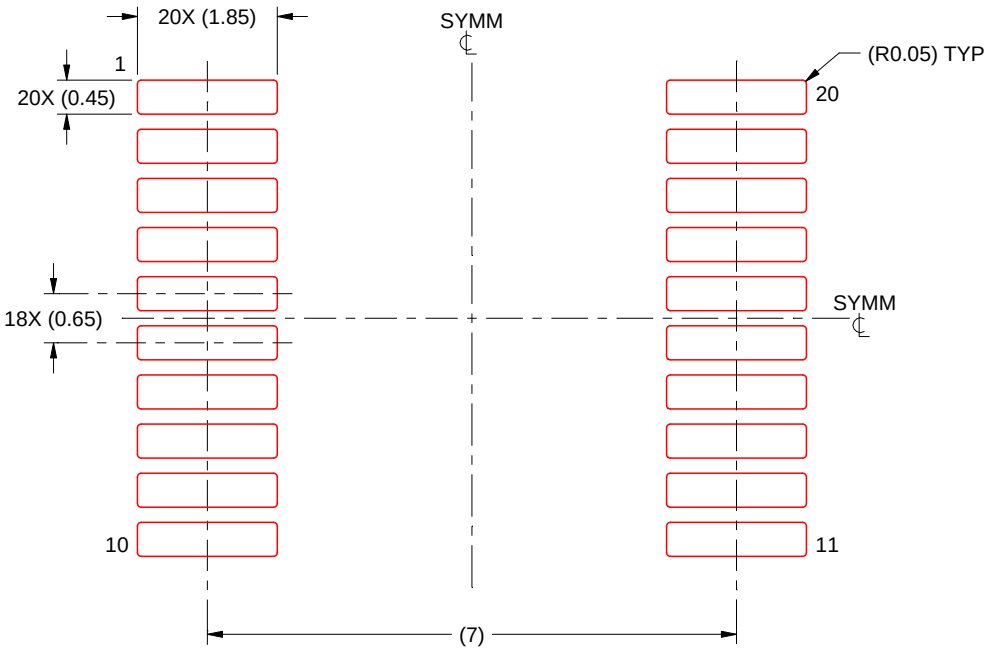
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

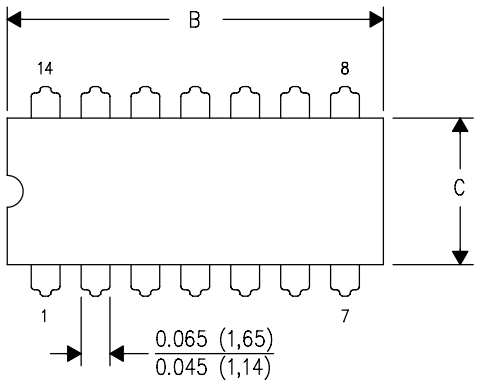
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

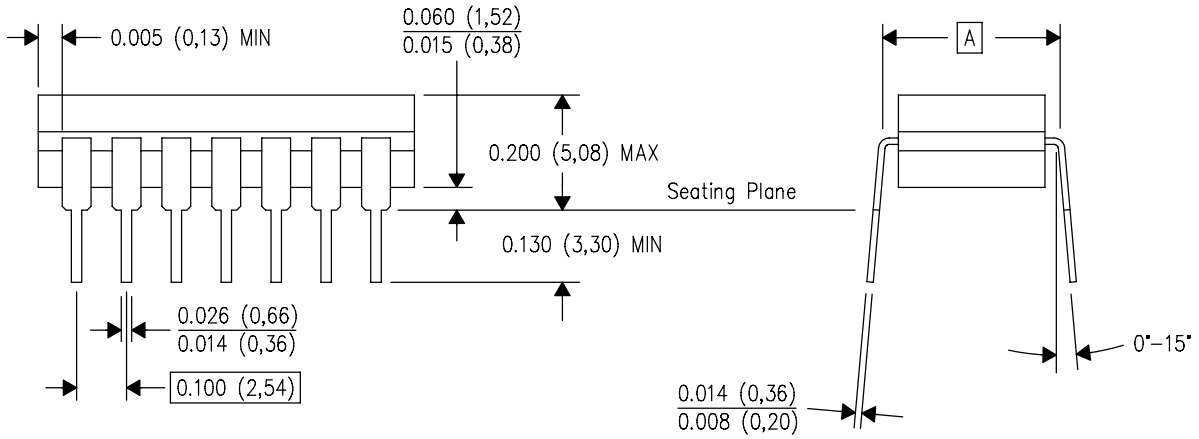
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



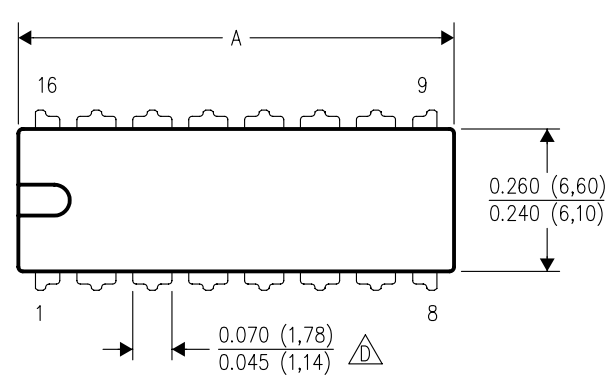

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

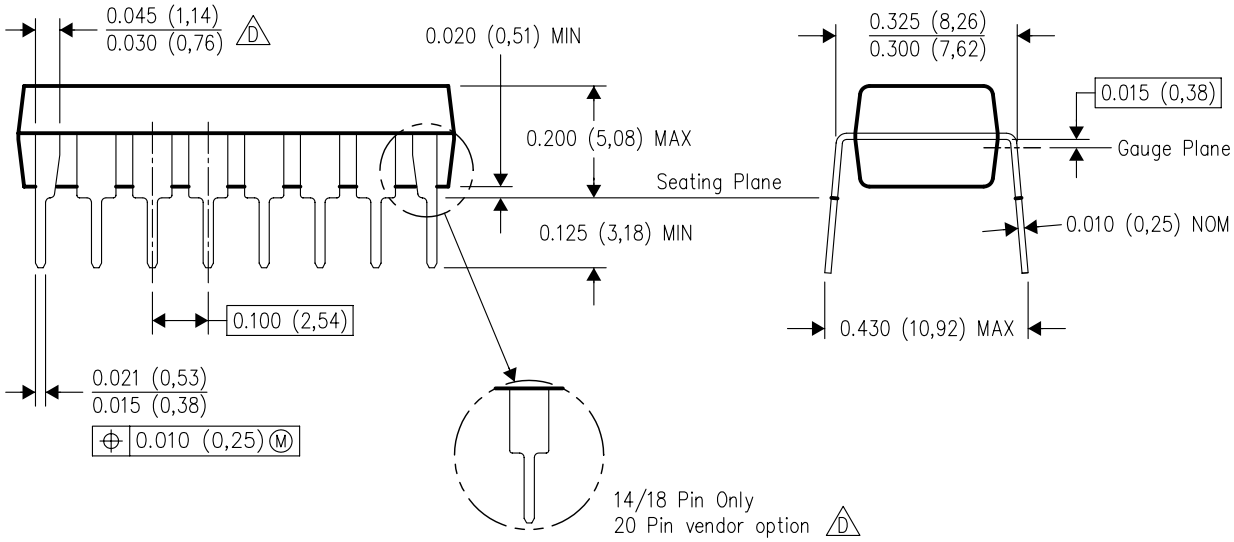
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

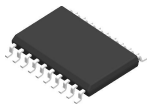



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

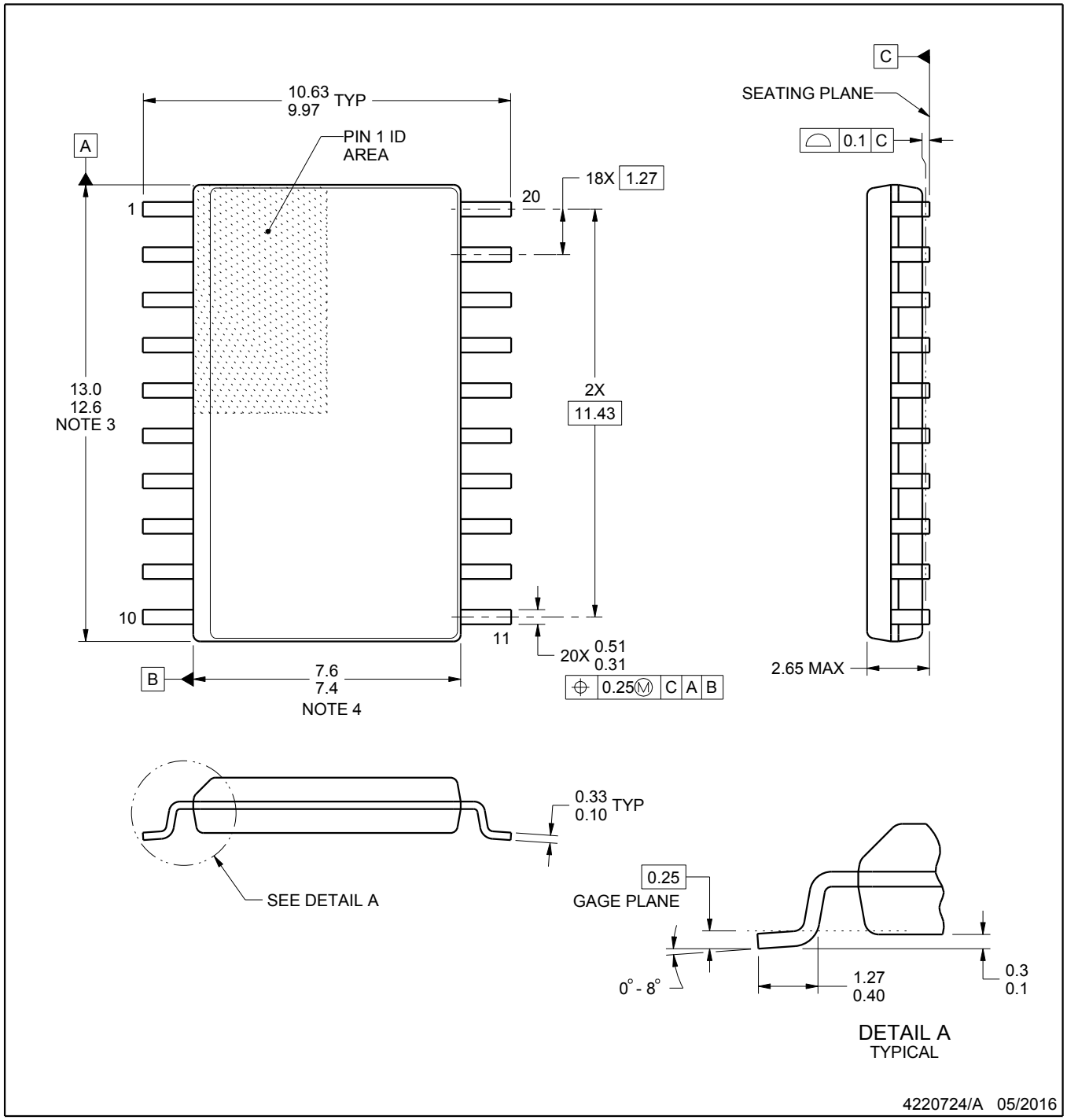


# PACKAGE OUTLINE

## DW0020A

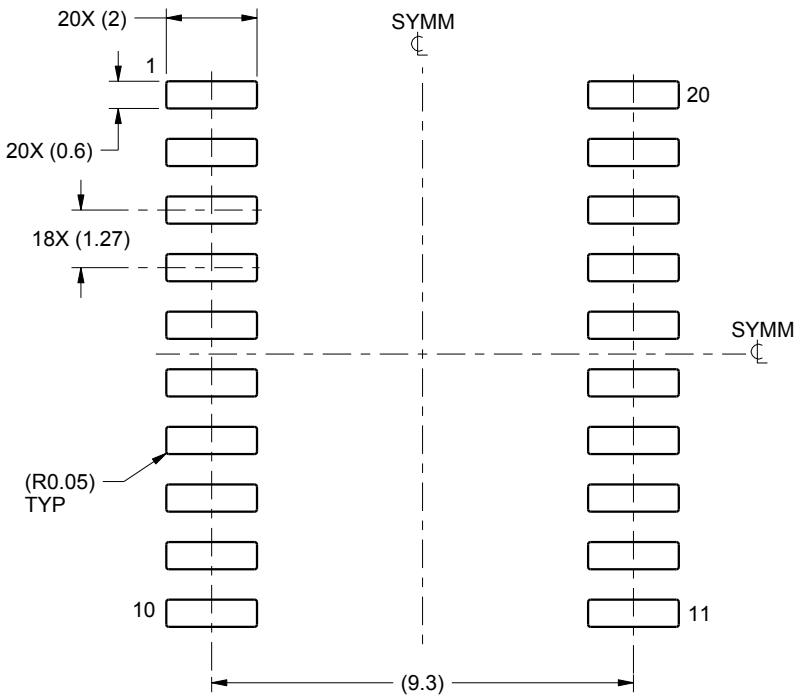
## SOIC - 2.65 mm max height

SOIC

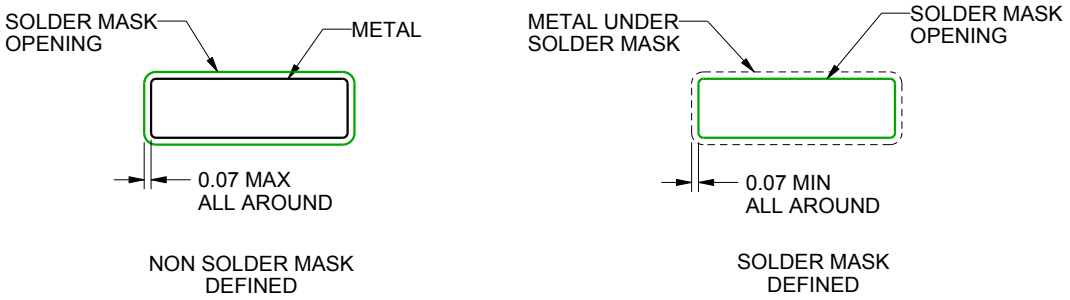



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

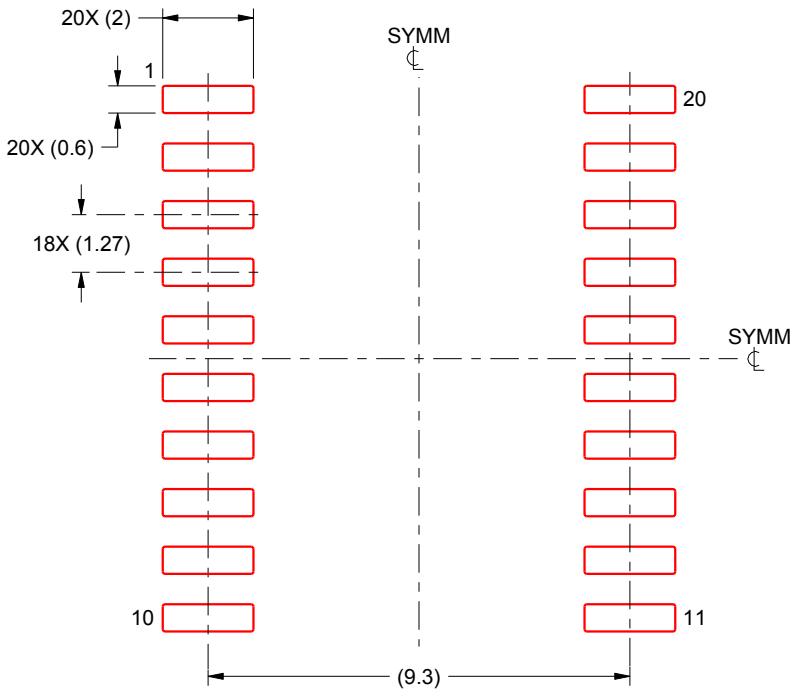



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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