

FEATURES

- Two Precision Timing Circuits Per Package
- Astable or Monostable Operation
- TTL-Compatible Output Can Sink or Source up to 150 mA
- Active Pullup or Pulldown
- Designed to Be Interchangeable With Signetics NE556, SA556, and SE556

APPLICATIONS

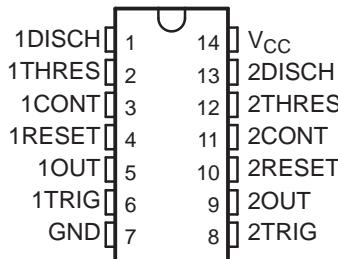
- Precision Timers From Microseconds to Hours
- Pulse-Shaping Circuits
- Missing-Pulse Detectors
- Tone-Burst Generators
- Pulse-Width Modulators
- Pulse-Position Modulators
- Sequential Timers
- Pulse Generators
- Frequency Dividers
- Application Timers
- Industrial Controls
- Touch-Tone Encoders

DESCRIPTION/ORDERING INFORMATION

These devices provide two independent timing circuits of the NA555, NE555, SA555, or SE555 type in each package. These circuits can be operated in the astable or the monostable mode with external resistor-capacitor (RC) timing control. The basic timing provided by the RC time constant can be controlled actively by modulating the bias of the control-voltage input.

The threshold (THRES) and trigger (TRIG) levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by using the control voltage (CONT) terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset, and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between the discharge (DISCH) terminal and ground (GND).

NA556...D OR N PACKAGE
NE556...D, N, OR NS PACKAGE
SA556...D OR N PACKAGE
SE556...J PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T_A	V_T (MAX) $V_{CC} = 15$ V	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING			
0°C to 70°C	11.2 V	PDIP – N	Tube of 25	NE556N	NE556N			
		SOIC – D	Tube of 50	NE556D	NE556			
			Reel of 2500	NE556DR				
-40°C to 85°C		SOP – NS	Reel of 2000	NE556NSR	NE556			
-40°C to 105°C	11.2 V	PDIP – N	Tube of 25	SA556N	SA556N			
		SOIC – D	Tube of 50	NA556N	NA556			
			Reel of 2500	NA556D				
-55°C to 125°C	10.6 V	CDIP – J	Tube of 25	NA556DR	NA556			
				SE556J	SE556J			
				SE556JB	SE556JB			

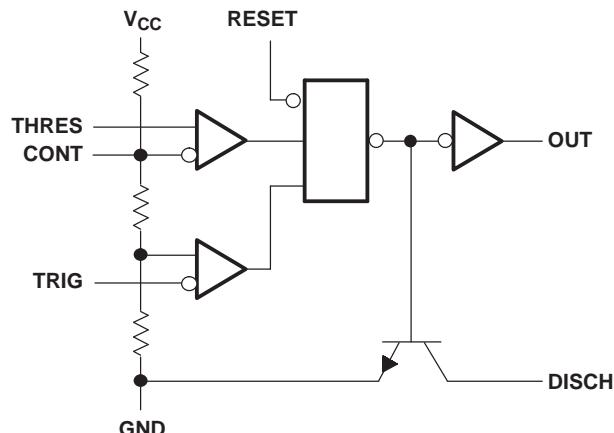
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
 (each timer)

RESET	TRIGGER VOLTAGE ⁽¹⁾	THRESHOLD VOLTAGE ⁽¹⁾	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{DD}	Irrelevant	High	Off
High	>1/3 V_{DD}	>2/3 V_{DD}	Low	On
High	>1/3 V_{DD}	<2/3 V_{DD}	As previously established	

(1) Voltage levels shown are nominal.

FUNCTIONAL BLOCK DIAGRAM, EACH TIMER



RESET can override TRIG, which can override THRES.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾		18	V
V_I	Input voltage	CONT, RESET, THRES, and TRIG	V_{CC}	V
I_O	Output current		± 225	mA
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package	86	°C/W
		N package	80	
		NS package	76	
θ_{JC}	Package thermal impedance ⁽⁵⁾⁽⁶⁾	J package	15.05	°C/W
T_J	Operating virtual junction temperature		150	°C
	Lead temperature 1.6 mm (1/16 in) from case for 60 s	J package	300	°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s	D, N, or NS package	260	°C
T_{stg}	Storage temperature range		-65 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Maximum power dissipation is a function of T_J (max), θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Maximum power dissipation is a function of T_J (max), θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(\max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with MIL-STD-883.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	NA556, NE556, SA556	4.5	16
		SE556	4.5	18
V_I	Input voltage	CONT, RESET, THRES, and TRIG	V_{CC}	V
I_O	Output current		± 200	mA
T_A	Operating free-air temperature	NA556	-40	105
		NE556	0	70
		SA556	-40	85
		SE556	-55	125

Electrical Characteristics

$V_{CC} = 5$ V to 15 V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	NA556 NE556 SA556			SE556			UNIT		
		MIN	TYP	MAX	MIN	TYP	MAX			
V_T Threshold voltage level	$V_{CC} = 15$ V	8.8	10	11.2	9.4	10	10.6	V		
	$V_{CC} = 5$ V	2.4	3.3	4.2	2.7	3.3	4			
I_T Threshold current ⁽¹⁾			30	250	30		250	nA		
V_{TRIG} Trigger voltage level	$V_{CC} = 15$ V	4.5	5	5.6	4.8	5	5.2	V		
		$T_A = -55^\circ\text{C}$ to 125°C		3		6				
	$V_{CC} = 5$ V	1.1	1.67	2.2	1.45	1.67	1.9			
		$T_A = -55^\circ\text{C}$ to 125°C		1.9						
I_{TRIG} Trigger current	TRIG at 0 V		0.5	2	0.5		0.9	µA		
V_{RESET} Reset voltage level			0.3	0.7	1	0.3	0.7	1		
	$T_A = -55^\circ\text{C}$ to 125°C				1.1					
I_{RESET} Reset current	RESET at V_{CC}		0.1	0.4	0.1		0.4	mA		
	RESET at 0 V		-0.4	1.5	-0.4		-1			
I_{DISCH} Discharge switch off-state current			20	100	20		100	nA		
V_{CONT} Control voltage (open circuit)	$V_{CC} = 15$ V	9	10	11	9.6	10	10.4	V		
		$T_A = -55^\circ\text{C}$ to 125°C		9.6		10.4				
	$V_{CC} = 5$ V	2.6	3.3	4	2.9	3.3	3.8			
		$T_A = -55^\circ\text{C}$ to 125°C		2.9		3.8				
V_{OL} Low-level output voltage	$V_{CC} = 15$ V, $I_{OL} = 10$ mA	0.1	0.25	0.1		0.15	V			
		$T_A = -55^\circ\text{C}$ to 125°C		0.2						
	$V_{CC} = 15$ V, $I_{OL} = 50$ mA	0.4	0.75	0.4		0.5				
		$T_A = -55^\circ\text{C}$ to 125°C		1						
	$V_{CC} = 15$ V, $I_{OL} = 100$ mA	2	2.5	2		2.2				
		$T_A = -55^\circ\text{C}$ to 125°C		2.7						
	$V_{CC} = 15$ V, $I_{OL} = 200$ mA		2.5		2.5					
	$V_{CC} = 5$ V, $I_{OL} = 3.5$ mA	$T_A = -55^\circ\text{C}$ to 125°C				0.35				
	$V_{CC} = 5$ V, $I_{OL} = 5$ mA	0.1	0.25	0.1		0.15				
		$T_A = -55^\circ\text{C}$ to 125°C		0.8						
V_{OH} High-level output voltage	$V_{CC} = 5$ V, $I_{OH} = 8$ mA	0.15	0.3	0.15		0.25	V			
	$V_{CC} = 15$ V, $I_{OH} = -100$ mA	12.75	13.3	13		13.3				
		$T_A = -55^\circ\text{C}$ to 125°C		12						
	$V_{CC} = 15$ V, $I_{OH} = -200$ mA		12.5		12.5					
	$V_{CC} = 5$ V, $I_{OH} = -100$ mA	2.75	3.3	3		3.3				
I_{CC} Supply current		$T_A = -55^\circ\text{C}$ to 125°C		2						
Output low, No load	$V_{CC} = 15$ V	20	30	20		24	mA			
	$V_{CC} = 5$ V	6	12	6		10				
Output high, No load	$V_{CC} = 15$ V	18	26	18		20				
	$V_{CC} = 5$ V	4	10	4		8				

(1) This parameter influences the maximum value of the timing resistors R and R_B in the circuit of Figure 1. For example, when $V_{CC} = 5$ V, the maximum value is $R = R_A + R_B \approx 3.4$ MΩ, and for $V_{CC} = 15$ V, the maximum value is ≈ 10 MΩ.

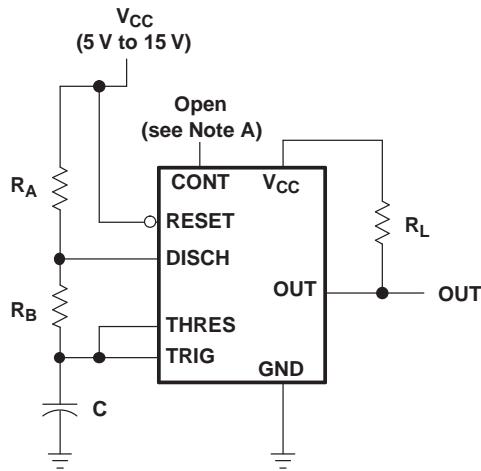
Operating Characteristics

 V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS ⁽¹⁾	NA556 NE556 SA556			SE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval ⁽²⁾	Each timer, monostable ⁽³⁾	T _A = 25°C	1	3		0.5	1.5 ⁽⁴⁾		
	Each timer, astable ⁽⁵⁾		2.25%			1.5%			
	Timer 1 – Timer 2		±1			±0.5			
Temperature coefficient of timing interval	Each timer, monostable ⁽³⁾	T _A = MIN to MAX	50			30	100 ⁽⁴⁾		ppm/°C
	Each timer, astable ⁽⁵⁾		150			90			
	Timer 1 – Timer 2		±10			±10			
Supply voltage sensitivity of timing interval	Each timer, monostable ⁽³⁾	T _A = 25°C	0.1	0.5		0.05	0.2 ⁽⁴⁾		%/V
	Each timer, astable ⁽⁵⁾		0.3			0.15			
	Timer 1 – Timer 2		±0.2			±0.1			
Output-pulse rise time		C _L = 15 pF, T _A = 25°C	100	300		100	200 ⁽⁴⁾	ns	
Output-pulse fall time		C _L = 15 pF, T _A = 25°C	100	300		100	200 ⁽⁴⁾	ns	

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
- (2) Timing-interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
- (3) Values specified are for a device in a monostable circuit similar to [Figure 2](#), with the following component values: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
- (4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (5) Values specified are for a device in an astable circuit similar to [Figure 1](#), with the following component values: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

APPLICATION INFORMATION



NOTE A: Bypassing the control-voltage input to ground with a capacitor might improve operation. This should be evaluated for individual applications.

Figure 1. Circuit for Astable Operation

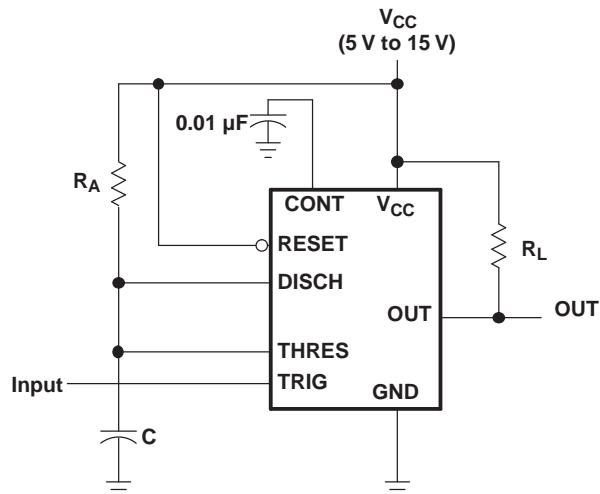


Figure 2. Circuit for Monostable Operation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/10902BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10902BCA	Samples
M38510/10902BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /10902BCA	Samples
NA556D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA556	Samples
NA556DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA556	Samples
NA556N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	NA556N	Samples
NE556D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE556	Samples
NE556DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	N556	Samples
NE556DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE556	Samples
NE556DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE556	Samples
NE556DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE556	Samples
NE556N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	NE556N	Samples
NE556NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	NE556N	Samples
NE556NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NE556	Samples
SA556N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SA556N	Samples
SA556NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SA556N	Samples
SE556J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SE556J	Samples
SE556JB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SE556JB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

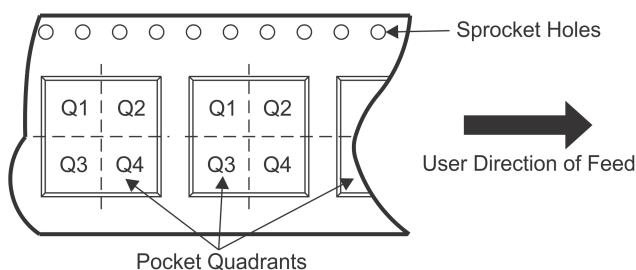
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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


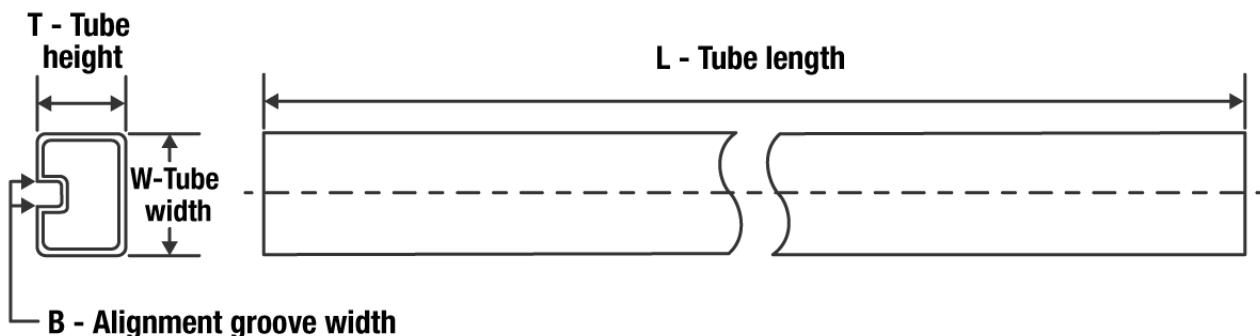
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NA556DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
NE556DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
NE556DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
NE556NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NA556DR	SOIC	D	14	2500	853.0	449.0	35.0
NE556DBR	SSOP	DB	14	2000	853.0	449.0	35.0
NE556DR	SOIC	D	14	2500	853.0	449.0	35.0
NE556NSR	SO	NS	14	2000	853.0	449.0	35.0

TUBE


*All dimensions are nominal

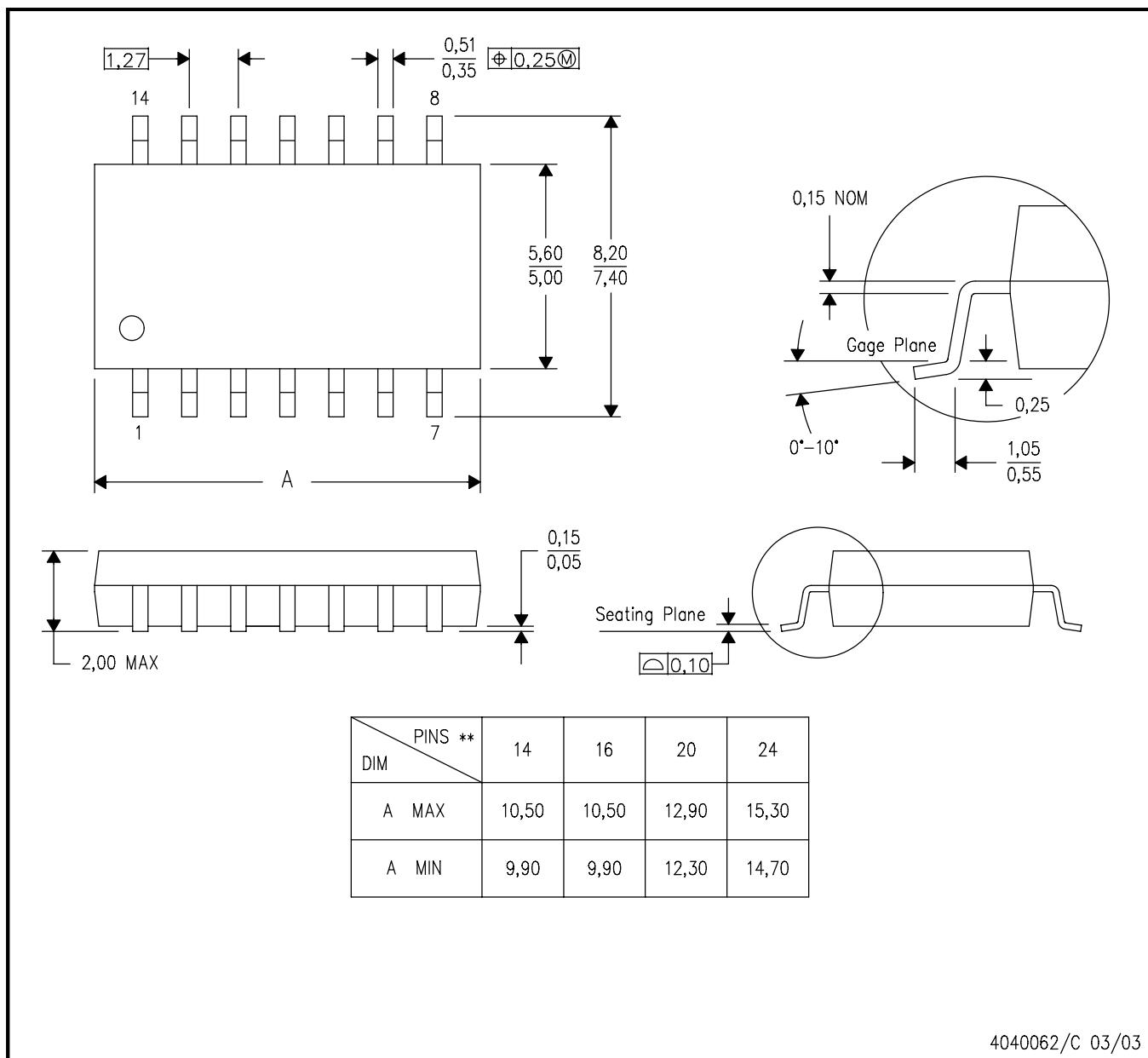
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
NA556D	D	SOIC	14	50	506.6	8	3940	4.32
NA556N	N	PDIP	14	25	506	13.97	11230	4.32
NA556N	N	PDIP	14	25	506	13.97	11230	4.32
NE556D	D	SOIC	14	50	506.6	8	3940	4.32
NE556N	N	PDIP	14	25	506	13.97	11230	4.32
NE556N	N	PDIP	14	25	506	13.97	11230	4.32
NE556NE4	N	PDIP	14	25	506	13.97	11230	4.32
NE556NE4	N	PDIP	14	25	506	13.97	11230	4.32
SA556N	N	PDIP	14	25	506	13.97	11230	4.32
SA556NE4	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

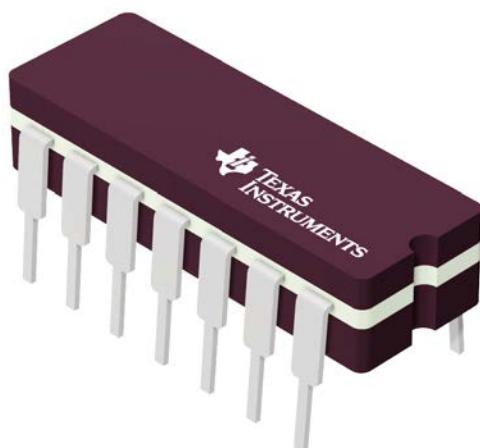
NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

J 14

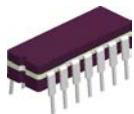
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

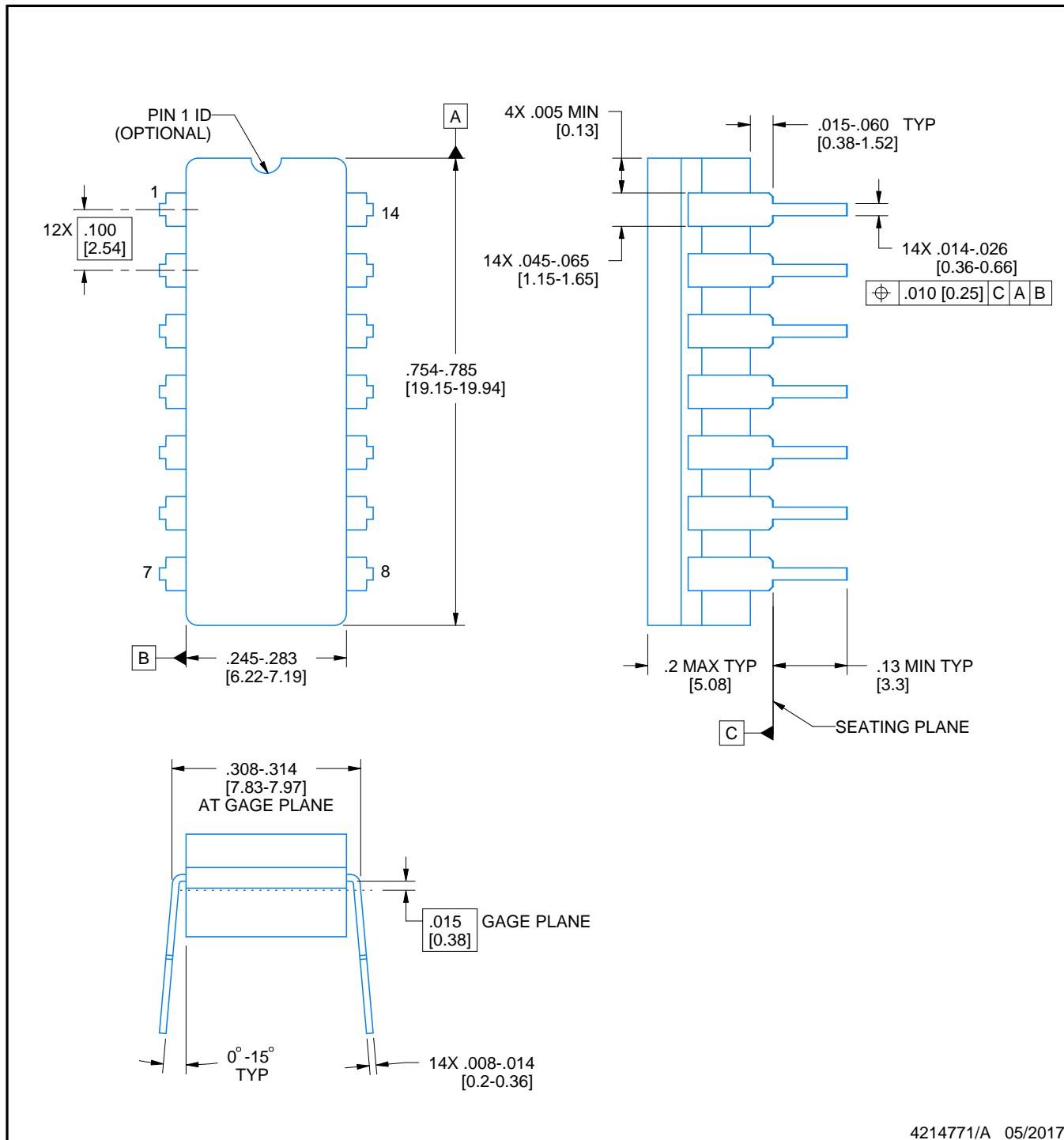


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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NOTES:

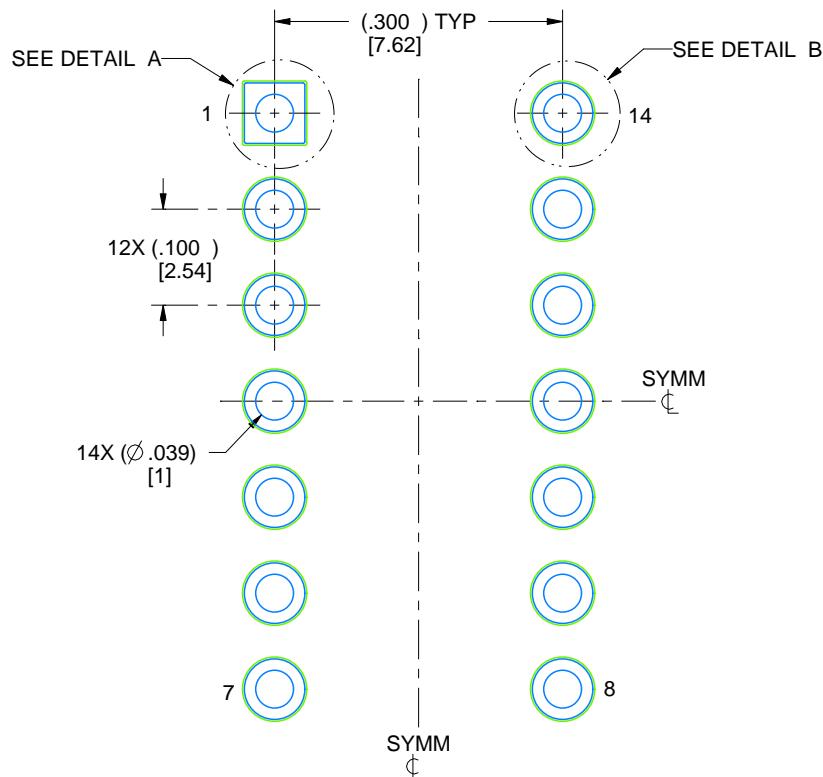
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

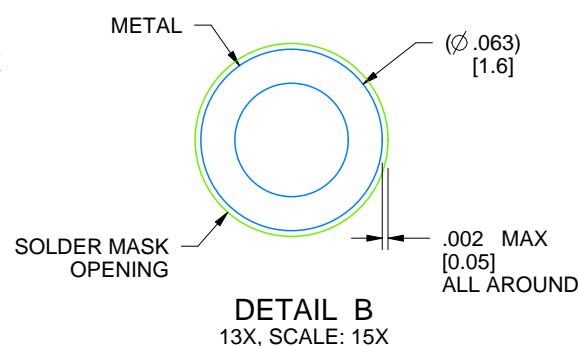
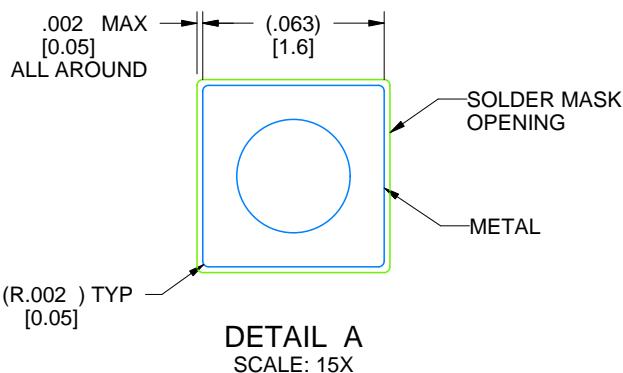
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



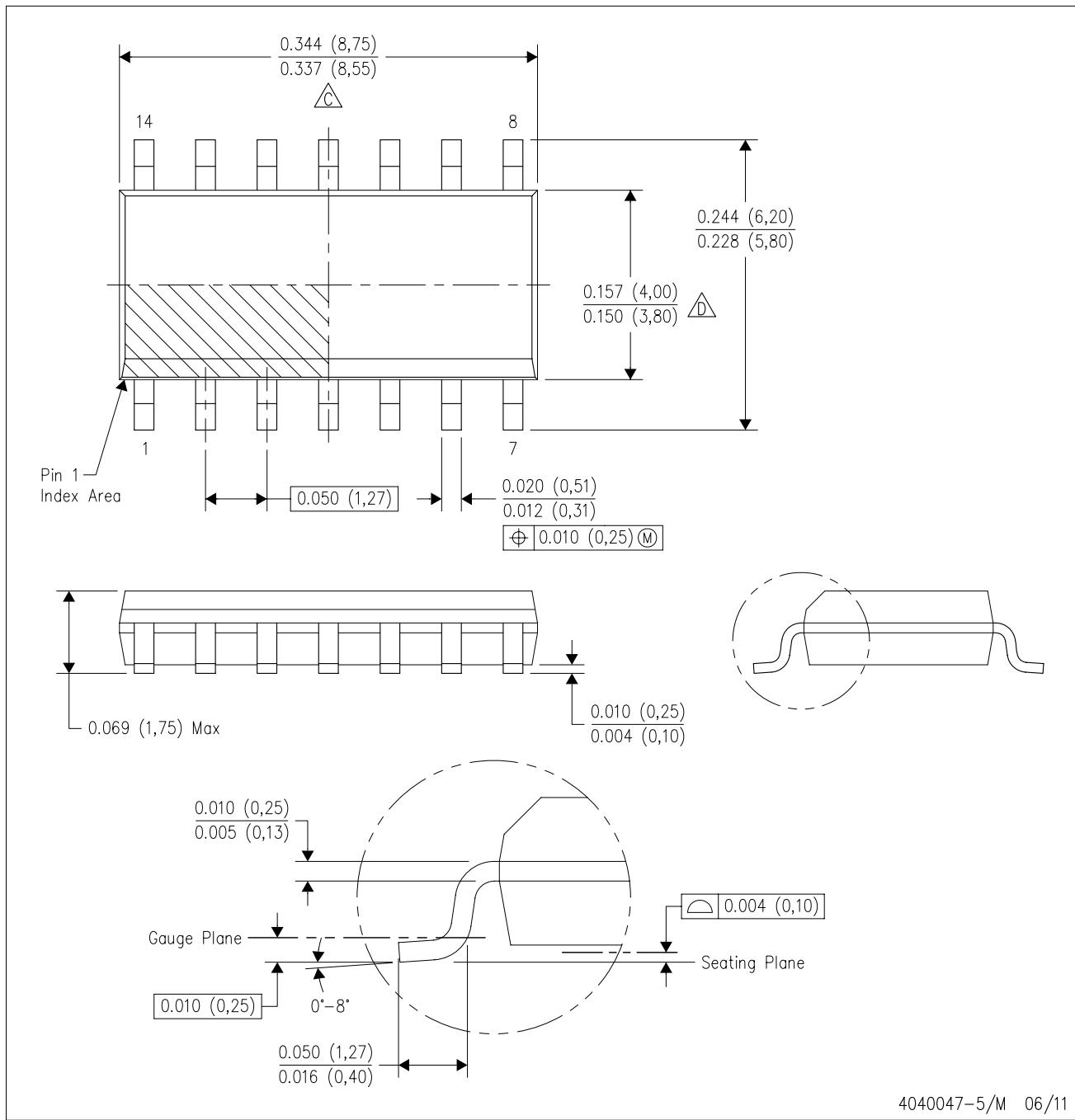
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

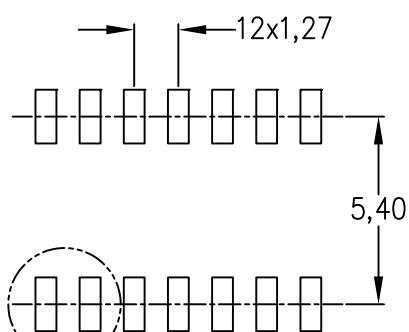
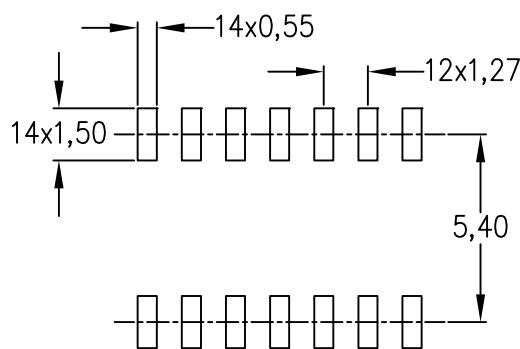
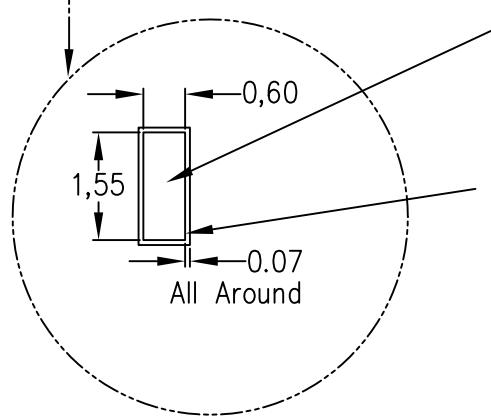
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-3/E 08/12

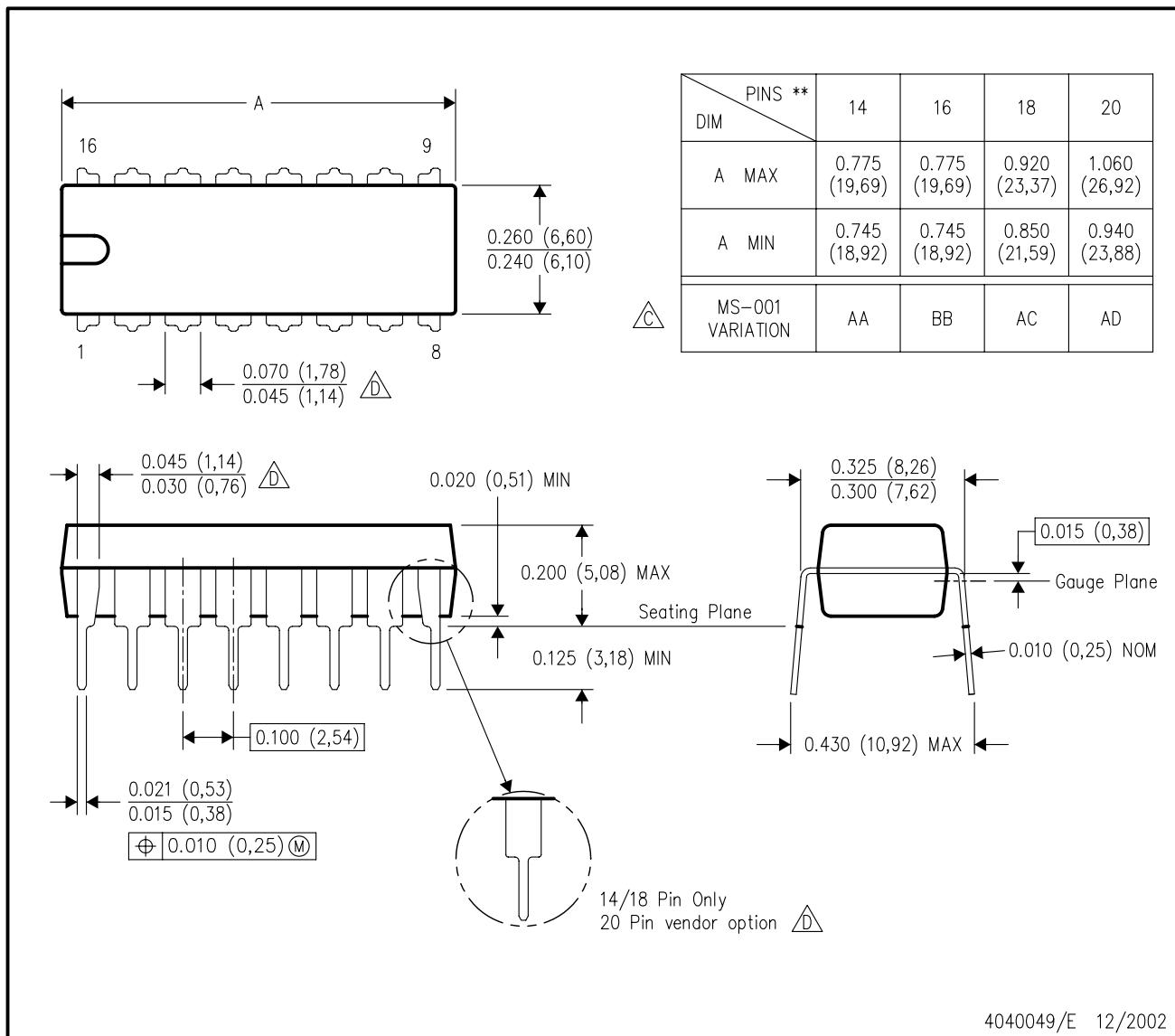
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

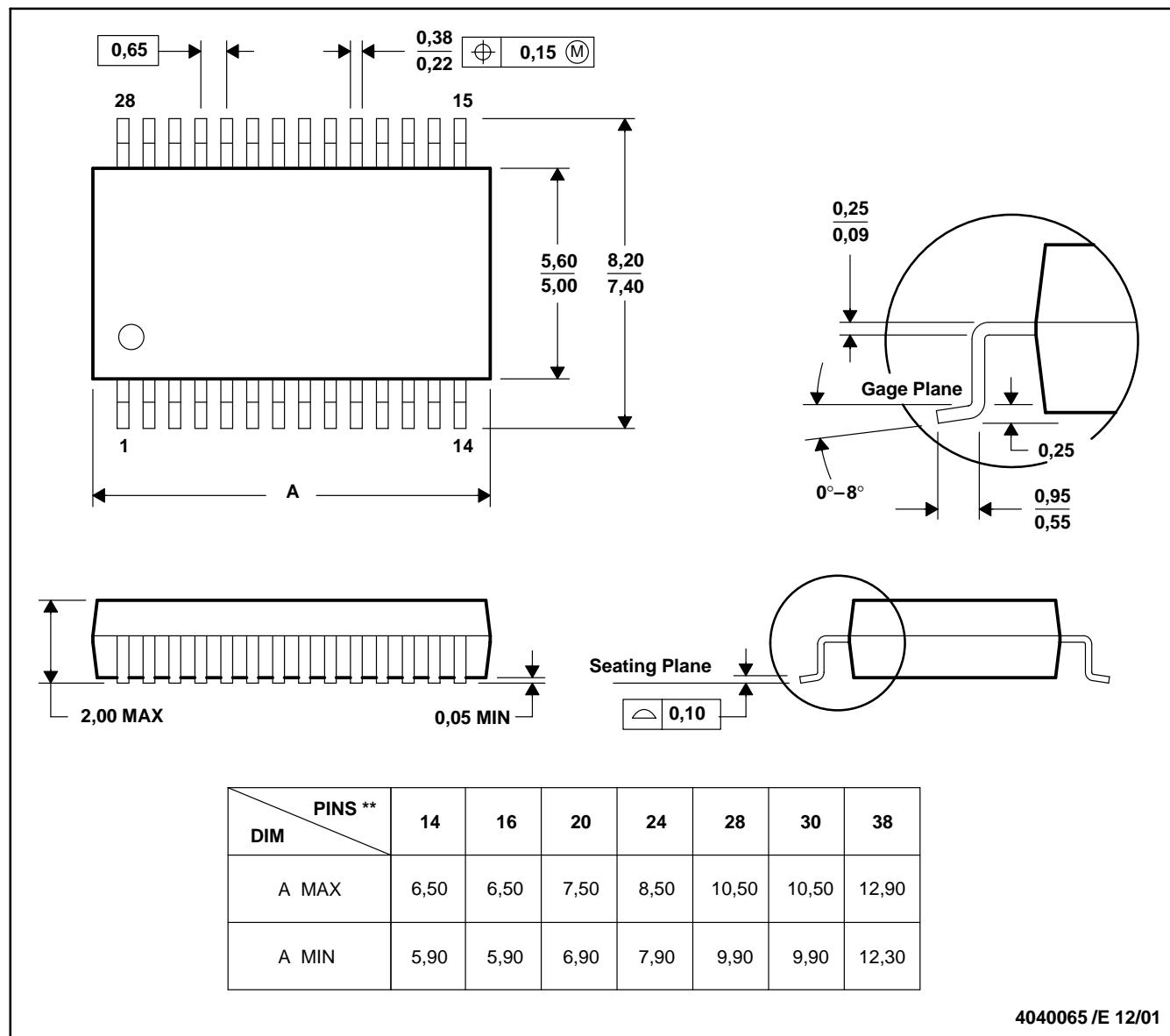
△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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