高速，三路数字隔离器

查询样品: ISO7230C-Q1, ISO7231C-Q1

特性

- 符合汽车应用要求
- **25** 和 **150-Mbps** 信号传输速率选项
  - 通道到通道低输出偏移
  - 低脉宽失真 **(PWD)**
  - 低抖动（在速率为 **150Mbps** 时为 **1ns**）（典型值）
- 在额定工作电压下使用寿命通常为 **25** 年（请参阅应用注释 **SLLA197** 和 **Figure 14**）
- **4000-$V_{峰值电压}$**隔离**, 560-$V_{峰值}$ V_{IORM}**
  - 符合 **UL 1577**、**IEC 60747-5-2 (VDE 0884, Rev 2)**、**IE 61010-1** 和 **CSA**
- **4kV ESD** 保护
- 使用 **3.3V** 或 **5V** 的电源
- 高电磁抗扰度 **(**请参阅应用注释 **SLLA181)**
- **-40°C** 至 **125°C** 工作温度范围

说明

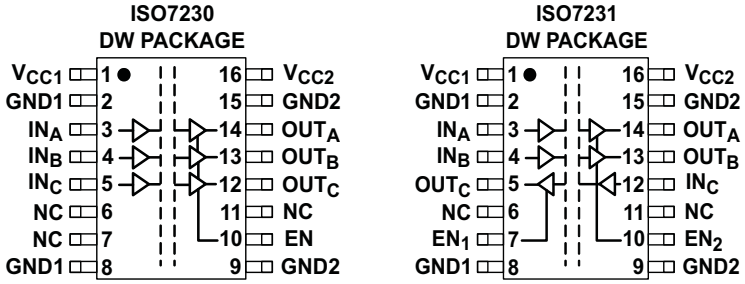
ISO7230C-Q1 和 ISO7231C-Q1 是三通道数字隔离器，每个隔离器具有多通道配置和输出允许功能。 这些器件具有逻辑输入和输出缓冲器，TI的二氧化硅 (SiO_2) 隔离栏栅将这这两类缓冲器分开。 当与隔离电源配合使用时，这些器件可以阻止高电压、隔离接地以及防止数据总线或者其它电路上的噪声电流进入本地接地和干扰或损害敏感的电路。

ISO7230C-Q1 三通道器件的所有三通道都在同一方向而 ISO7231C-Q1 有两个通道在一个方向，另外一个通道在反方向。 这些器件有一个高电平有效输出开启，当驱动到低电平时，将输出置于一个高阻抗状态。

ISO7230C-Q1 和 ISO7231C-Q1 设有 TTL 输入阀值和一个输入端的噪音过滤器，这能够防止持续时间高达 2 ns的瞬态脉冲被传递给设备的输出端。

在每个器件中，周期性更新脉冲也会通过隔离栏栅发送，以确保输出正确的 DC 电平。 如果没有接收到这个DC刷新脉冲，则这个输入就被假定为没被供电或者没有被正常驱动, 故障自保电路将输出驱动至一个逻辑高电平状态。(如需低故障自保选项请与 TI取得联系)。

这个设备要求 3.3 V, 5 V两个供电电压,或者任一组合。 当采用一个 3.3V 电源来供电并且所有的输出都是4-mA CMOS时，所有的输入为 5V 允差。 这些器件额定工作环境温度范围为 –40°C 至 125°C。



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM

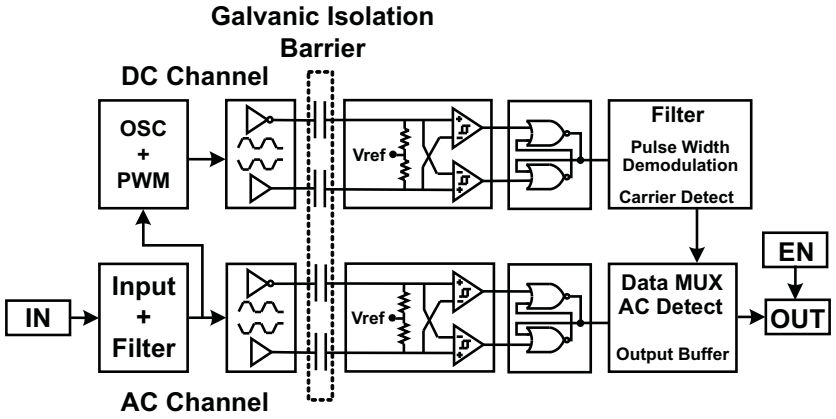

Table 1. Device Function Table ISO723xC-Q1 (1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC - DW	Reel of 2000	ISO7230CQDWRQ1	PREVIEW
			ISO7231CQDWRQ1	ISO7231CQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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ABSOLUTE MAXIMUM RATINGS(1)

				VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}			–0.5 to 6	V
V_I	Voltage at IN, OUT, EN			–0.5 to 6	V
I_O	Output current			±15	mA
ESD	Electrostatic discharge	Human Body Model	All pins	±4	kV
		Field-Induced-Charged Device Model		±1	
		Machine Model		±200	V
T_J	Maximum junction temperature			150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	3.15		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
t_{ui}	Input pulse width	40			ns
$1/t_{ui}$	Signaling rate	0	30(2)	25	Mbps
V_{IH}	High-level input voltage (IN) (EN on all devices)	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)	0		0.8	
T_A	Operating free-air temperature	-40		125	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
(2) Typical sigalling rate under ideal conditions at 25°C.

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ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA
		25 Mbps			7	9.5	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
		25 Mbps			11	17	
I_{CC2}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA
		25 Mbps			17	24	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		25 Mbps			17.5	27	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	18		45	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				5	
$t_{sk(pp)}$	Part-to-part skew (2)				8	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0	4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			1	3	mA
		25 Mbps				7	9.5	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
		25 Mbps				11	17	
I_{CC2}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			9	15	mA
		25 Mbps				10	17	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			8	12	mA
		25 Mbps				10.5	16	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	ISO7230C-Q1	V_{CC} – 0.4			V
				ISO7231C-Q1 (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1				0.4	V
			I_{OL} = 20 µA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	See Figure 1	20		50	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				4	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0	4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			0.5	1	mA
		25 Mbps				3	5	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			4.5	7	mA
		25 Mbps				6.5	11	
I_{CC2}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			15	22	mA
		25 Mbps				17	24	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			13	20	mA
		25 Mbps				17.5	27	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	ISO7230C-Q1	V_{CC} – 0.4			V
				ISO7231C-Q1 (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20 µA, See Figure 1		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1				0.4	V
			I_{OL} = 20 µA, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V and V_{CC2} at 5-V OPERATION

, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	20		51	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				4	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)			0	4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		µs

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

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ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V(1) OPERATION

, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_2 at 3 V		0.5	1	mA
		25 Mbps			3	5	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		4.5	7	mA
		25 Mbps			6.5	11	
I_{CC2}	ISO7230C-Q1	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_2 at 3 V		9	15	mA
		25 Mbps			10	17	
	ISO7231C-Q1	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	12	mA
		25 Mbps			10.5	16	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 4	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

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SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See Figure 1	25		56	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				4	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew			0	4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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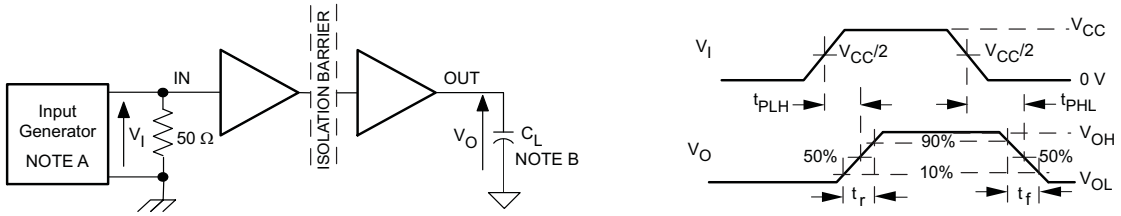
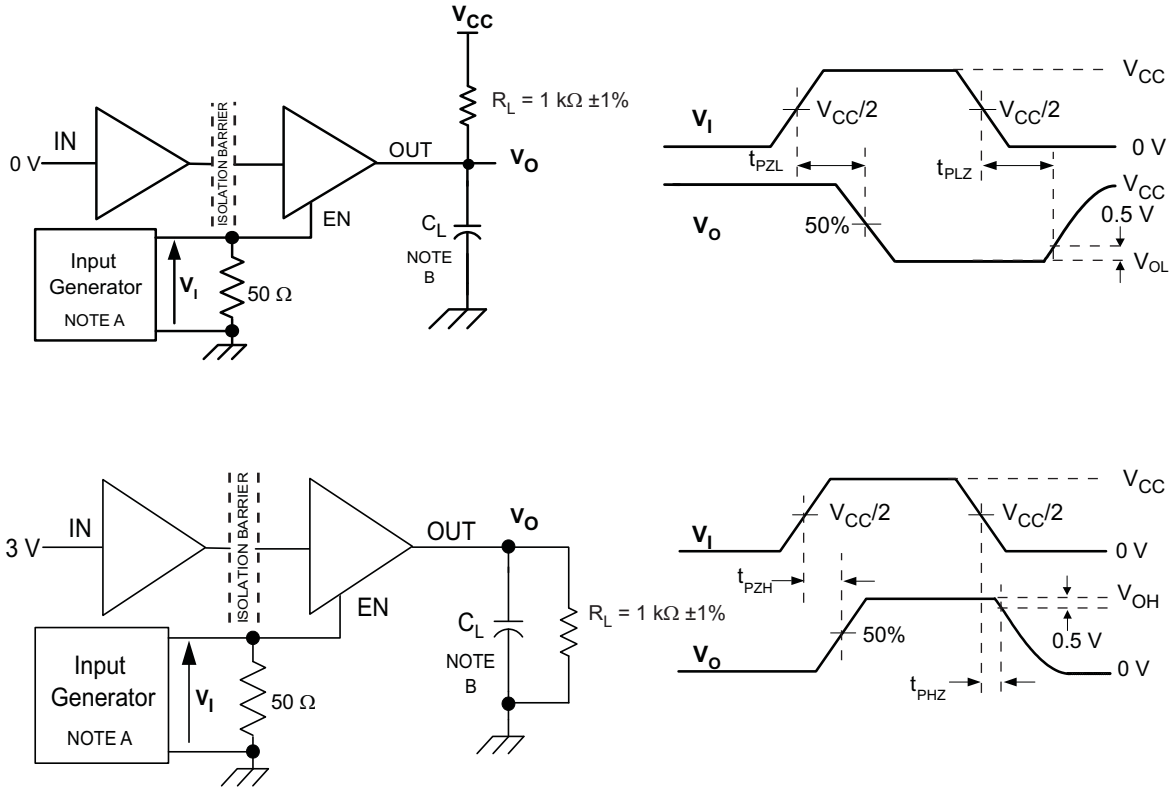
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

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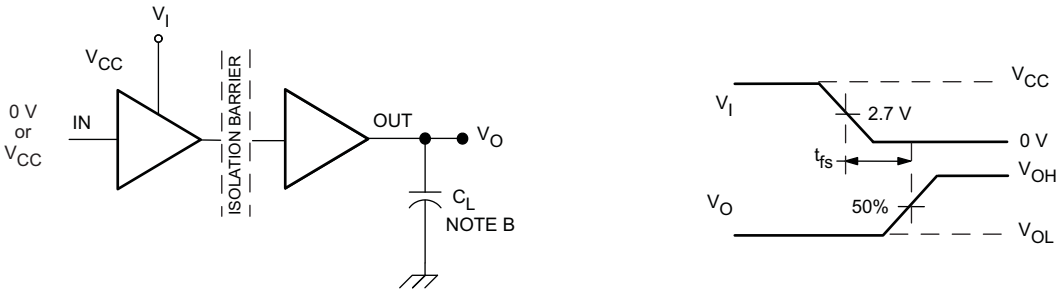
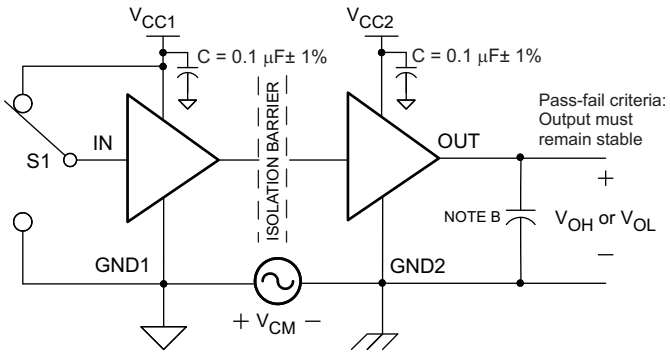
PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

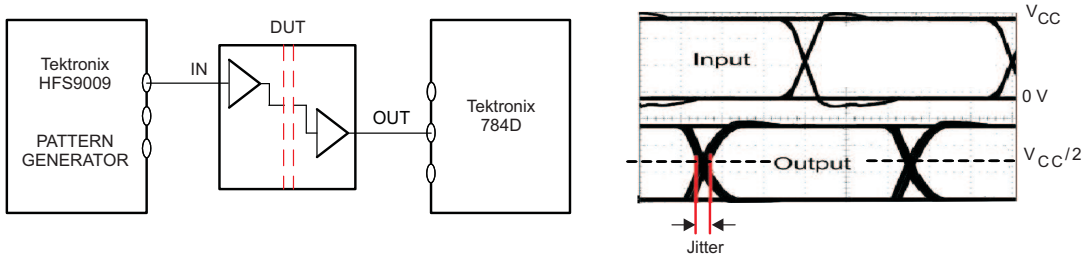
Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 5. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

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DEVICE INFORMATION

PACKAGE CHARACTERISTICS

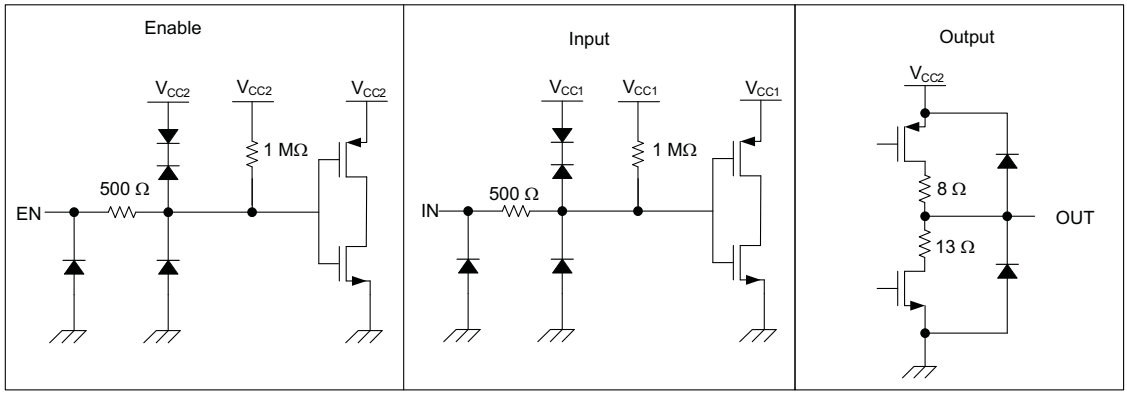
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		2		pF

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File Number: 40016131	File Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS



NOTE: Input is assumed to be on V_{CC1} side and Output on V_{CC2} side.

THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		168		°C/W
		High-K Thermal Resistance		96.1		
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P_D	Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

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TYPICAL CHARACTERISTIC CURVES

ISO7230 C/M RMS SUPPLY CURRENT vs SIGNALING RATE

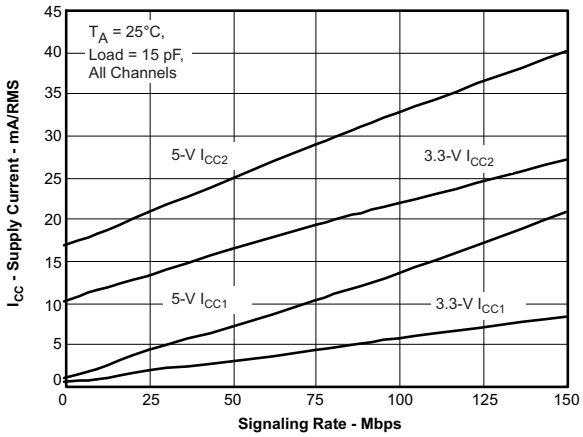

Figure 6.

ISO7231 C/M RMS SUPPLY CURRENT vs SIGNALING RATE

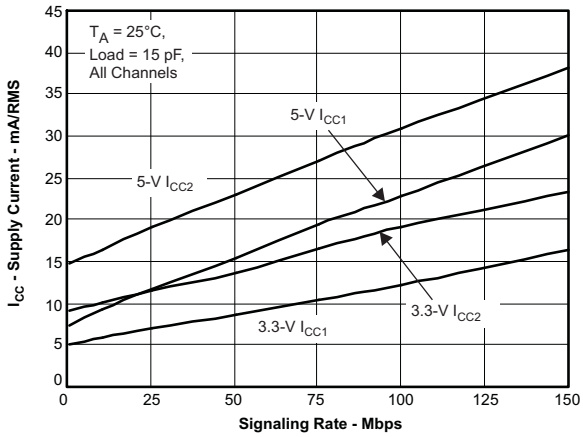

Figure 7.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE

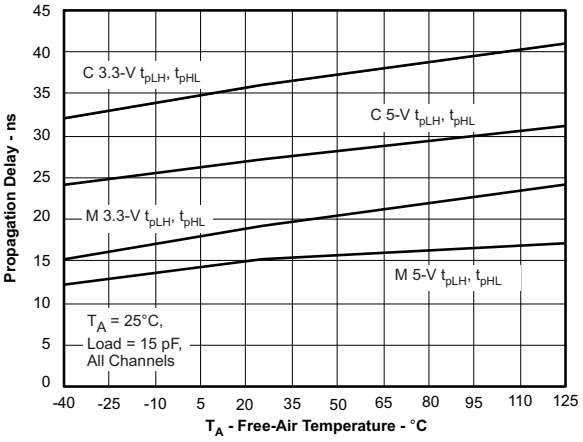

Figure 8.

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

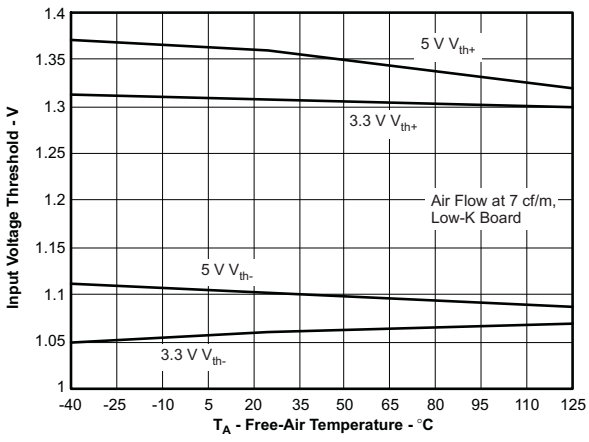

Figure 9.

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TYPICAL CHARACTERISTIC CURVES (continued)

V_{CC1} FAILSAFE THRESHOLD VS FREE-AIR TEMPERATURE

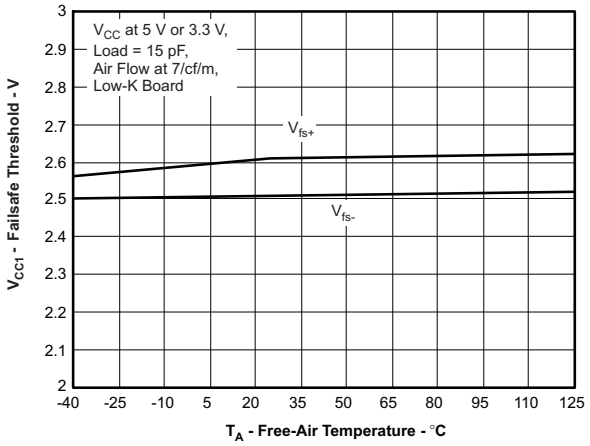

Figure 10.

HIGH-LEVEL OUTPUT CURRENT VS HIGH-LEVEL OUTPUT VOLTAGE

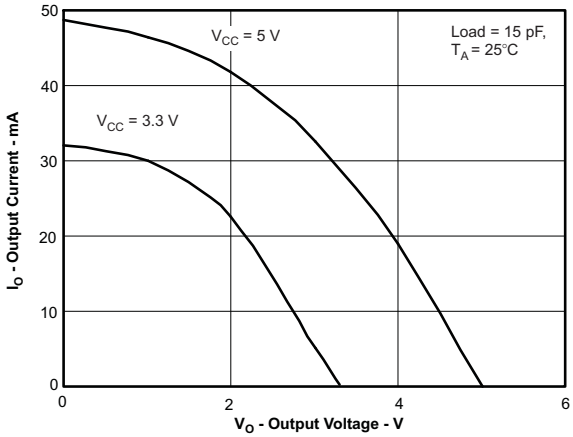

Figure 11.

LOW-LEVEL OUTPUT CURRENT VS LOW-LEVEL OUTPUT VOLTAGE

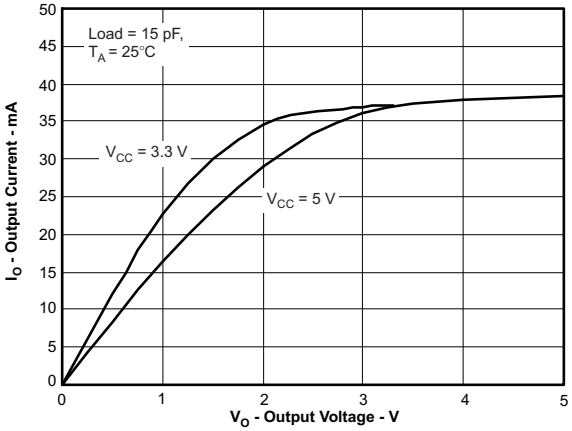

Figure 12.

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APPLICATION INFORMATION

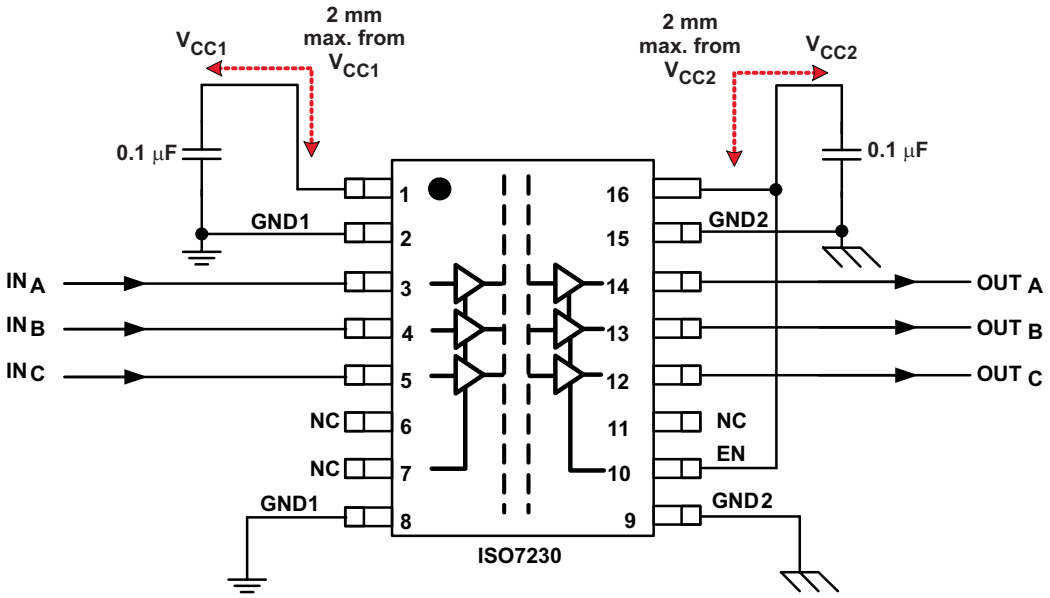

Figure 13. Typical ISO7230 Application Circuit

LIFE EXPECTANCY vs WORKING VOLTAGE

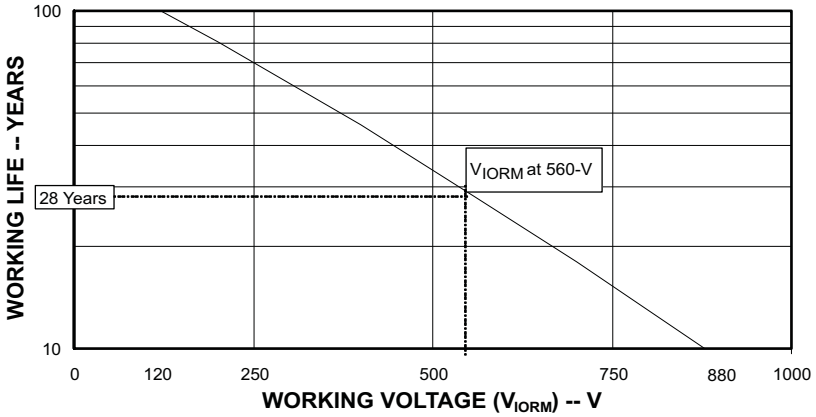

Figure 14. Time Dependant Dielectric Breakdown Testing Results

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7231CQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7231CQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

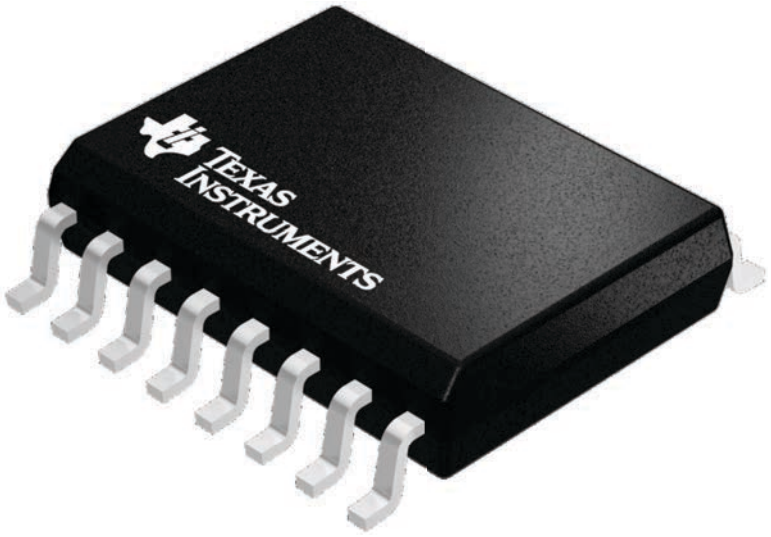
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

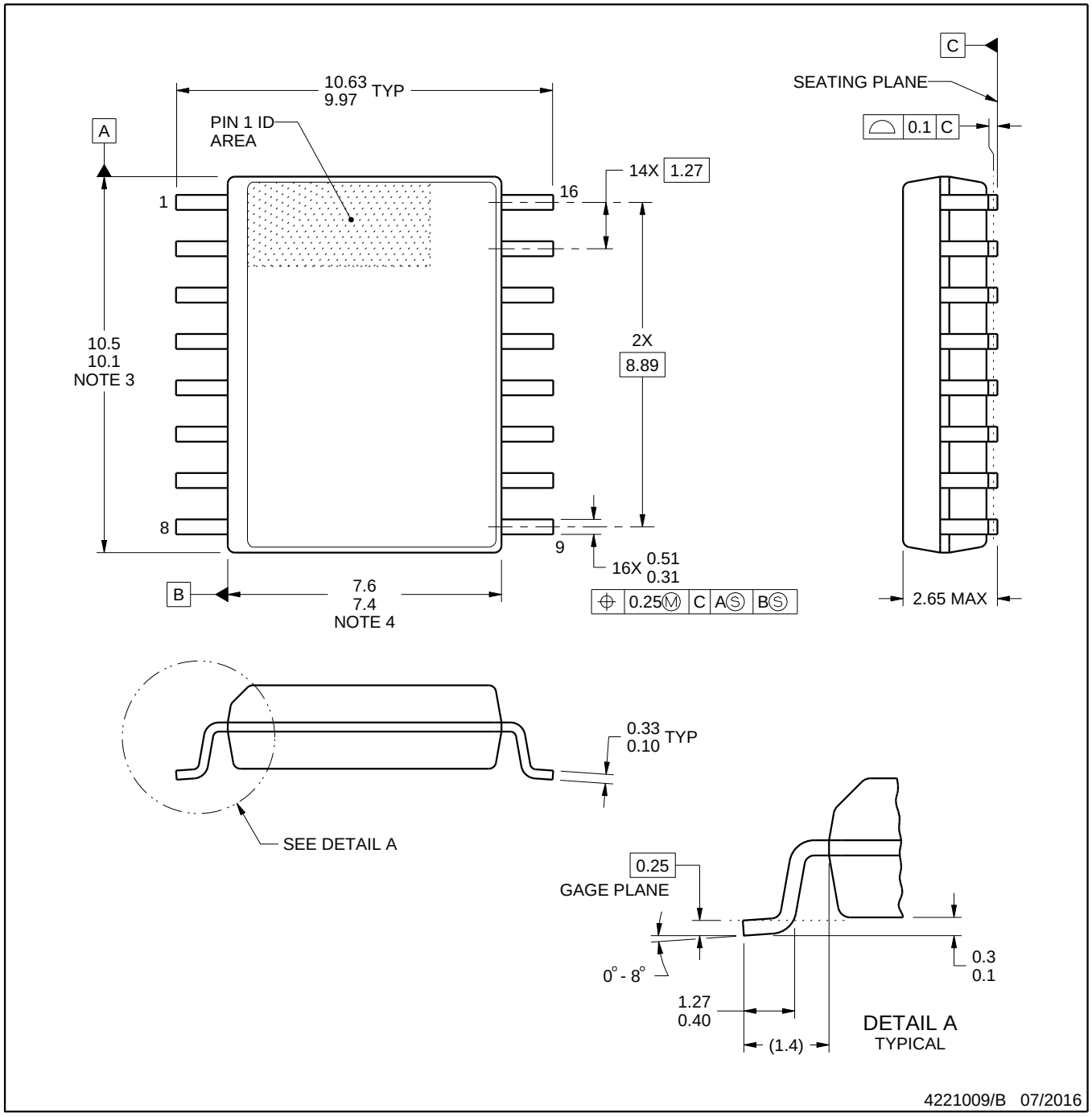
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



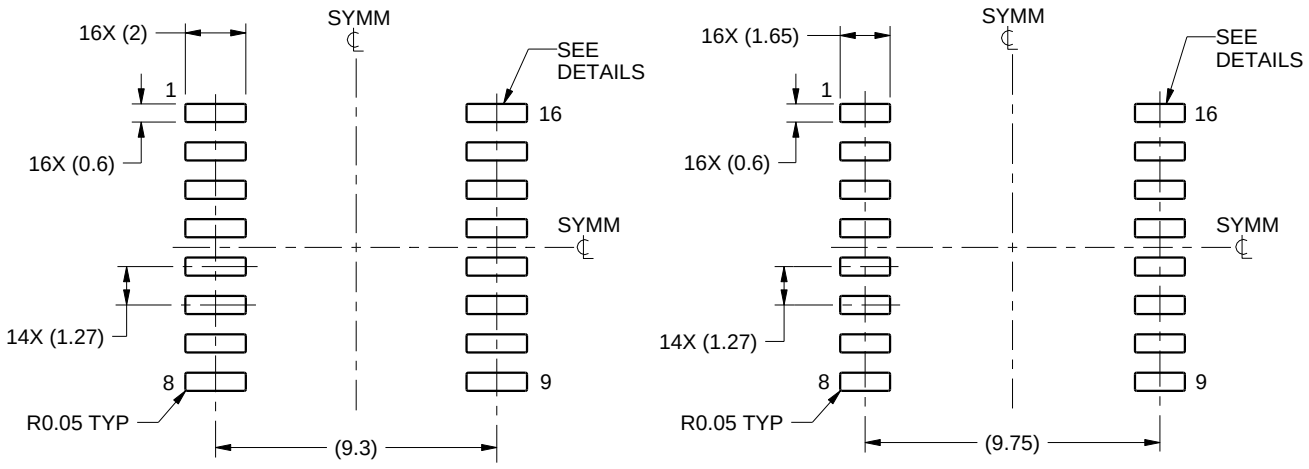
4224780/A

SOIC



NOTES:

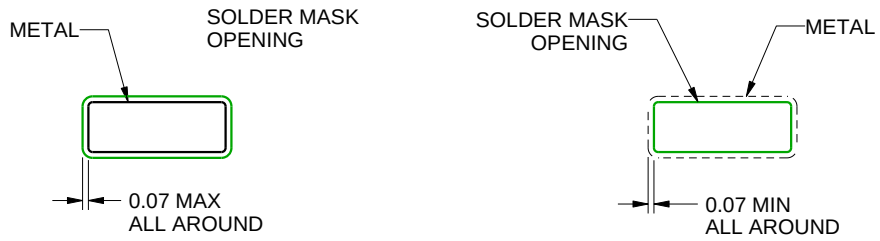
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

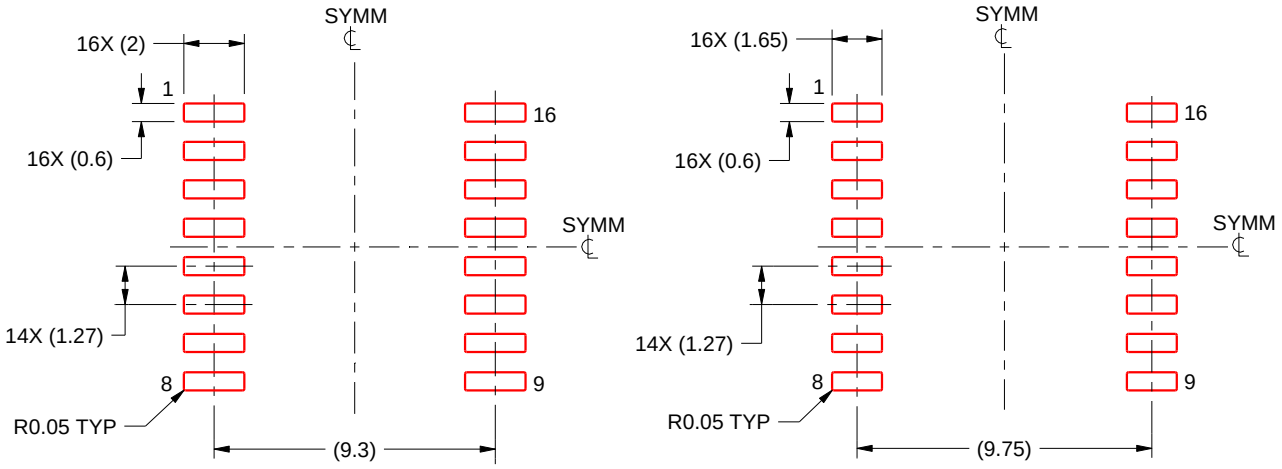
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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