

CDCDB803 适用于第 1 代到第 5 代 PCIe、符合 DB800ZL 标准的 8 输出时钟缓冲器

1 特性

- 具有可编程集成 85Ω (默认值) 或 100Ω 差分输出终端的 8 个 LP-HCSL 输出
- 8 硬件输出使能端 (OE#) 控制装置
- 使用第 5 代 PCIE 滤波器之后的附加相位抖动 : < 25fs RMS (最大值)
- 使用 DB2000Q 滤波器之后的附加相位抖动 : < 38fs RMS (最大值)
- 支持 PCIe 第 4 代和第 5 代常见时钟 (CC) 频率和单独基准 (IR) 架构
 - 与扩频兼容
- 输出到输出偏斜 : < 50ps
- 输入到输出延迟 : < 3ns
- 失效防护输入
- 可编程输出转换率控制
- 9 个可选 SMBus 地址
- 3.3V 内核和 IO 电源电压
- 硬件控制的低功耗模式 (PD#)
- 电流消耗 : 72mA (最大值)
- 6mm × 6mm 48 引脚 VQFN 封装

2 应用

- [微服务器和塔式服务器](#)
- [存储区域网络和主机总线适配器卡](#)
- [网络连接存储](#)
- [硬件加速器](#)
- [机架式服务器](#)

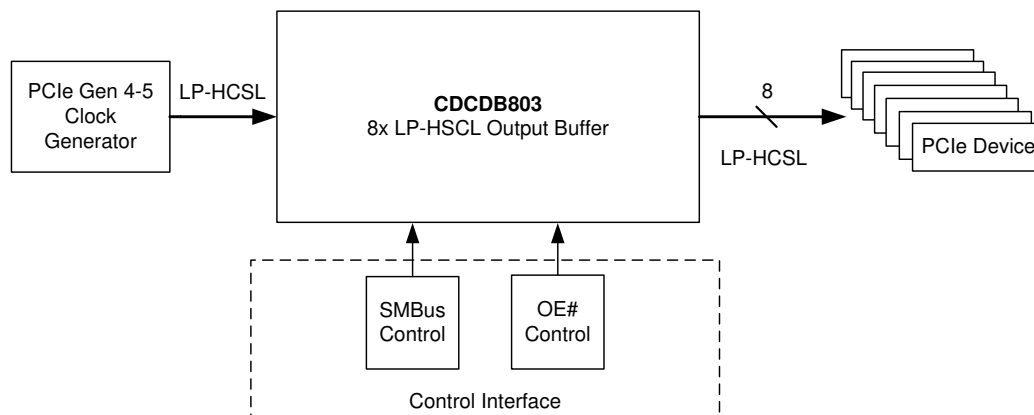
3 说明

CDCDB803 是一款符合 DB800ZL 标准的 8 路输出 LP-HCSL 时钟缓冲器，能够为第 1 代到第 5 代 PCIe、QuickPath Interconnect (QPI)、UPI、SAS 和 SATA 接口分配基准时钟。使用 SMBus 接口和 8 输出使能引脚，可以单独配置和控制所有 8 个输出。CDCDB803 是一款 DB800ZL 衍生缓冲器，符合或超过 DB800ZL 中的系统参数规格。它还符合或超过了 DB2000Q 的参数规格。CDCDB803 采用 6mm × 6mm 48 引脚 VQFN 封装。

器件信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 (标称值) |
|----------|-------------------|-----------------|
| CDCDB803 | VQFN (48) | 6.00mm × 6.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



CDCDB803 系统图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| DATE | REVISION | NOTES |
|-------------|----------|-----------------|
| August 2021 | * | Initial Release |

5 Pin Configuration and Functions

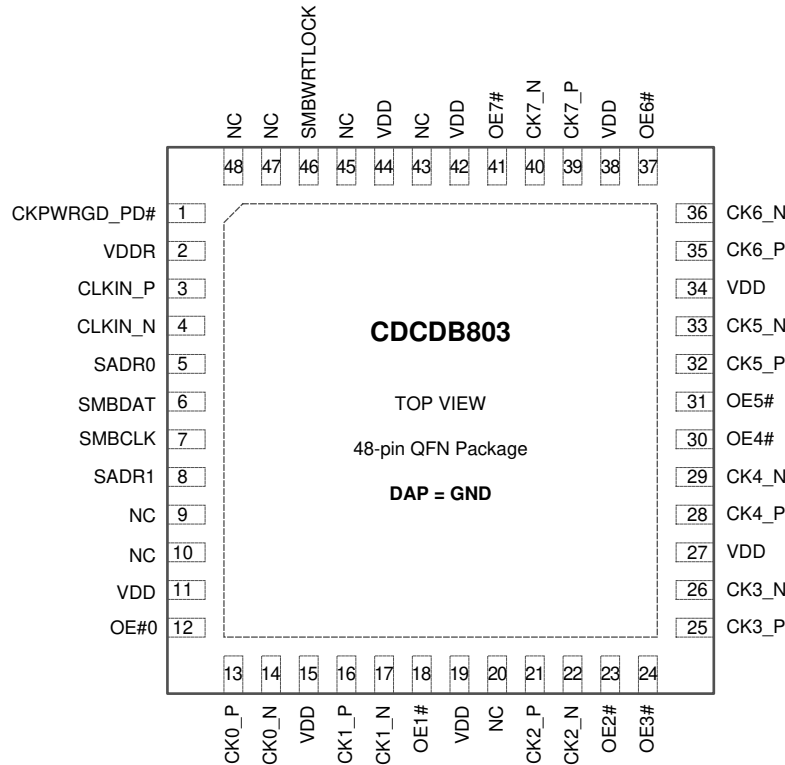


图 5-1. CDCDB803 RSL Package 48-Pin VQFN Top View

表 5-1. Pin Functions

| PIN | | I/O TYPE ⁽²⁾ | DESCRIPTION |
|----------------------|-----|-------------------------|--|
| NAME | NO. | | |
| INPUT CLOCK | | | |
| CLKIN_P | 3 | I | LP-HCSL differential clock input. Typically connected directly to the differential output of clock source. |
| CLKIN_N | 4 | I | |
| OUTPUT CLOCKS | | | |
| CK0_P | 13 | O | LP-HCSL differential clock output of channel 0. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK0_N | 14 | O | |
| CK1_P | 16 | O | LP-HCSL differential clock output of channel 1. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK1_N | 17 | O | |
| CK2_P | 21 | O | LP-HCSL differential clock output of channel 2. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK2_N | 22 | O | |
| CK3_P | 25 | O | LP-HCSL differential clock output of channel 3. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK3_N | 26 | O | |
| CK4_P | 28 | O | LP-HCSL differential clock output of channel 4. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK4_N | 29 | O | |
| CK5_P | 32 | O | LP-HCSL differential clock output of channel 5. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK5_N | 33 | O | |
| CK6_P | 35 | O | LP-HCSL differential clock output of channel 6. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK6_N | 36 | O | |
| CK7_P | 39 | O | LP-HCSL differential clock output of channel 7. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect. |
| CK7_N | 40 | O | |

表 5-1. Pin Functions (continued)

| PIN | | I/O TYPE ⁽²⁾ | DESCRIPTION |
|--|-----|-------------------------|--|
| NAME | NO. | | |
| MANAGEMENT AND CONTROL ⁽¹⁾ | | | |
| CKPWRGD_PD# | 1 | I, S, PD | Clock Power Good and Power Down multi-function input pin with internal 180-kΩ pulldown. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. After PWRGD has been asserted high for the first time, the pin becomes a PD# pin and it controls power-down mode: LOW: Power-down mode, all output channels tri-stated. HIGH: Normal operation mode. |
| OE0# | 12 | I, S, PD | Output Enable for channel 0 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 0. HIGH: disable output channel 0. |
| OE1# | 18 | I, S, PD | Output Enable for channel 1 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 1. HIGH: disable output channel 1. |
| OE2# | 23 | I, S, PD | Output Enable for channel 2 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 2. HIGH: disable output channel 2. |
| OE3# | 24 | I, S, PD | Output Enable for channel 3, with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 3. HIGH: disable output channel 3. |
| OE4# | 30 | I, S, PD | Output Enable for channel 4, with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 4. HIGH: disable output channel 4. |
| OE5# | 31 | I, S, PD | Output Enable for channel 5, with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 5. HIGH: disable output channel 5. |
| OE6# | 37 | I, S, PD | Output Enable for channel 6 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 6. HIGH: disable output channel 6. |
| OE7# | 41 | I, S, PD | Output Enable for channel 7 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 7. HIGH: disable output channel 7. |
| SMBUS AND SMBUS ADDRESS | | | |
| SADR0 | 5 | I, S, PU / PD | SMBus address strap bit[0]. This is a 3-level input that is decoded in conjunction with pin 8 to set SMBus address. It has internal 120-kΩ pullup / pulldown network biasing to VDD/2 when no connect. For a high-level input configuration, the pin should be pulled up to 3.3-V VDD through an external pullup resistor from 1k to 5k with 5% tolerance. For a low-level input configuration input, the pin should be pulled down to ground through an external pulldown resistor from 1k to 5k with 5% tolerance. For a mid-level input configuration, the pin should be left floating and not connected to VDD or ground. |
| SMBDAT | 6 | I / O | Data pin of SMBus interface. Typically pulled up to 3.3-V VDD using external pullup resistor. The recommended pullup resistor value is > 8.5k. |
| SMBCLK | 7 | I | Clock pin of SMBus interface. Typically pulled up to 3.3-V VDD using external pullup resistor. The recommended pullup resistor value is > 8.5k. |

表 5-1. Pin Functions (continued)

| PIN | | I/O TYPE ⁽²⁾ | DESCRIPTION |
|----------------------------------|-----------------------------------|-------------------------|---|
| NAME | NO. | | |
| SADR1 | 8 | I, S, PU / PD | SMBus address strap bit[1]. This is a 3-level input that is decoded in conjunction with pin B4 to set SMBus address. It has internal 120-kΩ pullup / pulldown network biasing to VDD/2 when no connect. For a high-level input configuration, the pin should be pulled up to 3.3-V VDD through an external pullup resistor from 1k to 5k with 5% tolerance. For a low-level input configuration, the pin should be pulled down to ground through an external pulldown resistor from 1k to 5k with 5% tolerance. For a mid-level input configuration, the pin should be left floating and not connected to VDD or ground. |
| SMBWRTLOCK | 46 | I, PD | SMBWRTLOCK: Disables write commands on SMBus. All writes will be ignored when SMBWRTLOCK is asserted (reads are not affected). Internal 180-kΩ pulldown, active low 0 = SMBus write enabled. 1 = SMBus write disabled. |
| SUPPLY VOLTAGE AND GROUND | | | |
| VDDR | 2 | P | Power supply input for input clock receiver. Connect to 3.3-V power supply rail with decoupling capacitor to GND. Place a 0.1-μF capacitor close to each supply pin between power supply and ground. |
| VDD | 11, 15, 19, 27, 34, 38, 42, 44 | P | 3.3-V power supply for output channels and core voltage. |
| GND | DAP | G | Ground. Connect ground pad to system ground. |
| NO CONNECT | | | |
| NC | 9, 10, 20, 43, 45, 47, 48 | — | Do not connect to GND or VDD. |

- (1) The “#” symbol at the end of a pin name indicates that the active state occurs when the signal is at a low voltage level. When “#” is not present, the signal is active high.
- (2) The definitions below define the I/O type for each pin.
- I = Input
 - O = Output
 - I / O = Input / Output
 - PU / PD = Internal 180-kΩ Pullup / Pulldown network biasing to VDD/2
 - PD = Internal 180-kΩ Pulldown
 - S = Hardware Configuration Pin
 - P = Power Supply
 - G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|----------------------|------|-----|------|
| V_{DD}, V_{DD_R} | Power supply voltage | -0.3 | 3.6 | V |
| V_{IN} | IO input voltage | -0.3 | 3.6 | V |
| T_J | Junction temperature | | 125 | °C |
| T_{stg} | Storage temperature | -65 | 150 | °C |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±3500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------|-------------------------|-----|-----|-----|------|
| V_{DD} | IO, Core supply voltage | 3 | 3.3 | 3.6 | V |
| V_{DD_R} | Input supply voltage | 3 | 3.3 | 3.6 | V |
| T_A | Ambient temperature | -40 | | 105 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | Device Package | | UNIT |
|-------------------------------|--|----------------|--|------|
| | | RSL (QFN) | | |
| | | 48 PINS | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 32.2 | | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 22.3 | | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 14.3 | | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 0.5 | | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 14.2 | | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 6.1 | | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

VDD, VDD_R = 3.3 V ± 5 %, -40 °C ≤ T_A ≤ 105 °C. Typical values are at VDD = VDD_R = 3.3 V, 25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|---|------|-----|----------------------------|-------------------------|
| CURRENT CONSUMPTION | | | | | | |
| I _{DD_R} | Core supply current | Active mode. CKPWRGD_PD# = 1 | | | 9 | mA |
| | | Power down mode. CKPWRGD_PD# = 0 | | | 2.2 | |
| I _{DD} | IO supply current | All outputs disabled | | | 18 | mA |
| | | All outputs active, 100MHz (Per output) | | | 7.8 | |
| | | Power down mode. CKPWRGD_PD# = 0 | | | 1.5 | |
| CLOCK INPUT | | | | | | |
| f _{IN} | Input frequency | | 50 | 100 | 250 | MHz |
| V _{IN} | Input voltage swing | Differential voltage between CLKIN_P and CLKIN_N ⁽¹⁾ | 200 | | 2300 | mV _{Diff-peak} |
| dV/dt | Input voltage edge rate | 20% - 80% of input swing | 0.7 | | | V/ns |
| DV _{CROSS} | Total variation of V _{CROSS} | Total variation across V _{CROSS} | | 140 | | mV |
| DC _{IN} | Input duty cycle | | 40 | | 60 | % |
| C _{IN} | Input capacitance ⁽²⁾ | Differential capacitance between CLKIN_P and CLKIN_N pins | | 2.2 | | pF |
| CLOCK OUTPUT | | | | | | |
| f _{OUT} | Output frequency | | 50 | 100 | 250 | MHz |
| C _{OUT} | Output capacitance ⁽¹⁾ | Differential capacitance between CKx_P and CKx_N pins | | 4 | | pF |
| V _{OH} | Output high voltage | Single-ended ^{(2) (3)} | 225 | | 270 | mV |
| V _{OL} | Output low voltage | | 10 | | 150 | |
| V _{HIGH} | Output high voltage | Measured into an AC load as defined in DB800ZL | 660 | | 850 | |
| V _{LOW} | Output low voltage | Measured into an AC load as defined in DB800ZL | -150 | | 150 | |
| V _{MAX} | Output Max voltage | Measured into an AC load as defined in DB800ZL | | | 1150 | |
| V _{CROSS} | Crossing point voltage | ^{(3) (4)} | 130 | | 200 | |
| V _{CROSSAC} | Crossing point voltage (AC load) | Measured into an AC load as defined in DB800ZL | 250 | | 550 | |
| DV _{CROSS} | Total variation of V _{CROSS} | Variation of V _{CROSS} ^{(3) (4)} | | 35 | 140 | |
| V _{ovs} | Overshoot voltage | ⁽³⁾ | | | V _{OH} +75 | |
| V _{ovs(AC)} | Overshoot voltage (AC load) | Measured into an AC load as defined in DB800ZL | | | V _{HIGH} +30 0 | |
| V _{uds} | Undershoot voltage | ⁽³⁾ | | | V _{OL} -75 | |
| V _{uds(AC)} | Undershoot voltage | Measured into an AC load as defined in DB800ZL | | | V _{LOW} - 300 | |
| V _{rb} | Ringback Voltage | Measured into an AC load as defined in DB800ZL and taken from Single Ended waveform (relative to V _{HIGH} and V _{LOW}) | -0.2 | | 0.2 | V |
| Z _{DIFF} | Differential impedance (Default setting, 85 Ω) | Measured at V _{OL} /V _{OH} | 81 | 85 | 89 | Ω |
| | Differential impedance (Output impedance selection bit = 1, 100 Ω) | Measured at V _{OL} /V _{OH} | 95 | 100 | 105 | |
| Z _{DIFF_CROSS} | Differential impedance (Default setting, 85 Ω) | Measured at V _{CROSS} | 68 | 85 | 102 | |
| | Differential impedance (Output impedance selection bit = 1, 100 Ω) | Measured at V _{CROSS} | 80 | 100 | 120 | |

VDD, VDD_R = 3.3 V ± 5 %, -40 °C ≤ T_A ≤ 105 °C. Typical values are at VDD = VDD_R = 3.3 V, 25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|--|--|--|------|------|-------|---------------|
| t _{EDGE} | Differential edge rate | Measured (+-150 mV) around V _{CROSS} ⁽⁷⁾ | | 2 | | 4 | V/ns |
| D _{tEDGE} | Edge rate matching | Measured (+-75 mV) V _{CROSS} ⁽⁷⁾ | | | | 20 | % |
| t _{STABLE} | Power good assertion to stable clock output | CKPWRGD_PD# pin transitions from 0 to 1, f _{IN} = 100 MHz | Measured when positive output reaches 0.2V | | | 1.8 | ms |
| t _{DRIVE_PD#} | Power good assertion to outputs driven high | CKPWRGD_PD# pin transitions from 0 to 1, f _{IN} = 100 MHz | Measured when positive output reaches 0.2V | | | 300 | µs |
| t _{OE} | Output enable assertion to stable clock output | OEx# pin transitions from 1 to 0 | | | | 10 | CLKIN Periods |
| t _{OD} | Output enable de-assertion to no clock output | OEx# pin transitions from 0 to 1 | | | | 10 | |
| t _{PD} | Power down assertion to no clock output | CKPWRGD_PD# pin transitions from 1 to 0 | | | | 3 | |
| t _{DCD} | Duty cycle distortion | Differential; f _{IN} = 100MHz, f _{IN_DC} = 50% | | -1 | | 1 | % |
| t _{DLY} | Propagation delay | ⁽⁵⁾ | | 0.5 | | 3 | ns |
| t _{SKEW} | Skew between outputs | ⁽⁶⁾ | | | | 50 | ps |
| t _{DELAY(IN-OUT)} | Input to output delay variation | Input-to-output delay variation at 100 MHz across voltage and temperature | | -250 | | 250 | ps |
| J _{CKX_DB2000Q} ⁽⁷⁾ | Additive jitter for DB2000Q | DB2000Q filter, for input of 200 mV differential swing @ 1.5 V/ns | | | | 0.038 | ps, RMS |
| J _{CKX_PCIE} ⁽⁷⁾ | Additive jitter for PCIe6.0 | PLL BW: 0.5 - 1 MHz; CDR = 10 MHz | Input clock slew rate = 2 V/ns | | | 0.02 | ps, RMS |
| | Additive jitter for PCIe5.0 | PCIe5.0 filter | | | | 0.025 | |
| | Additive jitter for PCIe4.0 | PLL BW = 2 - 5 MHz; CDR = 10 MHz | Input clock slew rate ≥ 1.8 V/ns | | | 0.06 | |
| | Additive jitter for PCIe3.0 | | Input clock slew rate ≥ 0.6 V/ns | | | 0.1 | |
| J _{CKX} | Additive jitter | f _{IN} = 100 MHz; slew rate ≥ 3 V/ns; 12 kHz to 20 MHz integration bandwidth. | | | 100 | 160 | fs, RMS |
| NF | Noise floor | f _{IN} = 100 MHz; f _{Offset} ≥ 10 MHz | Input clock slew rate ≥ 3 V/ns | | -160 | -155 | dBc/Hz |
| SMBUS INTERFACE, OEx#, CKPWRGD_PD# | | | | | | | |
| V _{IH} | High level input voltage | | | 2.0 | | | V |
| V _{IL} | Low level input voltage | | | | | 0.8 | |
| I _{IH} | Input leakage current | With internal pull-up/pull-down | GND ≤ V _{IN} ≤ V _{DD} | -30 | | 30 | µA |
| I _{IL} | Input leakage current | With internal pull-up/pull-down | GND ≤ V _{IN} ≤ V _{DD} | -30 | | 30 | µA |
| I _{IH} | Input leakage current | Without internal pull-up/pull-down | GND ≤ V _{IN} ≤ V _{DD} | -5 | | 5 | µA |
| I _{IL} | Input leakage current | Without internal pull-up/pull-down | GND ≤ V _{IN} ≤ V _{DD} | -5 | | 5 | µA |

VDD, VDD_R = 3.3 V ± 5 %, -40 °C ≤ T_A ≤ 105 °C. Typical values are at VDD = VDD_R = 3.3 V, 25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|----------------------------------|---------------------------------|-----------------------------------|------|--------------------|-------|------|
| C _{IN} | Input capacitance | | | | 4.5 | | pF |
| C _{OUT} | Output capacitance | | | | 4.5 | | pF |
| 3-LEVEL DIGITAL INTERFACE (SADR0, SADR1) | | | | | | | |
| V _{IH} | High level input voltage | | | 2.3 | | | V |
| V _{IM} | Mid level input voltage | | | 1.25 | V _{DD} /2 | 1.725 | |
| V _{IL} | Low level input voltage | | | | | 0.85 | |
| I _{IH} | Input leakage current | With internal pull-up/pull-down | V _{IN} = V _{DD} | -30 | | 30 | μA |
| I _{IL} | Input leakage current | With internal pull-up/pull-down | V _{IN} = GND | -30 | | 30 | μA |
| C _{IN} | Input capacitance ⁽¹⁾ | | | | 4.5 | | pF |

- (1) Voltage swing includes overshoot.
- (2) Not tested in production. Ensured by design and characterization.
- (3) Measured into DC test load.
- (4) V_{CROSS} is single-ended voltage when CKx_P = CKx_N with respect to system ground. Only valid on rising edge of CKx, when CKx_P is rising.
- (5) Measured from rising edge of CLK_IN to any CKx output.
- (6) Measured from rising edge of any CKx output to any other CKx output.
- (7) Measured into AC test load.

6.6 Timing Requirements

VDD, VDD_R = 3.3 V ± 5 %, -40 °C ≤ T_A ≤ 105 °C. Typical values are at VDD = VDD_A = 3.3 V, 25 °C (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|--|--|-----|------|--------|
| SMBUS-COMPATIBLE INTERFACE TIMING | | | | | |
| f _{SMB} | SMBus operating frequency | 10 | | 400 | kHz |
| t _{BUF} | Bus free time between STOP and START | 4.7 | | | μs |
| t _{HD_STA} | START condition hold time | 4 | | | |
| t _{SU_STA} | START condition setup time | 4.7 | | | |
| t _{SU_STO} | STOP condition setup time | 4 | | | |
| t _{HD_DAT} | SMBDAT hold time | 300 | | | ns |
| t _{SU_DAT} | SMBDAT setup time | 250 | | | |
| t _{TIMEOUT} | Detect SMBCLK low timeout | In terms of device input clock frequency | | | cycles |
| t _{LOW} | SMBCLK low period | 4.7 | | | μs |
| t _{HIGH} | SMBCLK high period | 4 | | 50 | |
| t _F | SMBCLK/SMBDAT fall time ⁽¹⁾ | | | 300 | ns |
| t _R | SMBCLK/SMBDAT rise time ⁽²⁾ | | | 1000 | |

- (1) T_F = (VIHMIN + 0.15) to (VILMAX - 0.15)
- (2) T_R = (VILMAX - 0.15) to (VIHMIN + 0.15)

6.7 Typical Characteristics

Figure 6-1 shows both the phase noise of the source as well as the output of the DUT (CDCDB803). It can be seen from the phase noise plot that the DUT has a very low phase noise profile with total jitter of 71 fs, rms. If we rms subtract the clock reference noise, the additive jitter of CDCDB803 under typical conditions would be lower than 71 fs, rms.

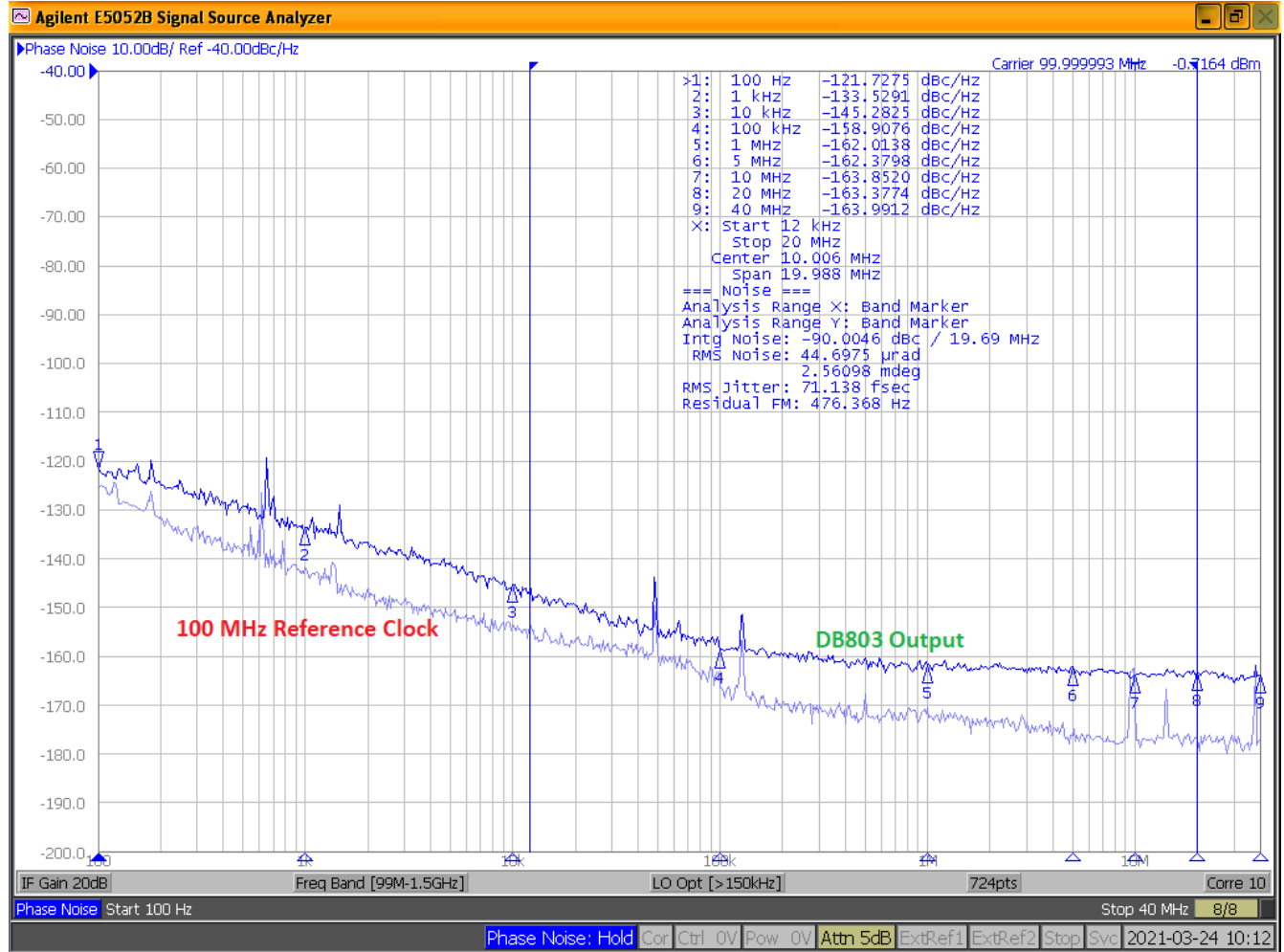


Figure 6-1. CDCDB803 Clock Out (CK0:8) Phase Noise

7 Parameter Measurement Information

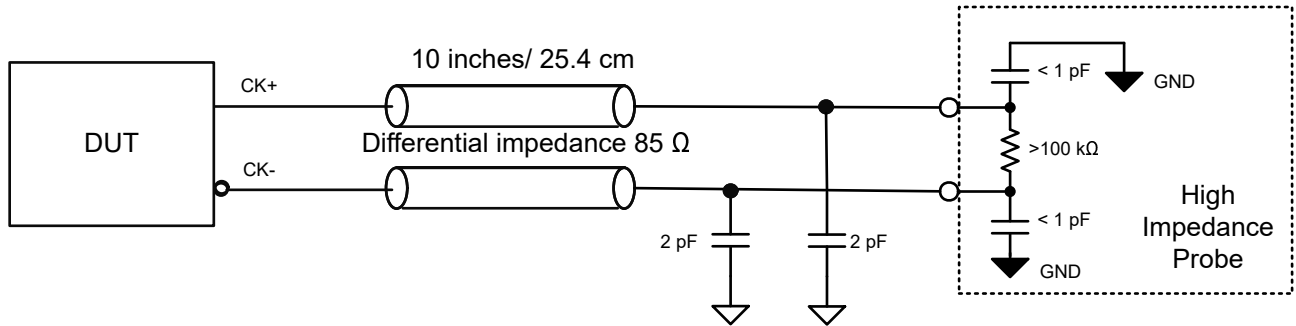
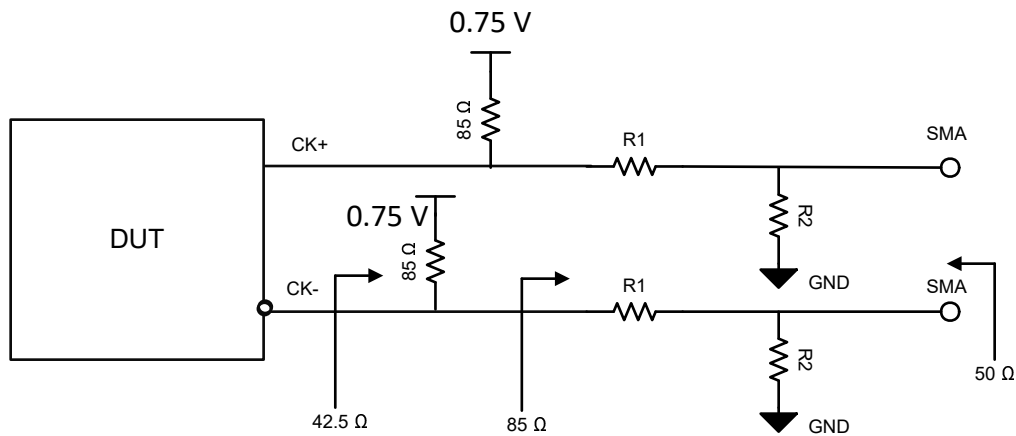


图 7-1. AC Test Load (Referencing Intel DB2000QL Document)



$R1 = 47\ \Omega$ and $R2 = 147\ \Omega$.

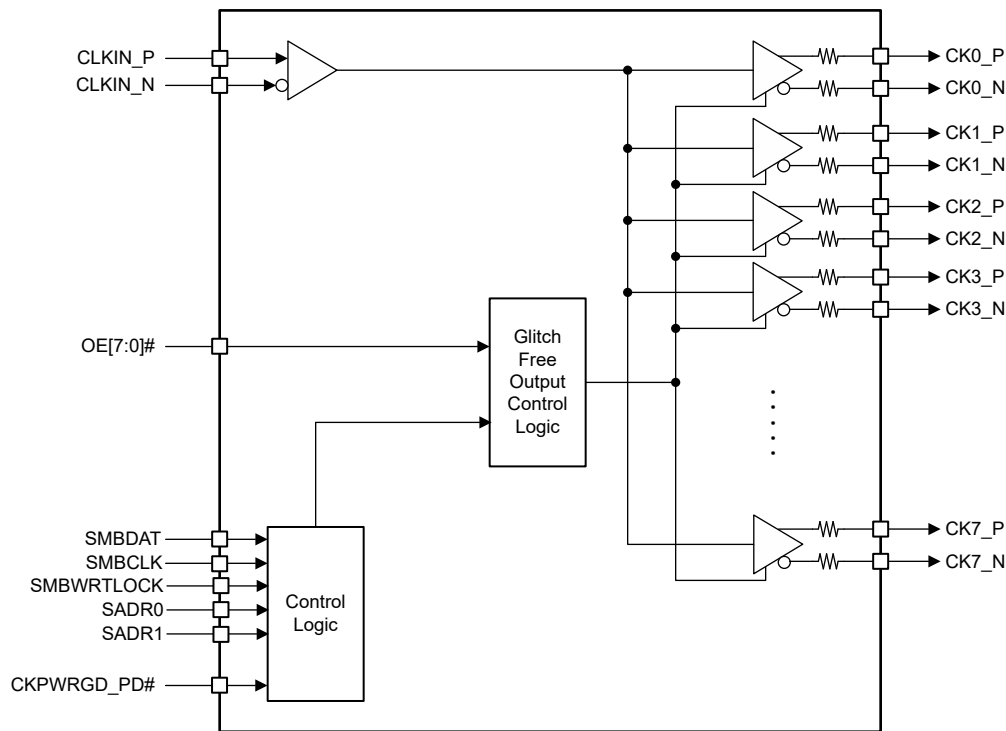
图 7-2. DC Simulation Load (Referencing Intel DB2000QL Document)

8 Detailed Description

8.1 Overview

The CDCDB803 is a low additive-jitter, low propagation delay clock buffer designed to meet the strict performance requirements for PCIe Gen 1-5, QPI, UPI, SAS, and SATA reference clocks. The CDCDB803 allows buffering and replication of a single clock source to up to eight individual outputs in the LP-HCSL format. The CDCDB803 also includes status and control registers accessible by an SMBus version 2.0 compliant interface. The device integrates a large amount of external passive components to reduce overall system cost.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fail-Safe Input

The CDCDB803 is designed to support fail-safe input operation feature. This feature allows the user to drive the device inputs before V_{DD} is applied without damaging the device. Refer to the [Absolute Maximum Ratings](#) table for more information on the maximum input supported by the device.

8.3.2 Output Enable Control

The CDCDB803 uses SMBus and OE# to control the state of the output channels. The OE# pins control the state of the output with the same number. For example, the OE5# pin controls the state of the CK5 output driver. The SMBus registers may enable or disable the output when the corresponding OE# pin is held low.

8.3.3 SMBus

The CDCDB803 has an SMBus interface that is active only when CKPWRGD_PD# = 1. The SMBus allows individual enable/disable of each output.

When CKPWRGD_PD# = 0, the SMBus pins are placed in a Hi-Z state, but all register settings are retained. The SMBus register values are only retained while V_{DD} remains inside of the recommended operating voltage.

8.3.3.1 SMBus Address Assignment

The SMBus address is assigned by configuration of two pins (SADR1 and SADR0) that each support three levels. This configuration allows the CDCDB803 to assume nine different SMBus addresses.

8.4.2 OE[7:0]# and SMBus Output Enables

Each output channel, 0 to 7, can be individually enabled or disabled by a SMBus control register bit, called SMB enable bits. Additionally, each output channel has a dedicated, corresponding, OE[7:0]# hardware pin. The OE[7:0]# pins are asynchronously asserted-low signals that may enable or disable the output.

Refer to [表 8-2](#) for enabling and disabling outputs through the hardware and software. Note that both the SMB enable bit must be a 1 and the OEx# pin must be an input low voltage 0 for the output channel to be active.

表 8-2. OE[7:0]# Functionality

| Control Inputs | Power State Variables (Internal) | | CLKIN | OE[7:0]# HARDWARE PINS AND SMBus CONTROL REGISTER BITS | | | CK[7:0]_P/ CK[7:0]_N |
|----------------|----------------------------------|------------------------|------------------|--|----------|-----------------|-------------------------|
| | CKPWRGD_PD# | PWRGD | | PD# | OE[7:0]# | OUT_EN_CLK[7:0] | |
| 0 | 0 | 0 | X | X | X | X | LOW/LOW |
| 1 | 1 | 1 | X ⁽¹⁾ | X | 0 | 0 | LOW/LOW |
| | | | | | | 1 | TRI-STATE |
| | | | | 1 | X | 0 | LOW/LOW |
| | | | | | 1 | TRI-STATE | |
| | | Running ⁽¹⁾ | 0 | 1 | X | Running | |
| 0 | 0 | 0 | X ⁽²⁾ | X | X | 0 | LOW/LOW |
| | | | | | | 1 | TRI-STATE |

(1) To enter the power-down state, CLKIN must remain active for at least 3 clock cycles after CKPWRGD_PD# transitions from 1 to 0.

(2) To enter the powered-up state with active clock outputs, CLKIN must be active before CKPWRGD_PD# transitions from 0 to 1.

8.4.3 Output Slew Rate Control

The CDCDB803 provides output slew rate control feature which customer can use to compensate for increased output trace length based on their board design. The slew rate of a bank of 4 outputs 0 to 3 and 4 to 7, can be changed within a given range by a SMBus control register called CAPTRIM. Refer to [表 8-16](#) for more information.

8.4.4 Output Impedance Control

The integrated termination on the CDCDB803 can be programmed either for 85 Ω or 100 Ω. This flexibility ensures that the customer can use the same device across various applications irrespective of the characteristic board impedance which is typically either 85 Ω or 100 Ω. This termination resistor can be changed for all the outputs as whole using bit 5 of a register called OUTSET. Refer to [表 8-14](#) for more information.

8.5 Programming

The CDCDB803 uses SMBus to program the states of its eight output drivers. See [SMBus](#) for more information on the SMBus programming, and [Register Maps](#) for information on the registers.

表 8-3. Command Code Definition

| BIT | DESCRIPTION |
|-------|--|
| 7 | 0 = <i>Block Read</i> or <i>Block Write</i> operation 1 = <i>Byte Read</i> or <i>Byte Write</i> operation |
| (6:0) | Register address for <i>Byte</i> operations, or starting register address for <i>Block</i> , operations |

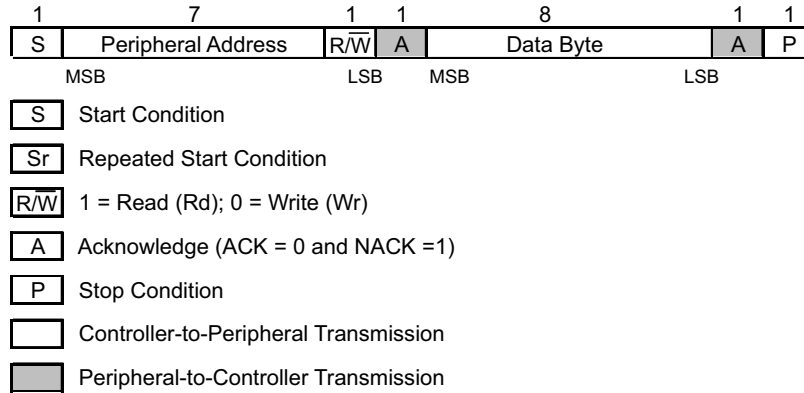


图 8-2. Generic Programming Sequence

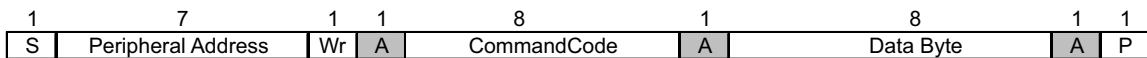


图 8-3. Byte Write Protocol

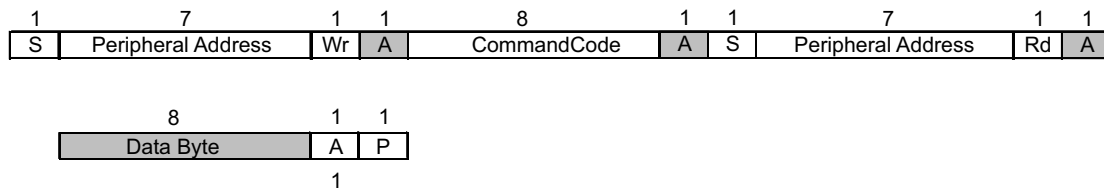


图 8-4. Byte Read Protocol

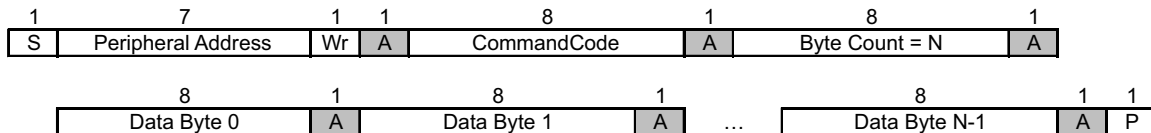


图 8-5. Block Write Protocol

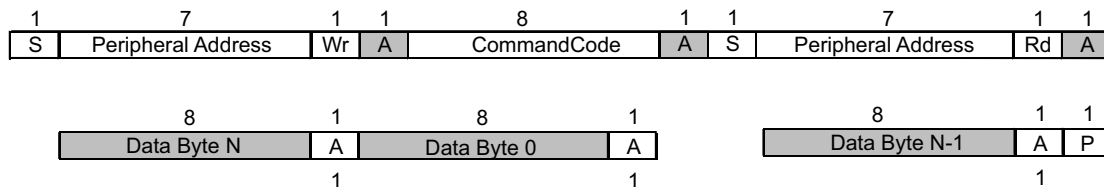


图 8-6. Block Read Protocol

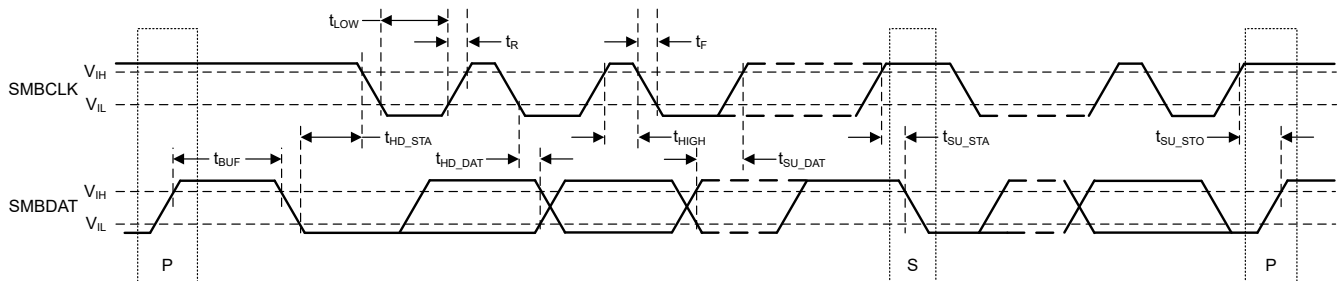


图 8-7. SMBus Timing Diagram

8.6 Register Maps

8.6.1 CDCDB803 Registers

表 8-4 lists the CDCDB803 registers. All register locations not listed in 表 8-4 should be considered as reserved locations and the register contents should not be modified.

表 8-4. CDCDB803 Registers

| Address | Acronym | Register Name | Section |
|---------|----------|-----------------------------------|--------------------|
| 0h | RCR1 | Reserved Control Register 1 | Go |
| 1h | OECR1 | Output Enable Control 1 | Go |
| 2h | OECR2 | Output Enable Control 2 | Go |
| 3h | OERDBK | Output Enable# Pin Read Back | Go |
| 4h | RCR2 | Reserved Control Register 2 | Go |
| 5h | VDRREVID | Vendor/Revision Identification | Go |
| 6h | DEVID | Device Identification | Go |
| 7h | BTRDCNT | Byte Read Count Control | Go |
| 8h | OUTSET | Output Setting Control | Go |
| 4Ch | CAPTRIM | Slew Rate Capacitor Cluster 1 & 2 | Go |

Complex bit access types are encoded to fit into small table cells. 表 8-5 shows the codes that are used for access types in this section.

表 8-5. CDCDB803 Access Type Codes

| Access Type | Code | Description |
|------------------------|------|--|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| -n | | Value after reset or the default value |

8.6.1.1 RCR1 Register (Address = 0h) [reset = 47h]

RCR1 is shown in 表 8-6.

Return to the [Summary Table](#).

The RCR1 register contains reserved bits.

表 8-6. RCR1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-4 | Reserved | R | 4h | Reserved. |
| 3-0 | Reserved | R/W | 7h | Writing to these bits will not affect the functionality of the device. |

8.6.1.2 OECR1 Register (Address = 1h) [reset = FFh]

OECR1 is shown in [OECR1 Register Field Descriptions](#).

Return to the [Summary Table](#).

The OECR1 register contains bits that enable or disable individual output clock channels [5:0].

表 8-7. OECR1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | OUT_EN_CLK5 | R/W | 1h | This bit controls the output enable signal for output channel CK5_P/ CK5_N. 0h = Output Disabled 1h = Output Enabled |
| 6 | OUT_EN_CLK4 | R/W | 1h | This bit controls the output enable signal for output channel CK4_P/ CK4_N. 0h = Output Disabled 1h = Output Enabled |
| 5 | OUT_EN_CLK3 | R/W | 1h | This bit controls the output enable signal for output channel CK3_P/ CK3_N. 0h = Output Disabled 1h = Output Enabled |
| 4 | OUT_EN_CLK2 | R/W | 1h | This bit controls the output enable signal for output channel CK2_P/ CK2_N. 0h = Output Disabled 1h = Output Enabled |
| 3 | Reserved | R/W | 1h | Writing to this bit will not affect the functionality of the device. |
| 2 | OUT_EN_CLK1 | R/W | 1h | This bit controls the output enable signal for output channel CK1_P/ CK1_N. 0h = Output Disabled 1h = Output Enabled |
| 1 | OUT_EN_CLK0 | R/W | 1h | This bit controls the output enable signal for output channel CK0_P/ CK0_N. 0h = Output Disabled 1h = Output Enabled |
| 0 | Reserved | R/W | 1h | Writing to this bit will not affect the functionality of the device. |

8.6.1.3 OECR2 Register (Address = 2h) [reset = 0Fh]

OECR2 is shown in [OECR2 Register Field Descriptions](#).

Return to the [Summary Table](#).

The OECR2 register contains bits that enable or disable individual output clock channels [7:6].

表 8-8. OECR2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7-3 | Reserved | R/W | 1h | Writing to these bits will not affect the functionality of the device. |
| 2 | OUT_EN_CLK7 | R/W | 1h | This bit controls the output enable signal for output channel CK7_P/ CK7_N. 0h = Output Disabled 1h = Output Enabled |
| 1 | Reserved | R/W | 1h | Writing to this bit will not affect the functionality of the device. |
| 0 | OUT_EN_CLK6 | R/W | 1h | This bit controls the output enable signal for output channel CK6_P/ CK6_N. 0h = Output Disabled 1h = Output Enabled |

8.6.1.4 OERDBK Register (Address = 3h) [reset = 0h]

OERDBK is shown in [表 8-9](#).

Return to the [Summary Table](#).

The OERDBK register contains bits that report the current state of the OE[7:0]# input pins.

表 8-9. OERDBK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 7 | RB_OE7 | R | 0h | This bit reports the logic level present on the OE7# pin. |
| 6 | RB_OE6 | R | 0h | This bit reports the logic level present on the OE6# pin. |
| 5 | RB_OE5 | R | 0h | This bit reports the logic level present on the OE5# pin. |
| 4 | RB_OE4 | R | 0h | This bit reports the logic level present on the OE4# pin. |
| 3 | RB_OE3 | R | 0h | This bit reports the logic level present on the OE3# pin. |
| 2 | RB_OE2 | R | 0h | This bit reports the logic level present on the OE2# pin. |
| 1 | RB_OE1 | R | 0h | This bit reports the logic level present on the OE1# pin. |
| 0 | RB_OE0 | R | 0h | This bit reports the logic level present on the OE0# pin. |

8.6.1.5 RCR2 Register (Address = 4h) [reset = 0h]

RCR2 is shown in [RCR2 Register Field Descriptions](#).

Return to the [Summary Table](#).

The RCR2 register contains reserved bits.

表 8-10. RCR2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7-0 | Reserved | R | 0h | Reserved. |

8.6.1.6 VDRREVID Register (Address = 5h) [reset = 0Ah]

VDRREVID is shown in [表 8-11](#).

Return to the [Summary Table](#).

The VDRREVID register contains a vendor identification code and silicon revision code.

表 8-11. VDRREVID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7-4 | REV_ID | R | 0h | Silicon revision code. Silicon revision code bits [3:0] map to register bits [7:4] directly. |
| 3-0 | VENDOR_ID | R | Ah | Vendor identification code. Vendor ID bits [3:0] map to register bits [3:0] directly. |

8.6.1.7 DEVID Register (Address = 6h) [reset = E7h]

DEVID is shown in [表 8-12](#).

Return to the [Summary Table](#).

The DEVID register contains a device identification code.

表 8-12. DEVID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 7-0 | DEV_ID | R | E7h | Device ID code. Device ID bits[7:0] map to register bits[7:0] directly. |

8.6.1.8 BTRDCNT Register (Address = 7h) [reset = 8h]

BTRDCNT is shown in [表 8-13](#).

Return to the [Summary Table](#).

The BTRDCNT register contains bits [4:0] which configure the number of bytes which will be read back.

表 8-13. BTRDCNT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-5 | Reserved | R/W | 0h | Writing to these bits will not affect the functionality of the device. |
| 4-0 | BYTE_COUNTER | R/W | 8h | Writing to this register configures how many bytes will be read back. |

8.6.1.9 OUTSET Register (Address = 8h) [reset = 0h]

OUTSET is shown in [表 8-14](#).

Return to the [Summary Table](#).

Bit5 of the OUTSET register sets the termination for all the outputs while bit4 can be used to set the power-down state for all outputs. The remaining bits for this register are reserved.

表 8-14. OUTSET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 7-6 | Reserved | R | 0h | Reserved. |
| 5 | CH_ZOUT_SEL | R/W | 0h | Select between 85 Ω (0) and 100 Ω (1) Output impedance |
| 4 | d_DRIVE_OP_STATE_CTRL | R/W | 0h | Power-down state of all output clocks. 0: LOW/LOW 1: TRI_STATE |
| 3-0 | Reserved | R/W | 0h | Register bits can be written to 0. Writing a different value than 0 will affect device functionality. |

8.6.1.10 CAPTRIM Register (Address = 4Ch) [reset = 66h]

CAPTRIM is shown in [表 8-16](#).

Return to the [Summary Table](#).

Bits [7:4] of the CAPTRIM register is used to control the slew rate for output channel cluster 2. Bits [3:0] control the slew rate for output channel cluster 1. Refer below for cluster identification.

表 8-15. Cluster Identification

| Cluster | Outputs |
|---------|--------------------|
| 1 | CK3, CK2, CK1, CK0 |
| 2 | CK7, CK6, CK5, CK4 |

表 8-16. CAPTRIM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7-4 | CLUSTER2_CAP_TRIM | R/W | 6h | Slew Rate Reduction Cap Trim for Cluster 2. Default value of 6h. 0: minimum F: maximum |
| 3-0 | CLUSTER1_CAP_TRIM | R/W | 6h | Slew Rate Reduction Cap Trim for Cluster 1. Default value of 6h. 0: minimum F: maximum |

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The CDCDB803 is a fanout buffer that supports PCIe generation 4 and PCIe generation 5 REFCLK distribution. It is used to distribute up to eight copies of a typically 100-MHz clock.

9.2 Typical Application

图 9-1 shows a CDCDB803 typical application. In this application, a clock generator provides a 100-MHz reference to the CDCDB803 which then distributes that clock to PCIe endpoints. The clock generator may be a discrete clock generator like the LMK03328 or it may be integrated in a larger component such as a Platform Controller Hub (PCH) or application processor.

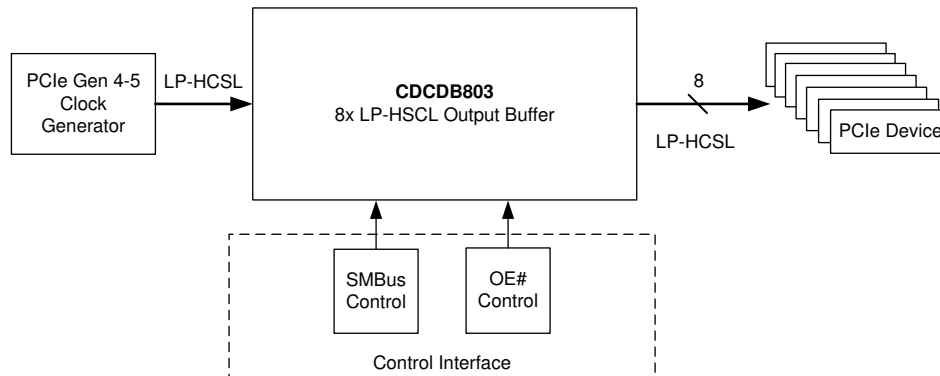


图 9-1. Typical Application

9.2.1 Design Requirements

Consider a typical server motherboard application which must distribute a 100-MHz PCIe reference clock from the PCH of a processor chipset to multiple endpoints. An example of clock input and output requirements is:

- Clock Input:
 - 100-MHz LP-HCSL
- Clock Output:
 - 2x 100-MHz to processors, LP-HCSL
 - 3x 100-MHz to riser/retimer, LP-HCSL
 - 3x 100-MHz to DDR memory controller, LP-HCSL

9.2.2 Detailed Design Procedure

The following items must be determined before starting design of a CDCDB803 socket:

- Output Enable Control Method
- SMBus address

9.2.2.1 Output Enable Control Method

The device provides an option to either use SMBus programmed registers (software) to control the outputs or by using the hardware OE# pins. In case of using software to control the outputs, the hardware OE# pins can be left floating as each of these pins have a pulldown to ground. Refer to 表 8-2 and the *Register Maps* section for more information on programming the register.

When the user wants to control the outputs with the hardware OE# pins, they can do so for example by connecting these pins to a GPIO controller and follow the *Pin Configuration and Functions* section to set the outputs to HIGH/LOW. The bits OUT_EN_CLK7 to OUT_EN_CLK0 used to control the outputs are shown in registers OECR1 (表 8-7) and OECR2 (表 8-8). These register bits are set to 1 by default to ensure that the outputs are "software enabled" and their state is therefore set by hardware OE# pins.

9.2.2.2 SMBus Address

An SMBus address should be selected from the listed potential addresses in 表 8-1. The appropriate pullup or pulldown resistor should be placed on the SADRx pins as indicated in the table. Ensure the SMBus address is not already in use to avoid conflict.

9.2.3 Application Curves

图 6-1 in the *Typical Characteristics* section can be used as both an application curve and a typical characteristics plot in this example.

The 图 9-2 and 图 9-3 show characterization data for the Output slew rate for various CAPTRIM codes and across temperature. Customers can use these plots as reference for choosing the appropriate output slew rate based on their system requirement.

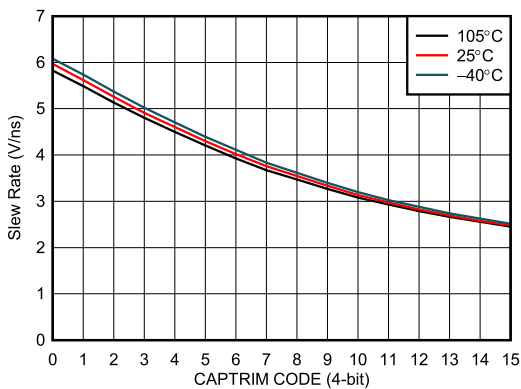


图 9-2. Output Slew Rate vs. CAPTRIM Code

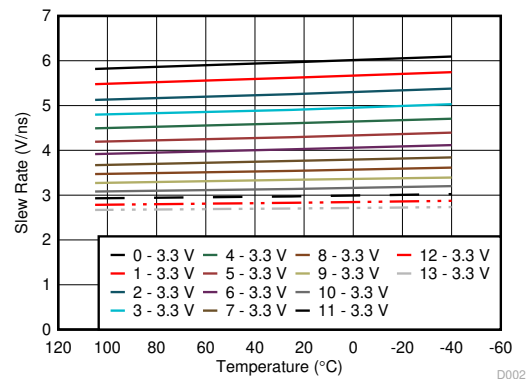


图 9-3. Slew Rate Variation Across Temperature for Different CAPTRIM Code

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power-supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, place the capacitors very close to the power-supply terminals and lay out with short loops to minimize inductance. TI recommends to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer. These beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 10-1 shows the recommended power supply filtering and decoupling method.

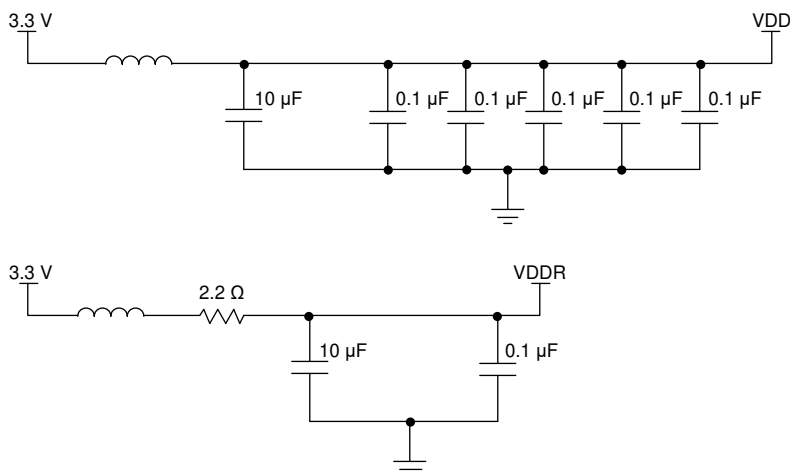


Figure 10-1. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

The following section provides the layout guidelines to ensure good thermal performance and power supply connections for the CDCDB803.

In [Layout Examples](#), the CDCDB803 has 85- Ω differential output impedance LP-HCSL format drivers as per register default settings. All transmission lines connected to CKx pins should be 85- Ω differential impedance, 42.5- Ω single-ended impedance to avoid reflections and increased radiated emissions. If 100- Ω output impedance is enabled, the transmission lines connected to CKx pins should be 100- Ω differential impedance, 50- Ω single-ended impedance. Take care to eliminate or reduce stubs on the transmission lines.

11.2 Layout Examples

[图 11-1](#) through [图 11-3](#) are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB.

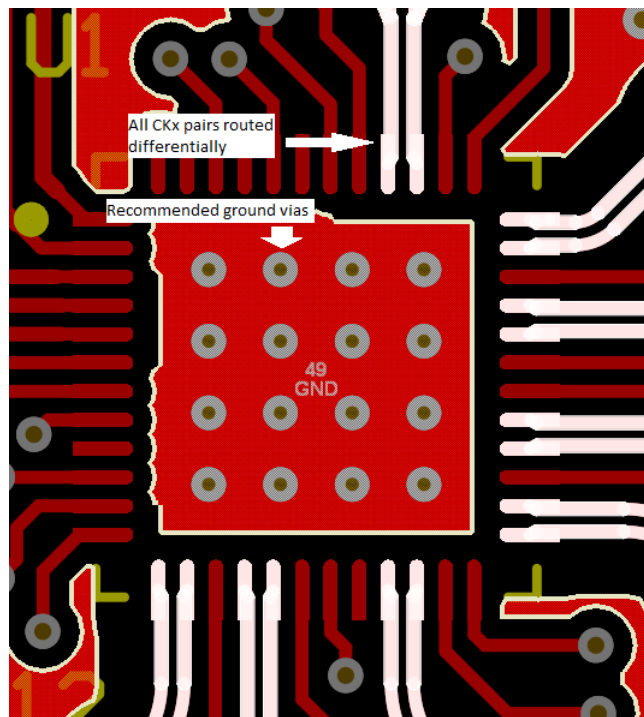


图 11-1. PCB Layout Example for CDCDB803, Top layer

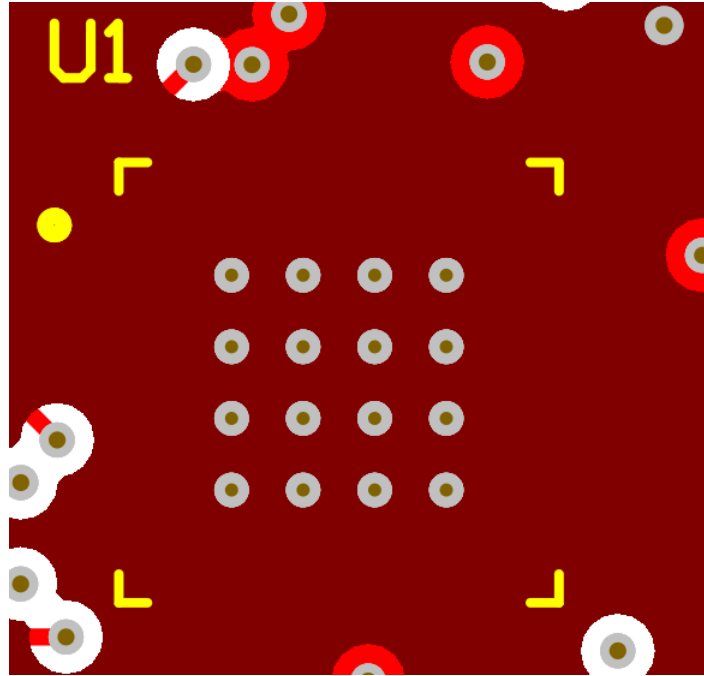


图 11-2. PCB Layout Example for CDCDB803, GND Layer

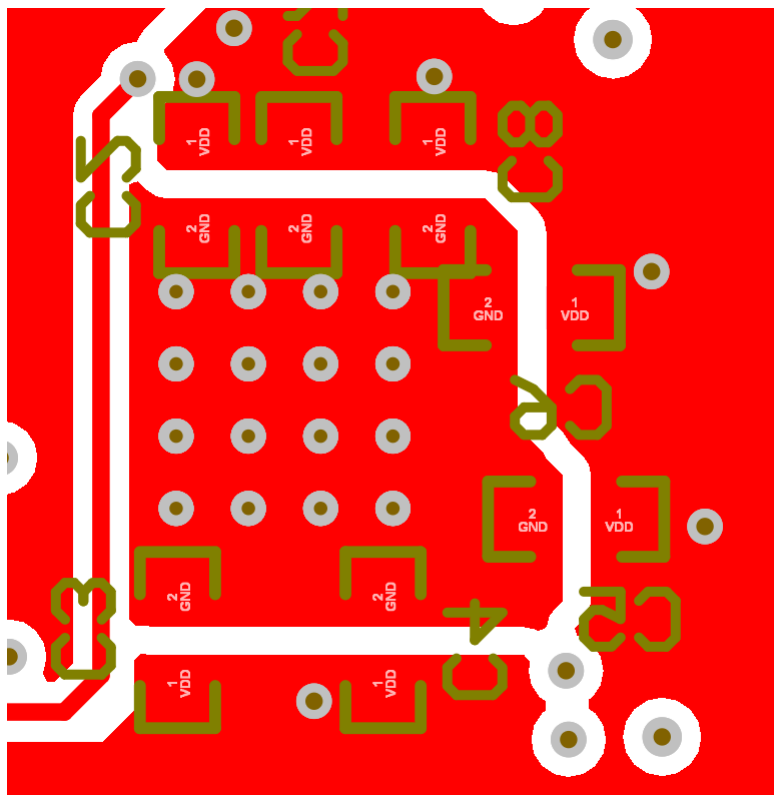


图 11-3. PCB Layout Example for CDCDB803, Bottom Layer

12 Device and Documentation Support

12.1 Device Support

12.1.1 TICS Pro

TICS Pro is an offline software tool for EVM programming and also for register map generation to program a device configuration for a specific application. For TICS Pro, go to <https://www.ti.com/tool/TICSPRO-SW>.

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDCDB803RSLR | ACTIVE | VQFN | RSL | 48 | 4000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | CDCB803 | Samples |
| CDCDB803RSLT | ACTIVE | VQFN | RSL | 48 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | CDCB803 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

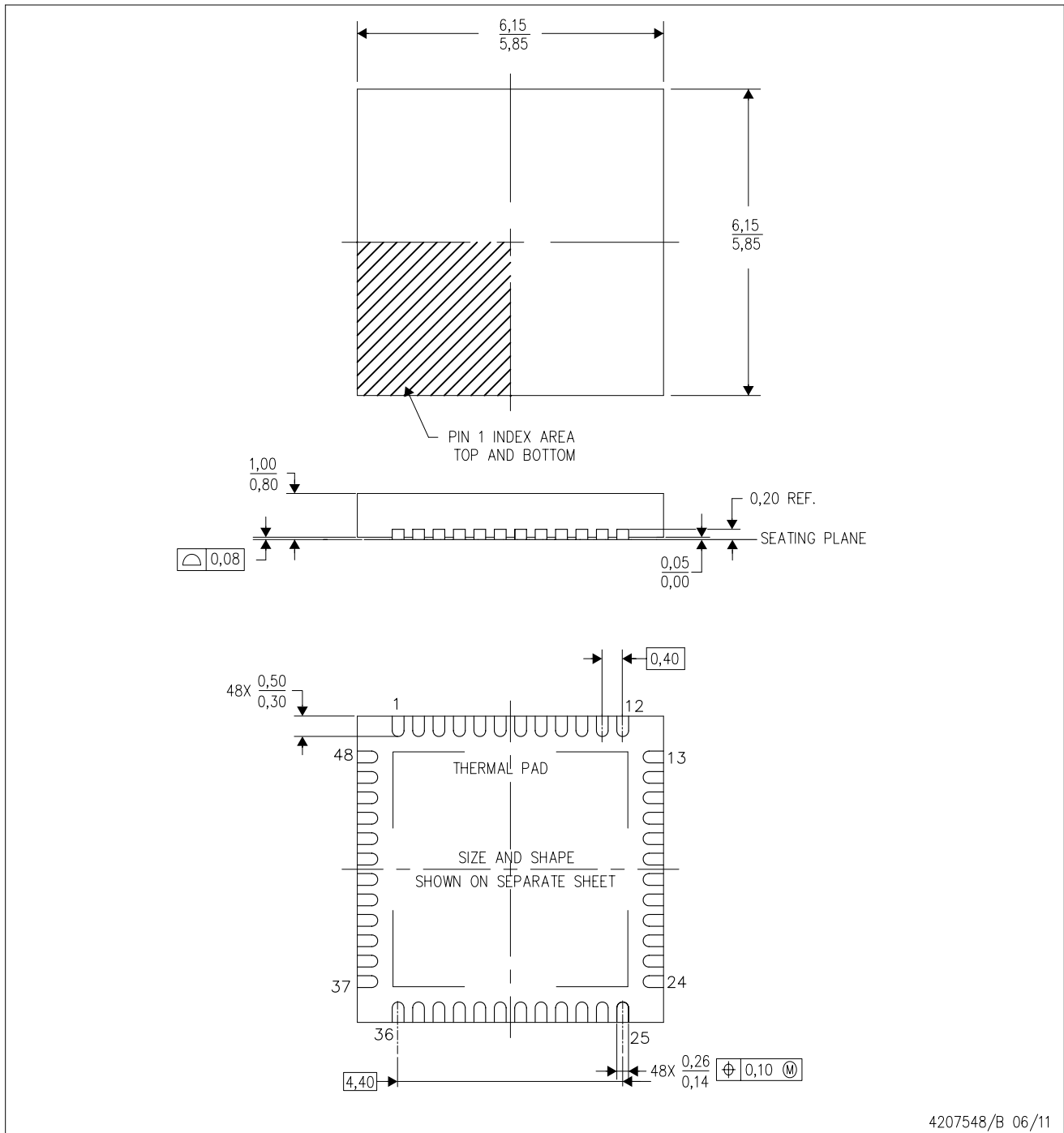
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MECHANICAL DATA

RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



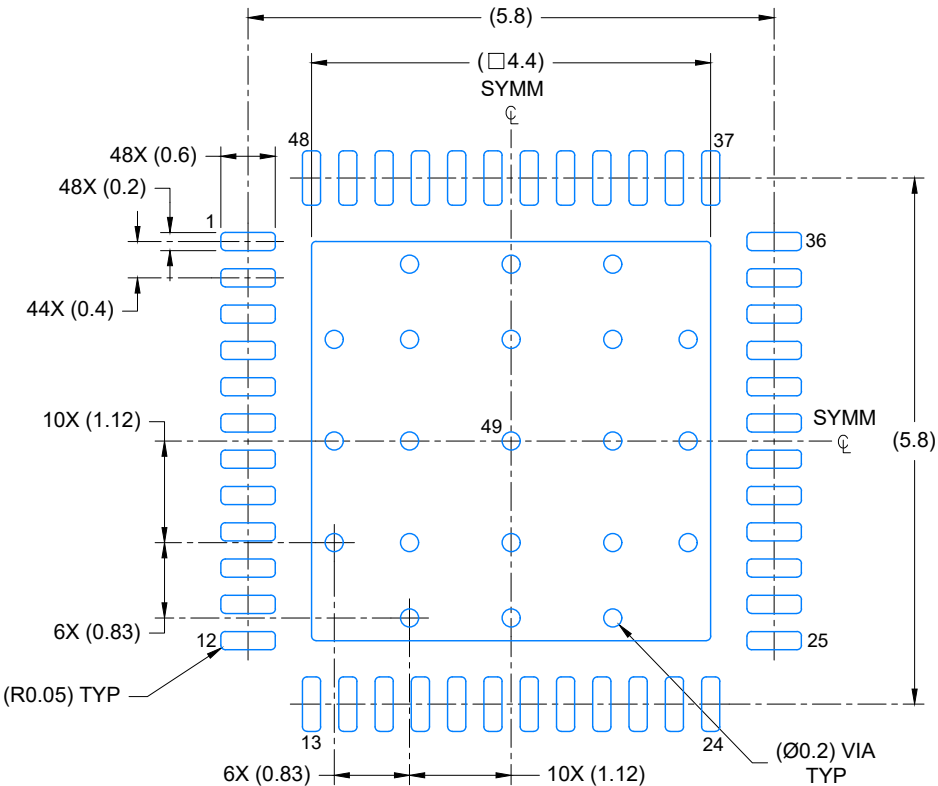
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

EXAMPLE BOARD LAYOUT

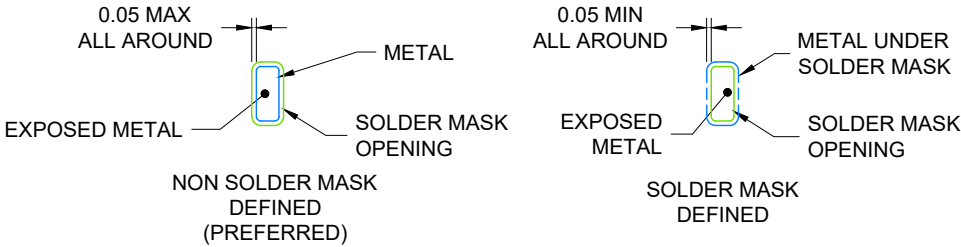
RSL0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4219205/A 02/2020

NOTES: (continued)

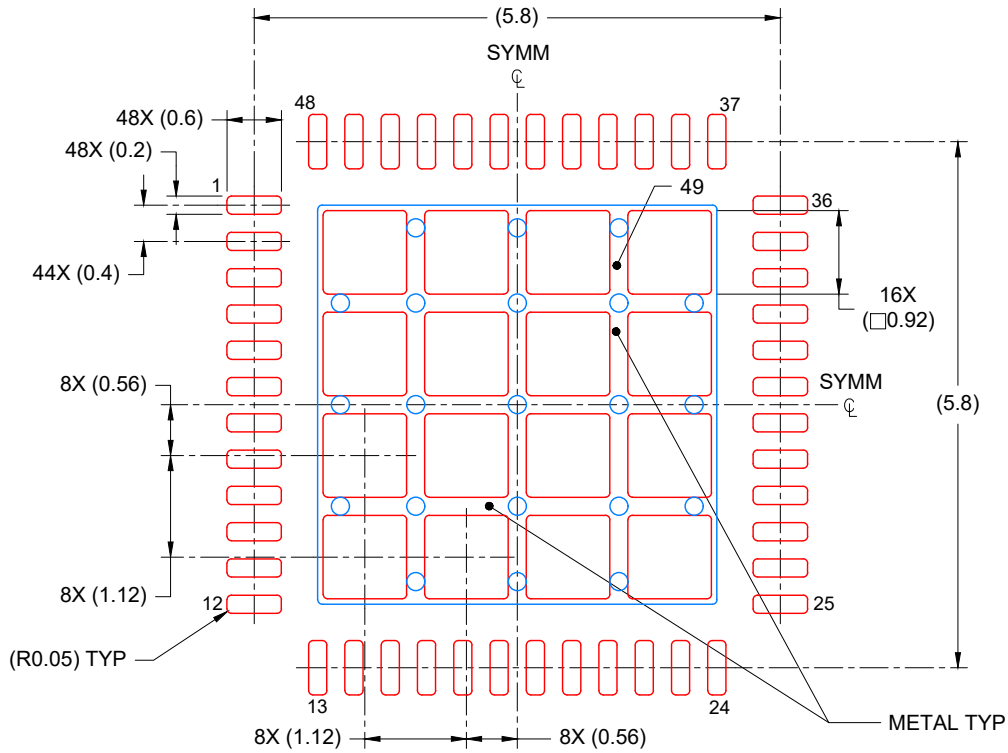
- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSL0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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