

SN74CB3T3245 8 位 FET 总线开关

2.5V 和 3.3V 低电压且可耐受 5V 电压的电平转换器

1 特性

- 标准 245 型引脚
- 输出电压转换跟踪 V_{CC}
- 所有数据 I/O 端口均支持混合模式信号运行
 - 5V 输入降至 3.3V 输出电位移, V_{CC} 为 3.3V
 - 5V/3.3V 输入降至 2.5V 输出电位移, V_{CC} 为 2.5V
- 支持器件加电与断电的 5V 耐压 I/O
- 支持近零传播延迟的双向数据流
- 低导通电阻 (r_{on}) 特性, (r_{on} 典型值 = 5Ω)
- 低输入/输出电容可减小负载 ($C_{io(OFF)}$ 典型值 = 5pF)
- 数据与控制输入提供下冲钳位二极管
- 低功耗 (I_{CC} 最大值 = 40μA)
- V_{CC} 工作电压范围: 2.3V 至 3.6V
- 数据 I/O 支持 0V 至 5V 信号电平 (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V)
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- I_{off} 支持部分断电模式工作
- 闩锁性能超过 JESD 17 所规定的 250mA
- ESD 性能测试符合 JESD 22 标准

- 2000V 人体放电模型 (A114-B, II 类)

- 1000V 充电器件模型 (C101)

- 低功耗便携式设备的理想选择

2 应用

- 支持数字 应用: 电平转换、PCI 接口、USB 接口、内存交错、总线隔离

3 说明

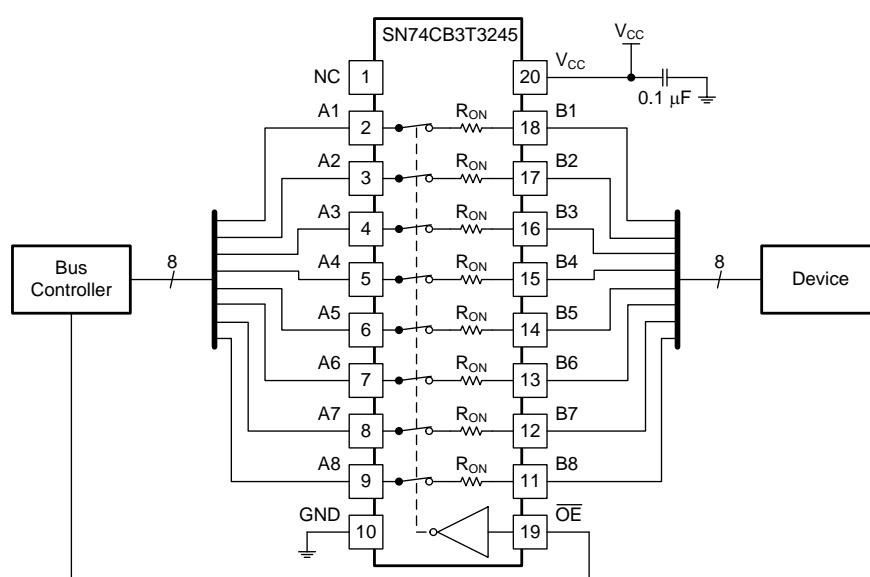
SN74CB3T3245 器件是一种具备低导通状态电阻 (r_{on}) 的高速 TTL 兼容型 8 位 FET 总线开关, 可实现最短传播延迟。该器件提供可跟踪 V_{CC} 的电压转换, 能够在所有数据 I/O 端口上全面支持混合模式信号运行。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN74CB3T3245DBQ	SSOP (20)	8.65mm x 3.90mm
SN74CB3T3245DGV	TVSOP (20)	5.00mm x 4.40mm
SN74CB3T3245DW	SOIC (20)	12.80mm x 7.50mm
SN74CB3T3245PW	TSSOP (20)	6.50mm x 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品目录。

典型应用功能图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

English Data Sheet: SCDS136

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

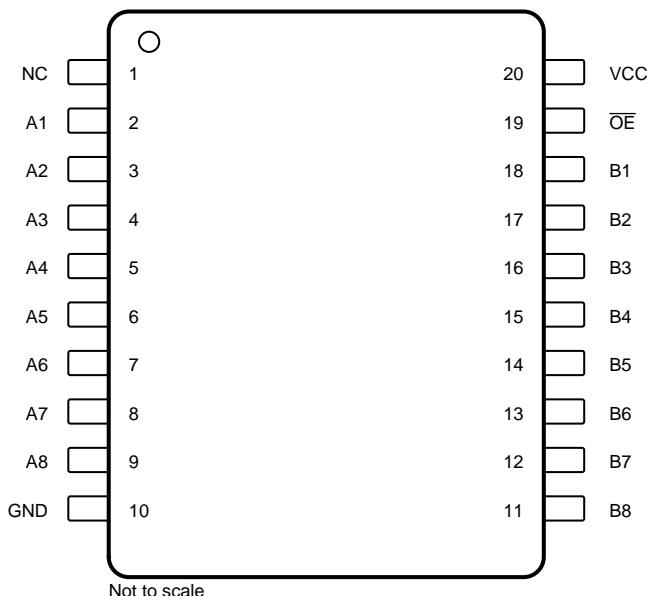
Changes from Revision B (June 2015) to Revision C	Page
• Changed the pin out image appearance	3
• Changed $I_O = 1 \text{ mA}$ To: $I_O = 1 \mu\text{A}$ in Figure 9 and Figure 10	11

Changes from Revision A (August 2012) to Revision B	Page
• 添加了应用、器件信息表、引脚配置和功能部分、 <i>ESD</i> 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1
• 删除了订购信息表。	1

Changes from Original (March 2005) to Revision A	Page
• Updated graphic note and picture in Figure 1.....	8

5 Pin Configuration and Functions

**DBQ, DGV, DW, and PW Package
20-Pin SSOP, TSSOP, SOIC, TSSOP
Top View**



NC — No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	Not internally connected
2	A1	I/O	Switch 1 A terminal
3	A2	I/O	Switch 2 A terminal
4	A3	I/O	Switch 3 A terminal
5	A4	I/O	Switch 4 A terminal
6	A5	I/O	Switch 5 A terminal
7	A6	I/O	Switch 6 A terminal
8	A7	I/O	Switch 7 A terminal
9	A8	I/O	Switch 8 A terminal
10	GND	—	Ground
11	B8	I/O	Switch 8 B terminal
12	B7	I/O	Switch 7 B terminal
13	B6	I/O	Switch 6 B terminal
14	B5	I/O	Switch 5 B terminal
15	B4	I/O	Switch 4 B terminal
16	B3	I/O	Switch 3 B terminal
17	B2	I/O	Switch 2 B terminal
18	B1	I/O	Switch 1 B terminal
19	OE	I	Output enable, active low
20	V _{CC}	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾	-0.5	7	V
V_{IN}	Control input voltage ⁽²⁾⁽³⁾	-0.5	7	V
$V_{I/O}$	Switch I/O voltage ⁽²⁾⁽³⁾⁽⁴⁾	-0.5	7	V
I_{IK}	Control input clamp current $V_{IN} < 0$		-50	mA
$I_{I/OK}$	I/O port clamp current $V_{I/O} < 0$		-50	mA
$I_{I/O}$	ON-state switch current ⁽⁵⁾		± 128	mA
	Continuous current through V_{CC} or GND		± 100	mA
T_J	Junction temperature		150	
T_{stg}	Storage temperature	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to ground unless otherwise specified.
- The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- V_I and V_O are used to denote specific conditions for $V_{I/O}$.
- I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level control input voltage $V_{CC} = 2.3$ V to 2.7 V	1.7	5.5	V
	$V_{CC} = 2.7$ V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage $V_{CC} = 2.3$ V to 2.7 V	0	0.7	V
	$V_{CC} = 2.7$ V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	-40	85	°C

- All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number **SCBA004**.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74CB3T3245				UNIT	
	DBQ (SSOP)	DGV (TSSOP)	DW (SOIC)	PW (TSSOP)		
	20 PINS	20 PINS	20 PINS	20 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68	92	58	83	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
V_{IK}		$V_{CC} = 3 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2		V	
V_{OH}		See and Figure 1					
I_{IN}	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_{IN} = 3.6 \text{ V}$ to 5.5 V or GND		± 10		μA	
I_I		$V_{CC} = 3.6 \text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7 \text{ V}$ to 5.5 V	± 20		μA	
			$V_I = 0.7 \text{ V}$ to $V_{CC} - 0.7 \text{ V}$	-40			
			$V_I = 0$ to 0.7 V	± 5			
$I_{OZ}^{(3)}$		$V_{CC} = 3.6 \text{ V}$, $V_O = 0$ to 5.5 V , $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND		± 10		μA	
I_{off}		$V_{CC} = 0$, $V_O = 0$ to 5.5 V , $V_I = 0$,		10		μA	
I_{CC}		$V_{CC} = 3.6 \text{ V}$, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND	40		μA	
			$V_I = 5.5 \text{ V}$	40			
$\Delta I_{CC}^{(4)}$	Control inputs	$V_{CC} = 3 \text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND		300		μA	
C_{in}	Control inputs	$V_{CC} = 3.3 \text{ V}$, $V_{IN} = V_{CC}$ or GND		4		pF	
$C_{io(OFF)}$		$V_{CC} = 3.3 \text{ V}$, $V_{I/O} = 5.5 \text{ V}$, 3.3 V , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND		5		pF	
$C_{io(ON)}$		$V_{CC} = 3.3 \text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5 \text{ V}$ or 3.3 V	5		pF	
			$V_{I/O} = \text{GND}$	13			
$r_{on}^{(5)}$		$V_{CC} = 2.3 \text{ V}$, TYP at $V_{CC} = 2.5 \text{ V}$, $V_I = 0$	$I_O = 24 \text{ mA}$	5	8.5	Ω	
			$I_O = 16 \text{ mA}$	5			
		$V_{CC} = 3 \text{ V}$, $V_I = 0$	$I_O = 64 \text{ mA}$	5	7		
			$I_O = 32 \text{ mA}$	5			

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A	0.15		0.25		ns
t_{en}	\overline{OE}	A or B	1	10.5	1	8	ns
t_{dis}	\overline{OE}	A or B	1	5.5	1	7.5	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

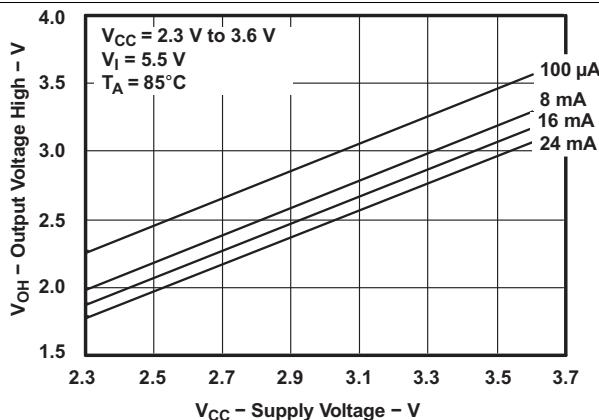


Figure 1. V_{OH} vs V_{CC}

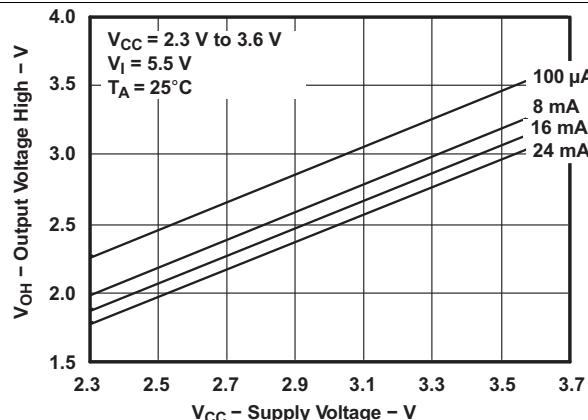


Figure 2. V_{OH} vs V_{CC}

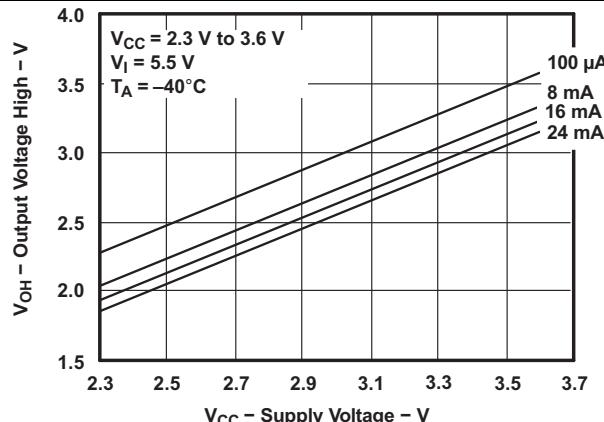
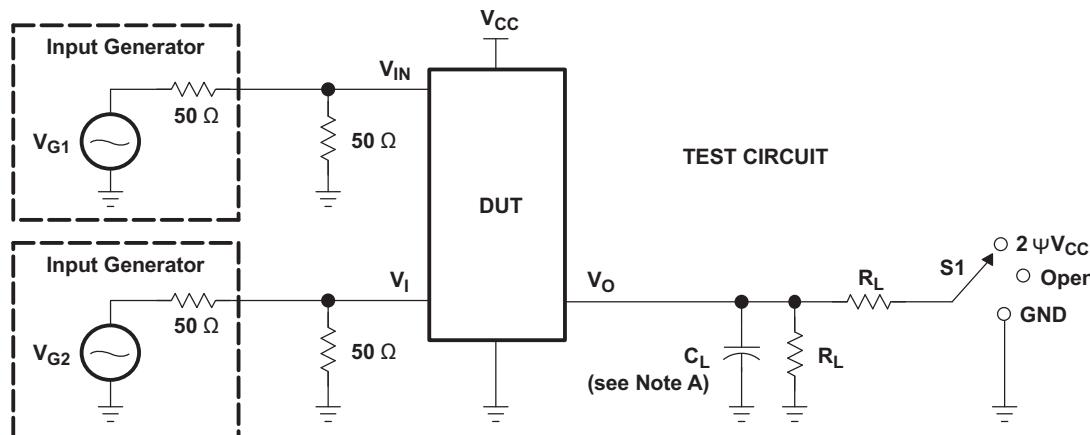
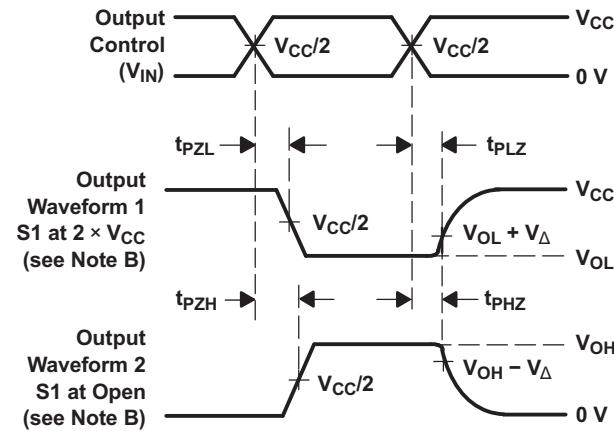
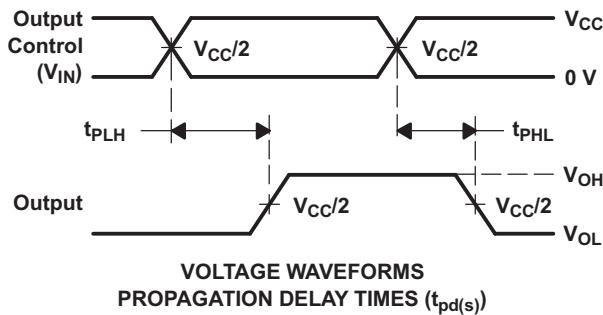


Figure 3. V_{OH} vs V_{CC}

7 Parameter Measurement Information



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V _{CC} 2 × V _{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- t_{PZL} and t_{PZH} are the same as t_{en}.
- t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- All parameters and waveforms are not applicable to all devices.

Figure 4. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

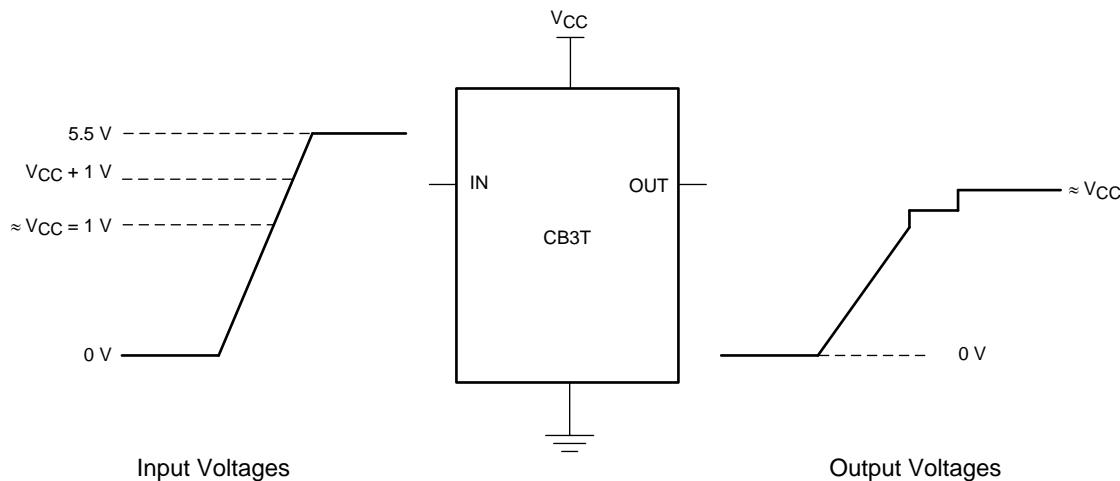
The SN74CB3T3245 device is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T3245 device supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see [Figure 5](#)).

The SN74CB3T3245 device is an 8-bit bus switch with a single output-enable (\overline{OE}) input and a standard '245 pinout. When \overline{OE} is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} + 1V$, and less than or equal to 5.5V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 5. Typical DC Voltage Translation Characteristics

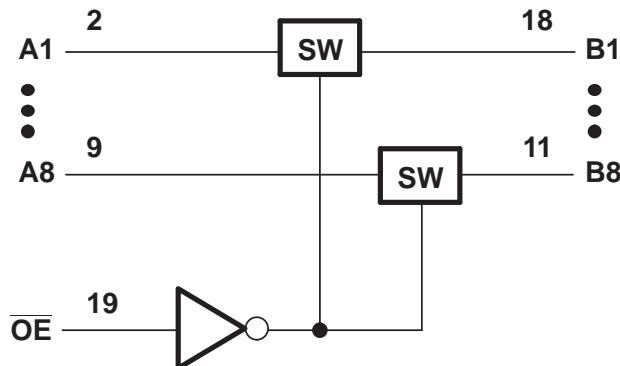
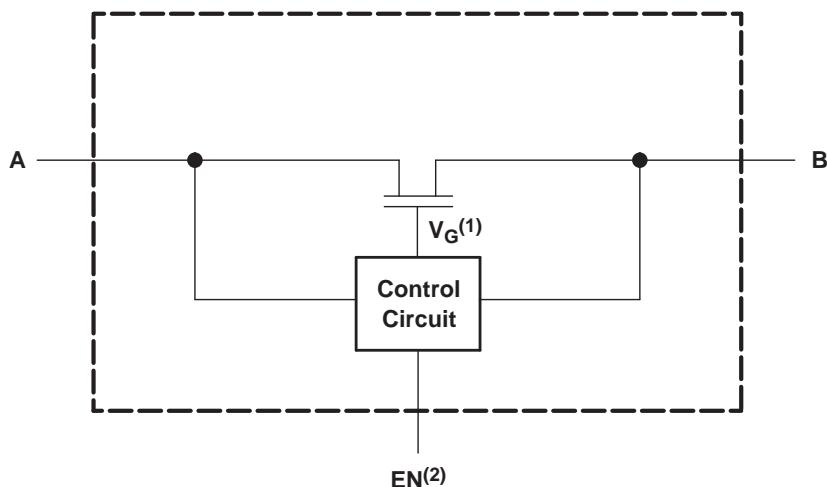


Figure 6. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



- 1) Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > (V_{CC} + V_T)$.
- 2) EN is the internal enable signal applied to the switch.

Figure 7. Simplified Schematic, Each FET Switch (SW)

8.3 Feature Description

The SN74CB3T3245 device uses the standard '245-type pinout. The output voltage tracks V_{CC} , allowing for easy down-translation. The device is ideal for low-power portable equipment.

Mixed-mode signal operation is supported on all data I/O ports. 5-V input down to 3.3-V output level shift with 3.3-V V_{CC} and 5-V/3.3-V input down to 2.5-V output level shift With 2.5-V V_{CC} are possible due to overvoltage tolerant inputs.

This part is friendly to partial power down systems. The I/Os are 5-V-tolerant with the device powered up or powered down and I_{off} supports partial-power-down mode operation

The SN74CB3T3245 has a bidirectional data flow with near-zero propagation delay.

The SN74CB3T3245 has low ON-state resistance (r_{on}) characteristics ($r_{on} = 5 \Omega$ Typical)

The SN74CB3T3245 has both low input and output capacitance minimizes loading ($C_{io(OFF)} = 5 \text{ pF}$ Typical)

Data and control inputs provide undershoot clamp diodes.

The SN74CB3T3245 has low power consumption ($I_{CC} = 40 \mu\text{A}$ Maximum)

The SN74CB3T3245 has a V_{CC} operating range from 2.3 V to 3.6 V.

The data I/Os support 0- to 5-V signaling levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)

Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74CB3T3245.

Table 1. Function Table

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This application is specifically to connect a 5-V bus to a 3.3-V device. It is assumed that communication in this particular application is one-directional, going from the bus controller to the device.

9.2 Typical Application

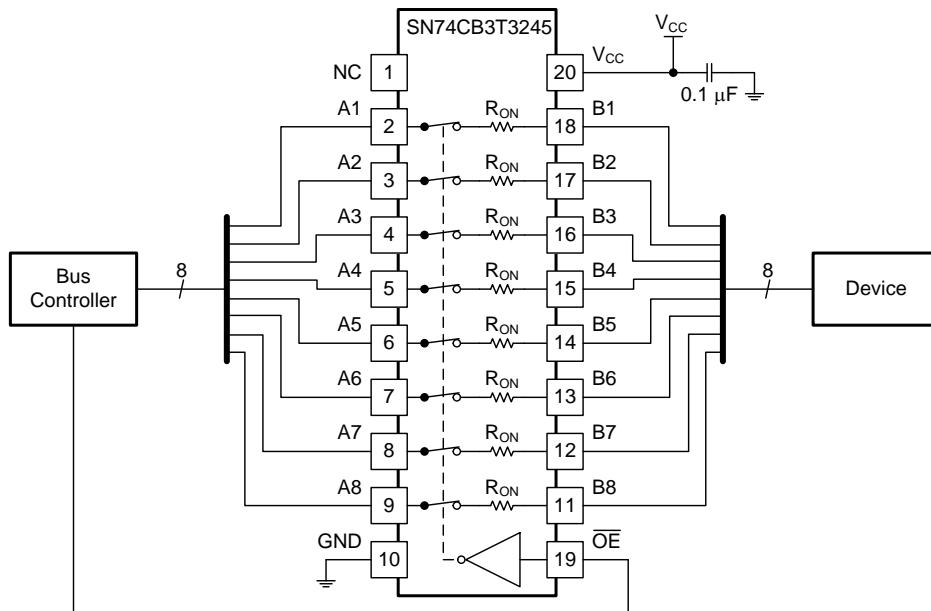


Figure 8. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

Because this design is for down-translating voltage, no pullup resistors are required.

9.2.2 Detailed Design Procedure

1. Recommended Input conditions
 - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*
 - Inputs are overvoltage tolerant allowing them to go as high as 7 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 128 mA on each channel

Typical Application (continued)

9.2.3 Application Curves

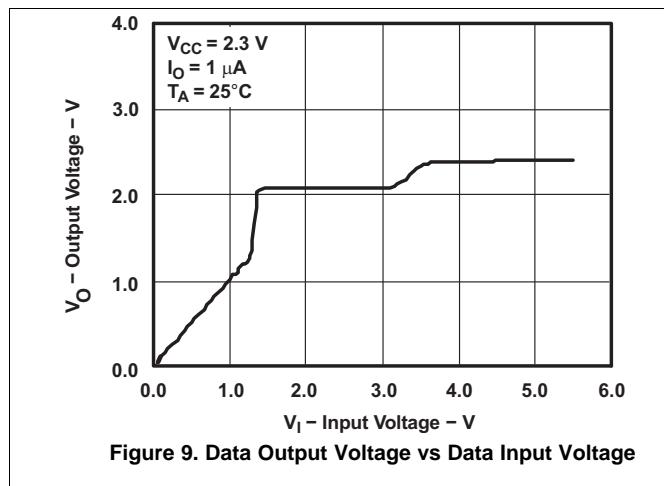


Figure 9. Data Output Voltage vs Data Input Voltage

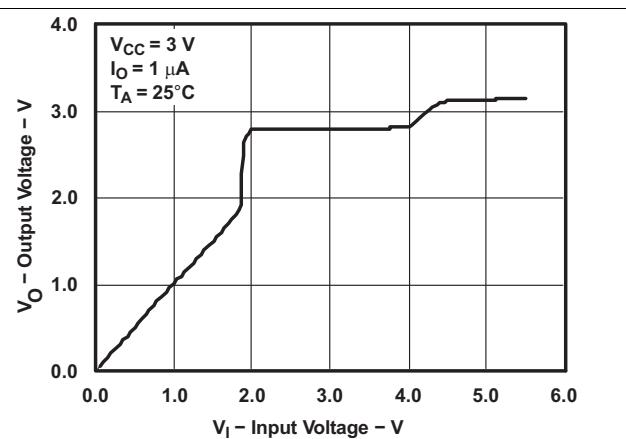


Figure 10. Data Output Voltage vs Data Input Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a $0.1\text{-}\mu\text{F}$ bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a $0.01\text{-}\mu\text{F}$ or $0.022\text{-}\mu\text{F}$ capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a $0.1\text{-}\mu\text{F}$ bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. $0.1\text{-}\mu\text{F}$ and $1\text{-}\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

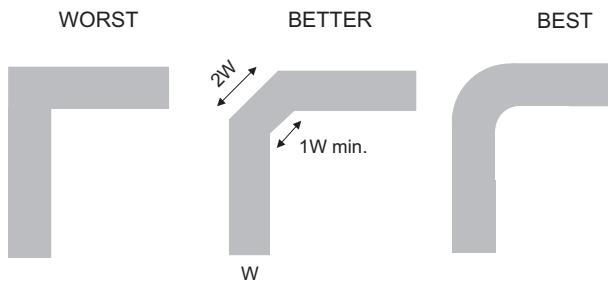


Figure 11. Trace Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

《CMOS 输入缓慢变化或悬空的影响》，[SCBA004](#)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 **TI 的工程师对工程师 (E2E) 社区**。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

[SLYZ022 — TI 术语表](#)。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3T3245DBQR	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245	Samples
SN74CB3T3245DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

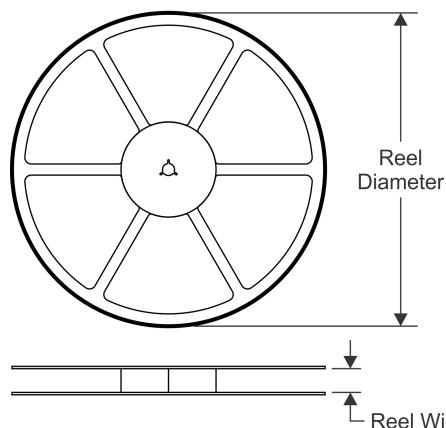
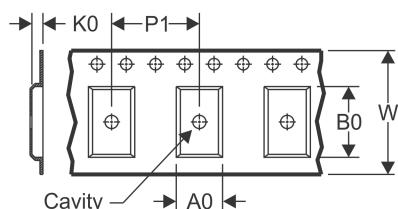
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

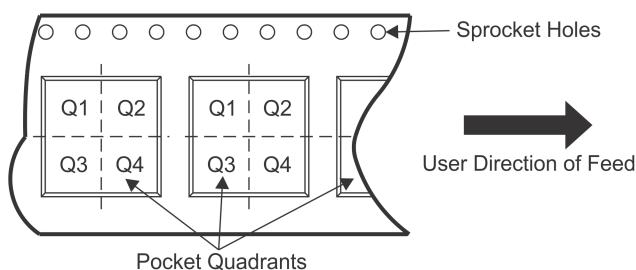
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


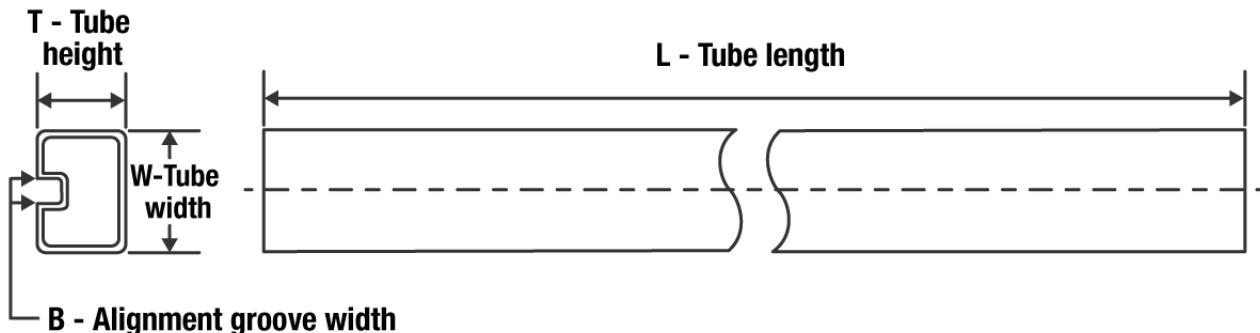
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CB3T3245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	853.0	449.0	35.0
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CB3T3245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74CB3T3245PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74CB3T3245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CB3T3245DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CB3T3245PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74CB3T3245PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

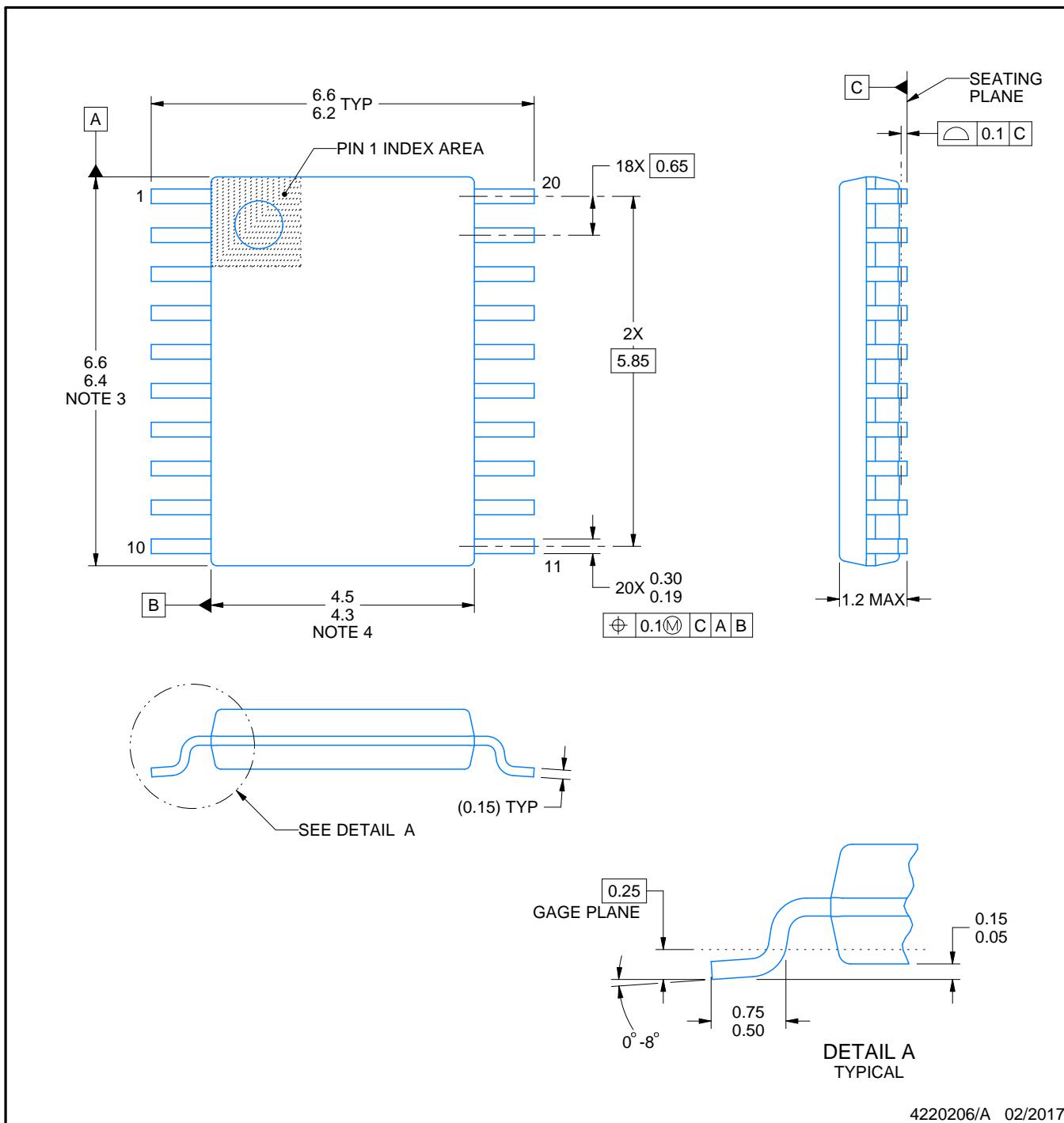
PACKAGE OUTLINE

PW0020A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

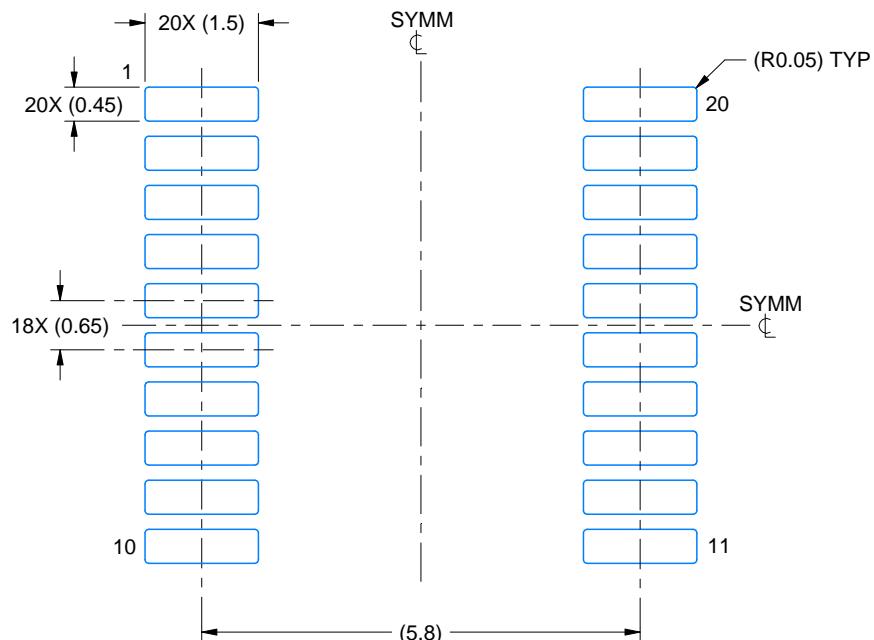
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

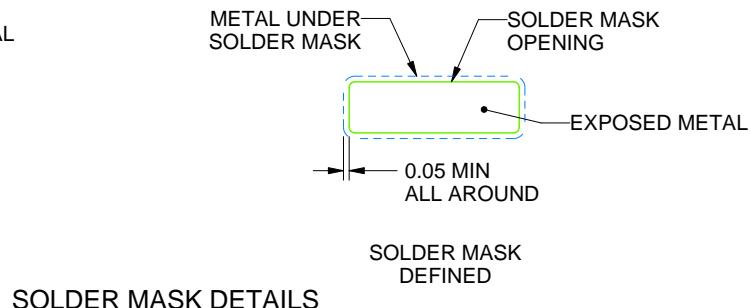
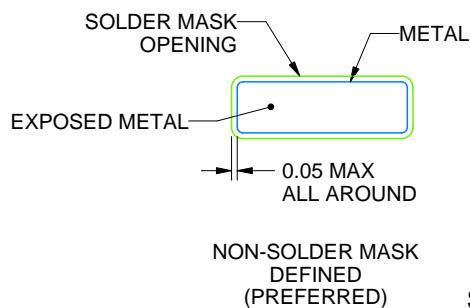
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

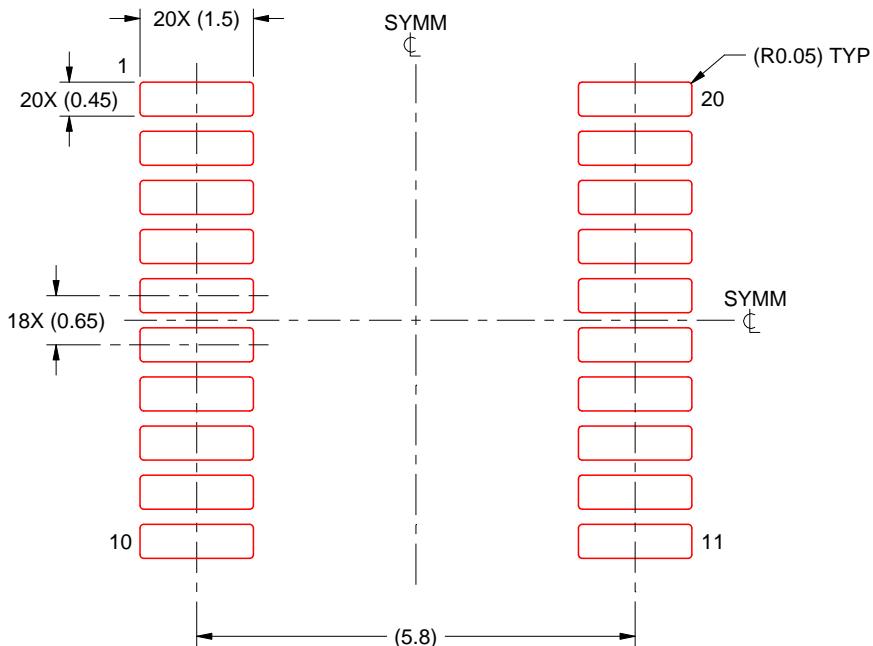
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

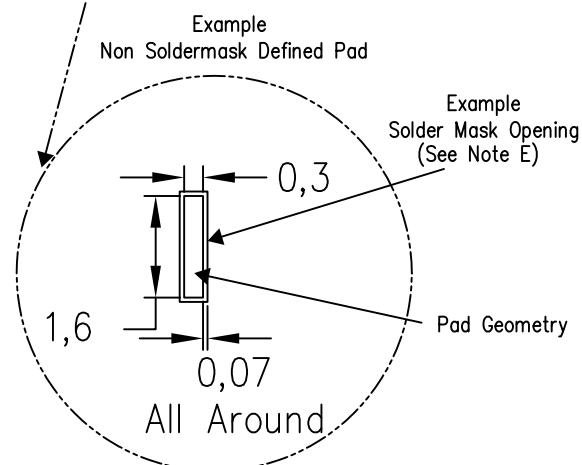
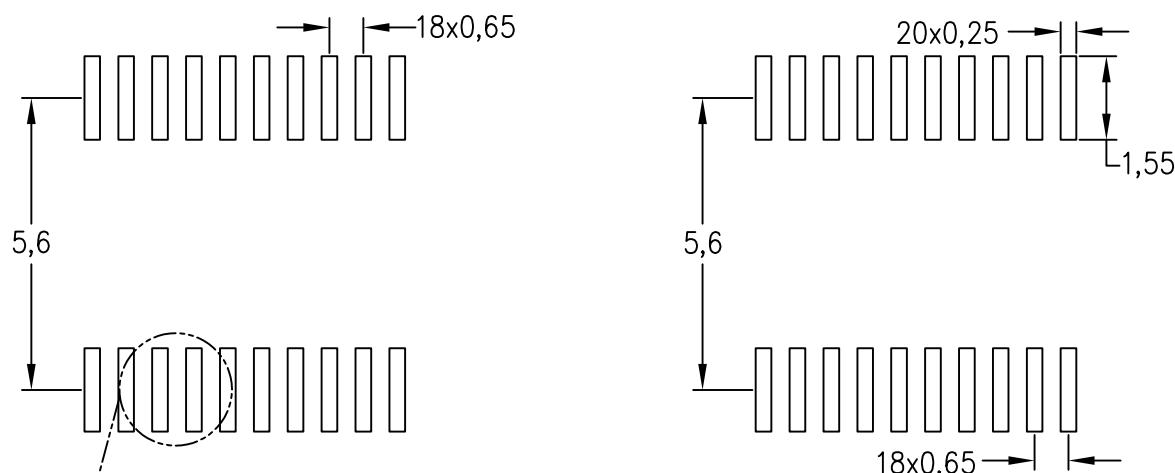
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

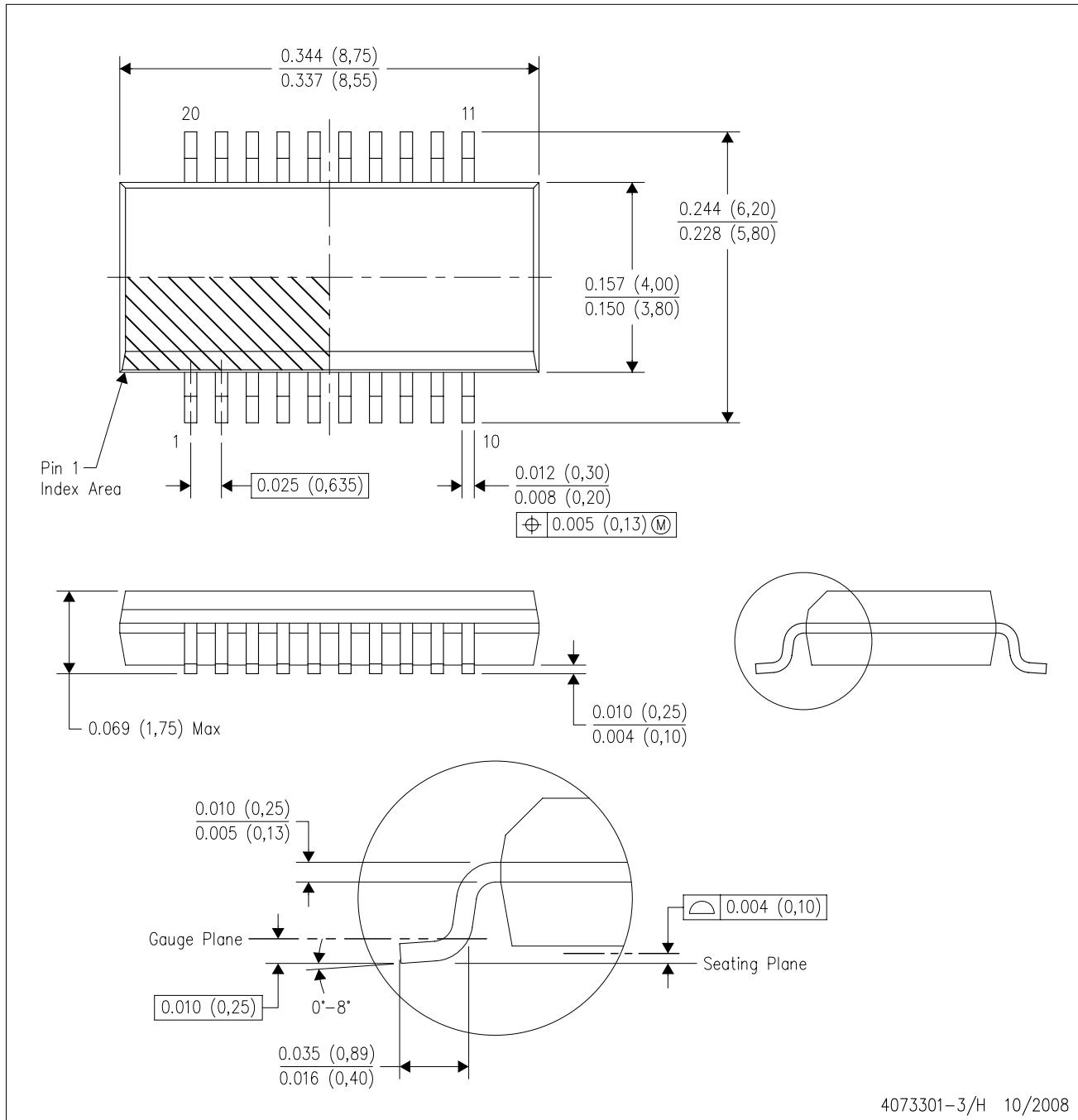
4211284-5/G 08/15

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



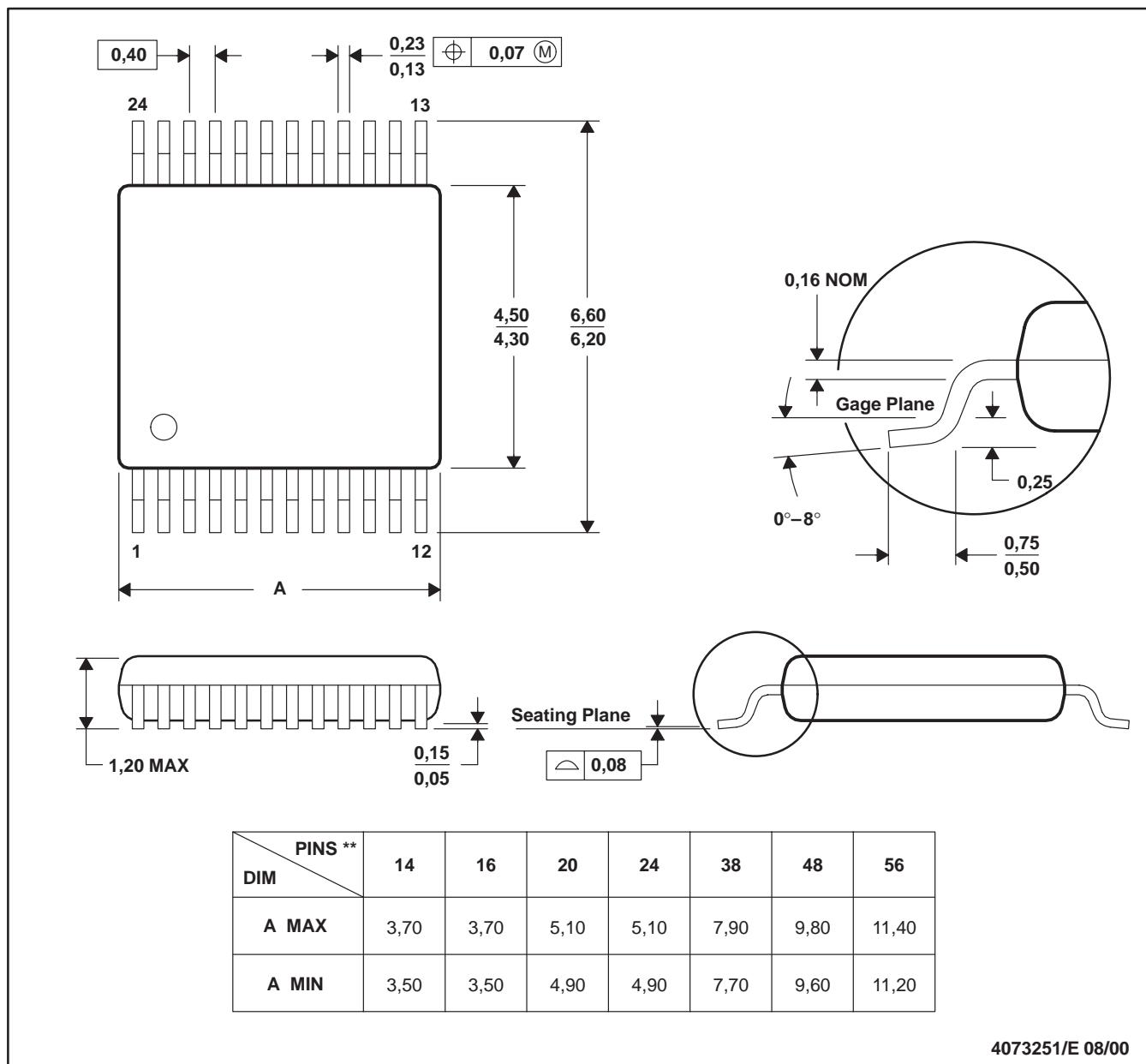
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- Falls within JEDEC MO-137 variation AD.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

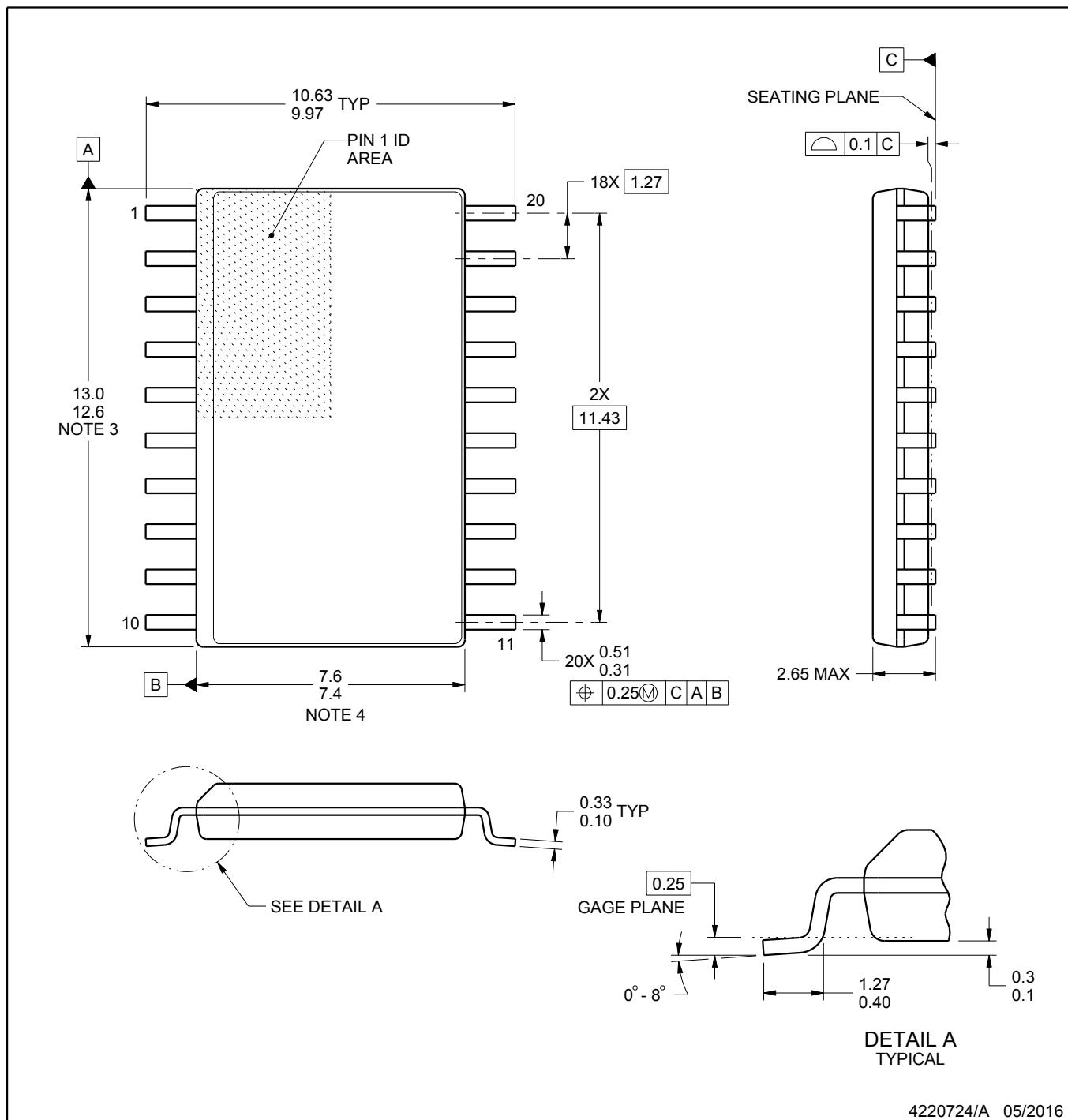


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIG



NOTES:

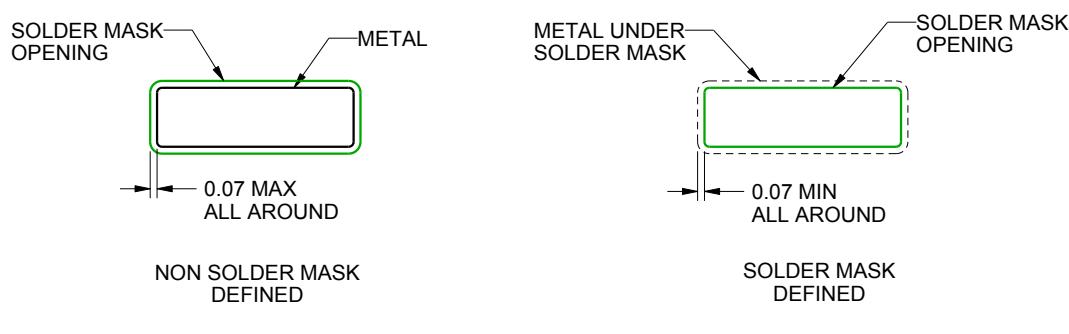
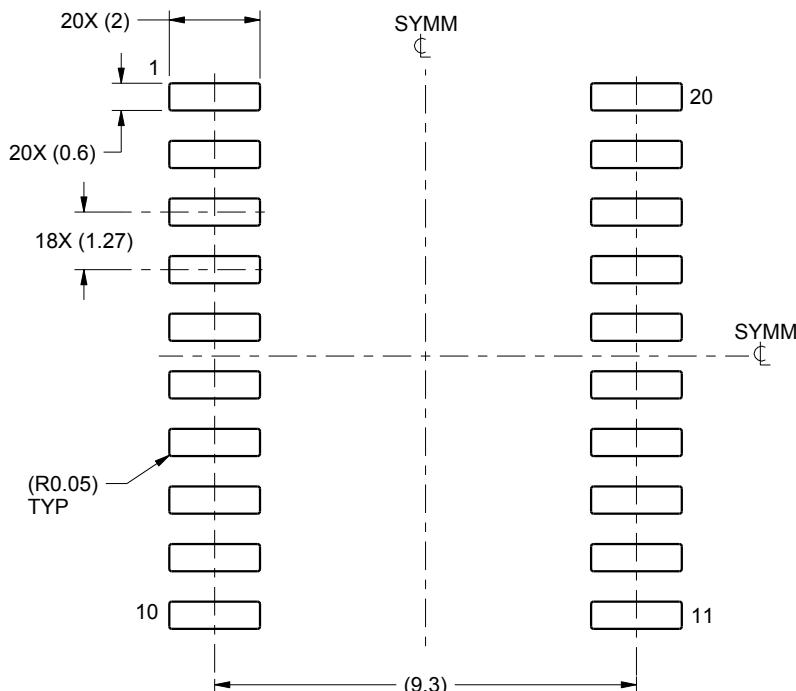
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

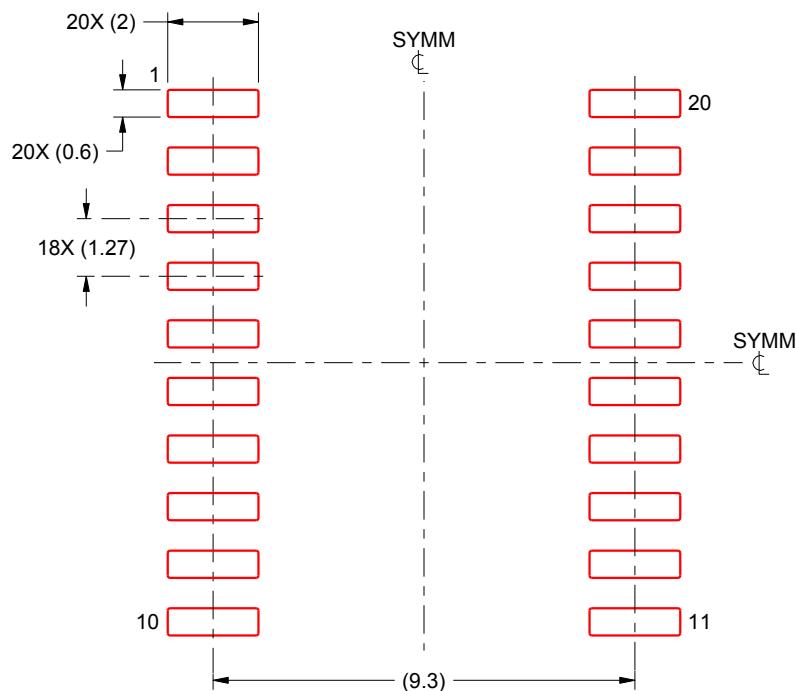
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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