14-BIT, 48-KSPS, DATA ACQUISITION SYSTEM WITH ANALOG-TO-DIGITAL CONVERTER, MUX, PGA, AND REFERENCE

FEATURES

- **PGA Gains: 1, 2, 4, 5, 8, 10, 16, 20 V/V**
- **Programmable Input (Up to 4-Channel Differential/Up to 8-Channel Single-Ended or Some Combination)**
- **1.15-V, 2.048-V, or 2.5-V Internal Reference**
- **SPI/DSP Compatible Serial Interface (≤ 20 MHz)**
- **Throughput Rate: 48 kSamples/sec**
- **Error Overload Indicator**
- **Programmable Output 2s Complement/Binary**
- **2.7-V to 5.5-V Single Supply Operation**
- **4-Bit Digital I/O Via Serial Interface**
- **Pin-Compatible With ADS7870**
- **SSOP-28 Package**

APPLICATIONS

- **Portable Battery-Powered Systems**
- **Low-Power Instrumentation**
- **Low-Power Control Systems**
- **Smart Sensor Applications**

DESCRIPTION

The ADS7871 (US patents 6140872, 6060874) is a complete low power data acquisition system on a single chip. It consists of a 4-channel differential/8-channel single-ended multiplexer, precision programmable gain amplifier, 14-bit successive approximation analog-to-digital (A/D) converter, and a precision voltage reference.

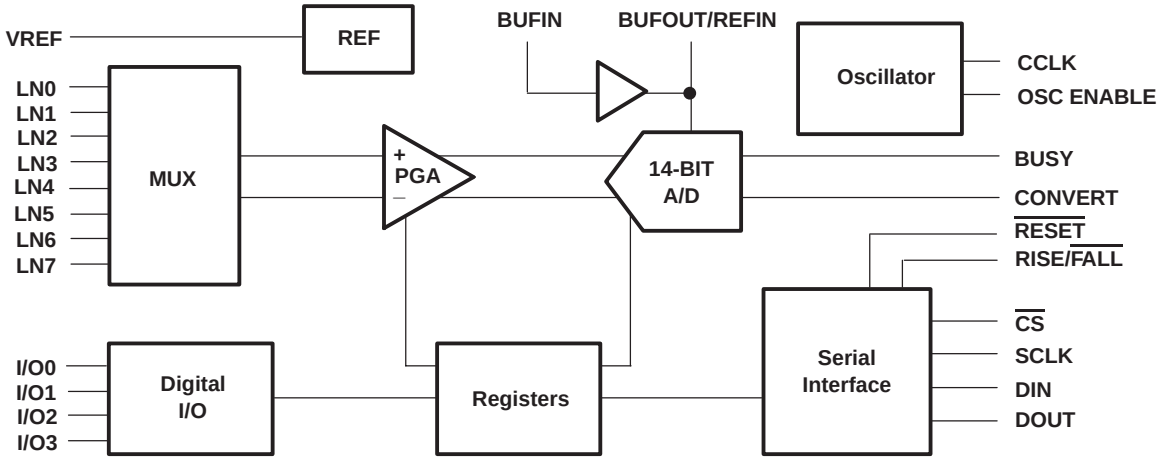
The programmable-gain amplifier provides high input impedance, excellent gain accuracy, good common-mode rejection, and low noise.

For many low-level signals, no external amplification or impedance buffering is needed between the signal source and the A/D input.

The offset voltage of the PGA is auto-zeroed. Gains of 1, 2, 4, 5, 8, 10, 16, and 20 V/V allow signals as low as 125 mV to produce full-scale digital outputs.

The ADS7871 contains an internal reference, which is trimmed for high initial accuracy and stability vs temperature. Drift is typically 10 ppm/°C. An external reference can be used in situations where multiple ADS7871s share a common reference.

The serial interface allows the use of SPI™, QSPI™, Microwire™, and 8051-family protocols, without glue logic.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7871	SSOP-28 Surface Mount	DB	−40°C to +85°C	ADS7871	ADS7871IDB	Rails, 48
				ADS7871	ADS7871IDBR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the package option addendum located at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
Supply voltage, V_{DD}			5.5 V
Analog inputs	Input current	Momentary	100 mA
		Continuous	10 mA
	Input voltage		V_{DD} + 0.5 V to GND − 0.5 V
Operating free-air temperature range, T_A			−40°C to 85°C
Storage temperature range, T_{STG}			−65°C to 150°C
Junction temperature (T_J max)			150°C
Lead temperature, (10 sec)			300°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

For the Total System (1), −40°C ≤ T_A ≤ 85°C, V_{DD} = 5 V, BUFIN = 2.5 V (using external reference), 2.5-MHz CCLK and 2.5-MHz SCLK (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
Input voltage (LNx inputs)		Linear operation	−0.2		V_{DD} + 0.2	V
Input capacitance (2)			4		9.7	pF
Input impedance (2)	Common mode			6		MΩ
	Differential			7		
Channel-to-channel crosstalk		V_I = 2 V_{PP}, 60 Hz (3)		100		dB
Maximum leakage current				100		pA
Static Accuracy						
Resolution				14		Bits
No missing codes		G = 1 to 20 V/V	13			Bits
Integral linearity		G = 1 to 20 V/V	−4	±2	4	LSB
Differential linearity		G = 1 to 20 V/V	−2	±0.5	4	LSB
Offset error		G = 1 to 20 V/V	−24	±1	24	LSB
Full-scale gain error	Ratiometric configuration or external reference (4)	G = 1 to 10 V/V	−0.2		0.2	%FSR
		G = 16 and 20 V/V	−0.25		0.25	%FSR
	Internal reference	G = 1 to 10 V/V	−0.35		0.35	%FSR
		G = 16 and 20 V/V	−0.4		0.4	%FSR
DC common-mode rejection ratio, RTI		V_I = −0.2 V to 5.2 V, G = 20 V/V		80		dB
Power supply rejection ratio, RTI		V_{DD} = 5 V ±10%, G = 20 V/V		88		dB
Dynamic Characteristics						
Throughput rate	Continuous mode	One channel			48	ksample/s
	Address mode	Different channels			48	
External clock, CCLK (5)			0.1		20	MHz
Internal oscillator frequency				2.5		MHz
Serial interface clock, SCLK					20	MHz
Data setup time			10			ns
Data hold time			10			ns
Digital Inputs						
Logic levels	Low-level input voltage, V_{IL}				0.8	V
	High-level input voltage, V_{IH}	V_{DD} ≤ 3.6 V	2			V
		V_{DD} > 3.6 V	3			V
	Low-level input current, I_{IL}				1	μA
	High-level input current, I_{IH}				1	

(1) The specifications for the total system are overall analog input to digital output specifications. The specifications for internal functions indicate the performance of the individual functions in the ADS7871.
(2) The ADS7871 uses switched capacitor techniques for the programmable gain amplifier and A/D converter. A characteristic of such circuits is that the input capacitance at any selected LNx pin changes during the conversion cycle.
(3) One channel on with its inputs grounded. All other channels off with sinewave voltage applied to their inputs.
(4) Ratiometric configuration exists when the input source is configured such that changes in the reference cause corresponding changes in the input voltage. The same accuracy applies when a perfect external reference is used.
(5) The CCLK is divided by the DF value specified by the contents of register 3, A/D Control register, bits D0 and D1 to produce DCLK. The maximum value of DCLK is 2.5 MHz.

ELECTRICAL CHARACTERISTICS

For the Total System (1), −40°C ≤ T_A ≤ 85°C, V_{DD} = 5 V, BUFIN = 2.5 V (using external reference), 2.5-MHz CCLK and 2.5-MHz SCLK (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Outputs						
Data coding		Binary 2s complement				
Logic levels	Low-level output voltage, V_{OL}	I_{SINK} = 5 mA			0.4	V
		I_{SINK} = 16 mA		0.8		
	High-level output voltage, V_{OH}	I_{SOURCE} = 0.5 mA	V_{DD} − 0.4			V
		I_{SOURCE} = 5 mA		4.6		
Leakage current		Hi-Z state, V_O = 0 V to V_{DD}			1	µA
Output capacitance				5		pF
Voltage Reference						
Bandgap voltage reference	V_{REF} = 2.048 V, 2.5 V	Pin 26 used as output, Use internal OSC or external CCLK as conversion clock	−0.25	±0.05	0.25	%FSR
	V_{REF} = 1.15 V			1.15		V
Output drive				±0.6		µA
Reference Buffer						
Input voltage, BUFIN			0.9		V_{DD} − 0.2	V
Input impedance, BUFIN		At pin 27		1000||3		GΩ||pF
Input offset			−10	±1	10	mV
Output voltage accuracy vs temperature, BUFOUT/REFIN (2) (3)		Pin 28 used as output, V_{REF} = 2.048 V and 2.5 V	−0.25	±0.05	0.25	%FSR
				10	50	ppm/°C
Output drive, BUFOUT/REFIN				20		mA
Power Supply Requirements						
Supply voltage			2.7		5.5	V
Power supply current (2)	1-kHz Sample rate	REF and BUF on, Internal oscillator on		1.2		mA
	48-kHz Sample rate	REF and BUF on, External CCLK		1.7	2	mA
	Power down	REF, BUF, Internal oscillator off			1	µA
Power dissipation (2)	1-kHz Sample rate	REF and BUF on, Internal oscillator on		6		mW
	48-kHz Sample rate	REF and BUF on, External CCLK		8.5	11	mW
	Power down	REF and BUF off			5	µW
Temperature Range						
Operating free-air			−40		85	°C
Storage range			−65		150	°C
Thermal resistance, Θ_{JA}				65		°C/W

(1) The specifications for the total system are overall analog input to digital output specifications. The specifications for internal functions indicate the performance of the individual functions in the ADS7871.

(2) REF and BUF contribute 190 µA and 150 µA (950 µW and 750 µW) respectively. At initial power up the default condition for both REF and BUF functions is power off. They can be turned on under software control by writing a 1 to D3 and D2 of register 7, REF/OSCILLATOR CONTROL register.

(3) For V_{DD} < 3 V, V_{REF} = 2.5 V is not usable.

ELECTRICAL CHARACTERISTICS

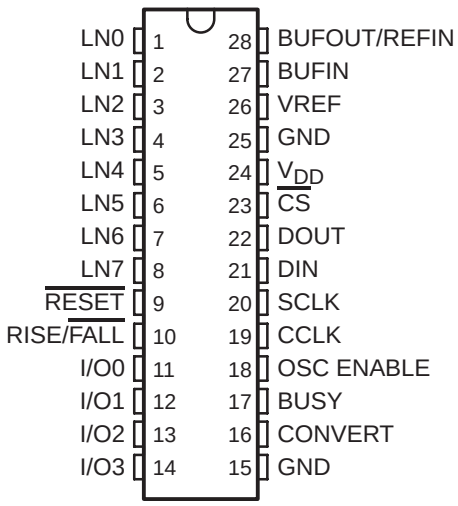
For Internal Functions (1), −40°C ≤ T_A ≤ 85°C, V_{DD} = 5 V, BUFIN = 2.5 V (using external reference), 2.5-MHz CCLK and 2.5-MHz SCLK (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multiplexer						
On resistance				100		Ω
Off resistance				1		GΩ
Off channel leakage current	On channel = 5.2 V, Off channel = 0 V	V_{LNx} = 5.2 V		100		pA
	On channel = 0 V, Off channel = 5.2 V			100		pA
On channel leakage current	On channel = 5.2 V, Off channel = 0 V			100		pA
	On channel = 0 V, Off channel = 5.2 V			100		pA
PGA Amplifier						
Offset voltage				100		μV
Small signal bandwidth				5/Gain		MHz
Settling time		G = 1		0.3		μs
		G = 20		6.4		μs
Analog-To-Digital Converter DC Characteristics						
Resolution				14		Bits
Integral linearity error				±2		LSB
Differential linearity error				±0.5		LSB
No missing codes				14		Bits
Offset error		REFIN = 2.5 V		±2		LSB
Full-scale (gain) error				±0.02		%
Common mode rejection, RTI of A/D				60		dB
Power supply rejection, RTI of ADS7871		External reference, V_{DD} = 5 V ±10%		60		dB
PGA Plus A/D Converter Sampling Dynamics		f_{CCLK} = 2.5 MHz, DF = 1				
Throughput rate		50 CCLK cycles		50		kHz
Conversion time		14 CCLK cycles		5.6		μs
Acquisition time		28 CCLK cycles		9.6		μs
Auto zero time		8 CCLK cycles		3.2		μs
Aperture delay		36 CCLK cycles		12.8		μs
Small signal bandwidth				5		MHz
Step response				1 Complete Conversion Cycle		

(1) The specifications for the total system are overall analog input to digital output specifications. The specifications for internal functions indicate the performance of the individual functions in the ADS7871.

PIN ASSIGNMENTS

SSOP-28 PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NO.	TERMINAL NAME	I/O	DESCRIPTION
1−8	LN0−LN7	AI	MUX input lines 0−7
9	$\overline{\text{RESET}}$	DI	Master reset, zeros all registers
10	RISE/$\overline{\text{FALL}}$	DI	Sets the active edge for SCLK. 0 sets SCLK active on falling edge. 1 sets SCLK active on rising edge.
11−14	I/O0−I/O3	DIO	Digital input or output signal
15	GND	−	Connect to ground. (This pin is grounded internally on the ADS7871. It has a weak pulldown on the ADS7870).
16	CONVERT	DI	0 to 1 transition starts a conversion cycle.
17	BUSY	DO	1 indicates converter is busy
18	OSC ENABLE	DI	0 sets CCLK as an input, 1 sets CCLK as an output and turns the oscillator on.
19	CCLK	DIO	If OSC ENABLE = 1, then the internal oscillator is output to this pin. If OSC ENABLE = 0, then this is the input pin for an external conversion clock.
20	SCLK	DI	Serial data input/output transfer clock. Active edge set by the RISE/$\overline{\text{FALL}}$ pin. If RISE/$\overline{\text{FALL}}$ is low, SCLK is active on the falling edge.
21	DIN	DIO	Serial data input. In the 3-wire mode, this pin is used for serial data input. In the 2-wire mode, serial data output appears on this pin as well as the DOUT pin.
22	DOUT	DO	Serial data output. This pin is driven when $\overline{\text{CS}}$ is low and is high impedance when $\overline{\text{CS}}$ is high. This pin behaves the same in both 3-wire and 2-wire modes.
23	$\overline{\text{CS}}$	DI	Chip select. When $\overline{\text{CS}}$ is low, the serial interface is enabled. When $\overline{\text{CS}}$ is high, the serial interface is disabled, the DOUT pin is high impedance, and the DIN pin is an input. The $\overline{\text{CS}}$ pin only affects the operation of the serial interface. It does not directly enable/disable the operation of the signal conversion process.
24	V_{DD}	−	Power supply voltage, 2.7 V to 5.5 V
25	GND	−	Power supply ground
26	VREF	AO	2.048-/2.5-V on-chip voltage reference
27	BUFIN	AI	Input to reference buffer amplifier
28	BUFOUT/REFIN	AIO	Output from reference buffer amplifier and reference input to ADC

TYPICAL PERFORMANCE CURVES

GAIN ERROR vs FREE-AIR TEMPERATURE

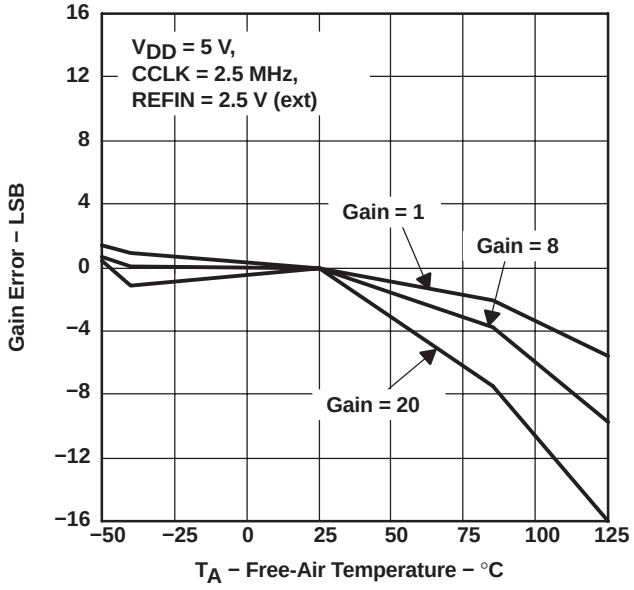


Figure 1

OFFSET ERROR vs FREE-AIR TEMPERATURE

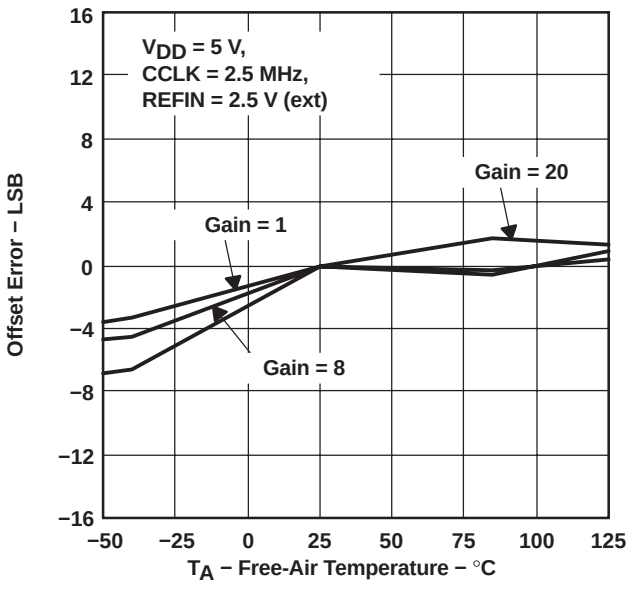


Figure 2

VOLTAGE REFERENCE ERROR vs FREE-AIR TEMPERATURE

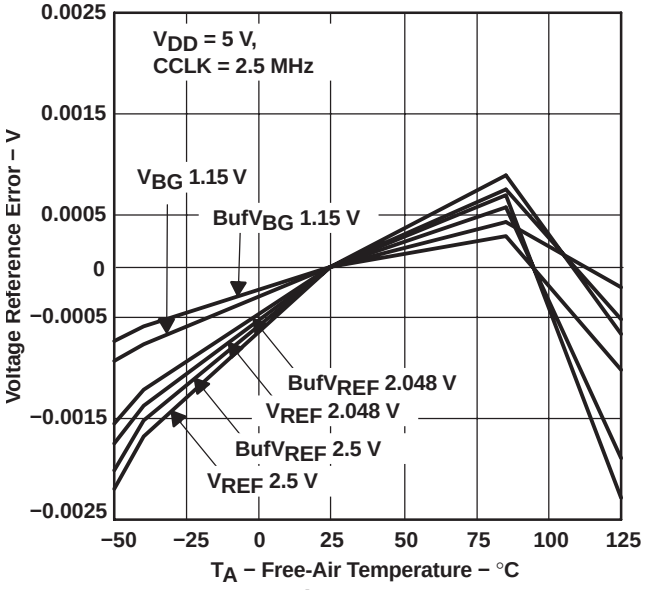


Figure 3

INTERNAL OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

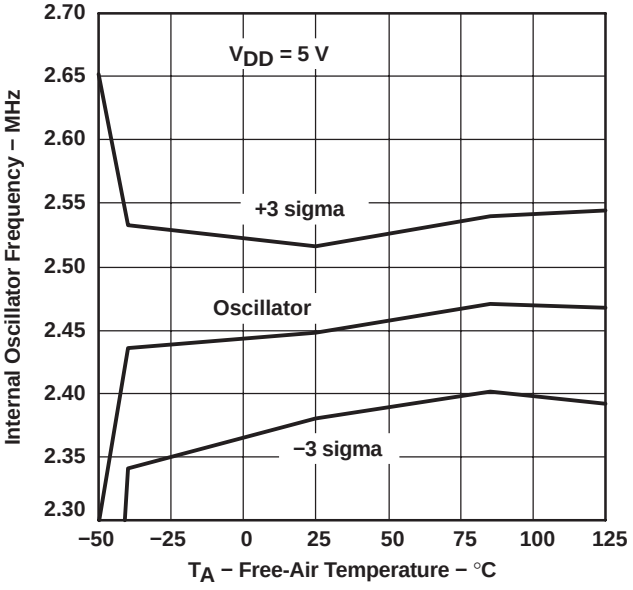


Figure 4

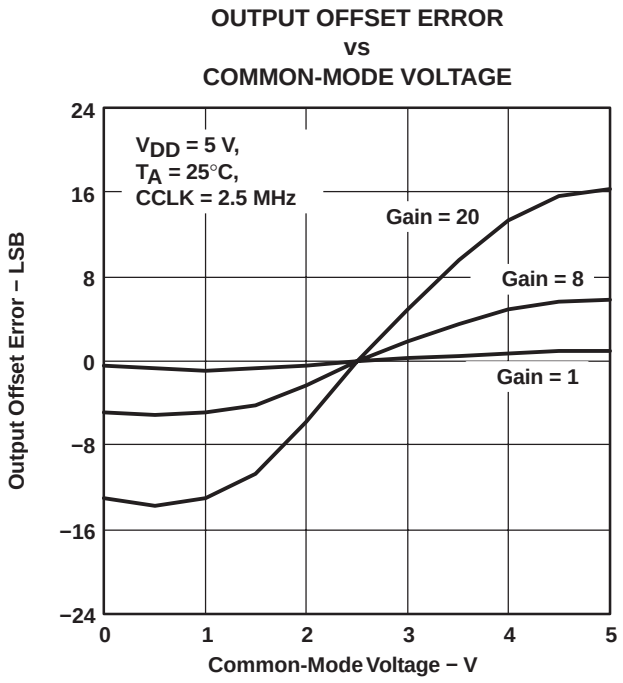


Figure 5

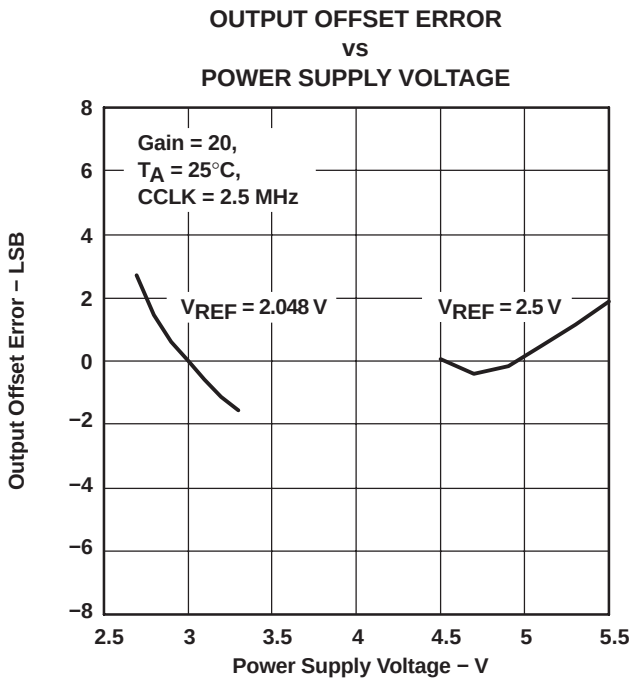


Figure 6

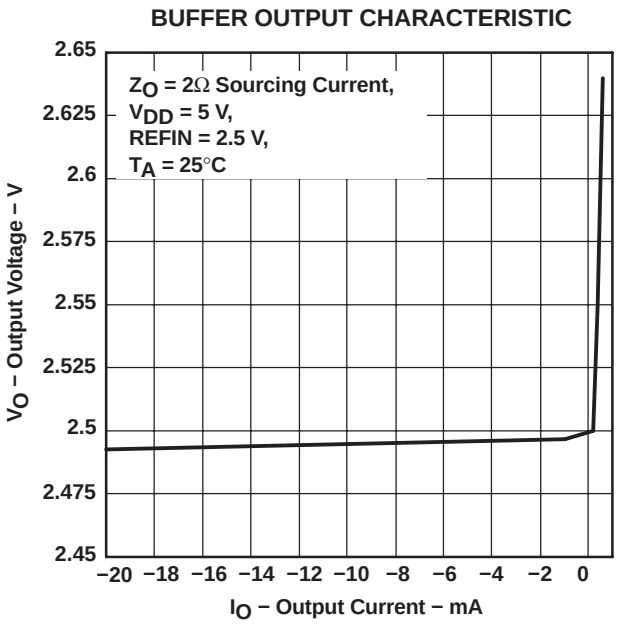


Figure 7

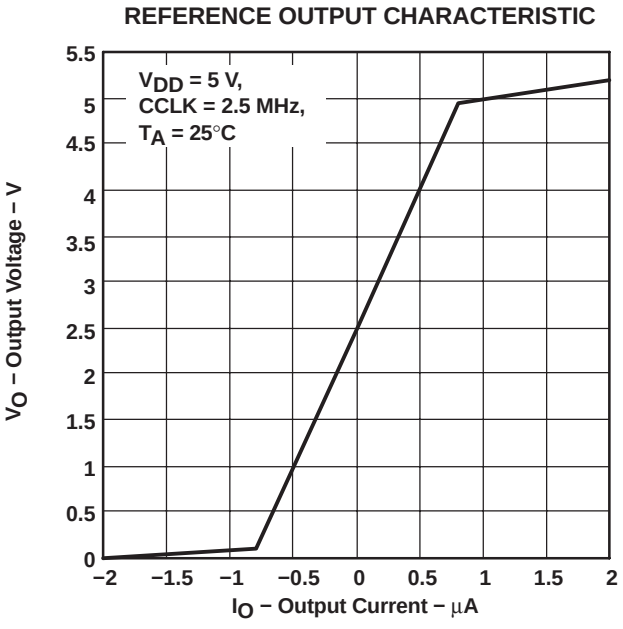


Figure 8

TYPICAL INPUT RANGE

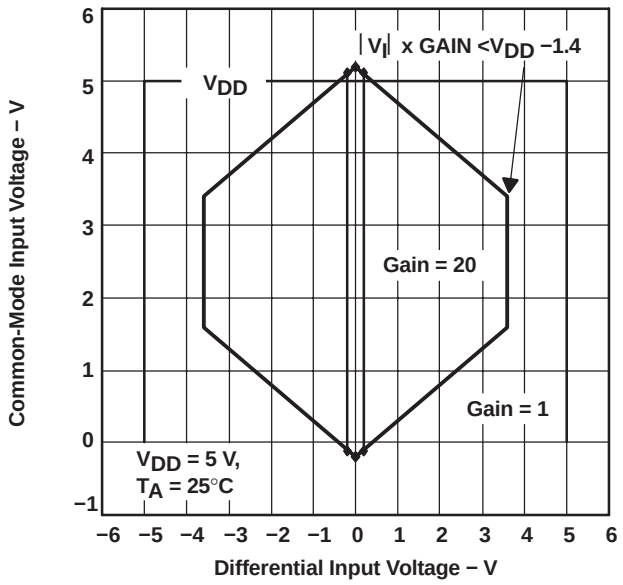


Figure 9

PGA OUTPUT

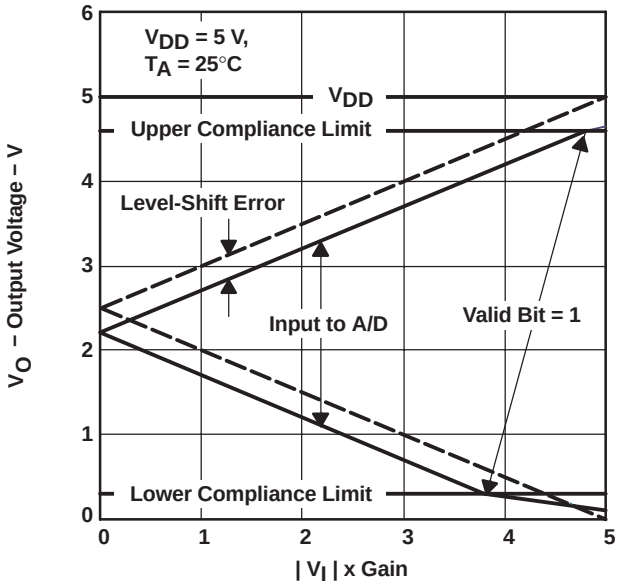


Figure 10

QUIESCENT CURRENT vs SAMPLING RATE

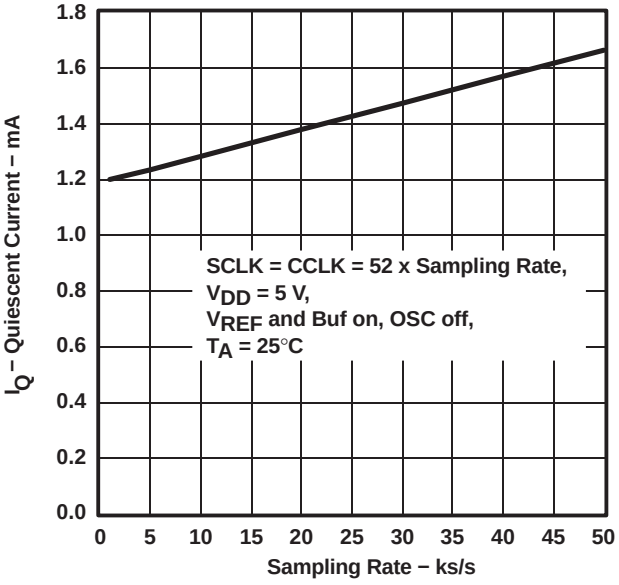


Figure 11

NOISE AND EFFECTIVE NUMBER OF BITS vs PGA GAIN

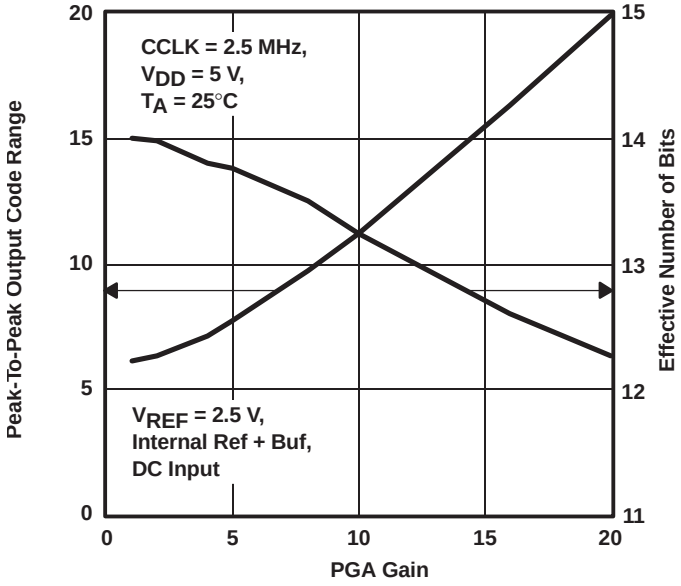


Figure 12

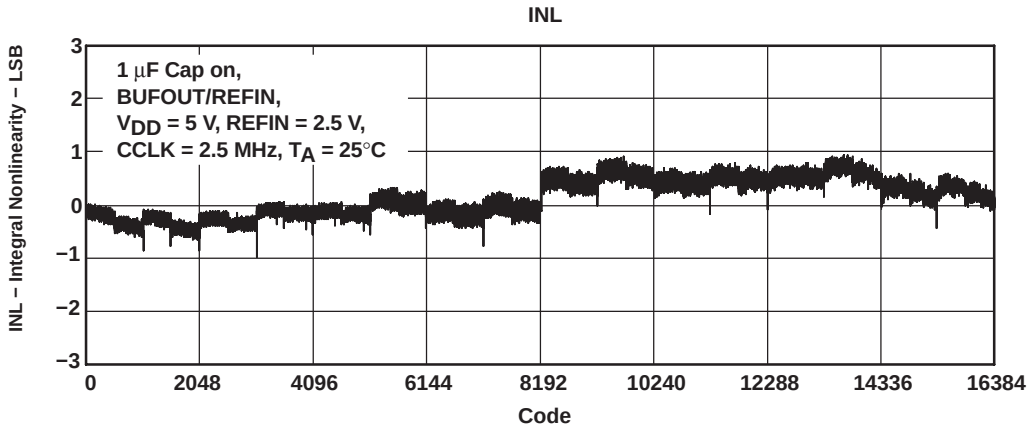


Figure 13

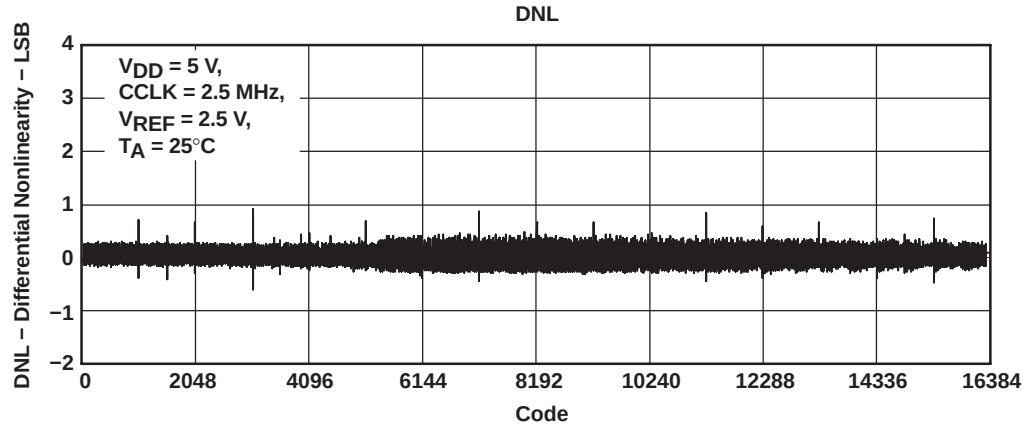


Figure 14

OVERVIEW

The ADS7871 is a complete data acquisition device composed of an input analog multiplexer (MUX), a programmable gain amplifier (PGA) and an analog-to-digital converter (A/D). Four lines of digital input/output (I/O) are also provided. Additional circuitry provides support functions including conversion clock, voltage reference, and serial interface for control and data retrieval.

The ADS7871 is based on the ADS7870 and shares the same interface, functionality, and pinout. The exceptions are: pin 15 is now hard-wired to ground; the SAR conversion cycle takes 14 clocks rather than 12; and the output data has only one defined zero at bit D1 (of Register 0), as opposed to three defined zeroes at bits D1, D2, and D3 (of Register 0) as in the ADS7870.

Control and configuration of the ADS7871 is accomplished by command bytes written to internal registers through the serial port. Command Register device control includes MUX channel selection, PGA gain, A/D start conversion command, and I/O line control. Command register configuration control includes internal voltage reference setting and oscillator control.

Operational modes and selected functions can be activated by digital inputs at corresponding pins. Pin settable configuration options include SCLK active-edge selection, master reset, and internal oscillator clock enable.

The ADS7871 has eight analog signal input pins, LN0 through LN7. These pins are connected to a network of analog switches (the MUX block). The inputs can be configured as 8 single-ended or 4 differential inputs, or some combination.

The four general-purpose digital I/O pins (I/O3 through I/O0) can be made to function individually as either digital inputs or digital outputs. These pins give the user access to four digital I/O pins through the serial interface without having to run additional wires to the host controller.

The programmable gain amplifier (PGA) provides gains of 1, 2, 4, 5, 8, 10, 16, and 20 V/V.

The 14-bit A/D converter in the ADS7871 is a successive approximation type. The default output of the converter is 2s complement format and can be read in a variety of ways depending on the program configuration.

The ADS7871 internal voltage reference can be software configured for output voltages of 1.15 V, 2.048 V, or 2.5 V. The reference circuit is trimmed for high initial accuracy and low temperature drift. A separate buffer amplifier is provided to buffer the high impedance VREF output.

The voltage reference, PGA, and A/D converter use the conversion clock (CCLK) and signals derived from it. CCLK can be either an input or output signal. The ADS7871 can divide the CCLK signal by a constant before it is applied to the A/D converter and PGA. This allows a higher frequency system clock to be used to control the A/D converter operation. Division factors (DF) of 1, 2, 4, and 8 are available. The signal that is actually applied to the PGA and A/D converter is DCLK, where DCLK = CCLK/DF.

The ADS7871 is designed so that its serial interface can be conveniently used with a wide variety of microcontrollers. It has four conventional serial interface pins: SCLK (serial data clock), DOUT (serial data out), DIN (serial data in, which may be set bidirectional in some applications), and $\overline{CS}$ (chip select function).

The ADS7871 has ten internal user accessible registers which are used in normal operation to configure and control the device (summarized in Figure 18).

FUNCTIONAL DESCRIPTION

Multiplexer

The ADS7871 has eight analog signal input pins, LN0 through LN7. These pins are connected to a network of analog switches (the MUX block in the block diagram). The switches are controlled by four bits in the Gain/Mux register.

LN0 through LN7 can be configured as 8 single-ended inputs or 4 differential inputs or some other combination. Some MUX combination examples are shown in Figure 23. The differential polarity of the input pins can be changed with the M2 bit in the MUX address. This feature allows reversing the polarity of the conversion result without having to physically reverse the input connections to the ADS7871.

For linear operation, the input signal at any of the LN0 through LN7 pins can range between GND – 0.2 V and V_{DD} + 0.2 V. The polarity of the differential signal can be changed through commands written to the Gain/Mux register, but each line must remain within the linear input common mode voltage range.

Inputs LN0 through LN7 have ESD protection circuitry as the first active elements on the chip. These contain protection diodes connected to VDD and GND that remain reverse biased under normal operation. If input voltages are expected beyond the absolute maximum voltage range, it is necessary to add resistance in series with the input to limit the current to 10 mA or less.

Conversion Clock

The conversion clock (CCLK) and signals derived from it are used by the voltage reference, the PGA, and the A/D converter. The CCLK pin can be made either an input or an output. For example, one ADS7871 can be made to be the conversion clock master (CCLK is an output), while the others are slaved to it with their CCLK pins all being inputs (by default). This can reduce A/D conversion errors caused by multiple clocks and other systems noise.

When the OSC ENABLE pin is low or zero, the CCLK pin is an input and the ADS7871 relies on an applied external clock for the conversion process. When OSC ENABLE is high or if the OSCE bit D4 in register 7 is set to a one, the internal oscillator and an internal buffer is enabled, making pin 19 an output. Either way the CCLK is sensed internally at the pin so all ADS7871s see the same clock delays. Capacitive loading on the CCLK pin can draw significant current compared with the supply current to the ADS7871 ($I_{LOAD} = f_{CCLK} \times V_{DD} \times C_{LOAD}$).

The internal reference requires a continuous clock and may be supplied by the internal oscillator independently of the system clock driving the CCLK pin. Setting OSCR (bit D5 in register 7) and REFE (bit D3 in register 7) both to one accomplishes this. Figure 11 illustrates all of these relationships.

The ADS7871 utilizes the power saving technique of turning on and off the biasing for the PGA and A/D as needed. This does not apply to the oscillator, reference, and buffer, these run continuously when enabled. The buffer output is high impedance when disabled, so for a low power data logging application the filter capacitor is not discharged when the buffer is turned off and does not require as much settling time when turned on.

The serial interface clock is independent of the conversion clock and can run faster or slower. If it is desirable to use a faster system clock than the 2.5-MHz nominal rate that the ADS7871 uses then this clock may be divided to a slower rate (1/2, 1/4, 1/8) by setting the appropriate bits in register 3. This clock divider applies equally to an external as well as internal clock to create the internal DCLK for the PGA and A/D conversion cycle.

The ADS7871 has both maximum and minimum DCLK frequency constraints (DCLK = CCLK/DF). The maximum DCLK is 2.5 MHz. The minimum DCLK frequency applied to the PGA, reference, and A/D is 100 kHz.

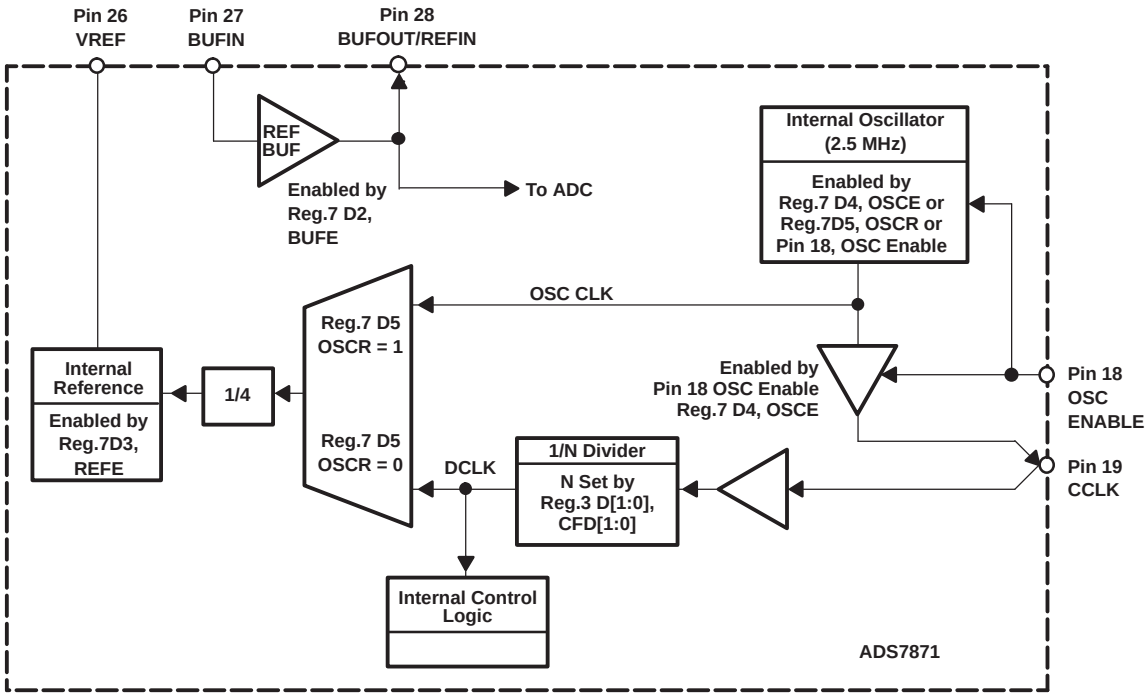


Figure 15. Block Diagram With Internal and External Clocks and References

Voltage Reference and Buffer Amplifier

The ADS7871 uses a patented switched capacitor implementation of a band-gap reference. The circuit has curvature correction for drift and can be software configured for output voltages of 1.15 V, 2.048 V, or 2.5 V (default). The internal reference output (VREF) is not designed to drive a typical load; a separate buffer amplifier must be used to supply any load current.

The internal reference buffer (REFBUF) can source many tens of milliamps to quickly charge a filter capacitor tied to its output, but it can only typically sink 200 μA. If there is any significant noise on the REFIN pin, then a resistor to ground (≥ 250 Ω) would improve the buffers ability to recover from a positive going noise spike. This would, of course, be at the expense of power dissipation.

The temperature compensation of the onboard reference is adjusted with the reference buffer in the circuit. Performance is specified in this configuration.

Programmable Gain Amplifier

The programmable gain amplifier (PGA) provides gains of 1, 2, 4, 5, 8, 10, 16, and 20 V/V. The PGA is a single supply, rail-to-rail input, auto-zeroed, capacitor based instrumentation amplifier. PGA gain is set by bits G2 through G0 of register 4.

The ability to detect when the PGA outputs are driven to clipping, or nonlinear operation, is provided by the least significant bit of the output data (register 0) being set to one. This result is the logical OR of fault detecting comparators within the ADS7871 monitoring the outputs of the PGA. The inputs are also monitored, for problems, often due to ac common mode or low supply operation and ORed to this OVL bit. Register 2 can be read to determine what fault conditions existed during the conversion. An illustration of how the OVL bit could be set without having reached the maximum output code of the A/D converter is shown in Figure 10. The OVL bit also facilitates a quick test to allow for an auto-ranging application, indicating to the system controller it should try reducing the PGA gain.

A/D Converter

The 14-bit A/D converter in the ADS7871 is a successive approximation type. The output of the converter is 2s complement format and can be read through the serial interface MSB first or LSB first. A plot of output codes vs input voltage is shown in Figure 16. With the input multiplexer configured for differential input, the A/D transfer function is:

$$-8192 \le \text{Code} \le 8191 \text{ for } \frac{-V_{REF}}{G} \le V_{IN} \le \frac{V_{REF} - 1\ \text{LSB}}{G} \quad (1)$$

With the input multiplexer configured for single-ended inputs, the A/D transfer function is:

$$0 \le \text{Code} \le 8191 \text{ for } 0 \le V_{IN} \le \frac{V_{REF} - 1\ \text{LSB}}{G} \quad (2)$$

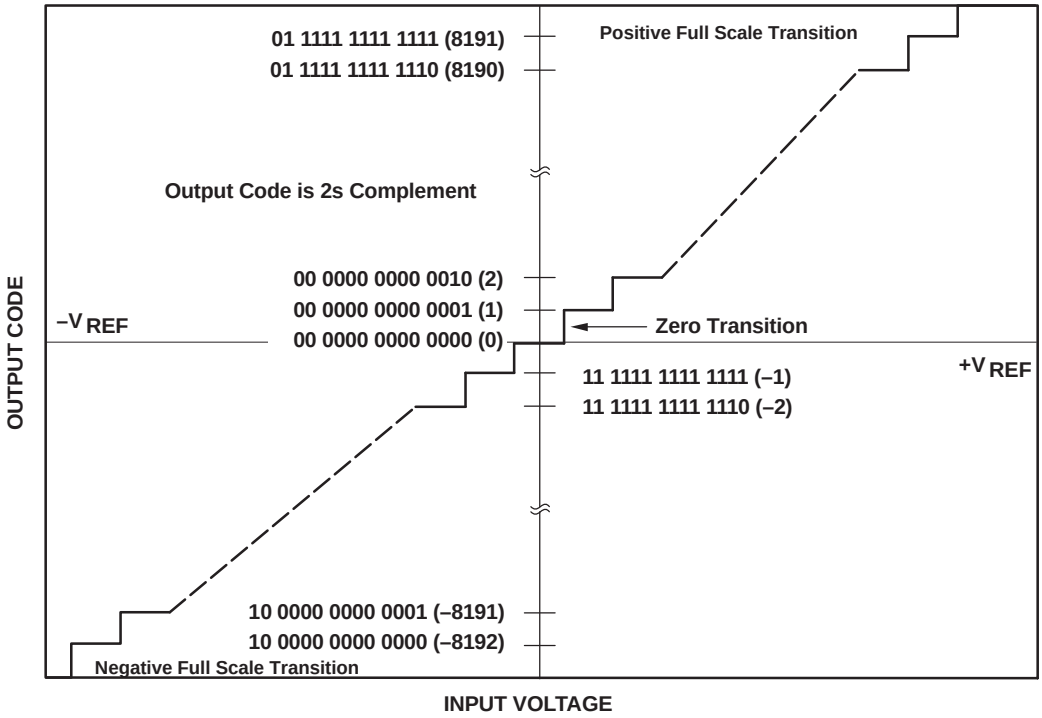


Figure 16. Output Codes Versus Input Voltage

Conversion Cycle

A conversion cycle requires 50 DCLKs, where DCLK = CCLK/DF, the divided-down clock. Operation of the PGA requires 36 DCLKs: capture the input signal, auto-zero the PGA, level-shift and amplify the input signal. The period of this cycle makes certain the settling time is sufficient for gain = 20 and (source impedance of 2 kΩ or less) even if the gain is less than 20. The SAR converter takes the last 14 DCLKs.

For maximum sampling rate the input command and output data must be communicated during this cycle, although this is not recommended for best performance.

During the conversion cycle the internal capacitive load at the selected MUX input changes between 6 pF and 9.7 pF. When the ADS7871 is not converting, the MUX inputs have a nominal 4-pF load capacitance.

The source impedance of the input causes the voltage to vary on the DCLK transitions as the internal capacitors are switched in and out. A 10-nF to 100-nF capacitor across the differential inputs helps filter these glitches and act as an antialias filter in combination with the source impedance. Source impedance greater than 2 kΩ requires longer settling times and so the CCLK should be reduced accordingly.

For minimum power dissipation, the bias needed for each function is turned on, allowed to settle, and run only for the duration required for each conversion. Low rate data logging applications can capitalize on this by utilizing the internal oscillator as needed rather than running a slow system clock.

Starting an A/D Conversion Cycle

There are four ways to cause the ADS7871 to perform a conversion:

1. Send a direct mode instruction.
2. Write to register 4 with the CNV bit = 1
3. Write to register 5 with the CNV bit = 1

} The next conversion queues up, waiting for the current conversion to complete

4. Assert the CONVERT pin (logic high) — A new conversion cycle starts at the second active edge of CCLK

Serial Interface

The ADS7871 communicates with microprocessors and other external circuitry through a digital serial port interface. It is compatible with a wide variety of popular microcontrollers and digital signal processors (DSP). These include TI's TMS320, MSC1210, and MSP430 product families. Other vendors products such as Motorola 68HC11, Intel 80C51, and MicroChip PIC Series are also supported.

The serial interface consists of four primary pins, SCLK (serial bit clock), DIN (serial data input), DOUT (serial data output) and $\overline{CS}$ (chip select). SCLK synchronizes the data transfer with each bit being transmitted on the falling or rising SCLK edge as determined by the RISE/$\overline{FALL}$ pin. SDIN may also be used as a serial data output line.

Additional pins expand the versatility of the basic serial interface and allow it to be used with different microcontrollers. The BUSY pin indicates when a conversion is in progress and may be used to generate interrupts for the microcontroller. The CONVERT pin can be used as a hardware-based method of causing the ADS7871 to start a conversion cycle. The $\overline{RESET}$ pin can be toggled in order to reset the ADS7871 to the power-on state.

Communication through the serial interface is dependent on the microcontroller providing an instruction byte followed by either additional data (for a write operation) or just additional SCLKs to allow the ADS7871 to provide data (for a read operation). Special operating modes for reducing the instruction byte overhead for retrieving conversion results are available.

Reset of device ($\overline{RESET}$), start of conversion (CONVERT), and oscillator enable (OSC ENABLE) can be done by signals to external pins or entries to internal registers. The actual execution of each of these commands is a logical OR function; either pin or register signal TRUE causes the function to execute. The CONVERT pin signal is an edge-triggered event, with a hold time of two CCLK periods for debounce.

Operating Modes

The ADS7871 serial interface operates based on an instruction byte followed by an action commanded by the contents of that instruction. The 8-bit instruction word is clocked into the DIN input. There are two types of instruction bytes that may be written to the ADS7871 as determined by bit D7 of the instruction word (see Figure 17). These two instructions represent two different operating modes. In direct mode (bit D7 = 1), a conversion is started. A register mode (bit D7 = 0) instruction is followed by a read or write operation to the specified register.

INSTRUCTION BYTE

	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
Start Conversion (Direct Mode)	1	G2	G1	G0	M3	M2	M1	M0
				OR				
Read/Write (Register Mode)	0	R/$\overline{W}$	16/$\overline{8}$	A4	A3	A2	A1	A0

START CONVERSION INSTRUCTION BYTE (Direct Mode)(1)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7		Mode select	1	Starts a conversion cycle (direct mode)
D6−D4	G2−G0	PGA gain select	000 001 010 011 100 101 110 111	PGA Gain = 1 (power up default condition) PGA Gain = 2 PGA Gain = 4 PGA Gain = 5 PGA Gain = 8 PGA Gain = 10 PGA Gain = 16 PGA Gain = 20
D3−D0	M3−M0	Input channel select	See Figure 24	Determines input channel selection for the requested conversion, differential or single-ended configuration.

(1) The seven lower bits of this byte are also written to register 4, the Gain/Mux register.

READ/WRITE INSTRUCTION BYTE (Register Mode)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7		Mode Select	0	Initiates a read or write operation (register mode)
D6	R/$\overline{W}$	Read/Write Select	0 1	Write operation Read operation
D5	16/$\overline{8}$	Word Length	0 1	8-Bit word 16-Bit word (2 8-bit bytes)
D4−D0	AS4−AS0	Register Address	See Figure 18	Determines the address of the register that is to be read from or written to

Figure 17. Instruction Byte Addressing

Direct Mode

In direct mode a conversion is initiated by writing a single 8-bit instruction byte to the ADS7871 (bit D7 is set to 1). Writing the direct mode command sets the configuration of the multiplexer, selects the gain of the PGA, and starts a conversion cycle. After the last bit of the instruction byte is received, the ADS7871 performs a conversion on the selected input channel with the PGA gain set as indicated in the instruction byte.

The conversion cycle begins on the second falling edge of DCLK after the eighth active edge of SCLK of the instruction byte. When the conversion is complete, the conversion result is stored in the A/D Output registers and is available to be clocked out of the serial interface by the controlling device using the READ operation in the register mode.

The structure of the instruction byte for direct mode is shown in Figure 17.

- D7: This bit is set to 1 for direct mode operation
- D6 through D4 (G2 − G0): These bits control the gain of the programmable gain amplifier. PGA gains of 1, 2, 4, 5, 8, 10,16, and 20 are available. The coding is shown in Figure 17.
- D3 through D0 (M3 − M0): These bits configure the switches that determine the input channel selection. The input channels may be placed in either differential or single-ended configurations. In the case of differential configuration, the polarity of the input signal is reversible. The coding is shown in Figure 27.

Note that the seven lower bits of this byte are written to register 4, the Gain/Mux register.

All other controllable ADS7871 parameters are values previously stored in their respective registers. These values are either the power-up default values (0) or values that were previously written to one of the control registers in a register mode operation. No additional data is required for a direct mode instruction.

Register Mode

In register mode (bit D7 of the instruction byte is 0) a read or write instruction to one of the ADS7871 registers is initiated. All of the user determinable functions and features of the ADS7871 can be controlled by writing information to these registers (see Figure 21). Conversion results can be read from the A/D Output registers.

REGISTER ADDRESS					ADDR NO.	READ/ WRITE	REGISTER CONTENT								REGISTER NAME
A4	A3	A2	A1	A0			D7(MSB)	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	Read	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	0	OVR	A/D Output Data, LS Byte
0	0	0	0	1	1	Read	ADC13	ADC12	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	A/D Output Data, MS Byte
0	0	0	1	0	2	Read	0	0	VLD5	VLD4	VLD3	VLD2	VLD1	VLD0	PGA Valid Register
0	0	0	1	1	3	R/W	0	0	BIN	0	RMB1	RBM0	CFD1	CFD0	A/D Control Register
0	0	1	0	0	4	R/W	CNV/BSY	G2	G1	G0	M3	M2	M1	M0	Gain/Mux Register
0	0	1	0	1	5	R/W	CNV/BSY	0	0	0	IO3	IO2	IO1	IO0	Digital I/O State Register
0	0	1	1	0	6	R/W	0	0	0	0	OE3	OE2	OE1	OE0	Digital I/O Control Register
0	0	1	1	1	7	R/W	0	0	OSCR	OSCE	REFE	BUFE	R2V	RBG	Ref/Oscillator Control Register
1	1	0	0	0	24	R/W	LSB	2W/3W	8051	0	0	8501	2W/3W	LSB	Serial Interface Control Register
1	1	1	1	1	31	Read	0	0	0	0	0	0	0	1	ID Register

Figure 18. Register Address Map

The instruction byte (see Figure 17) contains the address of the register for the next read/write operation, determines whether the serial communication is to be done in 8-bit or 16-bit word length, and determines whether the next operation is read-from or written-to the addressed register.

The structure of the instruction byte for register mode is shown in Figure 17.

- D7: This bit is set to 0 for register mode operation.
- D6 (R/W): Bit 6 of the instruction byte determines whether a read or write operation is performed, 1 for a read or 0 for a write.
- D5 (16/8): This bit determines the word length of the read or write operation that follows, 1 for sixteen bits (two eight-bit bytes) or 0 for eight bits.
- D4 through D0 (A4 − A0): These bits determine the address of the register that is to be read from or written to. Register address coding and other information are tabulated in Figure 18.

For 16-bit operations, the first eight bits are written-to/read-from the address encoded by the instruction byte, bits A4 through A0 (register address). The address of the next eight bits depends upon whether the register address for the first byte is odd or even. If it is even, then the address for the second byte is the register address + 1. If the register address is odd, then the address for the second byte is the register address – 1.

This arrangement allows transfer of conversion results from the two A/D Output Data registers either MS byte first or LS byte first (refer to the section Serial Interface Control Register).

Register Summary

A summary of information about the addressable registers is shown in Figure 18. Their descriptions follow, and more detailed information is provided later in the section Internal User-accessible Registers.

Registers 0 and 1, the A/D Output Data registers, contain the least significant and most significant bits of the A/D conversion result (ADC0 through ADC13). Register 0 also has one fixed zero (D1), and a bit to indicate if the internal voltage limits of the PGA have been over ranged (OVR). This is a read only register. Write an 8-bit word to register 0 and the ADS7871 is reset.

Register 2, the PGA Valid register, contains information that describes the nature of the problem in the event that the allowable input voltage to the PGA has been exceeded.

Register 3, the A/D Control register, has two test bits (best left set to zero), a bit to convert the output format to straight binary (BIN), an unused bit set to zero, two bits to configure an automatic read back mode of the A/D results (RBM1, RBM0), and two bits that program the frequency divider for the CCLK (CDF1, CDF0).

Register 4, the Gain/Mux register, contains the input channel selection information (M0 through M3) and the programmable gain amplifier gain set bits (G0 through G2).

Register 5, the Digital I/O State register, contains the state of each of the digital I/O pins (I/O3 through I/O0).

In addition, registers 4 and 5 contain a convert/busy bit (CNV/BSY) that can be used to start a conversion via a write instruction or sense when the converter is busy with a read instruction.

Register 6, the Digital I/O Control register, contains the information that determines whether each of the four digital I/O pins is to be an input or an output function (OE3 through OE0). This sets the mode of each I/O pin.

Register 7, the Ref/Oscillator Control register, controls whether the internal oscillator used for the conversion clock is on or off (OSCE), whether the internal voltage reference and buffer are on or off (REFE, BUFE), and whether the reference provides 2.5 V, 2.048 V, or 1.15 V.

Register 24, the Serial Interface Control register, controls whether data is presented MSB or LSB first (LSB bit), whether the serial interface is configured for 2-wire or 3-wire operation (2W/3W bit), and determines proper timing control for 8051-type microprocessor interfaces (8051 bit).

Register 31, the ID register, is read only.

Reset

There are three ways to reset.

All register contents and the serial interface are reset on:

1. Cycle power. The power down time must be long enough to allow internal nodes to discharge.
2. Toggle the RESET pin. Minimum pulse width to reset is 50 ns.
3. Write an 8-bit byte to register 0. The ADS7871 does not wait for the data which would normally follow this instruction.

All of these actions set all internal registers to zero, turns off the oscillator, reference, and buffer. Recovery time for the reference is dependent on capacitance on the reference and buffer outputs.

Only the serial interface is reset (and disabled) when the $\overline{CS}$ signal is brought high. If $\overline{CS}$ is continuously held low, and the ADS7871 is reset by an 8-bit write to register 0 (even if inadvertently) then the next 1 input to DIN is the synchronizing bit for the serial interface. The next active edge of SCLK following this 1 latches in the first bit of the new instruction byte.

For applications where $\overline{CS}$ cannot be cycled and system synchronization is lost, the ADS7871 must be reset by writing 39 zeros and a one. The serial interface is then ready to accept the next command byte. This string length is based on the worst case conditions to ensure that the device is synchronized.

NOTE:

A noisy SCLK, with excessive ringing, can cause the ADS7871 to inadvertently reset. Sufficient capacitance to correct this problem may be provided by just a scope probe, which would mask this issue during debugging. A 100-Ω capacitor in series with the SCLK pin is usually sufficient to correct this problem. Since the data is changed on the opposite edge of SCLK, it is usually settled before the active edge of SCLK and would not need its own 100-Ω resistor, although it would not be detrimental.

Write Operation

To perform a write operation an instruction byte must first be written to the ADS7871 as described previously (see Figure 17). This instruction determines the target register as well as the word length (8 bits or 16 bits). The $\overline{CS}$ pin must be asserted (0) prior to the first active SCLK edge (rising or falling depending on the state of the RISE/$\overline{FALL}$ pin) that latches the first bit of the instruction byte. The first active edge after $\overline{CS}$ must have the first bit of the instruction byte. The remaining seven bits of the instruction byte are latched on the next seven active edges of SCLK. $\overline{CS}$ must remain low for the entire sequence. Setting $\overline{CS}$ high resets the serial interface.

When starting a conversion by setting the CNV/BSY bit in the Gain/Mux register and/or the Digital I/O register, the conversion starts on the second falling edge of DCLK after the last active SCLK edge of the write operation.

Figure 19 shows an example of an eight-bit write operation with LSB first and SCLK active on the rising edge. The double arrows indicate the SCLK transition when data is latched into its destination register.

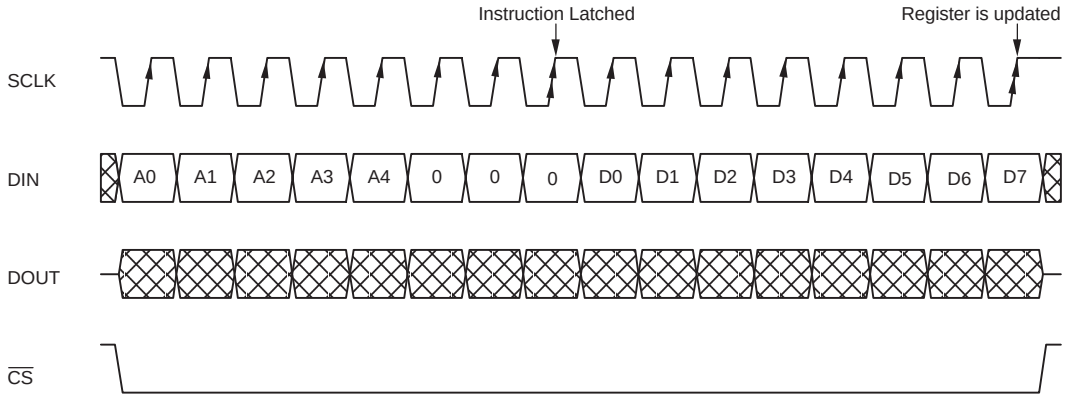


Figure 19. Timing Diagram for an 8-Bit Write Operation

Figure 20 shows an example of the timing for a 16-bit write to an even address with LSB first and SCLK active on the rising edge. Notice that both bytes are updated to their respective registers simultaneously. Also shown is that the address (ADDR) for the write of the second byte is incremented by one since the ADDR in the instruction byte was even. For an odd ADDR, the address for the second byte would be ADDR−1.

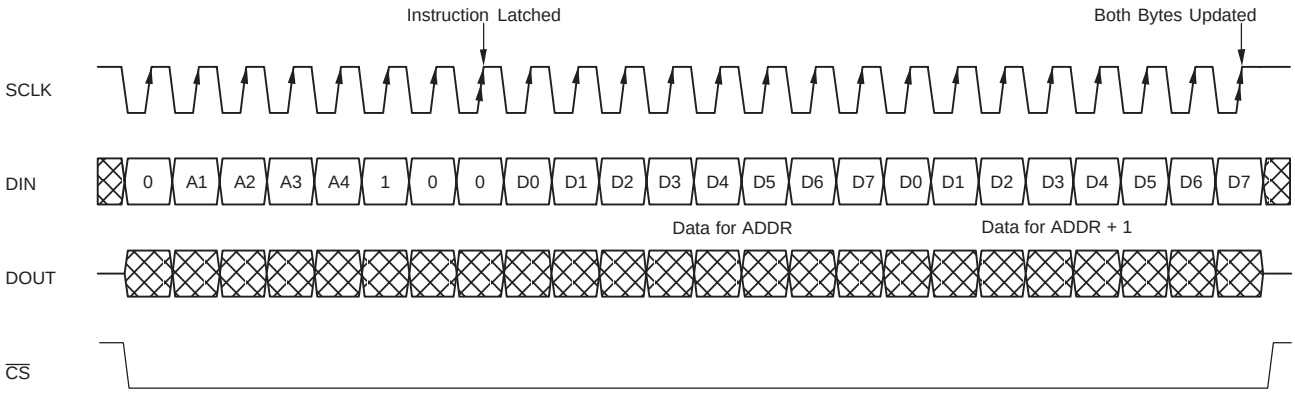


Figure 20. Timing Diagram of a 16-Bit Write Operation to an Even Address

Read Operation

A read operation is similar to a write operation except that data flow (after the instruction byte) is from the ADS7871 to the host controller. After the instruction byte has been latched (on the eighth active edge of SCLK), the DOUT pin (and the DIN pin if in two-wire mode) begins driving data on the next nonactive edge of SCLK. This allows the host controller to have valid data on the next active edge of SCLK.

The data on DOUT (or DIN) transitions on the nonactive edges of SCLK. The DIN pin (two-wire mode) ceases driving data (return to high impedance) on the nonactive edge of SCLK following the eighth (or sixteenth) active edge of the read data. DOUT is only high impedance when $\overline{CS}$ is not asserted. With $\overline{CS}$ high (1), DOUT (or DIN) is forced to high impedance mode. In general, the ADS7871 is insensitive to the idle state of the clock except that the state of SCLK may determine if DIN is driving data or not.

Upon completion of the read operation, the ADS7871 is ready to receive the next instruction byte. Read operations reflect the state of the ADS7871 on the first active edge of SCLK of the data byte transferred.

Figure 21 shows an example of an eight-bit read operation with LSB first and SCLK active on the rising edge. The double rising arrows indicate when the instruction is latched.

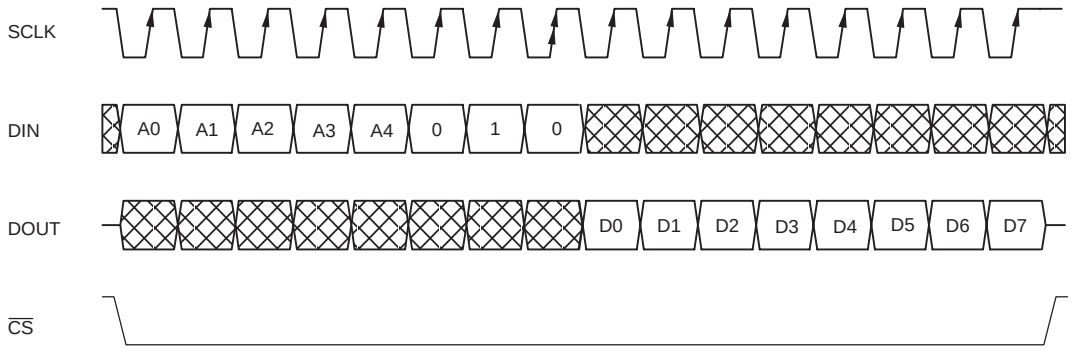


Figure 21. Timing Diagram for an 8-Bit Read Operation

Figure 22 provides an example of a 16-bit read operation from an odd address with LSB first and SCLK active on the rising edge. The address (ADDR) for the second byte is decremented by one since the ADDR in the instruction byte is odd. For an even ADDR, the address for the second byte would be incremented by one.

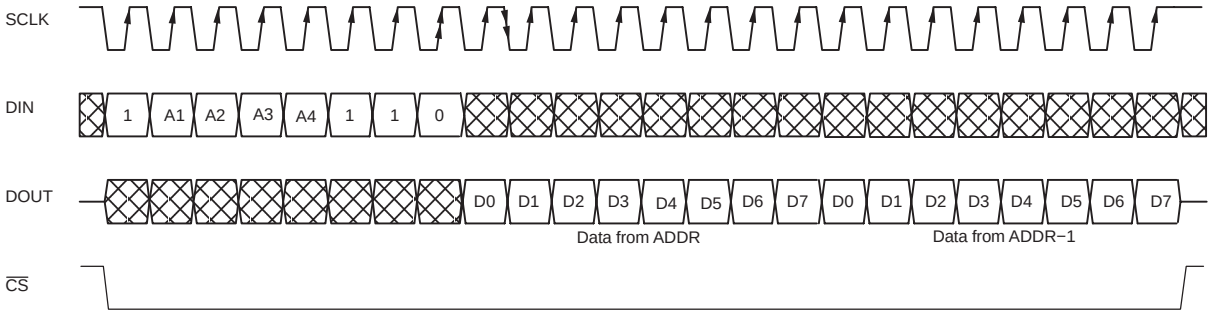


Figure 22. Timing Diagram for a 16-Bit Read Operation to an Odd Address

Multiplexer Addressing

The last four bits in the instruction byte (during a start conversion instruction) or the Gain/Mux register (ADDR = 4) assign the multiplexer configuration for the requested conversion. The input channels may be placed in either differential or single-ended configurations. For differential configurations, the polarity of the input signal is reversible by the state of M2 (Bit D2). In single-ended mode, all input channels are measured with respect to system ground (pin 25). Figure 23 shows some examples of multiplexer assignments and Figure 24 provides the coding for the input channel selection.

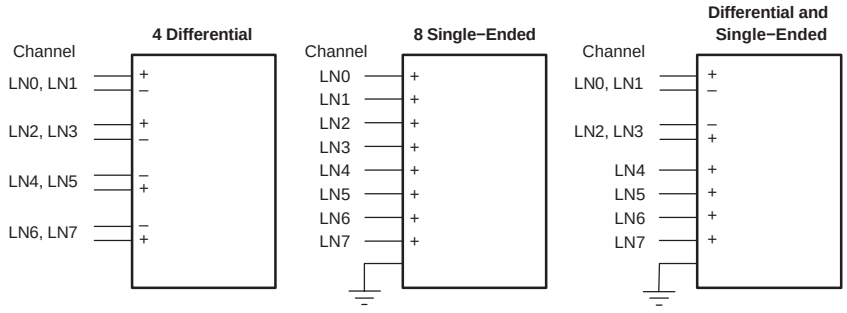


Figure 23. Examples of Multiplexer Options

CODING FOR DIFFERENTIAL INPUT CHANNEL SELECT												CODING FOR SINGLE-ENDED INPUT CHANNEL SELECT (negative input is ground)											
SELECTION BITS				INPUT LINES								SELECTION BITS				INPUT LINES							
M3	M2	M1	M0	LN0	LN1	LN2	LN3	LN4	LN5	LN6	LN7	M3	M2	M1	M0	LN0	NL1	LN2	LN3	LN4	LN5	LN6	LN7
0	0	0	0	+	−							1	0	0	0	+							
0	0	0	1			+	−					1	0	0	1		+						
0	0	1	0					+	−			1	0	1	0			+					
0	0	1	1							+	−	1	0	1	1				+				
0	1	0	0	−	+							1	1	0	0					+			
0	1	0	1			−	+					1	1	0	1						+		
0	1	1	0					−	+			1	1	1	0							+	
0	1	1	1							−	+	1	1	1	1								+

NOTE: Bit M3 selects either differential or single-ended mode. If differential mode is selected, bit M2 determines the polarity of the input channels. Bold items are power-up default conditions.

Figure 24. Multiplexer Addressing

INTERNAL USER-ACCESSIBLE REGISTERS

The registers in the ADS7871 are eight bits wide. Most of the registers are reserved, the ten user-accessible registers are summarized in the register address map (see Figure 18). Detailed information for each register follows. The default power-on/reset state of all bits in the registers is 0.

ADC Output Registers

The A/D Output registers are read only registers located at ADDR = 0 and ADDR = 1 that contain the results of the A/D conversion, ADC13 through ADC0 (see Figure 25). The conversion result is in 2s complement format. The bits can be taken out of the registers MSB (D7) first or LSB (D0) first, as determined by the state of the LSB bits (D7 or D0) in the Serial Interface Control register. The ADDR = 0 register also contains the OVR bit which indicates if the internal voltage limits to the PGA have been exceeded.

ADC OUTPUT REGISTERS

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
0	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	0	OVR
1	ADC13	ADC12	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6

ADDR = 0 (LS Byte)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7−D2	ADC5−ADC0	A/D Output	(1)	Six least significant bits of conversion result
D1	—	—	0	This bit is not used and is always 0.
D0	OVR	PGA Over-Range	0 1	Valid conversion result An analog over-range problem has occurred in the PGA. Conversion result may be invalid. Details of the type of problem are stored in register 2, the PGA Valid register.

ADDR = 1 (MS Byte)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7−D0	ADC13−ADC6	ADC Output	(1)	Eight most significant bits of conversion result

(1) Value depends on conversion result

Figure 25. ADC Output Registers (ADDR = 0 and ADDR = 1)

PGA Valid Register

The PGA Valid register (ADDR = 2) is a read only register that contains the individual results of each of the six comparators for the PGA, VLD5 through VLD0, as shown in Figure 26.

PGA VALID REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
2	0	0	VLD5	VLD4	VLD3	VLD2	VLD1	VLD0

ADDR = 2

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7−D6	—	—	0	These bits are not used and are always 0**.**
D5	VLD5	PGA Valid 5	**0** 1	**Voltage at minus (−) output from the PGA is within its minimum value.** Voltage at minus (−) output from the PGA has exceeded its minimum value.
D4	VLD4	PGA Valid 4	**0** 1	**Voltage at minus (−) output from the PGA is within its maximum value.** Voltage at minus (−) output from the PGA has exceeded its maximum value.
D3	VLD3	PGA Valid 3	**0** 1	**Voltage at minus (−) input to the PGA is within its maximum value.** Voltage at minus (−) input to the PGA has exceeded its maximum value.
D2	VLD2	PGA Valid 2	**0** 1	**Voltage at plus (+) output from the PGA is within its minimum value.** Voltage at plus (+) output from the PGA has exceeded its minimum value.
D1	VLD1	PGA Valid 1	**0** 1	**Voltage at plus (+) output from the PGA is within its maximum value.** Voltage at plus (+) output from the PGA has exceeded its maximum value.
D0	VLD0	PGA Valid 0	**0** 1	**Voltage at plus (+) input to the PGA is within its maximum value.** Voltage at plus (+) input to the PGA has exceeded its maximum value.

Bold items are power-up default conditions.

Figure 26. PGA Valid Register (ADDR = 2)

A/D Control Register

The A/D Control register (ADDR = 3) configures the CCLK divider and read back mode option as shown in Figure 27.

ADC CONTROL REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
3	0	0	BIN	0	RBM1	RBM0	CFD1	CFD0

ADDR = 3

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7−D6	—	—	0	These bits are reserved and must always be written 0.
D5	BIN	Output Data Format	**0** 1	**Mode 0 − Twos complement output data format** Mode 1 − Binary output data format
D4	—	—	**0**	**This is a reserve bit and must always be written 0**
D3−D2	RBM1−RBM0	Automatic Read Back Mode	**00** 01 10 11	**Mode 0 − Read instruction required to access ADC conversion result.** Mode 1 − Most significant byte returned first Mode 2 − Least significant byte returned first Mode 3 − Only most significant byte returned
D1−D0	CFD1−CFD0	CCLK Divide	**00** 01 10 11	**Division factor for CCLK = 1 (DCLK = CCLK)** Division factor for CCLK = 2 (DCLK = CCLK/2) Division factor for CCLK = 4 (DCLK = CCLK/4) Division factor for CCLK = 8 (DCLK = CCLK/8)

Bold items are power-up default conditions.

Figure 27. ADC Control Register (ADDR = 3)

Read Back Modes

RBM1 and RBM0 determine which of four possible modes is used to read the A/D conversion result from the A/D Output registers.

- Mode 0 (default mode) requires a separate read instruction to be performed in order to read the output of the A/D Output registers
- Mode 1, 2, and 3: Provide for different types of automatic read-back options of the conversion results from the A/D Output registers without having to use separate read instructions:

  Mode 1: Provides data MS byte first

  Mode 2: Provides data LS byte first

  Mode 3: Output only the MS byte

For more information refer to the read back mode section.

Clock Divider

CFD1 and CFD0 set the CCLK divisor constant which determines the DCLK applied to the A/D, PGA, and reference. The A/D and PGA operate with a maximum clock of 2.5 MHz. In situations where an external clock is used to pace the conversion process it may be desirable to reduce the external clock frequency before it is actually applied to the PGA and A/D. The signal that is actually applied to the A/D and PGA is DCLK, where DCLK = CCLK/DF (DF is the division factor determined by the CFD1 and CFD0 bits). For example, if the external clock applied to CCLK is 10 MHz and DF = 4 (CFD1 = 1, CFD0 = 0), DCLK equals 2.5 MHz.

Gain/Mux Register

The Gain/Mux register (ADDR = 4) contains the bits that configure the PGA gain (G2 − G0) and the input channel selection (M3 − M0) as shown in Figure 28. This register is also updated when direct mode is used to start a conversion so its bit definition is compatible with the instruction byte.

GAIN/MUX REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
4	CNV/BSY	G2	G1	G0	M3	M2	M1	M0

ADDR = 4

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7	CNV/BSY	Convert/Busy	**0** 1	**Idle Mode** Busy Mode; write = start conversion
D6−D4	G2−G0	PGA Gain Select	**000** 001 010 011 100 101 110 111	**PGA Gain = 1** PGA Gain = 2 PGA Gain = 4 PGA Gain = 5 PGA Gain = 8 PGA Gain = 10 PGA Gain = 16 PGA Gain = 20
D3−D0	M3−M0	Input Channel Select	see Figure 24	Determines input channel selection for the requested conversion, differential or single-ended configuration.

Bold items are power-up default conditions.

Figure 28. Gain/Mux Register (ADDR = 4)

Input Channel Selection

Bits M3 through M0 configure the switches that determine the input channel selection. The input channels may be placed in either differential or single-ended configurations. In the case of differential configuration, the polarity of the input pins is reversible by the state of the M2 bit. The coding for input channels is given in Figure 24 and examples of different input configurations are shown in Figure 23.

Convert/Busy

If the CNV/BSY bit is set to a 1 during a write operation, a conversion starts on the second falling edge of DCLK after the active edge of SCLK that latched the data into the Gain/Mux register. The CNV/BSY bit may be read with a read instruction. The CNV/BSY bit is set to 1 in a read operation if the ADS7871 is performing a conversion at the time the register is sampled in the read operation.

Gain Select

Bits G2 through G0 control the gain of the programmable gain amplifier. PGA gains of 1, 2, 4, 5, 8, 10, 16, and 20 are available. The coding is shown in Figure 28.

Digital Input/Output State Register

The Digital I/O State register (ADDR = 5) contains the state of each of the four digital I/O pins. Each pin can function as a digital input (the state of the pin is set by an external signal connected to it) or a digital output (the state of the pin is set by data from a serial input to the ADS7871). The input/output functional control is established by the digital I/O mode control bits (OE3−OE0) in the Digital I/O Control register. In addition, the convert/busy bit (CNV/BSY) can be used to start a conversion via a write instruction or determine if the converter is busy by executing a read instruction.

Digital I/O State Bits

Bits D3 through D0 (I/O3−I/O0) of the Digital I/O State register are the state bits. If the corresponding mode bit makes the pin a digital input, the state bit indicates whether the external signal connected to the pin is a 1 or a 0, and it is not possible to control the state of the corresponding bit with a write operation. The state of the bit is only controlled by the external signal connected to the digital I/O pin. Coding is shown in Figure 29.

DIGITAL I/O STATE REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
5	CNV/BSY	0	0	0	IO3	IO2	IO1	IO0

ADDR = 5

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7	CNV/BSY	Convert/Busy	**0** 1	**Idle Mode** Busy Mode; write = start conversion
D6−D4	—	—	0	These bits are not used and are always 0.
D3	IO3	State for I/O3	**0** 1	**Input or Output State = 0** Input or Output State = 1
D2	IO2	State for I/O2	**0** 1	**Input or Output State = 0** Input or Output State = 1
D1	IO1	State for I/O1	**0** 1	**Input or Output State = 0** Input or Output State = 1
D0	IO0	State for I/O0	**0** 1	**Input or Output State = 0** Input or Output State = 1

Bold items are power-up default conditions.

NOTE: When the mode control makes a pin a digital input, it is not possible to control the state of the corresponding bit in the Digital I/O State register with a write operation. The state of the bit is only controlled by the external signal connected to the digital I/O pin.

Figure 29. Digital I/O State Register (ADDR = 5)

The four digital I/O pins allow control of external circuitry, such as a multiplexer, or allow the digital status lines from other devices to be read without using any additional microcontroller pins. Reads from this register always reflect the state of the pin, not the state of the latch inside the ADS7871.

Convert/Busy

If CNV/BSY is set to a 1 during a write operation, a conversion starts on the second falling edge of DCLK after the active edge of SCLK that latched the data into the Digital I/O register. The CNV/BSY bit may be read with a read instruction. The CNV/BSY bit is set to 1 in a read operation if the ADS7871 is performing a conversion at the time the register is sampled in the read operation.

Digital I/O Control Register

The Digital I/O Control register (ADDR = 6) contains the information that determines whether each of the four digital I/O lines is configured as an input or output. Setting the appropriate OE bit to 1 enables the corresponding I/O pin as an output. Setting the appropriate OE bit to 0 enables the corresponding I/O pin as an input (see Figure 30).

DIGITAL I/O CONTROL REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
6	0	0	0	0	OE3	OE2	OE1	OE0

ADDR = 6

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7−D4	—	—	0	These bits are reserved and must always be set to 0.
D3	OE3	State for I/O3	**0** 1	**Digital I/O 1 − digital input** Digital I/O 1 = digital output
D2	OE2	State for I/O2	**0** 1	**Digital I/O 2− digital input** Digital I/O 2 − digital output
D1	OE1	State for I/O1	**0** 1	**Digital I/O 3− digital input** Digital I/O 3 − digital output
D0	OE0	State for I/O0	**0** 1	**Digital I/O 4− digital input** Digital I/O 4 − digital output

Bold items are power-up default conditions.

Figure 30. Digital I/O Control Register (ADDR = 6)

Reference/Oscillator Configuration Register

The Reference/Oscillator Configuration register (ADDR = 7) determines whether the internal oscillator is used (OSCE and OSCR), whether the internal voltage reference and buffer are on or off (REFE and BUFE), and whether the reference is 2.5 V, 2.048 V, or 1.15 V as shown in Figure 31.

REFERENCE/OSCILLATOR REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
7	0	0	OSCR	OSCE	REFE	BUFE	R2V	RBG

ADDR = 7

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7−D6	—	—	0	These bits are reserved and must always be set to 0.
D5	OSCR	Oscillator Control	**0** 1	**Source of clock for internal V_{REF} is CCLK pin.** Clocking signal comes from the internal oscillator.
D4	OSCE	Oscillator Enable	**0** 1	**CCLK is configured as an input.** CCLK outputs a 2.5-MHz signal (70 μA).
D3	REFE	Reference Enable	**0** 1	**Reference is powered down.** Reference is powered up.
D2	BUFE	Buffer Enable	**0** 1	**Buffer is powered down and draws no current.** Buffer is powered up and draws 150 μA of current.
D1	R2V	2-V Reference	**0** 1	**VREF = 2.5 V (RBG bit = 0)** VREF = 2.048 V (RBG bit = 0)
D0	RBG	Bandgap Reference	**0** 1	**Bit R2V determines the value of the reference voltage.** VREF = 1.15 V

Bold items are power-up default conditions.

Figure 31. Reference/Oscillator Configuration Register (ADDR = 7)

Oscillator Control

The internal voltage reference uses a switched capacitor technique which requires a clocking signal input. When OSCR = 1, the clocking signal for the reference comes from the internal oscillator. When OSCR = 0, the clocking signal for the reference is derived from the signal on the CCLK pin and affected by the frequency divider controlled by the CFD0 and CFD1 bits in the A/D Control register.

The OSCE bit is the internal oscillator enable bit. When it is set to 1, power is applied to the internal oscillator causing it to produce a 2.5-MHz output and causing the signal to appear at the CCLK pin. The internal oscillator is also enabled when the OSCR bit and the REFE bit are set to 1, but does not make CCLK an output pin.

The internal oscillator is also enabled when the OSC ENABLE pin is set to 1. The power-up default condition is 0 for OSCE and OSCR. If either the OSC ENABLE pin is held high, or either of these control register bits are 1, then the oscillator is turned on.

Voltage Reference and Buffer Enable

When the REFE bit = 0 (power-up default condition), the reference is powered down and draws no current. When REFE is set to 1, the reference is powered up and draws approximately 190 μA of current. When the BUFE bit = 0 (power-up default condition), the buffer amplifier is powered down and draws no current. When the buffer amplifier is set to 1, it is powered up and draws approximately 150 μA of current.

Selecting the Reference Voltage

When the RBG bit is set to 1, the voltage on the VREF pin is 1.15 V and the R2V bit has no effect. When this bit is set to 0 (power-up default condition), the R2V bit determines the value of the reference voltage.

When R2V = 0 and RBG = 0 (power-up default condition), the voltage at the VREF pin is 2.5 V. When R2V = 1 and RBG = 0, the reference voltage is 2.048 V.

A 14-bit bipolar input A/D converter has 16384 states and each state corresponds to 305 μV with the 2.5-V reference. With a 2.048-V reference, each A/D bit corresponds to 250 μV.

Serial Interface Control Register

The Serial Interface Control register (ADDR = 24), see Figure 32, allows certain aspects of the serial interface to be controlled by the user. It controls whether data is presented MSB or LSB first and whether the serial interface is configured for 2-wire or 3-wire operation, and it determines proper timing control for 8051-type microprocessor interfaces.

The information in this register is formatted with the information symmetric about its center. This is done so that it may be read or written either LSB (bit D7) or MSB (bit D0) first. Each control bit has two locations in the register. If either of the two is set, the function is activated. This arrangement can potentially simplify microcontroller communication code.

The instruction byte to write this configuration data to register 24 is itself symmetric. From Figure 17, a register mode write instruction of 8 bits to address 24 is 0001 1000 in binary form. Therefore, this command to write to this register is valid under all conditions.

SERIAL INTERFACE CONTROL REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
24	LSB	2W/3W	8051	0	0	8051	2W/3W	LSB

ADDR = 7

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7	LSB	LSB or MSB first	**0** 1	**Serial interface receives and transmits MSB first.** Serial interface receives and transmits LSB first.
D6	2W/3W	2 Wire or 3 Wire	**0** 1	**3-Wire mode** 2-Wire mode
D5	8051	Serial Interface	**0** 1	**DIN high impedance on the next inactive edge or when $\overline{CS}$ goes inactive.** DIN pin is high impedance on last active SCLK edge of the bye of data transfer
D4−D3	—	—	0	These bits are reserved and must always be set 0.
D2	8051	Serial Interface	**0** 1	**DIN high impedance on the next inactive edge or when $\overline{CS}$ goes inactive.** DIN pin is high impedance on last active SCLK edge of the byte of data transfer
D1	2W/3W	2 Wire or 3 Wire	**0** 1	**3-Wire mode** 2-Wire mode
D0	LSB	LSB or MSB first	**0** 1	**Serial interface receives and transmits MSB first.** Serial interface receives and transmits LSB first.

Bold items are power-up default conditions.

Figure 32. Serial Interface Control Register (ADDR = 24)

LSB or MSB

The LSB bit determines whether the serial interface receives and transmits either LSB or MSB first. Setting the LSB bit (1) configures the interface to expect all bytes LSB first as opposed to the default MSB first (LSB = 0).

2-Wire or 3-Wire Operation

The 2W/3W bit configures the ADS7871 for 2-wire or 3-wire mode. In two-wire mode (2W/3W = 1), the DIN pin is enabled as an output during the data output portion of a read instruction. The DIN pin accepts data when the ADS7871 is receiving and it outputs data when the ADS7871 is transmitting. When data is being sent out of the DIN pin, it also appears on the DOUT pin as well. In three-wire mode (2W/3W = 0), data to the ADS7871 is received on the DIN pin and is transmitted on the DOUT pin. The power-up default condition is three-wire mode.

Serial Interface Timing (8051 Bit)

The 8051 bit changes the timing of when the DIN pin goes to high impedance at the end of an operation. When the bit is a 1, the pin goes to high impedance on the last active SCLK edge of the last byte of data transfer instead of waiting for the next inactive edge, or $\overline{CS}$ to go inactive. This allows the ADS7871 to disconnect from the data lines soon enough to avoid contention with an 80C51-type interface. The 80C51 drives data four CPU cycles before an inactive SCLK edge and for two CPU cycles after an active SCLK edge. When the 8051 bit is a 0, the DIN pin goes high impedance on the next inactive SCLK edge or when $\overline{CS}$ goes inactive (1).

Figure 33 and Figure 34 show the timing of when the ADS7871 sets the DIN pin to high impedance at the end of a read operation when the 2W/3W bit is set. The behavior of DOUT does not depend of the state of 2W/3W. The 8051 bit is not set for these two examples.

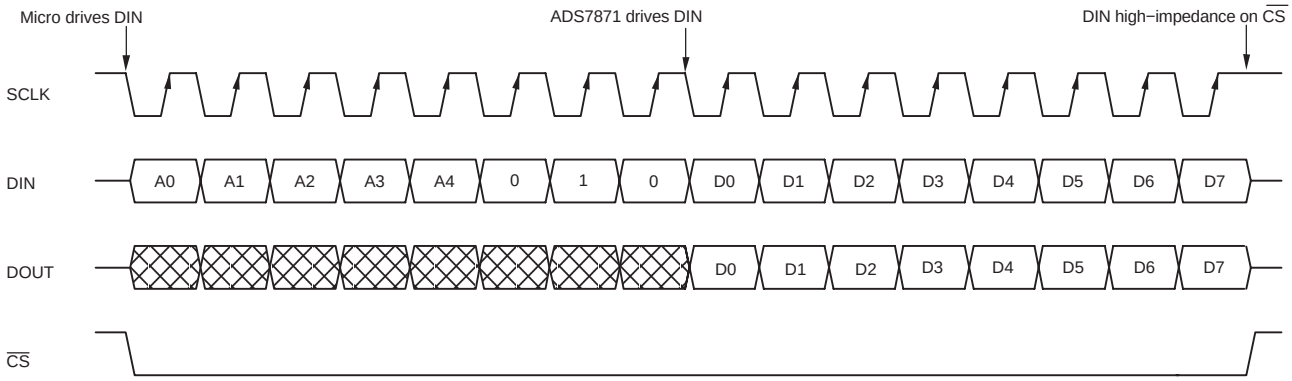


Figure 33. Timing for High Impedance State on DIN/DOUT ($\overline{CS}$ = 1)

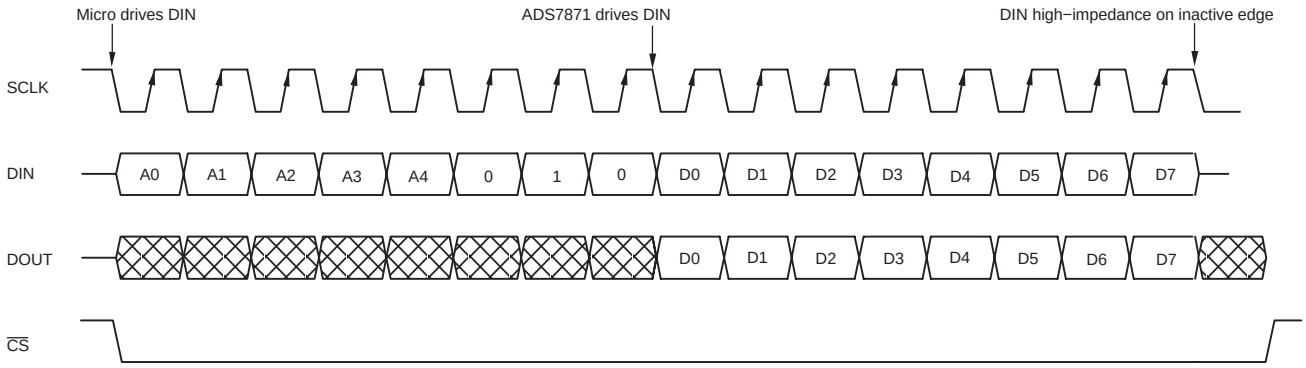


Figure 34. Timing for High Impedance State on DIN/DOUT (Inactive SCLK Edge)

Figure 35 shows the timing for entering the high impedance state when the 8051 bit is set. Notice that on the last bit of the read operation the DIN (and DOUT) pin goes to the high impedance state on the active edge of SCLK instead of waiting for the inactive edge of SCLK or $\overline{CS}$ going high as shown in Figure 33 and Figure 34. This is for compatibility with 80C51 mode 0 type serial interfaces. An 80C51 forces DIN valid before the SCLK falling edge and holds it valid until after the SCLK rising edge. This can lead to contention but setting the 8051 bit fixes this potential problem without requiring $\overline{CS}$ to be toggled high after every read operation.

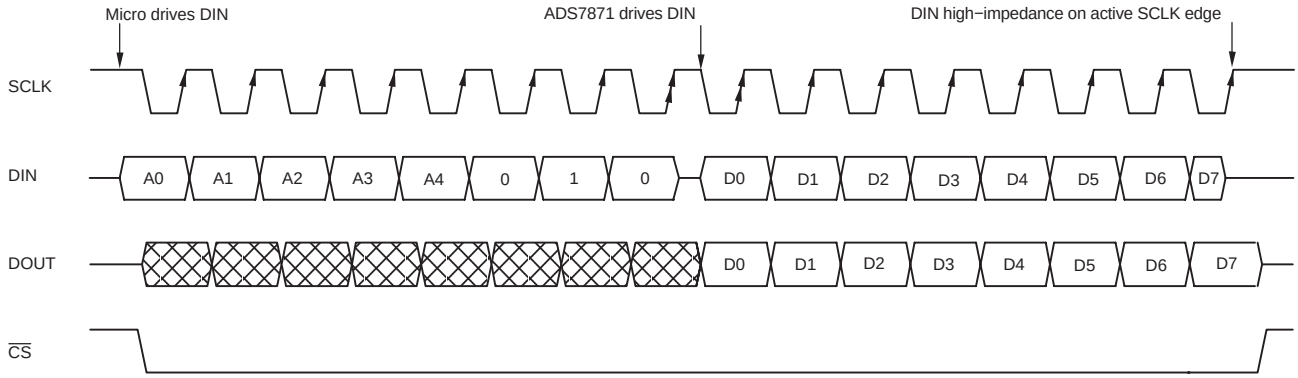


Figure 35. Timing for High-Impedance State on DIN/DOUT (8051 Bit = 1)

ID Register

The ADS7871 has an ID register (at ADDR = 31) to allow the user to identify which revision of the ADS7871 is installed. This is shown in Figure 36.

ID REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
31	0	0	0	0	0	0	0	1

ADDR = 31

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7−D0	—	—	—	The contents of this register identify the revision of the ADS7871

Figure 36. ID Register (ADDR = 31)

Remaining Registers

The remaining register addresses are not used in the normal operation of the ADS7871. These registers return random values when read and nonzero writes to these registers cause erratic behavior. Unused bits in the partially used registers must always be written low.

STARTING A CONVERSION THROUGH THE SERIAL INTERFACE

There are two methods of starting a conversion cycle through the serial interface. The first (nonaddressed or direct mode) is by using the start conversion byte as described earlier. The second (addressed mode) is by setting the CNV/BSY bit of register 4 or register 5 by performing a write instruction.

The conversion starts on the second falling edge of DCLK after the eighth active edge of SCLK (for the instruction in nonaddressed mode or the data in addressed mode). The BUSY pin goes active (1) one DCLK period (1, 2, 4, or 8 CCLK periods depending on CFD1 and CFD0) after the start of a conversion. This delay is to allow BUSY to go inactive when conversions are queued to follow in immediate succession. BUSY goes inactive at the end of the conversion.

If a conversion is already in progress when the CNV/BSY bit is set on the eighth active SCLK edge, the CNV/BSY bit is placed in the queue and the current conversion is allowed to finish. If a conversion is already queued, the new one replaces the currently queued conversion. The queue is only one conversion long. Immediately upon completion of the current conversion, the next conversion starts. This allows for maximum throughput through the A/D converter. Since BUSY is defined to be inactive for the first DCLK clock period of the conversion, the inactive (falling) edge of BUSY can be used to mark the end of a conversion (and start of the next conversion).

Figure 37 shows the timing of a conversion start using the convert start instruction byte. The double rising arrow on SCLK indicates when the instruction is latched. The double falling arrow on CCLK indicates where the conversion cycle actually starts (second falling edge of CCLK after the eighth active edge of SCLK). This example is for LSB first, CCLK divider = 1, and SCLK active on rising edge. Notice that BUSY goes active one CCLK period later since CCLK divider = 1.

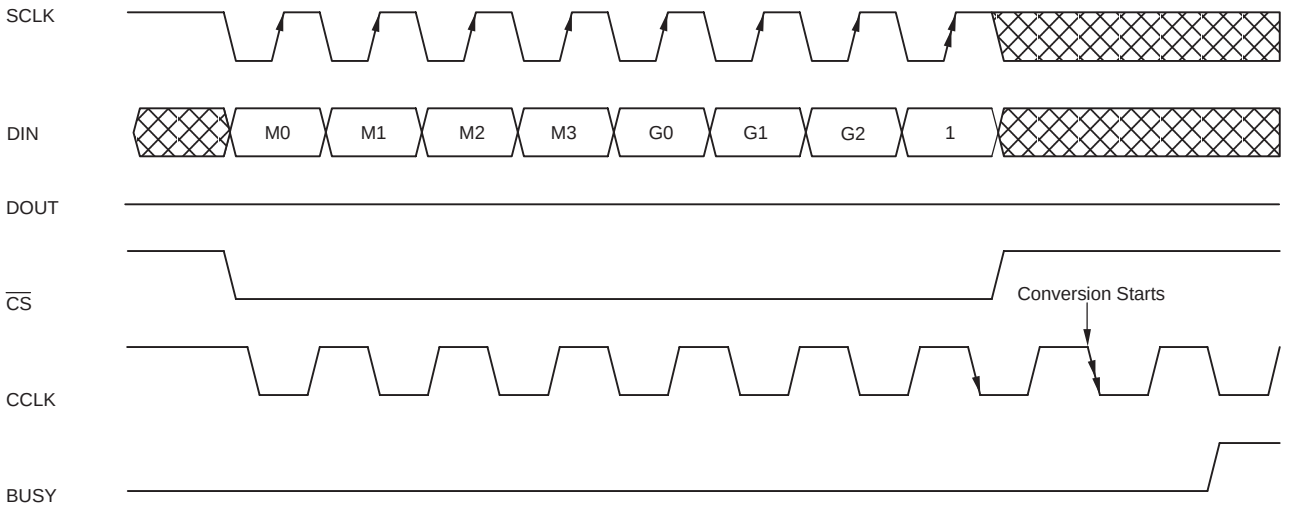


Figure 37. Timing Diagram for a Conversion Start Using Serial Interface Convert Instruction

Figure 38 shows an example of a conversion start using an 8-bit write operation to the Gain/Mux register with the CNV/BSY bit set to 1. The double rising arrow on SCLK indicates where the data is latched into the Gain/Mux register and the double arrow on CCLK indicates when the conversion starts. The example is for LSB first, CCLK divider = 1, and SCLK active on the rising edge.

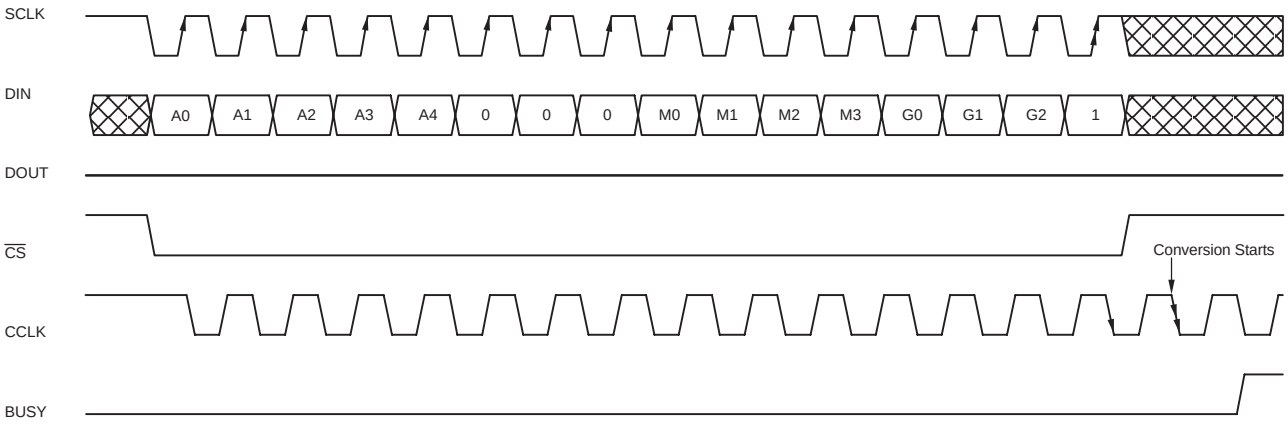


Figure 38. Timing Diagram for a Conversion Start Using 8-Bit Write to the Gain/Mux Register

Figure 39 shows the timing of a conversion start using the convert start instruction byte when a conversion is already in progress (indicated by BUSY high). The double rising arrow on SCLK indicates when the instruction is latched. The second falling arrow on CCLK indicates when the conversion cycle would have started had a conversion not been in progress. The double falling arrow on CCLK indicates where the conversion cycle actually starts (immediately after completion of the previous conversion). This example is for LSB first, CCLK divider = 2, and SCLK active on the rising edge. Notice that BUSY is low for two CCLK periods because the CCLK divider = 2.

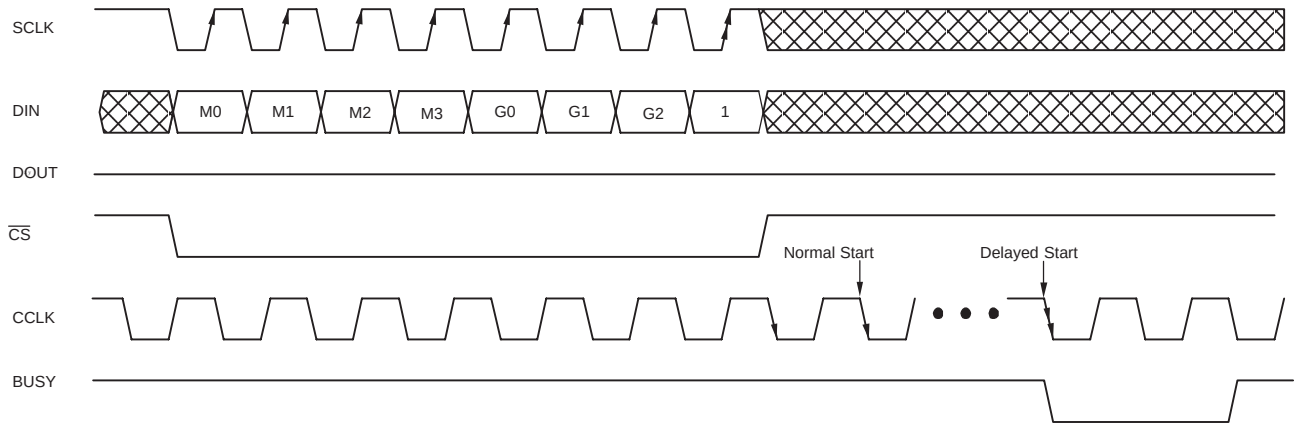


Figure 39. Timing Diagram of Delayed Conversion Start with Serial Interface

STARTING A CONVERSION USING THE CONVERT PIN

A conversion can also be started by an active (rising) edge on the CONVERT pin. Similar to the CNV/BSY register bit, the conversion starts on the second falling edge of CCLK after the CONVERT rising edge.

The CONVERT pin must stay high for at least two CCLK periods. CONVERT must also be low for at least two CCLK periods before going high. BUSY goes active one DCLK period after the start of the conversion.

Contrary to the CNV/BSY bit in the register, the CONVERT pin aborts any conversion in process and restart a new conversion. BUSY goes low at the end of the conversion. $\overline{CS}$ may be either high or low when the CONVERT pin starts a conversion.

Figure 40 shows the timing of a conversion start using the CONVERT pin. The double falling arrow on CCLK indicates when the conversion cycle actually starts (the second active CCLK edge after CONVERT goes active). This example is for CCLK divider = 4. Notice that BUSY goes active four CCLK periods later.

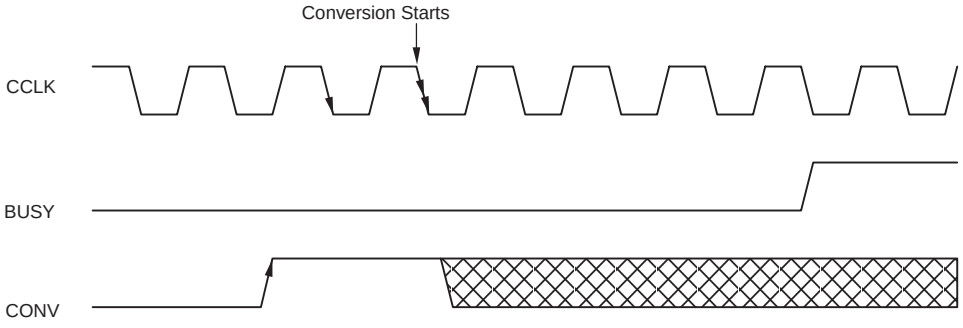


Figure 40. Timing Diagram of Conversion Start Using CONVERT Pin

READ BACK MODES

There are four modes available to read the A/D conversion result from the A/D Output registers. The RBM1 and RBM0 bits in the A/D Control register (ADDR = 3) control which mode is used by the ADS7871.

Read Back Mode 0 (default mode) requires a separate read instruction to retrieve the conversion result

Read Back Mode 1 (automatic) provides the output most significant byte first

Read Back Mode 2 (automatic) provides the output least significant byte first

Read Back Mode 3 (automatic) provides only the most significant byte

Mode 3 does not short cycle the A/D. Automatic read back mode is only triggered when starting a conversion using the serial interface. Conversions started using the CONVERT pin do not trigger the read back mode.

The first bit of data for an automatic read back is loaded on the first active SCLK edge of the read portion of THE instruction. The remaining bits are loaded on the next inactive SCLK edge (the first one after the first active edge). To avoid getting one bit from one conversion and the remainder of the byte from another conversion, a conversion should not finish between the first active SCLK edge and the next inactive edge.

Mode 0

Mode 0 (default operating mode) requires a read instruction to be performed to retrieve a conversion result. MS byte first format is achieved by performing a sixteen bit read from ADDR = 1. LS byte first format is achieved by performing a sixteen bit read from ADDR = 0. Reading only the most significant byte can be achieved by performing an eight bit read from ADDR = 1.

To increase throughput it is possible to read the result of a conversion while a conversion is in progress. The last conversion completed prior to the first active SCLK edge of the conversion data word (not the instruction byte) is retrieved. This overlapping allows a sequence of start conversion N, read conversion N – 1, start conversion N +1, read conversion N, etc. For conversion 0, the result of conversion –1 would need to be discarded.

Mode 1

In this mode, the serial interface configures itself to clockout a conversion result as soon as a conversion is started. This is useful since a read instruction is not required so eight SCLK cycles are saved. This mode operates like an implied sixteen bit read instruction byte for ADDR = 1 was sent to the ADS7871 after starting the conversion.

It is not necessary to wait for the end of the conversion to start clocking out conversion results. The last completed conversion at the sampling edge of SCLK is read back (whether a conversion is in progress or not).

Mode 2

This mode is similar to Mode 1 except that the conversion result is provided LS byte first (equivalent to a sixteen bit read from ADDR = 0).

Figure 41 and Figure 42 show timing examples of an automatic read back operation using mode 2. In Figure 41, the result of the previous conversion is retrieved. This example is for LSB first, CCLK divider = 2, and SCLK active on the rising edge. The data may be read back immediately after the start conversion instruction. It is not necessary to wait for the conversion to actually start (or finish).

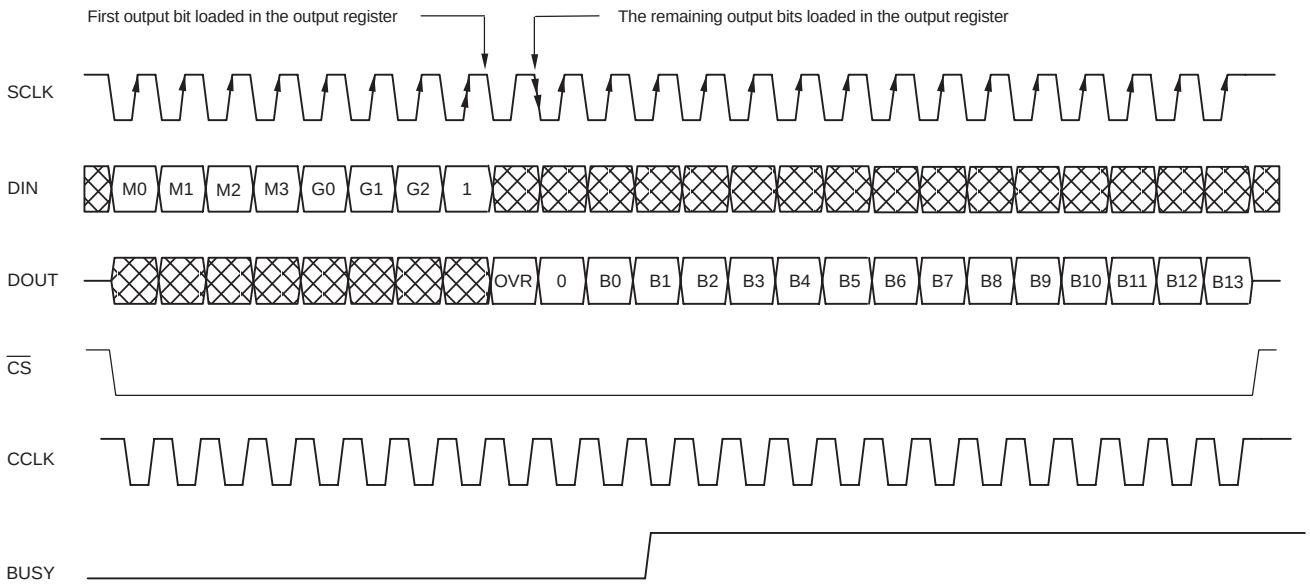


Figure 41. Timing Diagram for Automatic Read Back of Previous Conversion Result Using Mode 2

In Figure 42 the result of the just requested conversion is retrieved. The microcontroller must wait for BUSY to go inactive before clocking out the ADC Output register. $\overline{CS}$ must stay low while waiting for BUSY. This example is for LS byte first, CCLK divider = 1, and SCLK active on the falling edge. Notice that the DOUT pin is not driven with correct data until the appropriate active edge of SCLK.

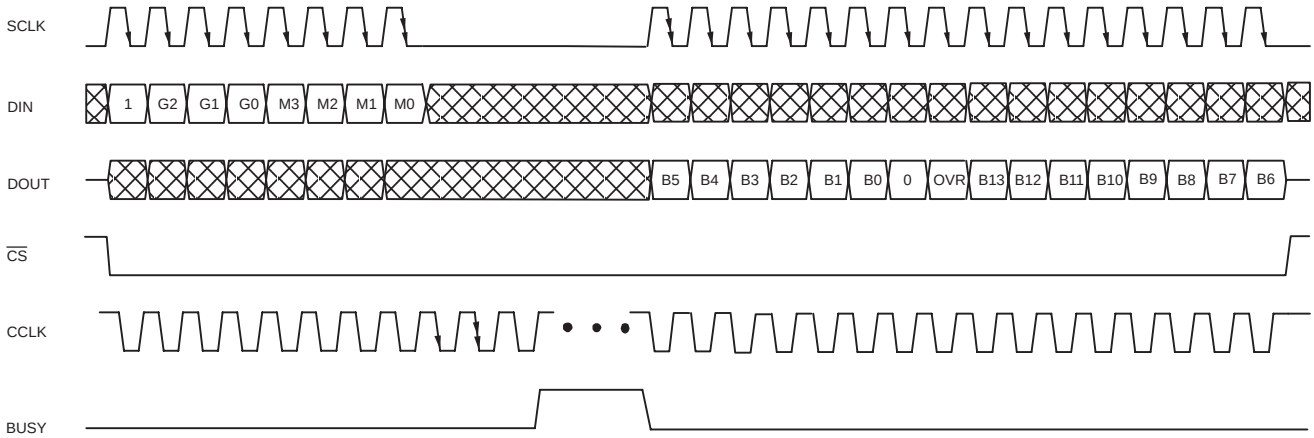


Figure 42. Timing Diagram for Automatic Read Back of Current Conversion Result Using Mode 2

Mode 3

This mode only returns the most significant byte of the conversion. It is equivalent to an eight bit read from ADDR = 1.

APPLICATION INFORMATION

REQUIRED SUPPORT ELEMENTS

As with any precision analog integrated circuit, good power supply bypassing is required. A low ESR ceramic capacitor in parallel with a large value electrolytic capacitor across the supply line furnishes the required performance. Typical values are 0.1 μF and 10 μF respectively. Noise performance of the internal voltage reference circuit is improved if a ceramic capacitor of approximately 0.01 μF is connected from VREF to ground. Increasing the value of this capacitor may bring slight improvement in the noise on VREF but increases the time required to stabilize after turn on.

If the internal buffer amplifier is used, it must have an output filter capacitor connected to ground to ensure stability. A nominal value of 0.47 μF provides the best performance. Any value between 0.1 μF and 10 μF is acceptable. In installations where one ADS7871 buffer is used to drive several devices, an additional filter capacitor of 0.1 μF should be installed at each of the slave devices.

The circuit in Figure 43 shows a typical installation with all control functions under control of the host embedded controller. The SCLK is active on the falling edge. If the internal voltage reference and oscillator are used, they must be turned on by setting the corresponding control bits in the device registers. These registers must be set on power up and after any reset operation.

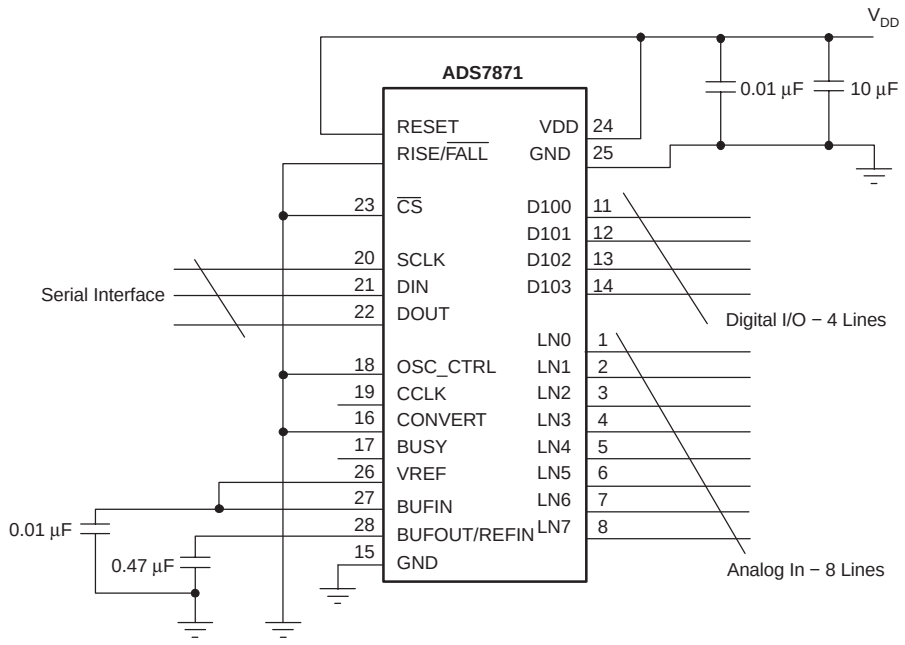


Figure 43. Typical Operation with Recommended Capacitor Values

APPLICATION INFORMATION

MICROCONTROLLER CONNECTIONS

The ADS7871 is quite flexible in interfacing to various microcontrollers. Connections using the hardware mode of two types of controllers (Motorola M68HC11, Intel 80C51) are described below.

Motorola M68HC11 (SPI)

The Motorola M68HC11 has a three-wire (four if you count the slave select) serial interface that is commonly referred to as SPI (serial peripheral interface), where the data is transmitted MSB first. This interface is usually described as the microcontroller and the peripheral each having two 8-bit shift registers (one for receiving and one for transmitting).

The transmit shift register of the microcontroller and the receive shift register of the peripheral are connected together and vice versa. SCK controls the shift registers. SPI is capable of full duplex operation (simultaneous read and write). The ADS7871 does not support full duplex operation. T**he ADS7871 can only be written to or read from. It cannot do both simultaneously.**

Since the M68HC11 can configure SCK to have either rising or falling edge active, the RISE/$\overline{\text{FALL}}$ pin on the ADS7871 can be in whichever state is appropriate for the desired mode of operation of the M68HC11 for compatibility with other peripherals.

In the Interface Control register (see Figure 32), the 2W/3W bit should be cleared (default). The LSB bit should be clear (default). The 8051 bit should also be clear (default). Since the ADS7871 defaults to SPI mode, the M68HC11 should not need to initialize the ADS7871 Interface Configuration register after power-on or reset.

Figure 44 shows a typical physical connection between an M68HC11 and a ADS7871. A pull-up resister on DOUT may be needed to keep DOUT from floating during write operations. $\overline{\text{CS}}$ may be permanently tied low if desired, but then the ADS7871 must be the only peripheral.

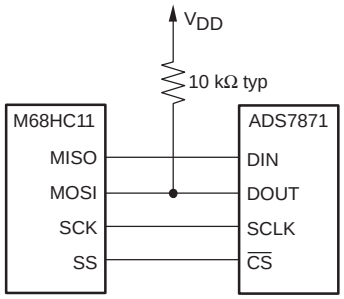


Figure 44. Connection of a M68HC11 to an ADS7871

APPLICATION INFORMATION

Intel 80C51

The Intel 80C51 operated in serial port mode 0 has a two-wire (three-wire if an additional I/O pin is used for $\overline{CS}$) serial interface. The TXD pin provides the clock for the serial interface and RXD serves as the data input and output. The data is transferred LSB first. Best compatibility is achieved by connecting the RISE/$\overline{FALL}$ pin of the ADS7871 high (rising edge of SCLK active). In the Interface Configuration register, the LSB bit and the 8051 bit should be set. The 2W/3W bit should also be set. **The first instruction after power-on or reset should be a write operation to the Interface Configuration register**.

Figure 45 shows a typical physical connection between an 80C51 and an ADS7871. $\overline{CS}$ may be permanently tied low if desired, but then the ADS7871 must be the only peripheral.

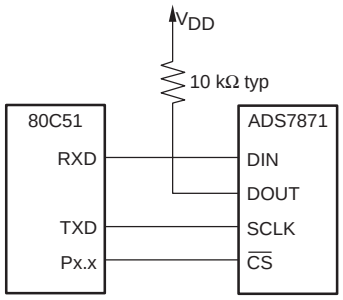


Figure 45. Connection of an 80C51 to an ADS7871

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7871IDB	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7871	Samples
ADS7871IDBG4	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7871	Samples
ADS7871IDBR	ACTIVE	SSOP	DB	28	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7871	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

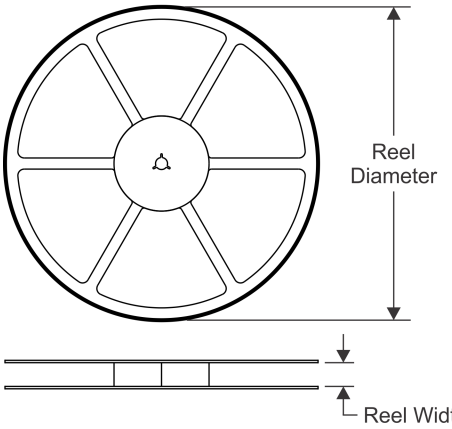
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

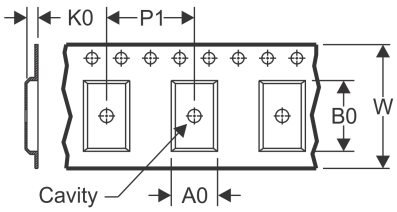
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

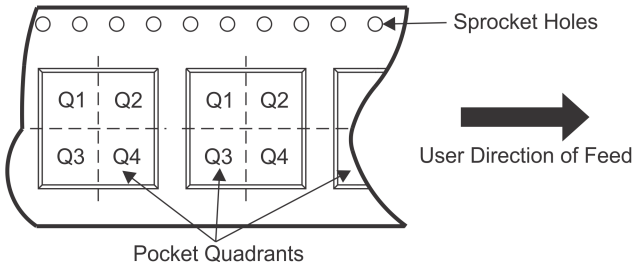


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

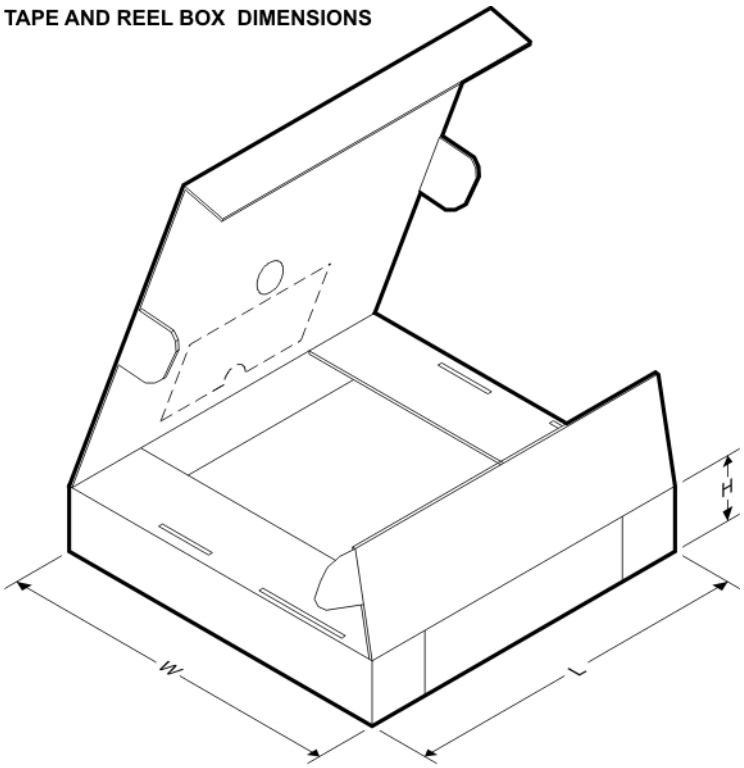
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7871IDBR	SSOP	DB	28	1000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

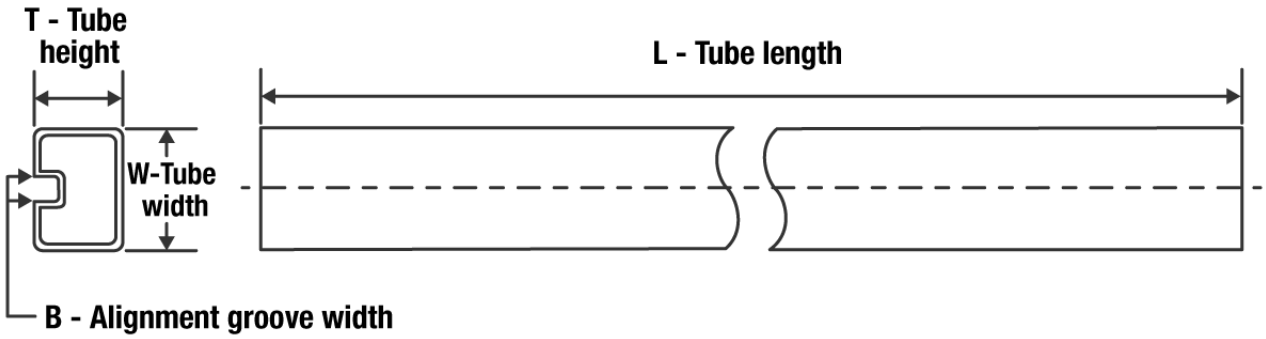
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7871IDBR	SSOP	DB	28	1000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

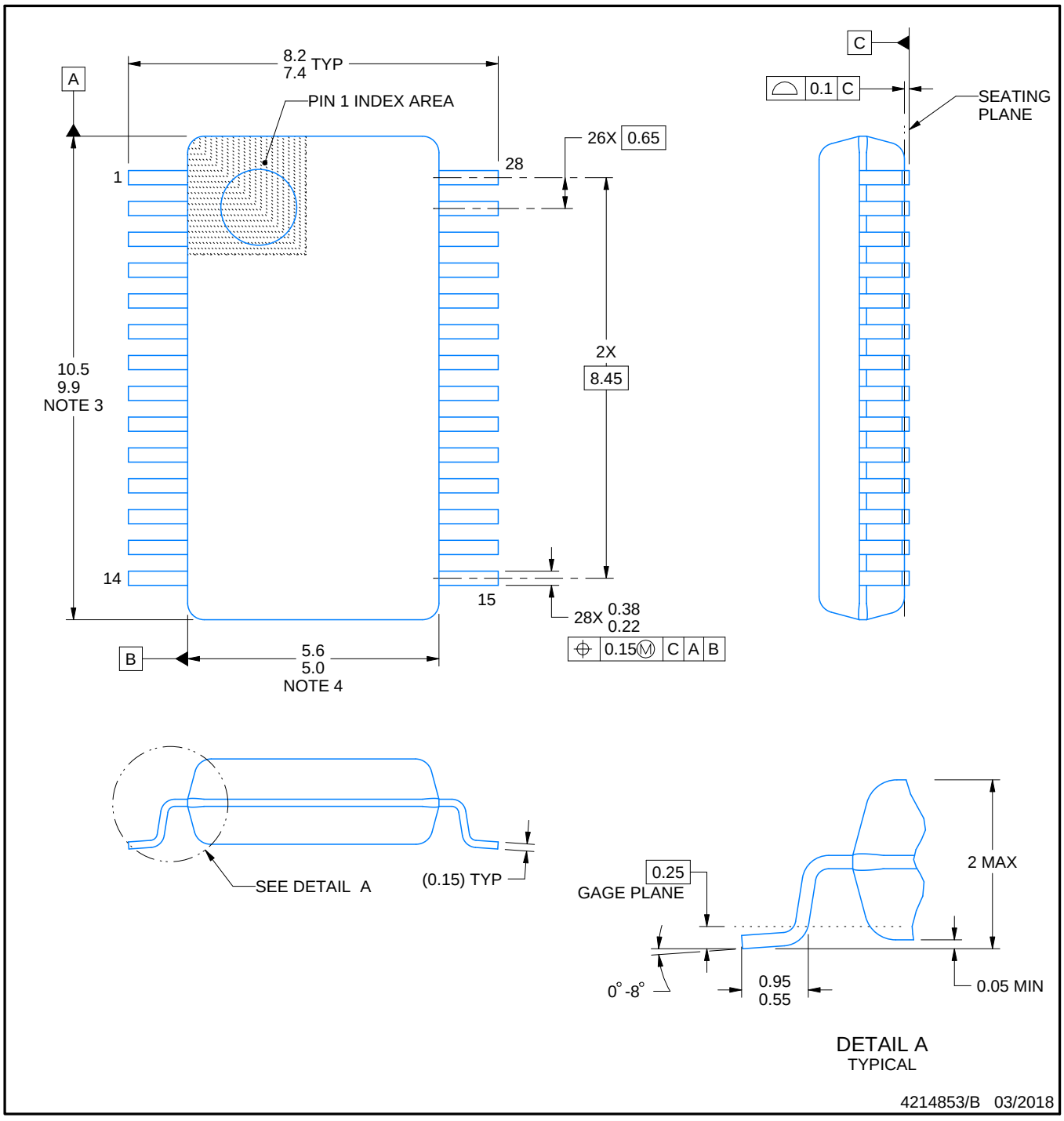
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS7871IDB	DB	SSOP	28	50	530	10.5	4000	4.1
ADS7871IDBG4	DB	SSOP	28	50	530	10.5	4000	4.1

PACKAGE OUTLINE

DB0028A

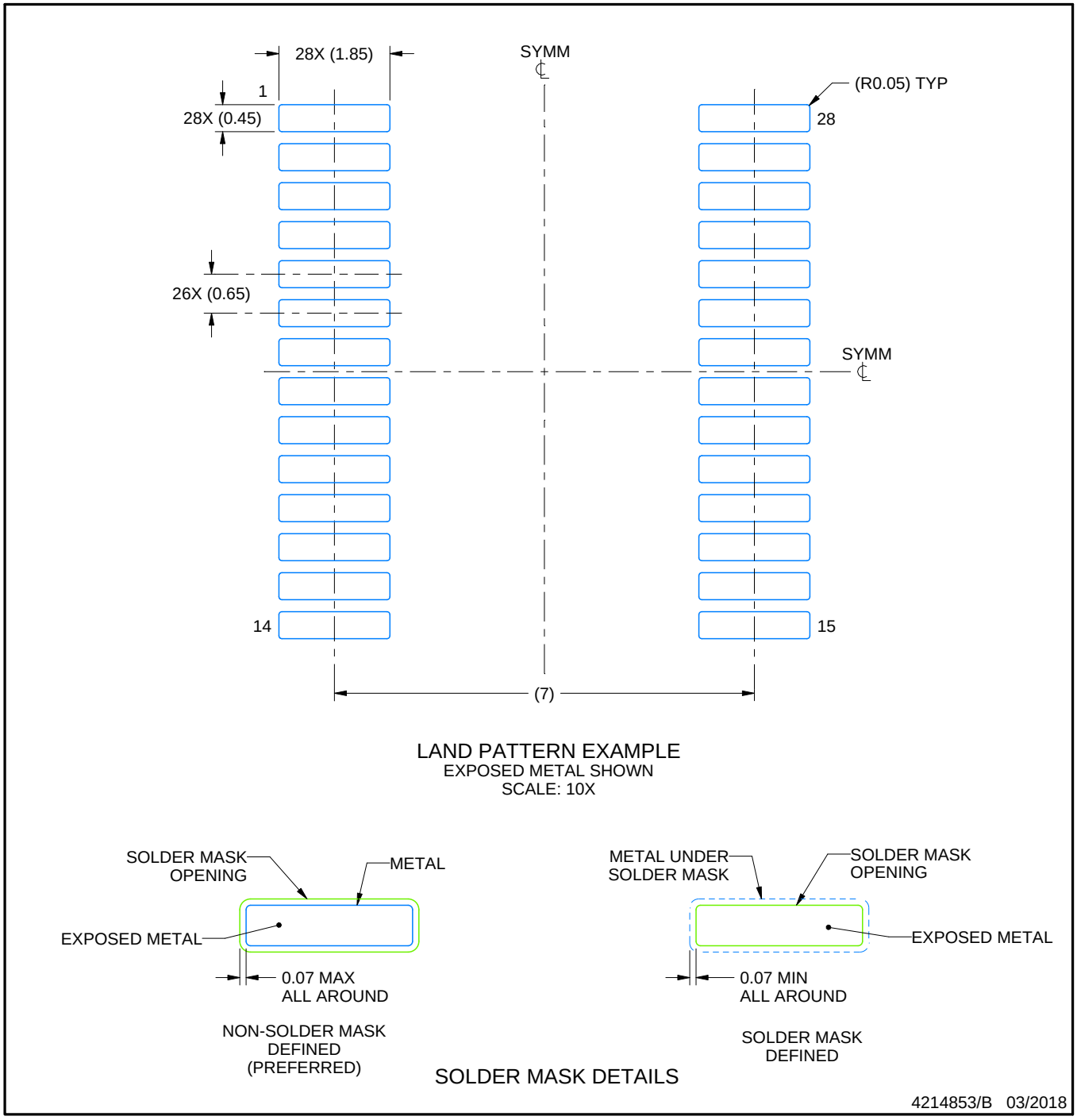
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



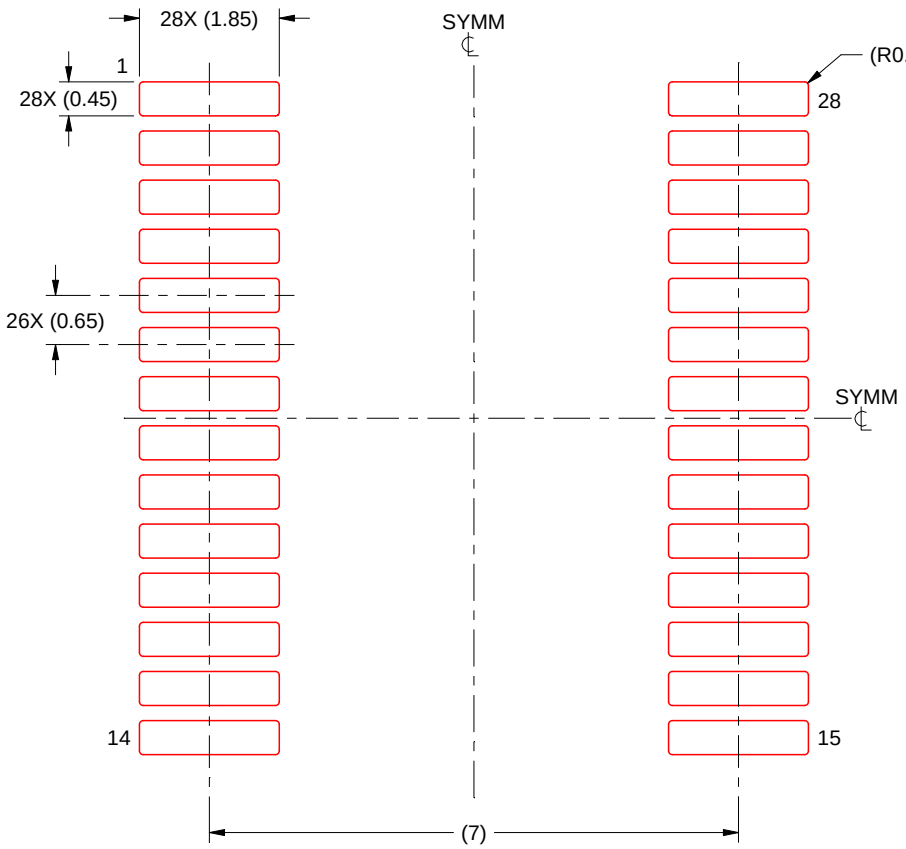
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265