TLV755P 500mA、低 I_Q、小型低压降稳压器

1 特性

- 输入电压范围：1.45V 至 5.5V
- 低 I_Q：25μA（典型值）
- 低压降：
  - 在 500mA 下为 238mV（最大值）（V_{OUT} 为 3.3V）
- 输出精度：1%（85°C 时达到最大）
- 内置软启动功能，具有单调 V_{OUT}上升
- 折返电流限制
- 有源输出放电
- 高 PSRR：100kHz 时为 46dB
- 与 1μF 陶瓷输出电容器搭配使用时可保持稳定
- 封装：
  - 2.9mm × 1.6mm SOT-23-5
  - 1mm x 1mm X2SON-4
  - 2mm × 2mm WSON-6

2 应用

- 机顶盒、电视和游戏机
- 便携式和电池供电类设备
- 台式机、笔记本和超级本
- 平板电脑和遥控器
- 白色家电和电器
- 电网基础设施和保护继电器
- 摄像头模块和图像传感器

3 说明

TLV755P 是一款超小型低静态电流、低压差稳压器 (LDO)，可提供 500mA 拉电流，具有良好的线路和负载瞬态性能。TLV755P 经过优化，支持 1.45V 至 5.5V 的输入电压 范围， 因此适用于各种应用。为最大程度地降低成本和解决方案尺寸，该器件可在 0.6V 至 5V 范围内提供固定输出电压，以支持现代微控制器 (MCU) 更低的内核电压。此外，TLV755P 具备带有使能功能的低 I_Q，从而可将待机功耗降至最低。该器件具有 内部软启动功能，旨在降低浪涌电流，因此可为负载提供受控电压并在启动过程中最大程度地降低输入电压压降。关断时，该器件可主动降低输出以快速释放输出并确保已知的启动状态。

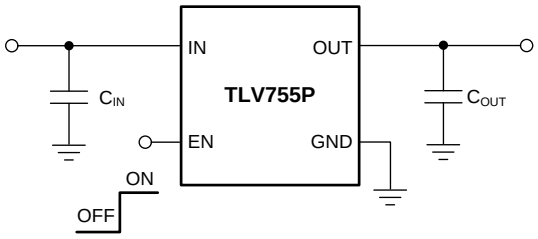
TLV755P 在与支持小尺寸总体解决方案的小型陶瓷输出电容器搭配使用时，可保持稳定。高精度带隙与误差放大器支持 1% 的典型精度。所有器件版本均具有集成的热关断保护、电流限制和低压锁定 (UVLO) 功能。TLV755P 具有内部折返电流限制，有助于在发生短路时减少热耗散。

器件信息(1)

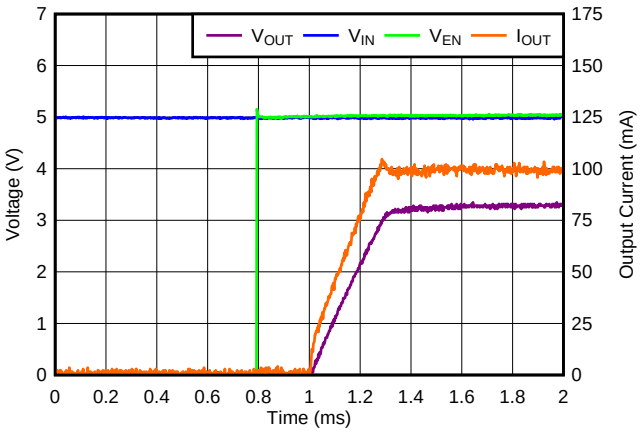
器件型号	封装	封装尺寸（标称值）
TLV755P	X2SON (4)	1.00mm x 1.00mm
	SOT-23 (5)	2.90mm × 1.60mm
	SON (6)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



启动波形



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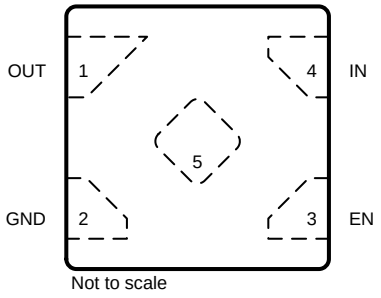
4 修订历史记录

Changes from Original (November 2017) to Revision A **Page**

- 已发布至生产 1

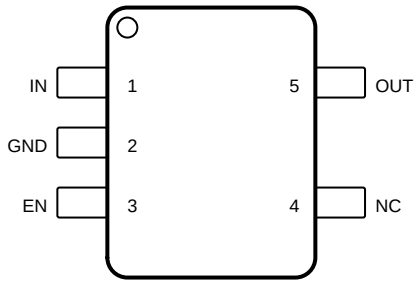
5 Pin Configuration and Functions

DQN Package
4-Pin X2SON
Top View



Not to scale

DBV Package
5-Pin SOT-23
Top View



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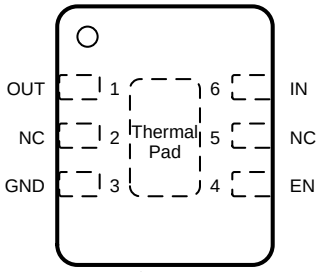
DRV Package
6-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

NC = no internal connection.

Pin Functions

PIN				I/O	DESCRIPTION
NAME	DQN	DBV	DRV		
EN	3	3	4	I	Enable pin. Drive EN greater than V_{HI} to turn on the regulator. Drive EN less than V_{LO} to place the LDO into shutdown mode.
GND	2	2	3	—	Ground pin.
IN	4	1	6	I	Input pin. A capacitor with a value of 1 µF or larger is required from this pin to ground(1). See the *Input and Output Capacitor Selection* section for more information.
NC	—	4	2, 5	—	No internal connection.
OUT	1	5	1	O	Regulated output voltage pin. A capacitor with a value of 1 µF or larger is required from this pin to ground(1). See the *Input and Output Capacitor Selection* section for more information.
Thermal pad	Pad	—	Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

(1) The nominal input and output capacitance must be greater than 0.47 µF; throughout this document the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 0.47 µF.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{IN}	-0.3	6.0	V
Enable voltage, V_{EN}	-0.3	6.0	V
Output voltage, V_{OUT}	-0.3	V_{IN} + 0.3(2)	V
Operating junction temperature range, T_J	-40	150	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.0 V, whichever is smaller

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.45		5.5	V
V_{OUT}	Output voltage	0.6		5.0	V
V_{EN}	Enable voltage	0		5.5	V
I_{OUT}	Output current	0		500	mA
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor	1		200	µF
f_{EN}	Enable toggle frequency			10	kHz
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV755			UNIT
		DQN (X2SON)	DBV (SOT-23-5)	DRV (SON)	
		4 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.4	231.1	100.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	139.1	118.4	108.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.4	64.4	64.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	28.4	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	101.7	63.8	64.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	88.4	N/A	34.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.45		5.5	V
V_{OUT}	Output voltage			0.6		5.0	V
	Output accuracy	-40°C ≤ T_J ≤ +85°C, DBV and DRV package		-1%		1%	
		V_{OUT} ≥ 1.0 V, DQN package		-1.2%		1.2%	
		-40°C ≤ T_J ≤ +85°C; 0.6 V ≤ V_{OUT} < 1.0 V		-10		10	mV
		V_{OUT} ≥ 1 V		-1.5%		1.5%	
		0.6 V ≤ V_{OUT} < 1 V		-15		15	mV
(ΔVOUT) ΔVIN	Line regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} > 1.5 V			2		mV
ΔVOUT/ ΔIOUT	Load regulation	0.1 mA ≤ I_{OUT} ≤ 500 mA	DQN package		0.036		V/A
			DBV package		0.060		
			DRV package		0.044		
I_{GND}	Ground current	T_J = 25°C, I_{OUT} = 0 mA		14	25	31	µA
		-40°C ≤ T_J ≤ +85°C, I_{OUT} = 0 mA				33	
		-40°C ≤ T_J ≤ +125°C, I_{OUT} = 0 mA				40	
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 1.4 V ≤ V_{IN} ≤ 5.5 V, -40°C ≤ T_J ≤ +125°C			0.1	1	µA
I_{CL}	Output current limit	V_{IN} = V_{OUT}+ $V_{DO(MAX)}$ + 0.25 V	V_{OUT} = V_{OUT} - 0.2 V, V_{OUT} ≤ 1.5V	560	720	865	mA
			V_{OUT} = 0.9 x V_{OUT}, 1.5V < V_{OUT} ≤ 4.5V	560	720	865	
I_{SC}	Short circuit current limit	V_{OUT} = 0 V			355		mA
V_{DO}	Dropout voltage	I_{OUT} = 500mA, -40°C ≤ T_J ≤ +85°C	0.6 V ≤ V_{OUT} < 0.8 V		675	1080	mV
			0.8 V ≤ V_{OUT} < 1.0V		600	930	
			1.0 V ≤ V_{OUT} < 1.2 V		550	780	
			1.2 V ≤ V_{OUT} < 1.5 V		500	630	
			1.5 V ≤ V_{OUT} < 1.8 V		350	400	
			1.8 V ≤ V_{OUT} < 2.5 V		325	380	
			2.5 V ≤ V_{OUT} < 3.3 V		250	300	
			3.3 V ≤ V_{OUT} < 5.0 V		150	215	
		I_{OUT} = 500mA, -40°C ≤ T_J ≤ +125°C	0.6 V ≤ V_{OUT} < 0.8 V			1140	
			0.8 V ≤ V_{OUT} < 1.0 V			985	
			1.0 V ≤ V_{OUT} < 1.2 V			825	
			1.2 V ≤ V_{OUT} < 1.5 V			665	
			1.5 V ≤ V_{OUT} < 1.8 V			425	
			1.8 V ≤ V_{OUT} < 2.5 V			400	
			2.5 V ≤ V_{OUT} < 3.3 V			325	
			3.3 V ≤ V_{OUT} < 5.0 V			238	
PSRR	Power-supply rejection ratio	f = 1 kHz, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50 mA			52		dB
		f = 100 kHz, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50 mA			46		
		f = 1 MHz, V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50 mA			52		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz; V_{OUT} = 1.2 V, I_{OUT} = 500 mA			71.5		$µV_{RMS}$
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.21	1.3	1.44	V
$V_{UVLO,HYST}$	Undervoltage lockout hysteresis	V_{IN} falling			40		mV
t_{STR}	Startup time				550		µs
V_{HI}	EN pin high voltage (enabled)			1			V

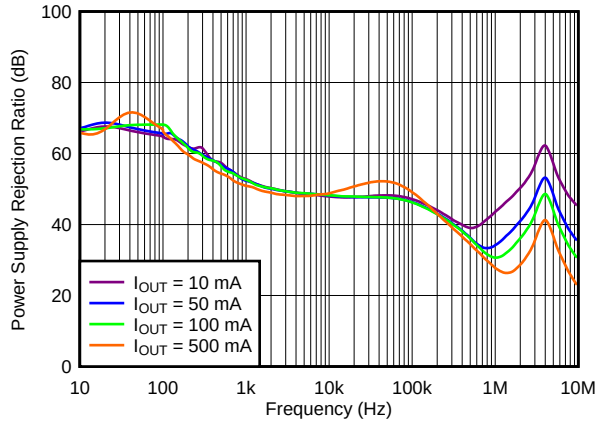
Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LO}	EN pin low voltage (enabled)				0.3	V
I_{EN}	Enable pin current	EN = 5.5V		10		nA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		155		
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 5.5V		120		Ω

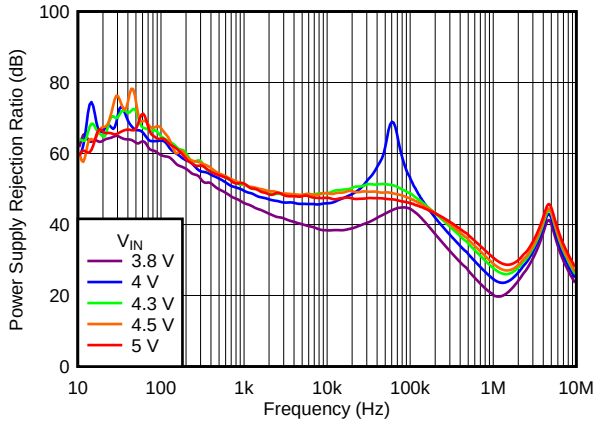
6.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



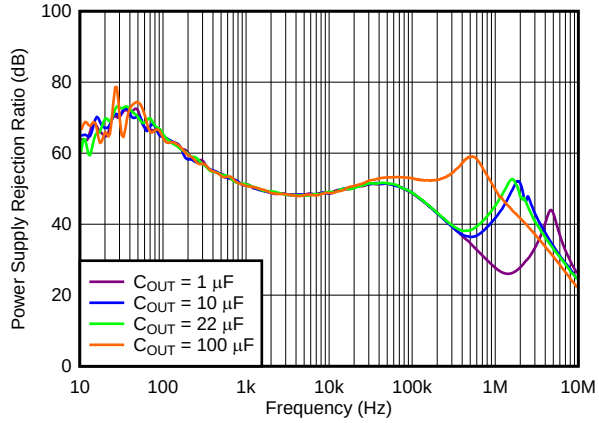
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

图 1. PSRR vs Frequency and I_{OUT}



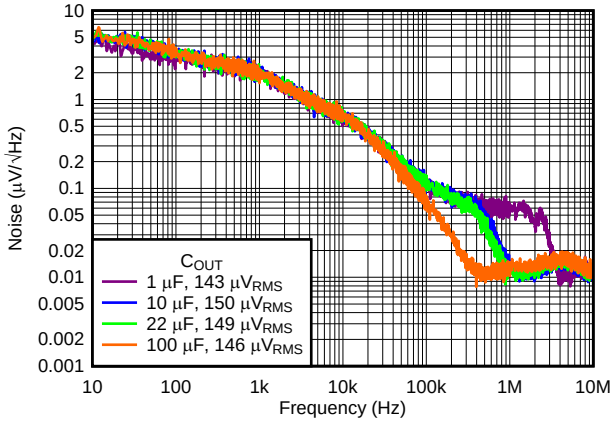
V_{OUT} = 3.3 V, C_{OUT} = 1 µF, I_{OUT} = 500 mA

图 2. PSRR vs Frequency and V_{IN}



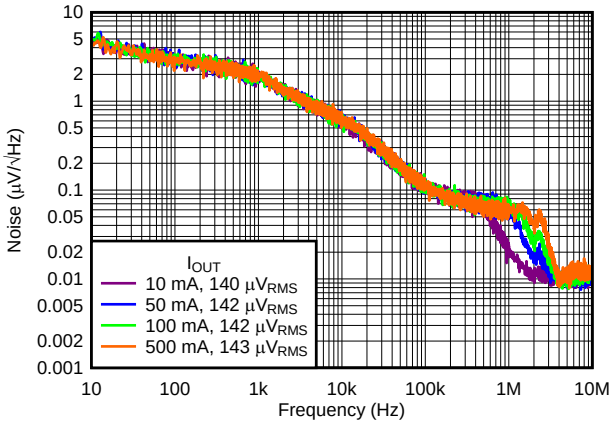
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

图 3. PSRR vs Frequency and C_{OUT}



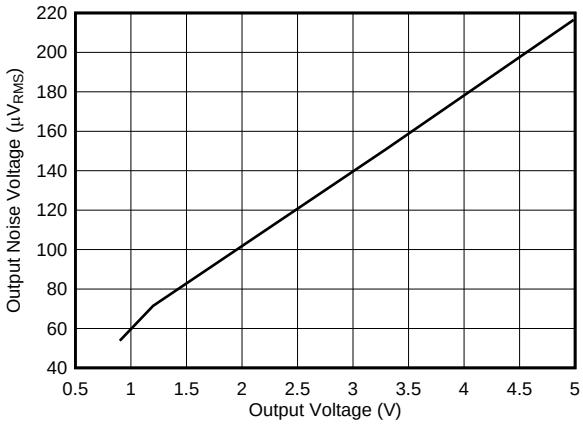
V_{OUT} = 3.3 V, V_{RMS} BW = 10 Hz to 100 kHz

图 4. Output Spectral Noise Density vs Frequency and C_{OUT}



V_{OUT} = 3.3 V, I_{OUT} = 500 mA, C_{OUT} = 1 µF, V_{RMS} BW = 10 Hz to 100 kHz

图 5. Output Spectral Noise Density vs Frequency and I_{OUT}

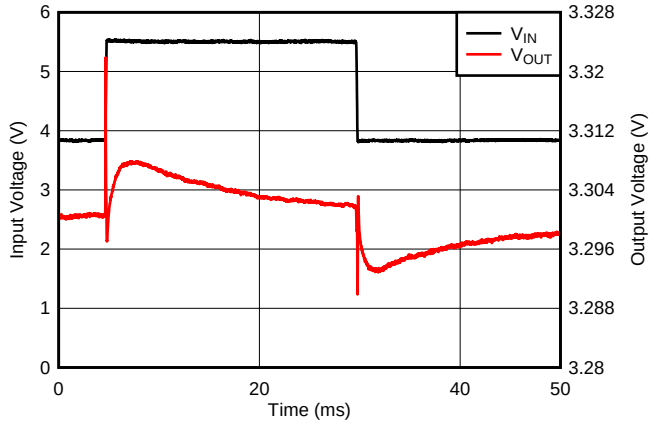


I_{OUT} = 500 mA, C_{OUT} = 1 µF, V_{RMS} BW = 10 Hz to 100 kHz

图 6. Output Noise Voltage vs V_{OUT}

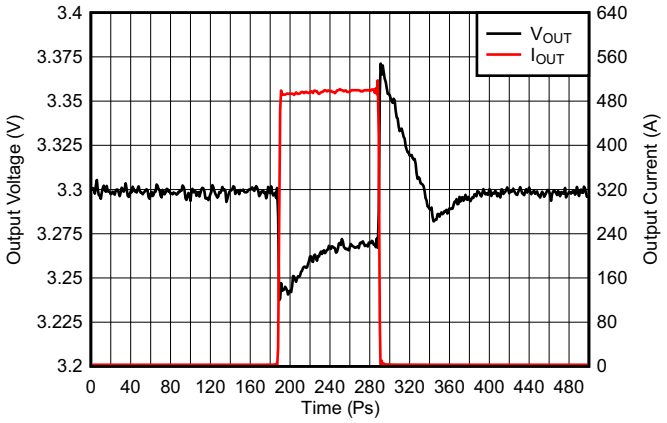
Typical Characteristics (接下页)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



V_{OUT} = 3.3 V, C_{OUT} = 1 µF, V_{IN} slew rate = 1 V/µs

图 7. Line Transient



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, I_{OUT} slew rate = 1 A/µs

图 8. 3.3-V, 1-mA to 500-mA Load Transient

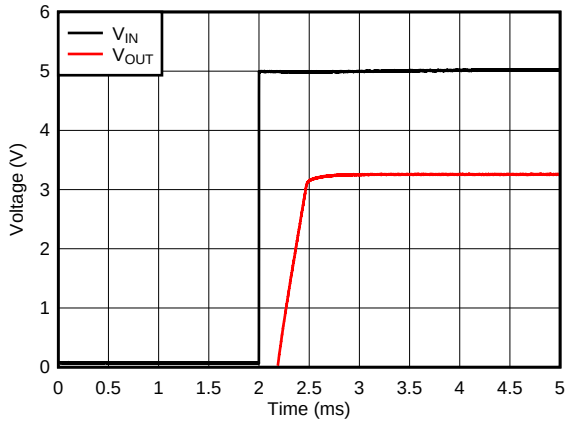


图 9. V_{IN} = V_{EN} Power-Up

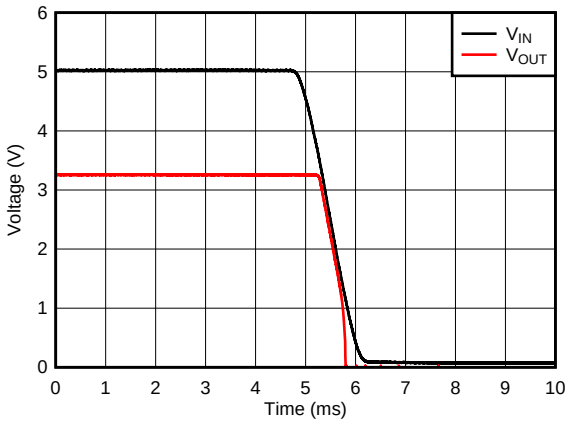
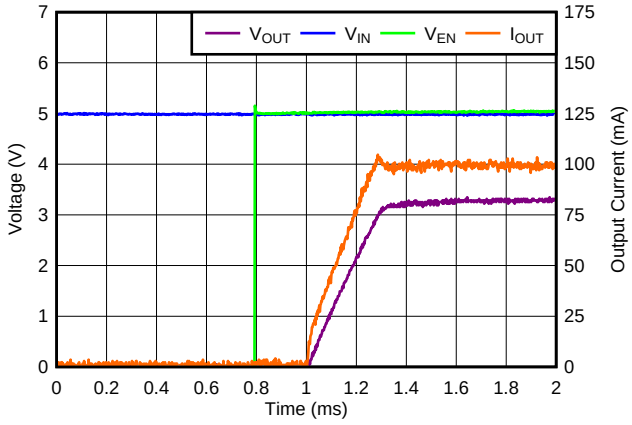


图 10. V_{IN} = V_{EN} Shutdown



V_{IN} = 5 V, I_{OUT} = 100 mA, V_{EN} slew rate = 1 V/µs, V_{OUT} = 3.3 V

图 11. EN Startup

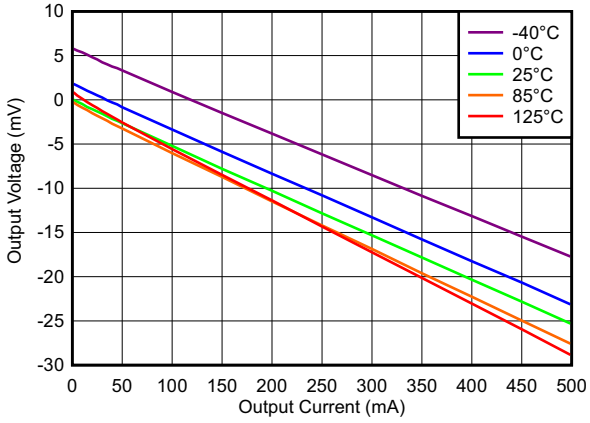


图 12. Load Regulation vs I_{OUT}

Typical Characteristics (接下页)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

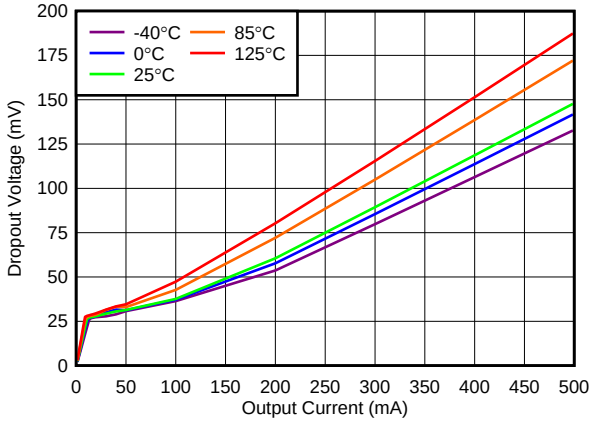


图 13. 3.3-V Dropout Voltage vs I_{OUT}

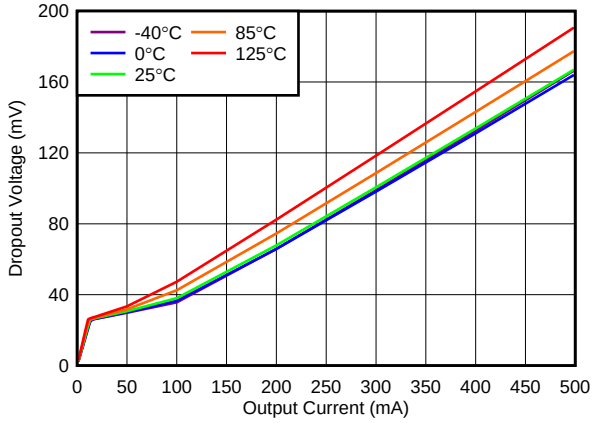
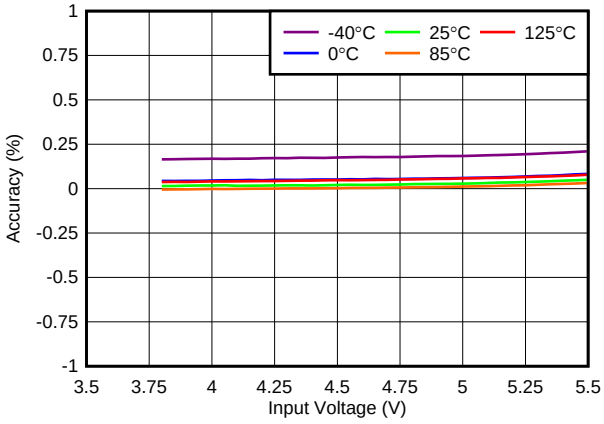
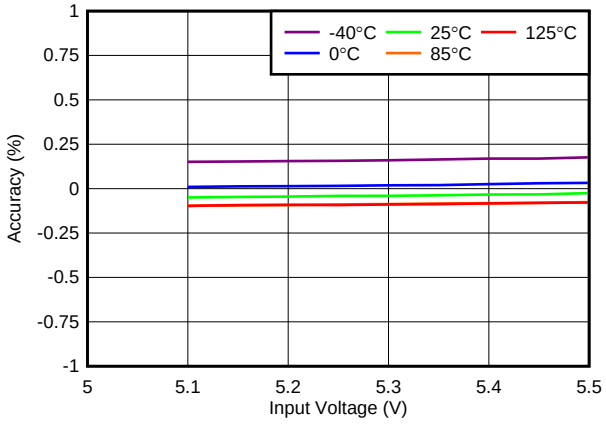


图 14. 5.0-V Dropout Voltage vs I_{OUT}



V_{OUT} = 3.3 V, I_{OUT} = 1 mA

图 15. 3.3-V Regulation vs V_{IN} (Line Regulation)



I_{OUT} = 1 mA, V_{OUT} = 5 V

图 16. 5.0-V Accuracy vs V_{IN} (Line Regulation)

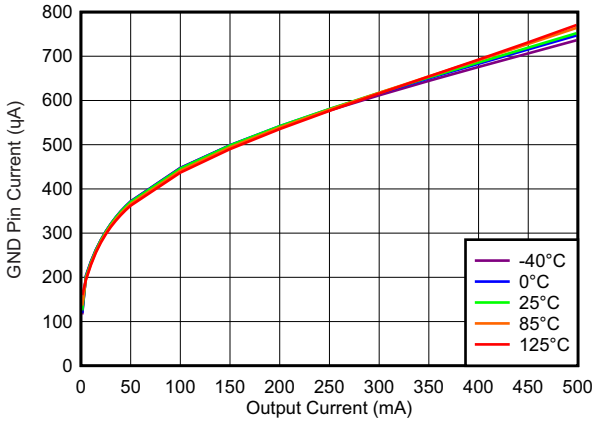
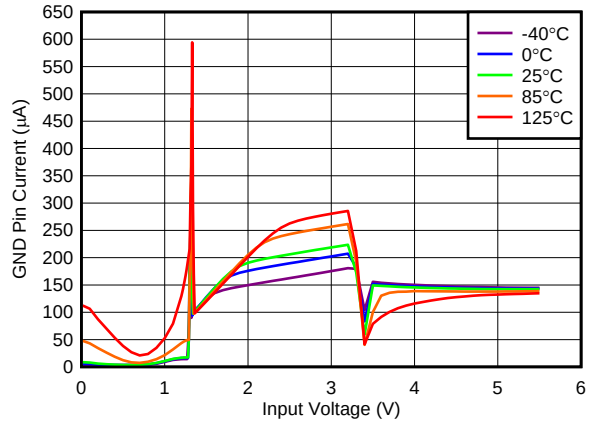


图 17. I_{GND} vs I_{OUT}



V_{OUT} = 3.3 V, I_{OUT} = 1 mA

图 18. I_{GND} vs V_{IN}

Typical Characteristics (接下页)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

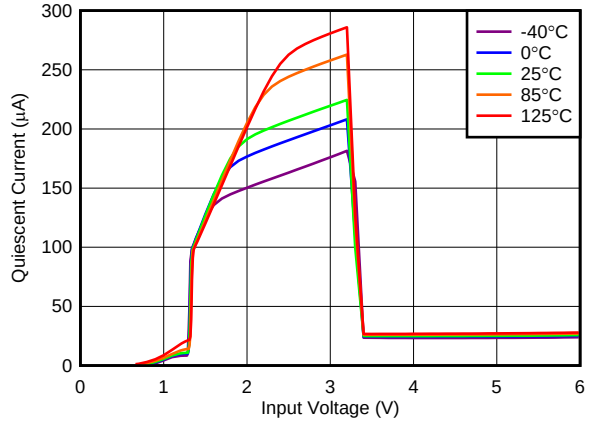


图 19. I_Q vs V_{IN}

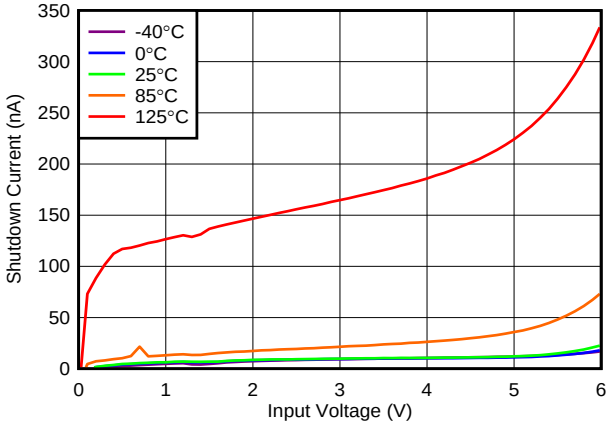


图 20. I_{SHDN} vs V_{IN}

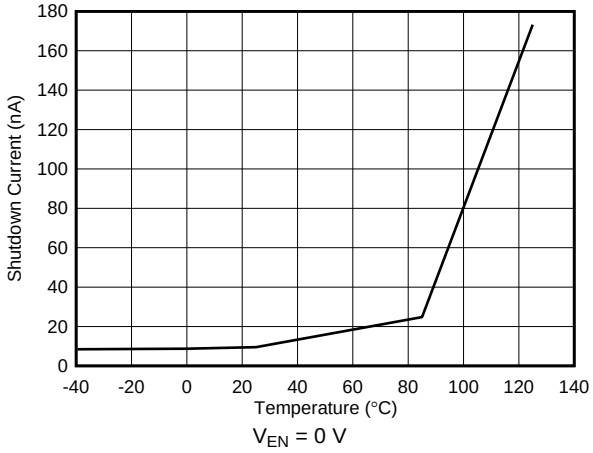


图 21. I_{SHDN} vs Temperature

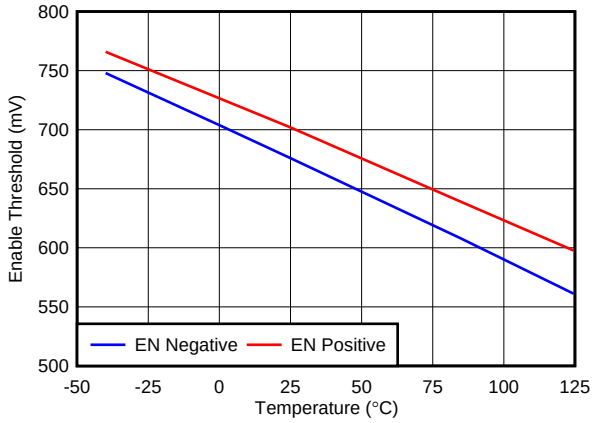


图 22. Enable Threshold vs Temperature

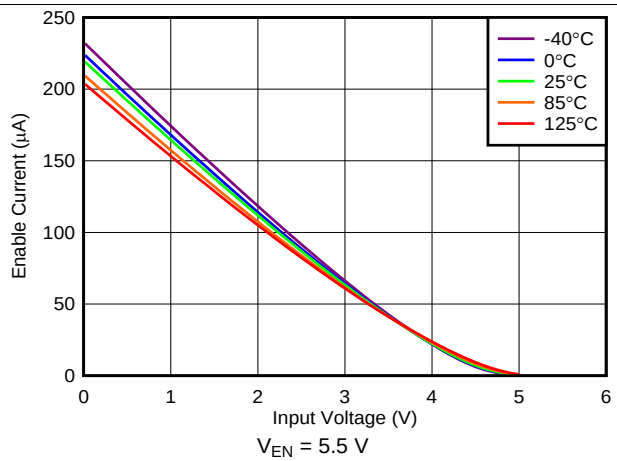


图 23. I_{EN} vs V_{IN}

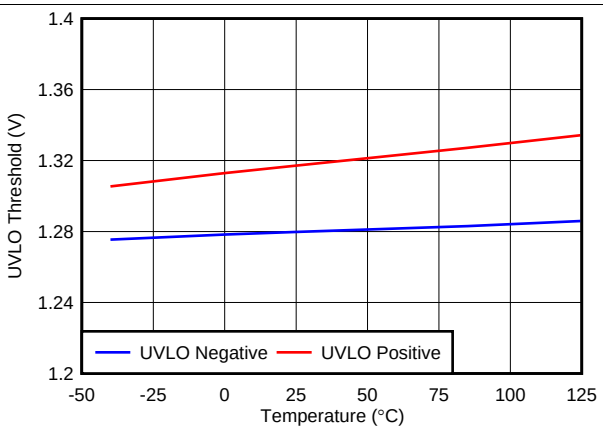


图 24. UVLO Threshold vs Temperature

Typical Characteristics (接下页)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

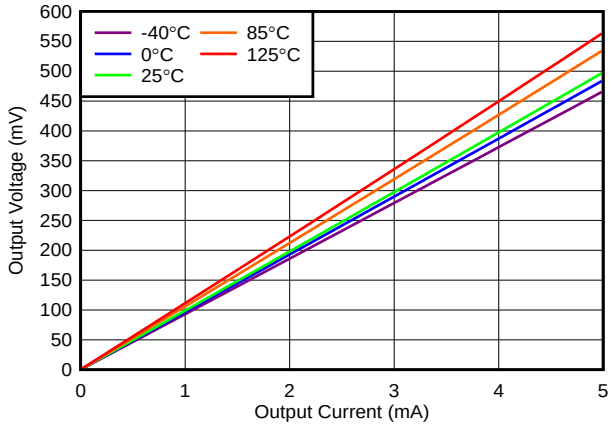


图 25. V_{OUT} vs I_{OUT} Pulldown Resistor

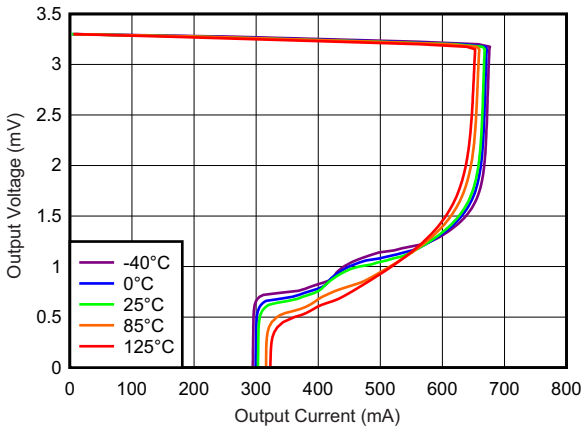


图 26. 3.3-V Foldback Current Limit, V_{OUT} vs I_{OUT}

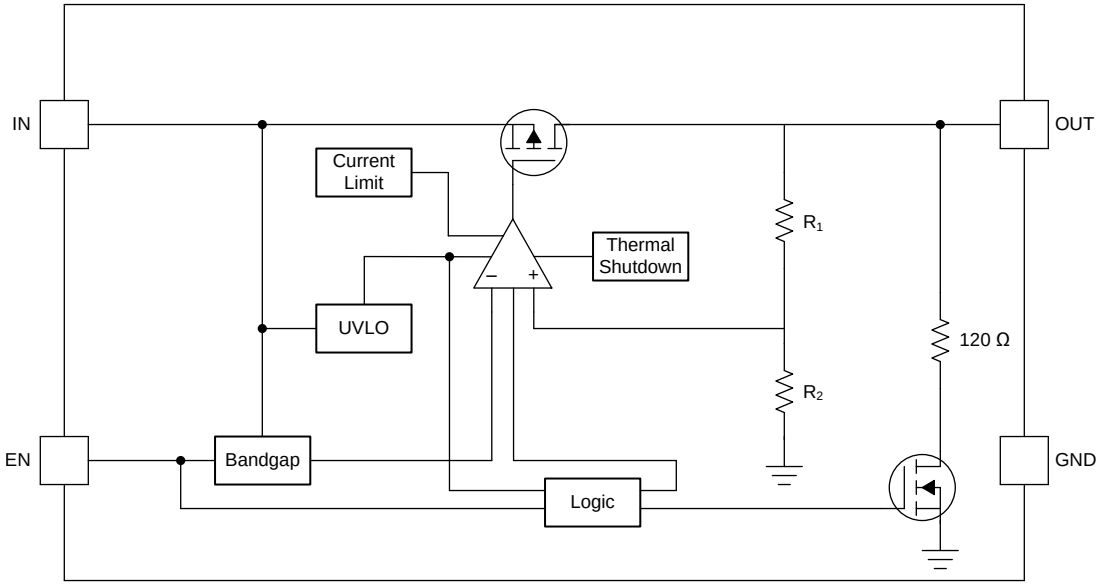
7 Detailed Description

7.1 Overview

The TLV755P belongs to a family of next-generation, low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. The TLV755P is optimized for a wide variety of applications by supporting an input voltage range from 1.45 V to 5.5 V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 0.6 V to 5 V to support the lower core voltages of modern microcontrollers (MCUs).

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature is –40°C to +125°C.

7.2 Functional Block Diagram



NOTE: R_2 = 550 kΩ, R_1 = adjustable.

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Enable (EN)

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed V_{HI}. Turn off the device by forcing the EN pin below V_{LO}. If shutdown capability is not required, connect EN to IN.

The device has an internal pulldown that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. 公式 1 calculates the time constant τ:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Feature Description (接下页)

The EN pin is independent of the input pin (IN), but if the EN pin is driven to a higher voltage than V_{IN}, the current into the EN pin increases. This effect is illustrated in 图 23. When the EN voltage is higher than the input voltage there is an increased current flow into the EN pin. If this increased flow causes problems in the application, sequence the EN pin after V_{IN} is high, or to tie EN to V_{IN} to prevent this flow increase from happening. If EN is driven to a higher voltage than V_{IN}, limit the frequency on EN to below 10 kHz.

7.3.3 Internal Foldback Current Limit

The TLV755P has an internal current limit that protects the regulator during fault conditions. The current limit is a hybrid scheme with brick wall until the output voltage is less than 0.4 V × $V_{OUT(NOM).}$ When the voltage drops below 0.4 V × $V_{OUT(NOM)}$, a foldback current limit is implemented that scales back the current as the output voltage approaches GND. When the output shorts, the LDO supplies a typical current of I_{SC}. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output shorts, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown.

The foldback current-limit circuit limits the current that is allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{CL}) during start up. See 图 26 for typical current limit values. If the output is loaded by a constant-current load during start up, or if the output voltage is negative when the device is enabled, then the load current demanded by the load may exceed the foldback current limit and the device may not rise to the full output voltage. For constant-current loads, disable the output load until the output has risen to the nominal voltage.

Excess inductance can cause the current limit to oscillate. Minimize the inductance to keep the current limit from oscillating during a fault condition.

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 165°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation that protects the circuit from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

表 1 lists a comparison between the normal, dropout, and disabled modes of operation.

表 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal(1)	$V_{IN} > V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout(1)	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	—	$T_J < T_{SD}$
Disabled(2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{LO}$	—	$T_J > T_{SD}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

7.4.1 Normal Operation

The device regulates to the nominal output voltage when all of the following conditions are met.

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device degrades because the pass device is in a triode state and no longer controls the output voltage of the LDO. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but not during startup), the pass-FET is driven as hard as possible when the control loop is out of balance. During the normal time required for the device to regain regulation, $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$, V_{OUT} can overshoot $V_{OUT(NOM)}$ during fast transients.

7.4.3 Disabled

The output is shut down by forcing the enable pin below V_{LO}. When disabled, the pass device is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal switch from the output to ground. The active pulldown is on when sufficient input voltage is provided.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TLV755P requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in capacitance value and equivalent series resistance (ESR) over temperature. When selecting a capacitor for a specific application, consider the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. As a general rule, ceramic capacitors must be derated by 50%. For best performance, TI recommends a maximum output capacitance value of 200 µF.

Place a 1 µF or greater capacitor on the input pin of the LDO. Some input supplies have a high impedance. Placing a capacitor on the input supply reduces the input impedance. The input capacitor counteracts reactive input sources and improves transient response and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors are used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

The TLV755P uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales linearly with the output current because the PMOS device functions like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See 图 13 and 图 14 for typical dropout values.

8.1.3 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up when the slew rate and voltage levels are in the correct range; see 图 27. Use an enable signal to avoid this condition.

Application Information (接下页)

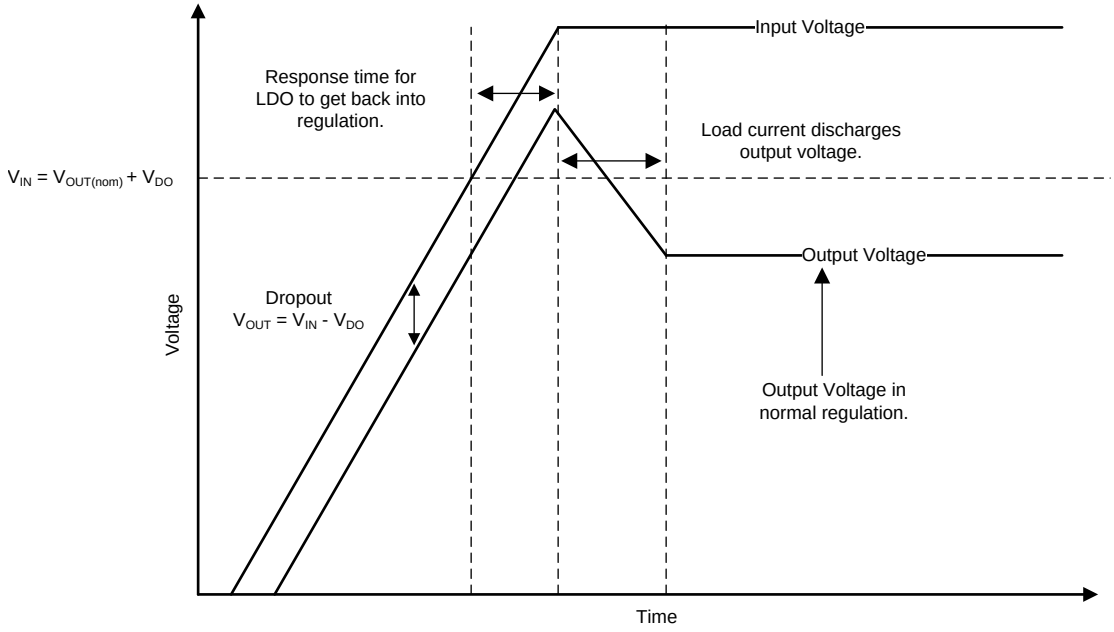


图 27. Startup Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. 图 28 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs while the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

Application Information (接下页)

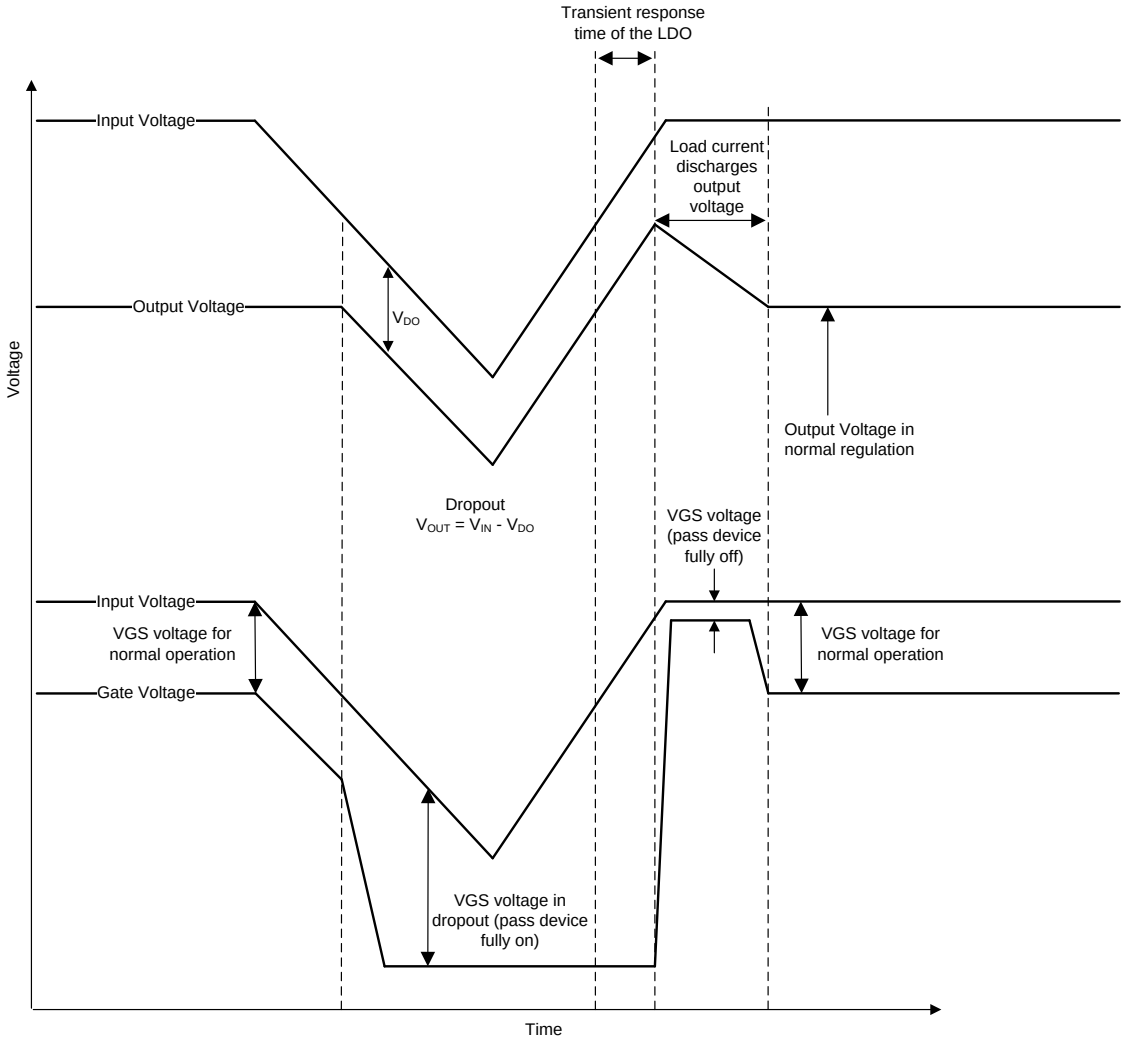


图 28. Line Transients From Dropout

8.1.4 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

Application Information (接下页)

If reverse current flow is expected in the application, external protection must be used to protect the device. 图 29 shows one approach of protecting the device.

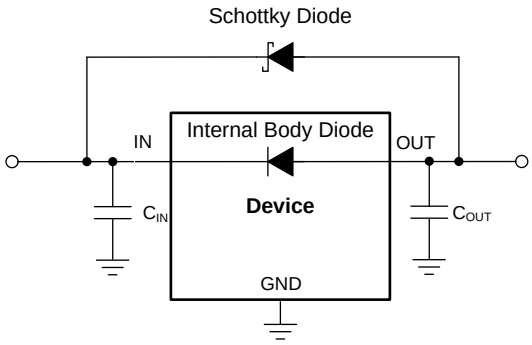


图 29. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free of other heat-generating devices as possible that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 公式 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation must be minimized to achieve greater efficiency. This minimizing process is achieved by selecting the correct system voltage rails. Proper selection helps obtain the minimum input-to-output voltage differential. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat-conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to inner plane areas or to a bottom-side copper plane.

The maximum allowable junction temperature (T_J) determines the maximum power dissipation for the device. According to 公式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air (T_A).

$$T_J = T_A + R_{\theta JA} \times P_D \quad (3)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ value is only used as a relative measure of package thermal performance. $R_{\theta JA}$ is the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

Application Information (接下页)

8.1.5.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not thermal resistances, but offer practical and relative means of estimating junction temperatures. These psi metrics are independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 公式 4 and are described in the table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as shown in 公式 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

(4)

8.2 Typical Application

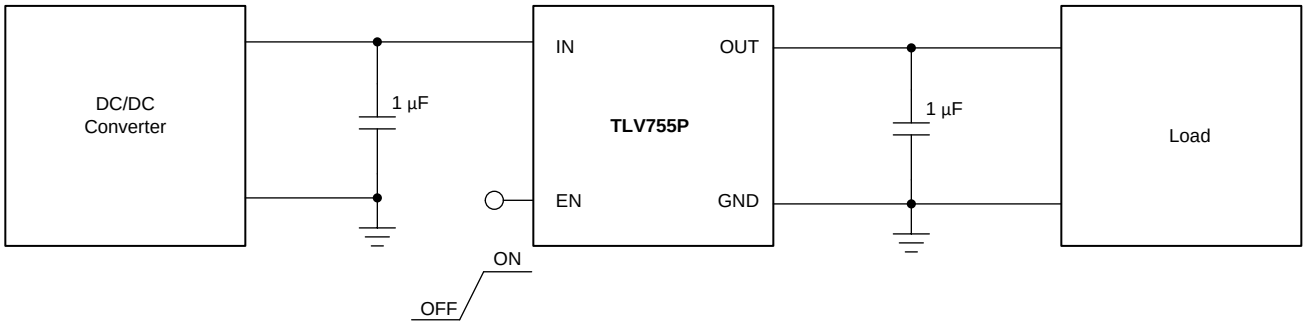


图 30. TLV755P Typical Application

8.2.1 Design Requirements

表 2 lists the design requirements for this application.

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.3 V
Output voltage	3.3 V
Input current	500 mA (maximum)
Output load	250-mA DC
Maximum ambient temperature	70°C

8.2.2 Detailed Design Procedure

8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use 公式 5 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right]$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance (5)

8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 公式 6 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ as 公式 7 shows and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (6)$$

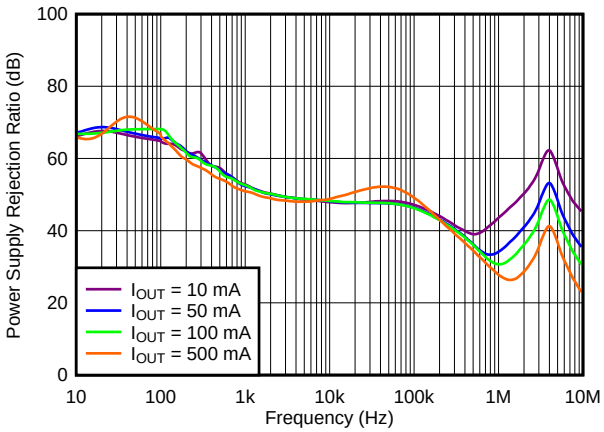
$$T_J = R_{\theta JA} \times P_D + T_A \quad (7)$$

Calculate the maximum ambient temperature as 公式 8 shows if the ($T_{J(MAX)}$) value does not exceed 125°C. 公式 9 calculates the maximum ambient temperature with a value of 99.95°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (8)$$

$$T_{A(MAX)} = 125°C - 100.2°C/W \times (4.3\ V - 3.3\ V) \times (0.25\ A) = 99.95°C \quad (9)$$

8.2.3 Application Curve



V_{IN} = 4.3 V, V_{OUT} = 3.3 V

图 31. PSRR vs Frequency (4.3 V to 3.3 V)

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV755P. If the input source is reactive, consider using multiple input capacitors in parallel with the 1-µF input capacitor to lower the input supply impedance over frequency.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close as possible to the device.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.

10.2 Layout Examples

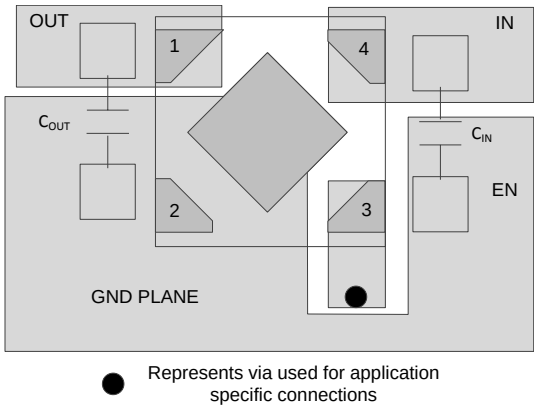


图 32. Layout Example for the DQN Package

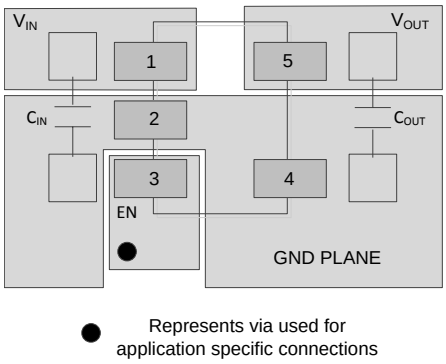


图 33. Layout Example for the DBV Package

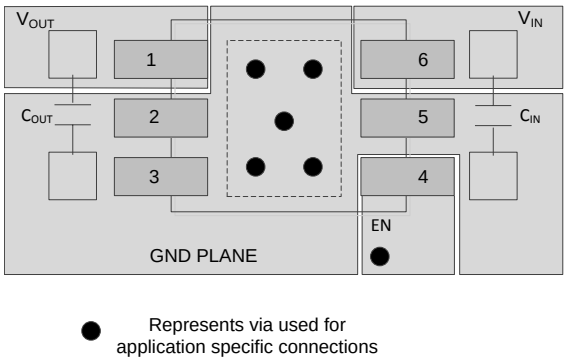


图 34. Layout Example for the DRV Package

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

表 3. 器件命名规则(1)(2)

产品	V_{OUT}
TLV755**xx(x)Pyyyz**	**xx(x)** 为标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；125 = 1.25V）。 **P** 表示有源输出放电功能。TLV755P 系列的所有产品在器件处于禁用状态时都可以对输出进行主动放电。 **yyy** 为封装标识符。 **z** 为封装数量。R 表示卷（3000 片），T 表示带（250 片）。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹（www.ti.com.cn）。
(2) 可提供 0.6V 至 5V 范围内的输出电压（以 50mV 为单位增加）。有关器件的详细信息和供货情况，请联系制造商。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV75507PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KD	Samples
TLV75507PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KD	Samples
TLV75509PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1HAF	Samples
TLV75509PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AX	Samples
TLV75509PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AX	Samples
TLV75509PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HDH	Samples
TLV75510PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FPF	Samples
TLV75510PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KE	Samples
TLV75510PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KE	Samples
TLV75510PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GUH	Samples
TLV75511PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E8	Samples
TLV75512PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FQF	Samples
TLV75512PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AG	Samples
TLV75512PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AG	Samples
TLV75512PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GVH	Samples
TLV75515PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FRF	Samples
TLV75515PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KF	Samples
TLV75515PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KF	Samples
TLV75515PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GWH	Samples
TLV755185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EZ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV75518PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FSF	Samples
TLV75518PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AI	Samples
TLV75518PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AI	Samples
TLV75518PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GXH	Samples
TLV75519PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1HBF	Samples
TLV75519PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B5	Samples
TLV75519PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B5	Samples
TLV75519PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HEH	Samples
TLV75525PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FTF	Samples
TLV75525PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AJ	Samples
TLV75525PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AJ	Samples
TLV75525PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GZH	Samples
TLV75528PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FUF	Samples
TLV75528PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KG	Samples
TLV75528PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KG	Samples
TLV75528PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H1H	Samples
TLV75529PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1HCF	Samples
TLV75529PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HFH	Samples
TLV75530PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FVF	Samples
TLV75530PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KI	Samples
TLV75530PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV75530PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H2H	Samples
TLV75533PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FWF	Samples
TLV75533PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AN	Samples
TLV75533PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AN	Samples
TLV75533PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H3H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

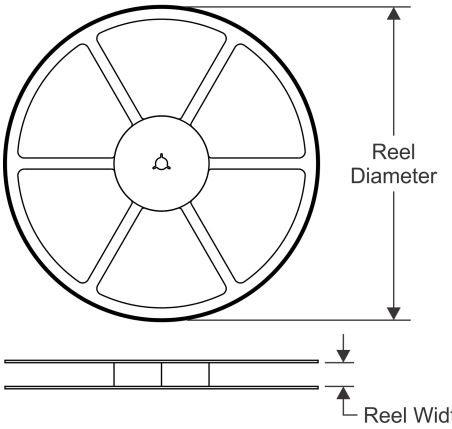
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

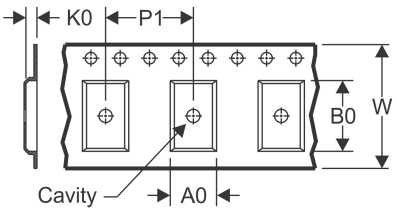
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

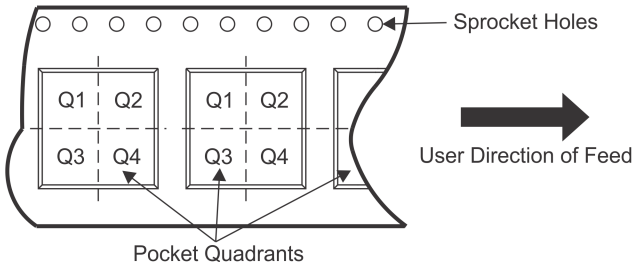


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



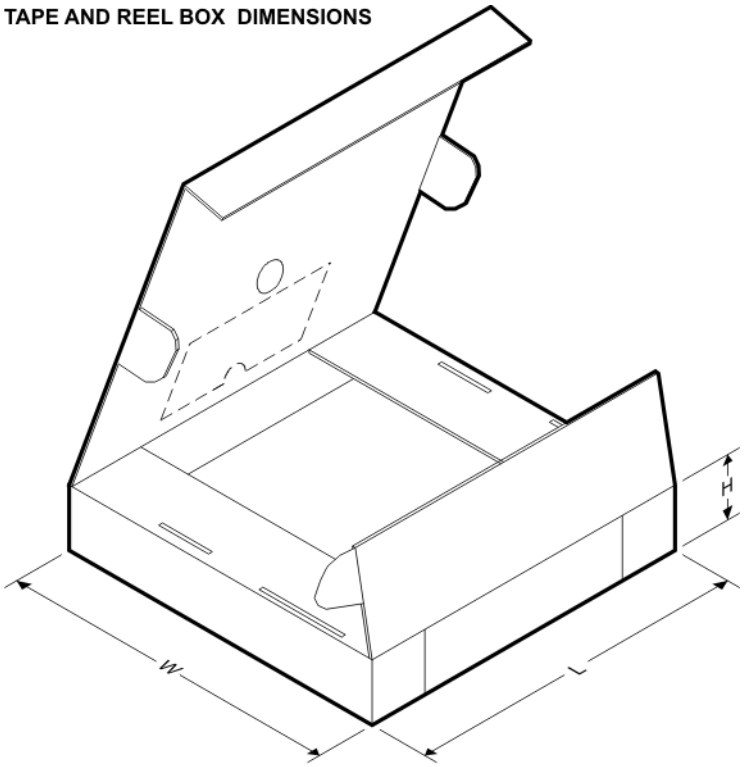
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75507PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75507PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75507PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75507PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75509PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV75509PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75509PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75509PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75509PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75509PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75509PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75510PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75510PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75510PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75510PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75510PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75510PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75511PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75512PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75512PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75512PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75512PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75512PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75512PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75515PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75515PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV75515PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75515PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75515PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75515PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75515PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV755185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75518PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV75518PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75518PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75518PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75518PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75518PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75518PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75519PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75519PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75519PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75519PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75519PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75519PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75525PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV75525PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75525PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75525PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75525PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75525PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75525PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75528PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75528PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75528PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75528PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75528PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75528PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75529PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75529PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75530PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75530PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75530PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75530PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75530PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75530PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75533PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75533PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV75533PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75533PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75533PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75533PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75533PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75507PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75507PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75507PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75507PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75509PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75509PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75509PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75509PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75509PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75509PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75509PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75510PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75510PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75510PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75510PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75510PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75510PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75511PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75512PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75512PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75512PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75512PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75512PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75512PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75515PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75515PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV75515PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75515PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75515PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75515PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75515PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV755185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75518PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV75518PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75518PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75518PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75518PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75518PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75518PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75519PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75519PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75519PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75519PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75519PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75519PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75525PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV75525PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75525PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75525PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0

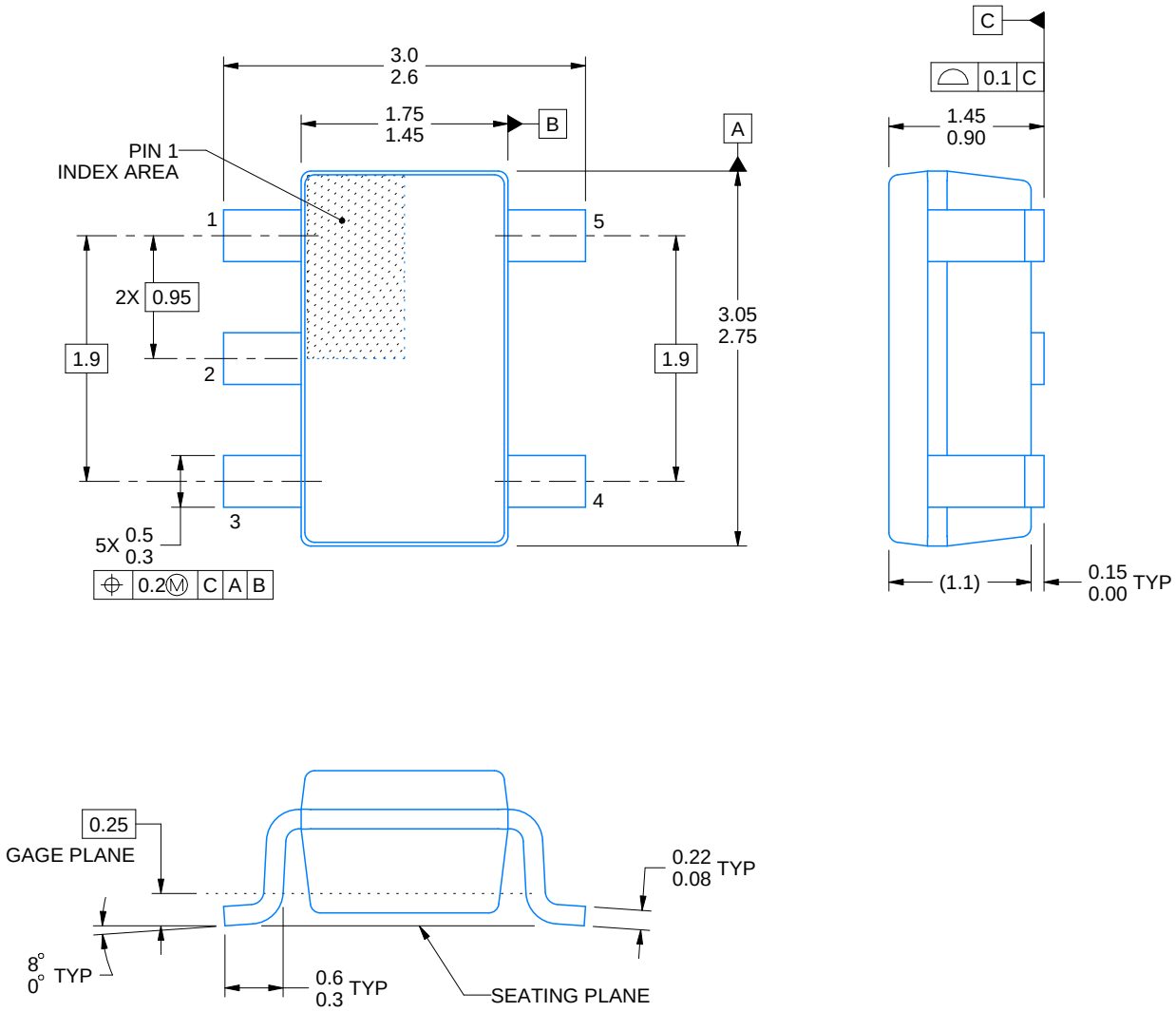
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75525PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75525PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75525PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75528PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75528PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75528PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75528PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75528PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75528PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75529PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75529PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75530PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75530PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75530PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75530PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75530PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75530PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75533PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75533PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV75533PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75533PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75533PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75533PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75533PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

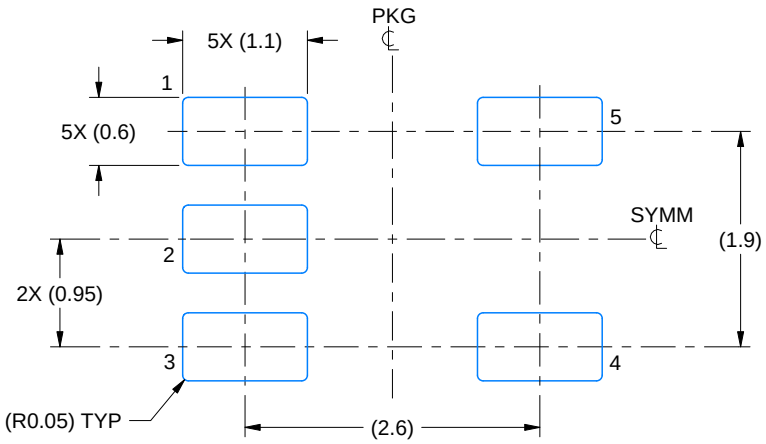
SMALL OUTLINE TRANSISTOR



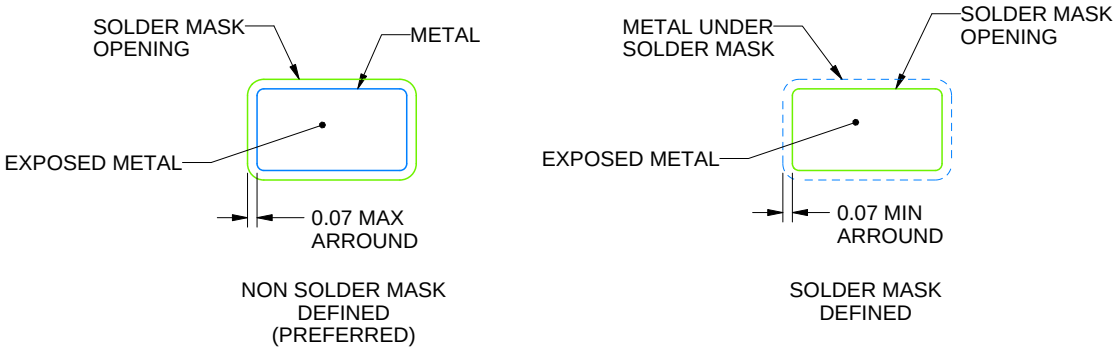
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

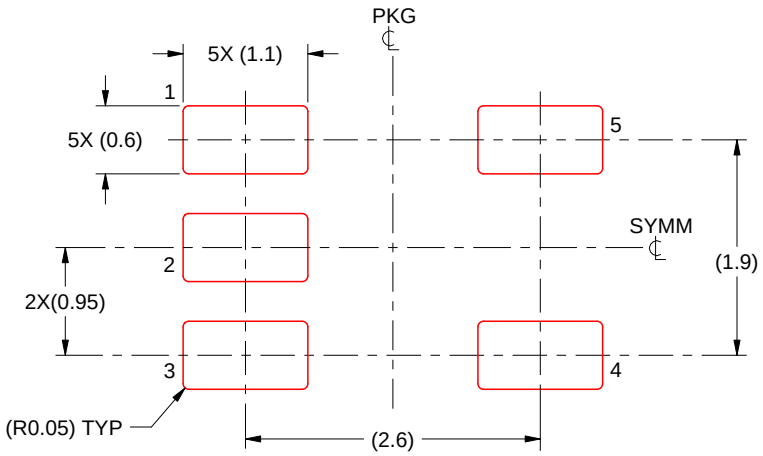


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

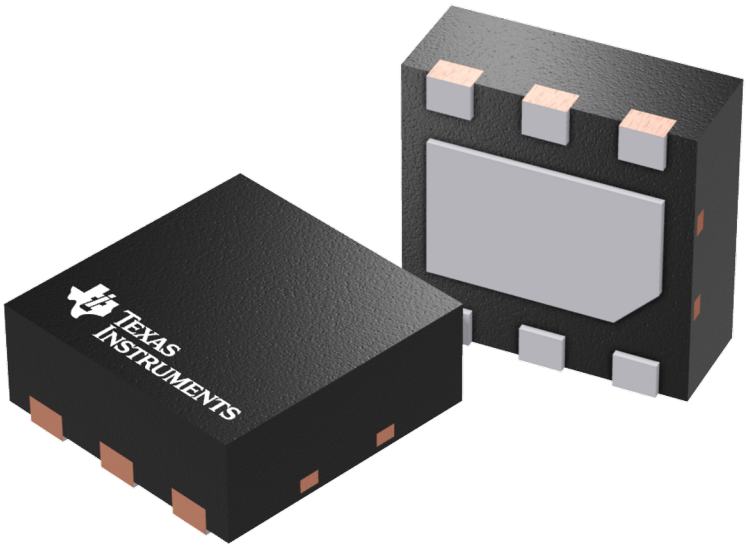
4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



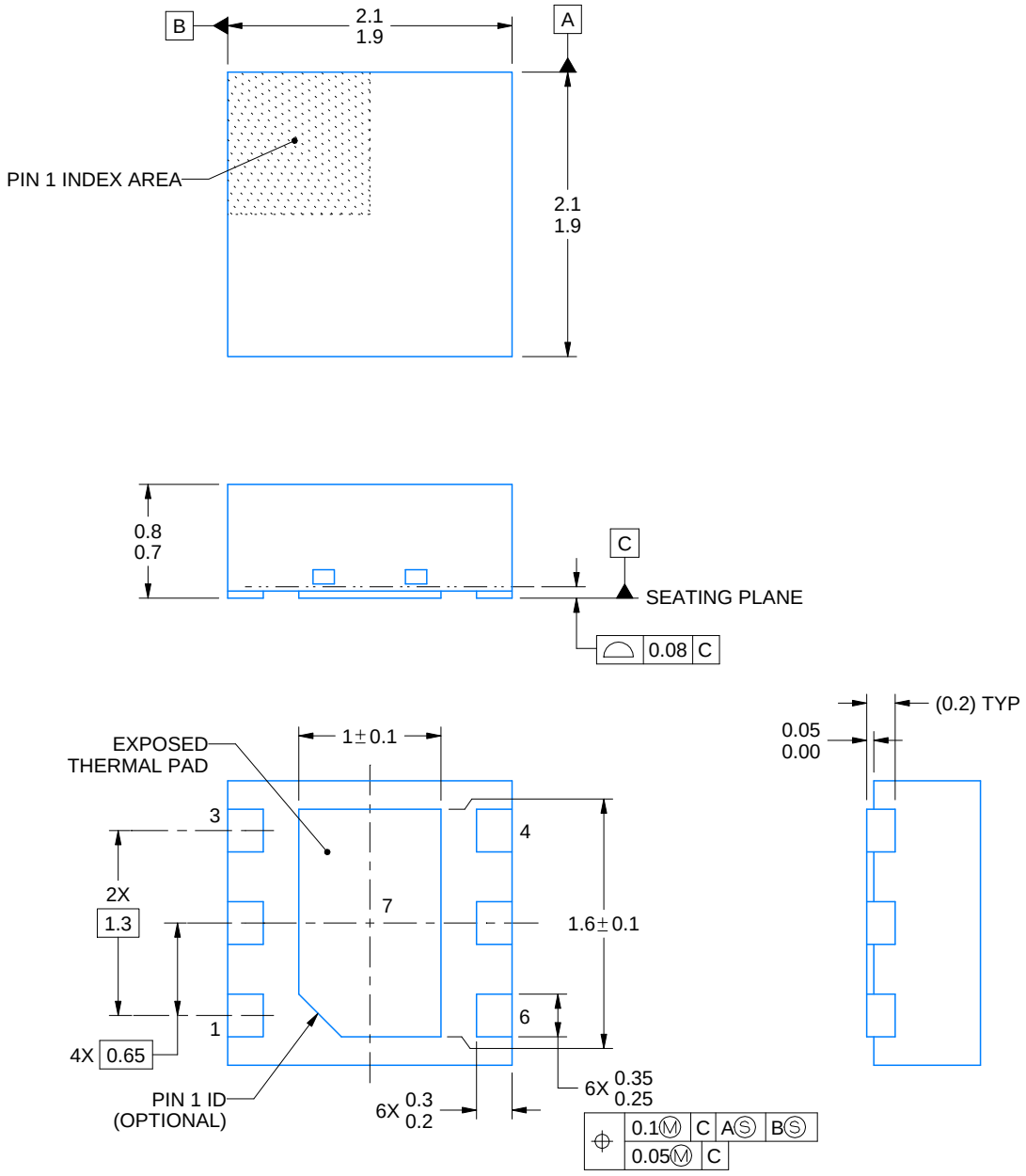
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

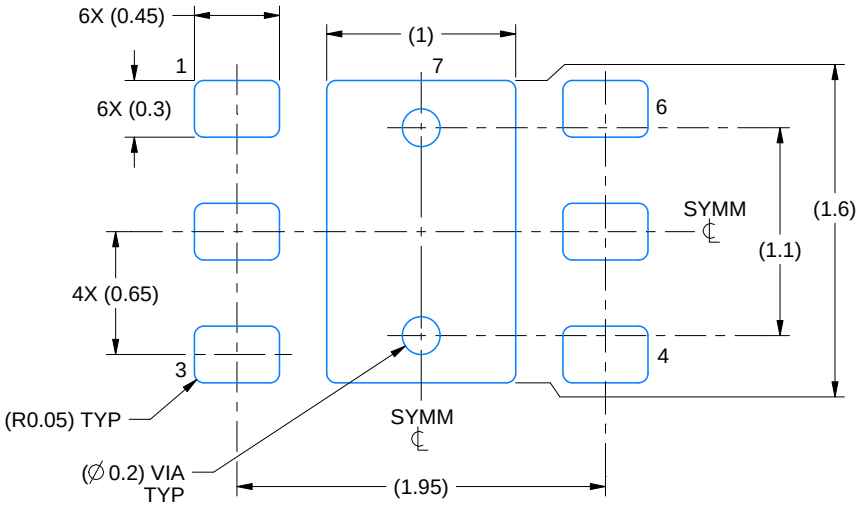
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

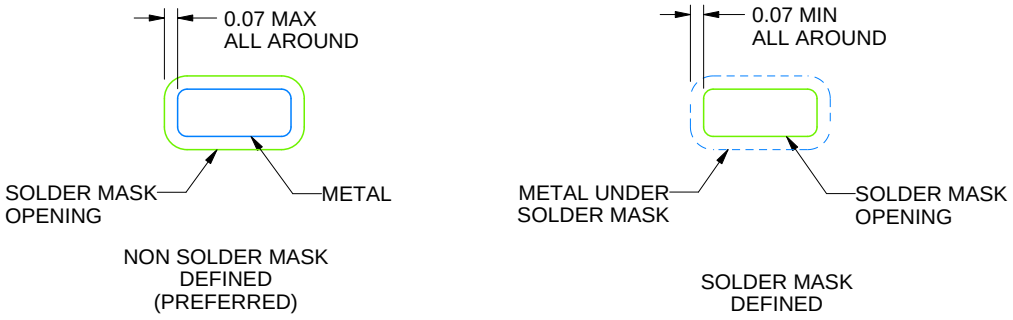


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

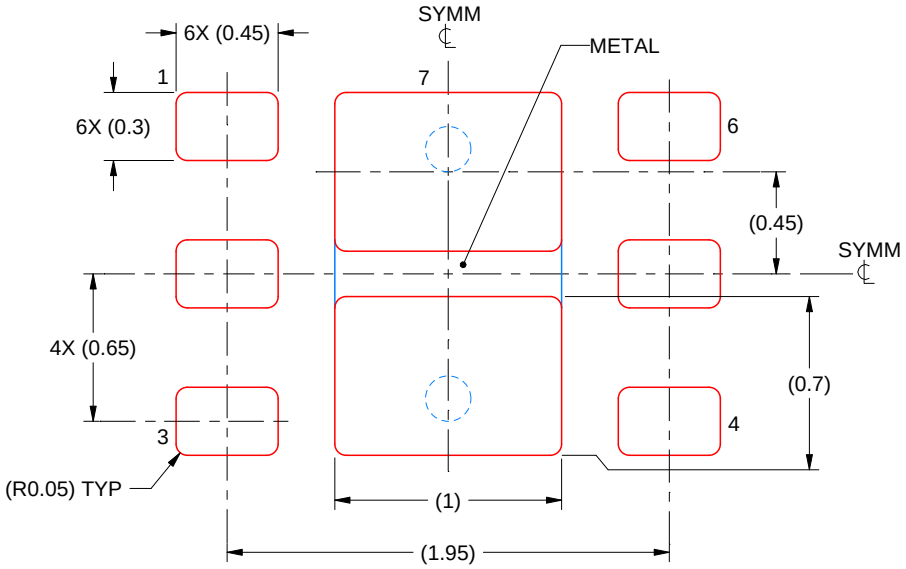
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

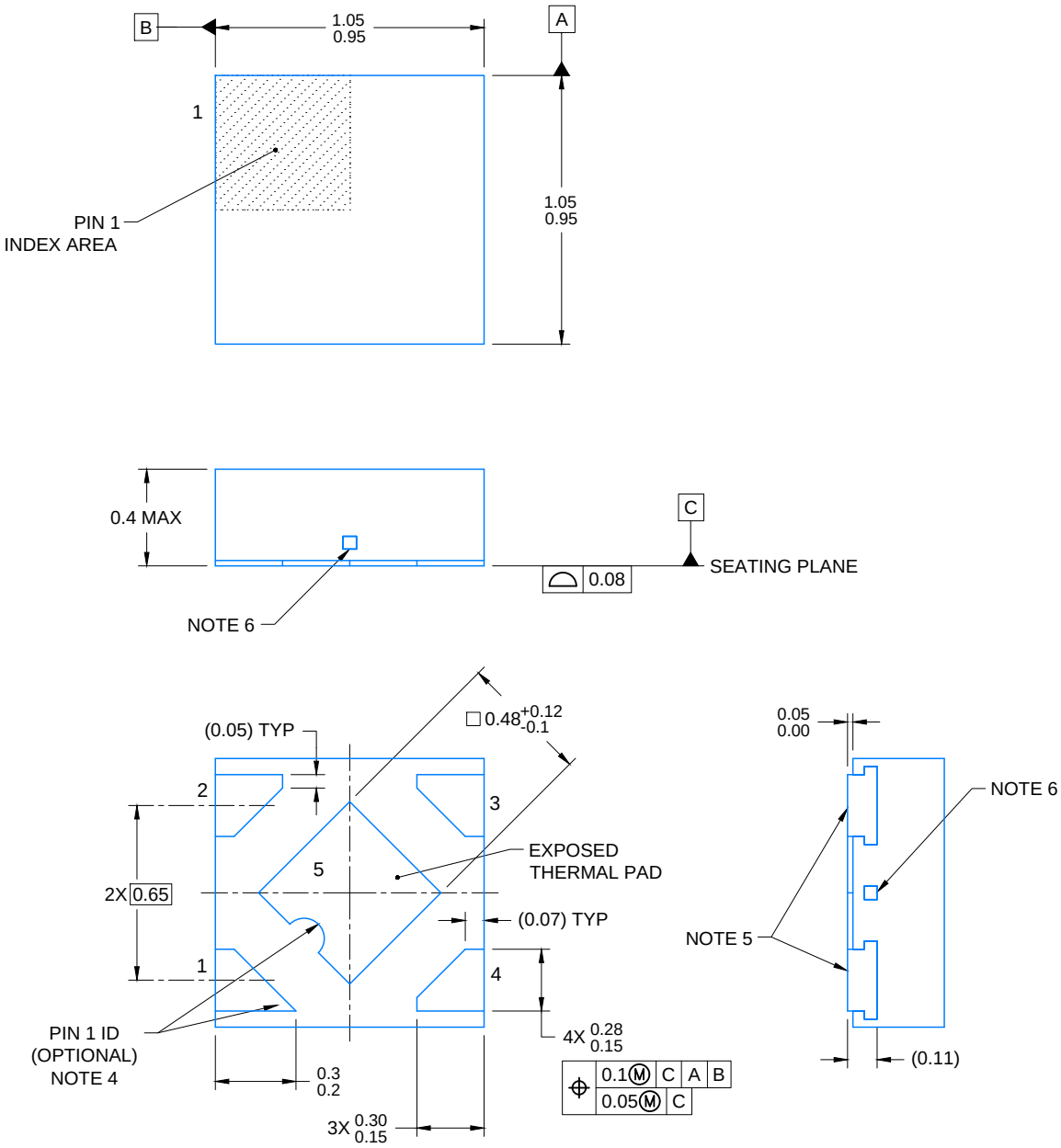
4210367/F

PACKAGE OUTLINE

DQN0004A

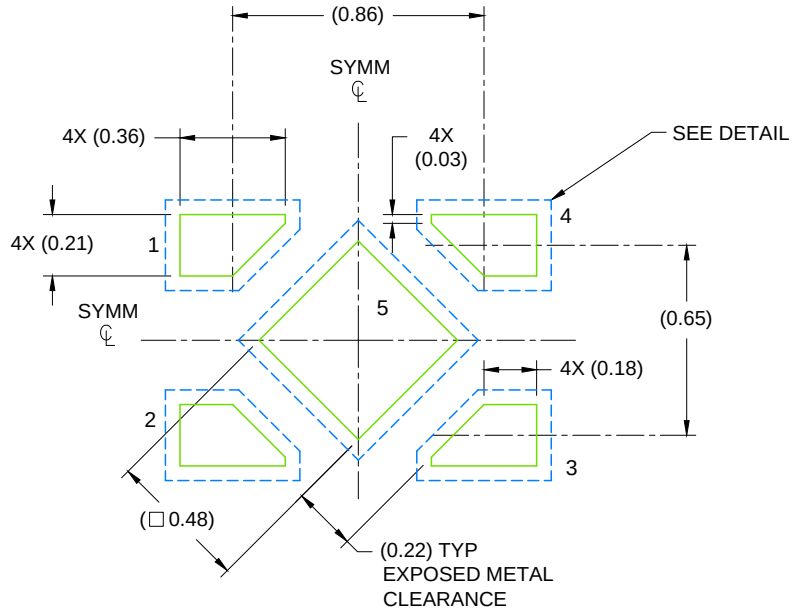
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



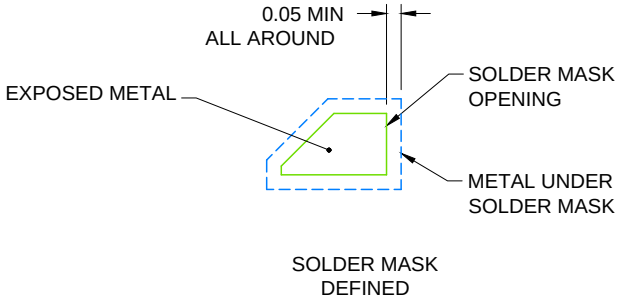
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

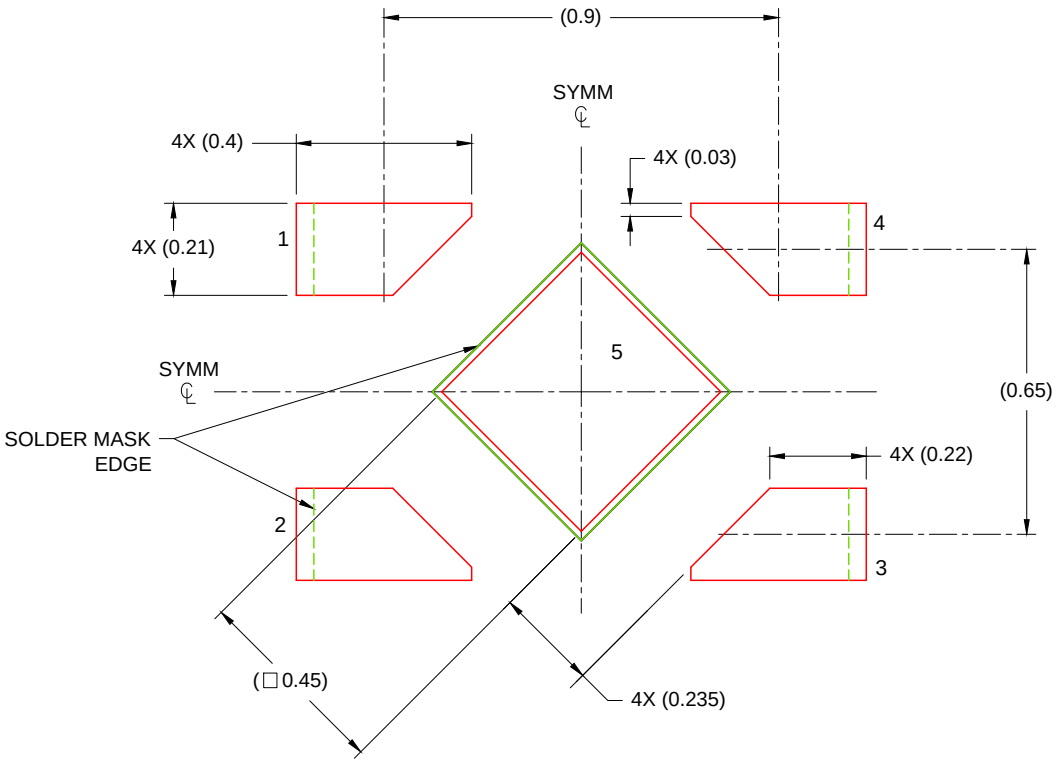


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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