

SN74LVC1G79 单路正缘触发 D 型触发器

1 特性

- 采用德州仪器 (TI) 的 NanoFree™ 封装
- 锁断性能超过 100mA, 符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
 - 2000V 人体放电模型 (A114-A)
 - 200V 机器放电模式 (A115-A)
 - 1000V 组件充电模式 (C101)
- 支持 5V V_{CC} 运行
- 输入接受的电压达到高达 5.5V
- 支持向下转换到 V_{CC}
- 3.3V 和 50pF 负载下最大 t_{pd} 为 6ns
- 低功耗, 10 μ A 最大 I_{CC}
- 电压为 3.3V 时, 输出驱动为 ± 24 mA
- I_{off} 支持部分断电模式和后驱动保护

2 应用

- 测试和测量
- 企业交换
- 电信基础设施
- 个人电子产品
- 白色家电

3 说明

SN74LVC1G79 器件是一种的单路正缘触发 D 型触发器, 专门为 1.65V 到 5.5V V_{CC} 操作而设计。

当数据输入 (D) 处的数据满足设置时间要求时, 将该数据传输到时钟脉冲正向缘上的 Q 输出。时钟触发出现在一个特定电压电平上, 并且不与时钟脉冲的上升时间直接相关。经过保持时间间隔后, 可以更改 D 输入处的数据而不影响输出处的电平。

NanoFree™ 封装技术是 IC 封装概念的一项重大突破, 它将硅晶片用作封装。

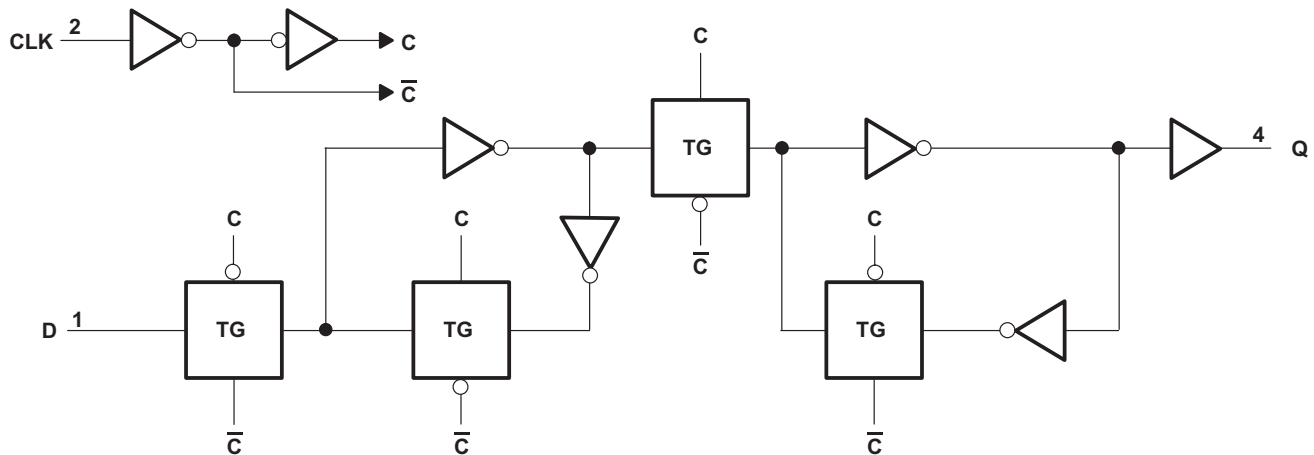
该器件完全适用于使用 I_{off} 的局部掉电应用。当器件断电时, I_{off} 电路将会禁用输出。这会抑制电流反流到器件中, 从而防止损坏器件。

器件信息⁽¹⁾

器件型号	封装	封装尺寸
SN74LVC1G79DBV	SOT-23 (5)	2.90mm × 1.60mm
SN74LVC1G79DCK	SC70 (5)	2.00mm × 1.25mm
SN74LVC1G79DRL	SOT (5)	1.60mm × 1.20mm
SN74LVC1G79YZP	DSBGA (5)	1.14mm × 0.91mm

(1) 要了解所有可用封装, 请参见数据表末尾的可订购产品附录。

逻辑图 (正逻辑)



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目录

1	特性	1	7	Parameter Measurement Information	9
2	应用	1	8	Detailed Description	11
3	说明	1	8.1	Overview	11
4	修订历史记录	2	8.2	Functional Block Diagram	11
5	Pin Configuration and Functions	3	8.3	Feature Description	11
6	Specifications	4	8.4	Device Functional Modes	12
6.1	Absolute Maximum Ratings	4	9	Application and Implementation	13
6.2	ESD Ratings	4	9.1	Application Information	13
6.3	Recommended Operating Conditions	5	9.2	Typical Application	13
6.4	Thermal Information	5	10	Power Supply Recommendations	14
6.5	Electrical Characteristics	6	11	Layout	14
6.6	Timing Requirements: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	6	11.1	Layout Guidelines	14
6.7	Timing Requirements: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	6	11.2	Layout Example	14
6.8	Switching Characteristics: $C_L = 15\text{ pF}$, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	7	12	器件和文档支持	15
6.9	Switching Characteristics: $C_L = 30$ or 50 pF , $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	7	12.1	文档支持	15
6.10	Switching Characteristics: $C_L = 30\text{ pF}$ or 50 pF , $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	7	12.2	接收文档更新通知	15
6.11	Operating Characteristics	7	12.3	社区资源	15
6.12	Typical Characteristics	8	12.4	商标	15
			12.5	静电放电警告	15
			12.6	Glossary	15
			13	机械、封装和可订购信息	15

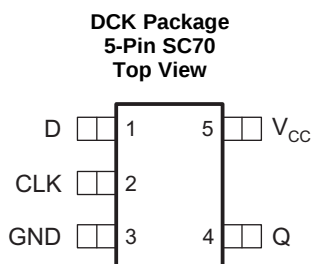
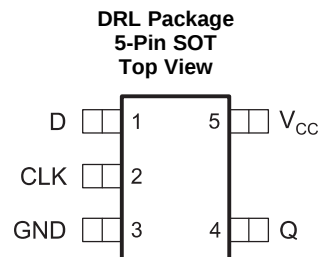
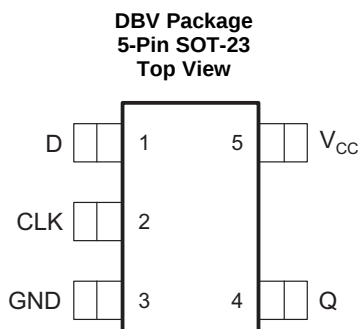
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

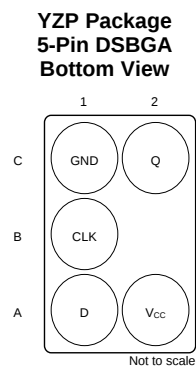
Changes from Revision T (December 2013) to Revision U	Page
• 已添加 器件信息 表、ESD 额定值 表、热性能信息 表、特性 说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分	1
• Changed thermal information to align with JEDEC standards.	5

Changes from Revision S (November 2007) to Revision T	Page
• 将文档更新为了新的 TI 数据表格式。	1
• 删除了订购信息表。	1
• 更新了 I_{off} 特性。	1
• Updated operating temperature range.	5
• 添加了 ESD 警告。	15

5 Pin Configuration and Functions



See mechanical drawings for dimensions.



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DBV, DCK, DRL	YZP		
D	1	A1	I	Data input
CLK	2	B1	I	Positive-Edge-Triggered Clock input
GND	3	C1	—	Ground
Q	4	C2	O	Non-inverted output
V _{CC}	5	A2	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±50		mA
	Continuous current through V _{CC} or GND		±100		mA
T _{stg}	Storage temperature		−65	150	°C
T _J	Junction temperature			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine Model (MM), A115-A	200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 3 V to 3.6 V	2	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.8	
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4	mA
		V _{CC} = 2.3 V	–8	
		V _{CC} = 3 V	–16	
			–24	
		V _{CC} = 4.5 V	–32	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	8	
		V _{CC} = 3 V	16	
			24	
		V _{CC} = 4.5 V	32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20	ns/V
		V _{CC} = 3.3 V ± 0.3 V	10	
		V _{CC} = 5 V ± 0.5 V	5	
T _A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G79				UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	247.2	277.6	294.3	144.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	154.5	179.5	129.9	1.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	86.8	75.9	143.4	39.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	58.0	49.7	14.3	0.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	86.4	75.1	144.0	39.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = –40°C to +85°C			T _A = –40°C to +125°C			UNIT
				MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = –100 μA		1.65 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –4 mA		1.65 V	1.2			1.2			
	I _{OH} = –8 mA		2.3 V	1.9			1.9			
	I _{OH} = –16 mA		3 V	2.4			2.4			
	I _{OH} = –24 mA			2.3			2.3			
	I _{OH} = –32 mA		4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 100 μA		1.65 V to 5.5 V	0.1			0.1			V
	I _{OL} = 4 mA		1.65 V	0.45			0.45			
	I _{OL} = 8 mA		2.3 V	0.3			0.3			
	I _{OL} = 16 mA		3 V	0.4			0.4			
	I _{OL} = 24 mA			0.55			0.55			
	I _{OL} = 32 mA		4.5 V	0.55			0.55			
I _I	All inputs	V _I = 5.5 V or GND	0 to 5.5 V	±10			±5			μA
I _{off}		V _I or V _O = 5.5 V	0	±10			±10			μA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10			10			μA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500			500			μA
C _i		V _I = V _{CC} or GND	3.3 V	4			4			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements: T_A = –40°C to +85°C

over operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER			T _A = –40°C to +85°C								UNIT
			V _{CC} = 1.8 ± 0.15 V		V _{CC} = 2.5 ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		160		160		160		160		MHz
t _w	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
t _{su}	Setup time before CLK↑	Data high	2.2		1.4		1.3		1.2		ns
		Data low	2.6		1.4		1.3		1.2		
t _h	Hold time, data after CLK↑		0.3		0.4		1		0.5		ns

6.7 Timing Requirements: T_A = –40°C to +125°C

over operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER			T _A = –40°C to +125°C								UNIT
			V _{CC} = 1.8 ± 0.15 V		V _{CC} = 2.5 ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		160		160		160		160		MHz
t _w	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
t _{su}	Setup time before CLK↑	Data high	2.2		1.4		1.3		1.2		ns
		Data low	2.6		1.4		1.3		1.2		
t _h	Hold time, data after CLK↑		0.3		0.4		1		0.5		ns

6.8 Switching Characteristics: $C_L = 15 \text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = −40°C to +85°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	Q	2.5	9.1	1.2	6	1	4	0.8	3.8	ns

6.9 Switching Characteristics: $C_L = 30$ or 50 pF , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = −40°C to +85°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	Q	3.9	9.9	2	7	1.7	5	1	4.5	ns

6.10 Switching Characteristics: $C_L = 30 \text{ pF}$ or 50 pF , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = −40°C to +125°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	Q	3.9	12	2	8.5	1.7	6	1	5	ns

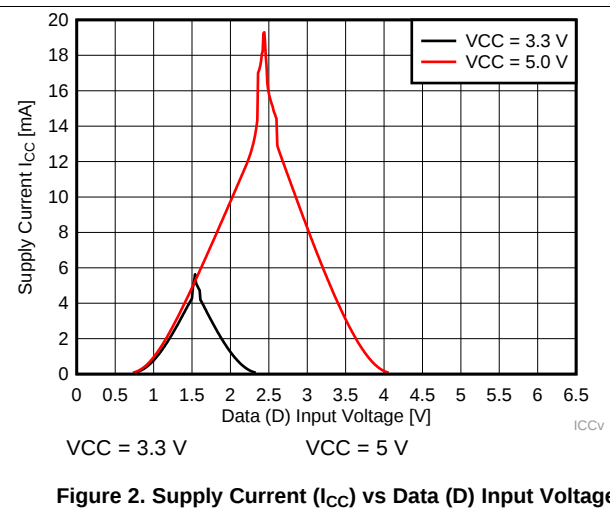
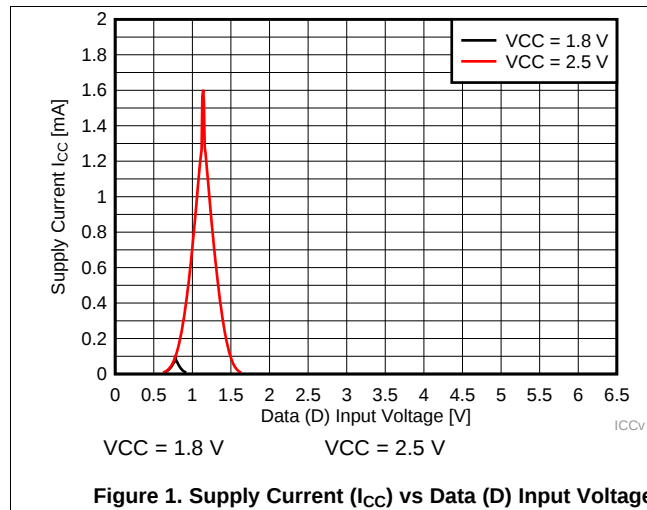
6.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

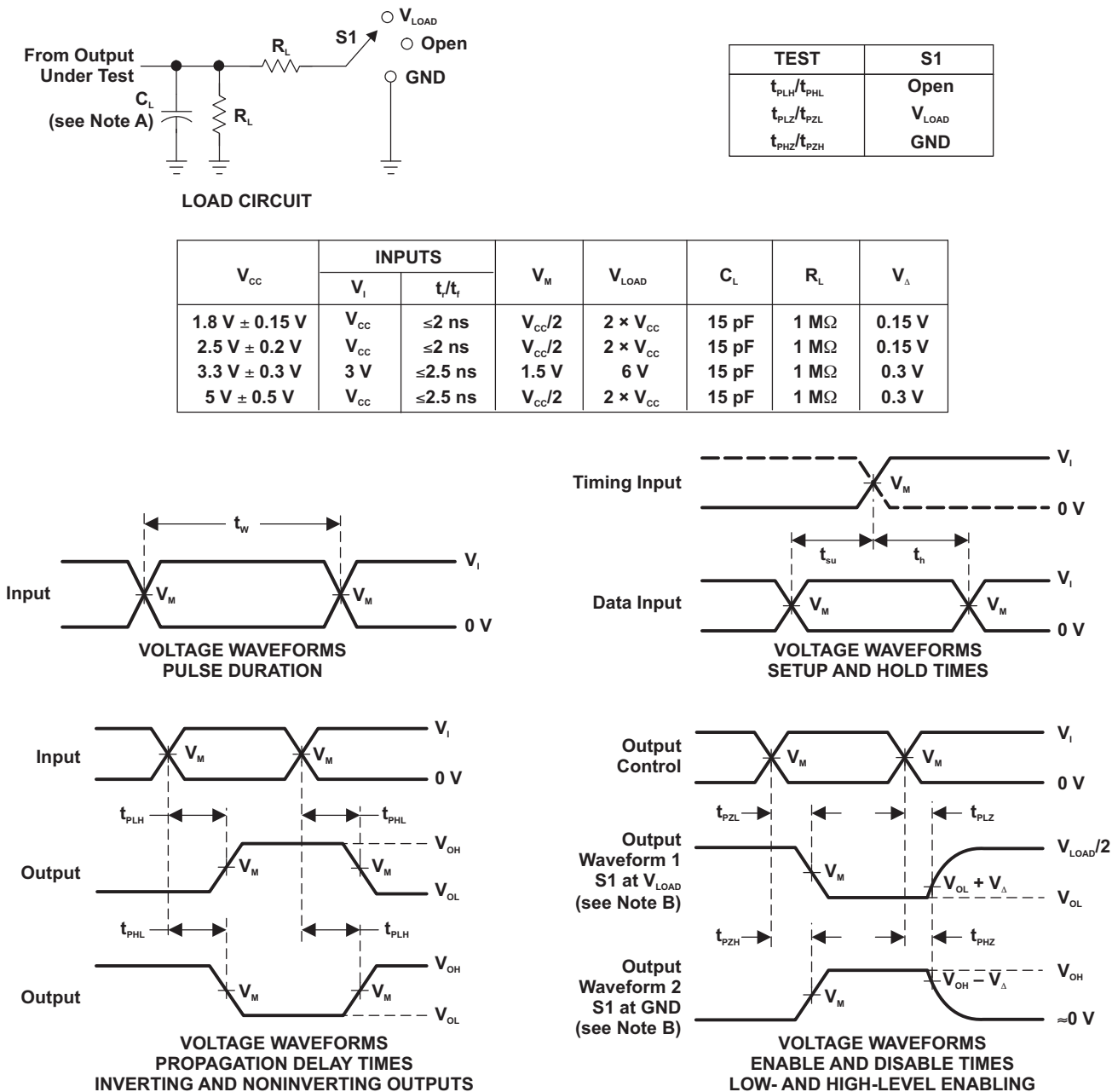
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	f = 10 MHz	26	26	27	30	pF

6.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0 V to 6.5 V.

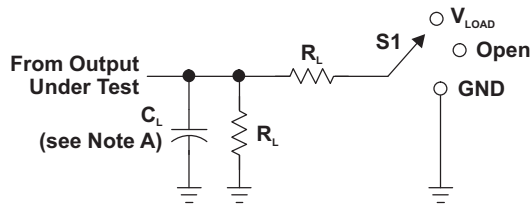


7 Parameter Measurement Information



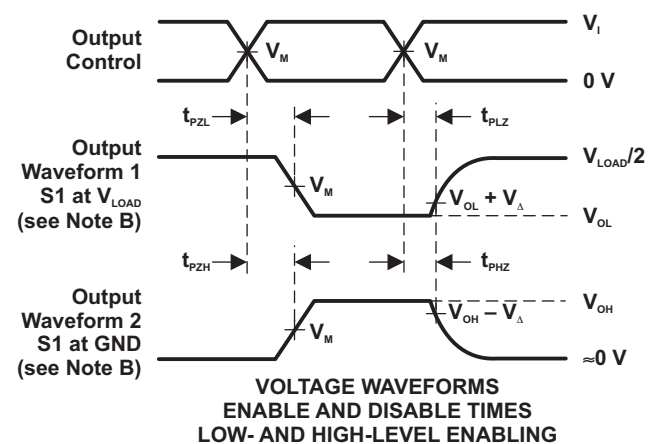
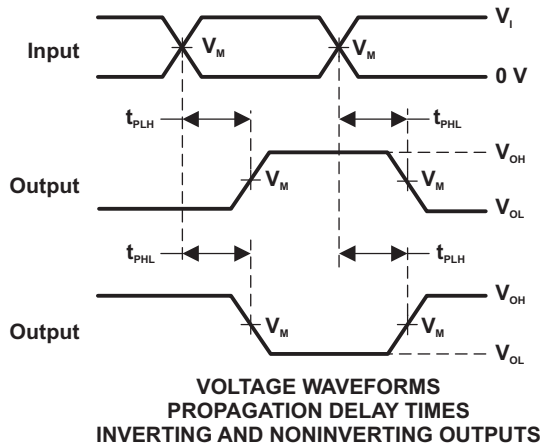
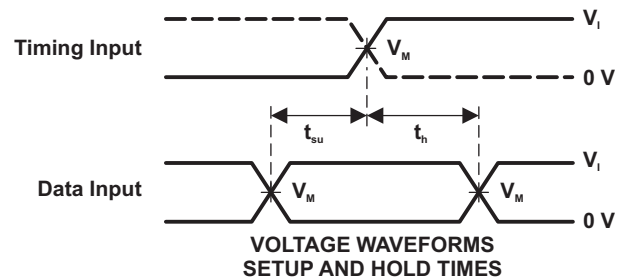
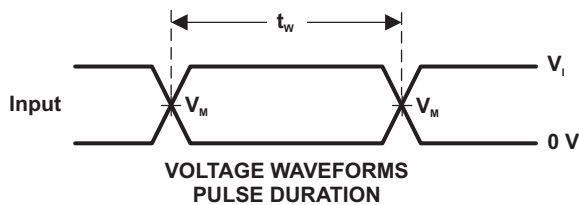
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{on} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G79 is a single positive-edge-triggered D-type flip-flop. Data at the input (D) is transferred to the output (Q) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

8.2 Functional Block Diagram

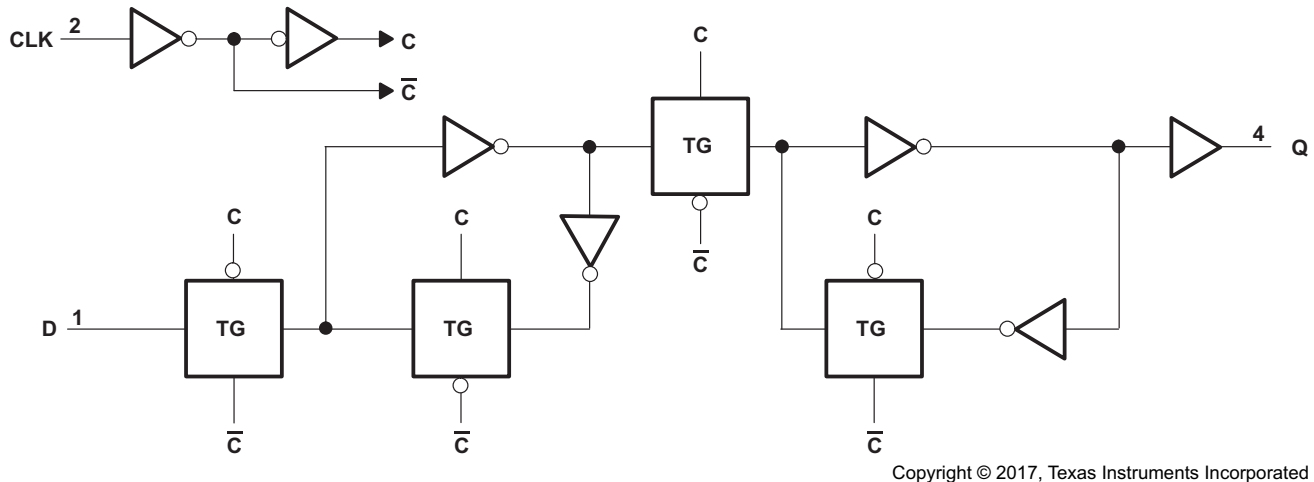


Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Recommended Operating Conditions](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [Recommended Operating Conditions](#) to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

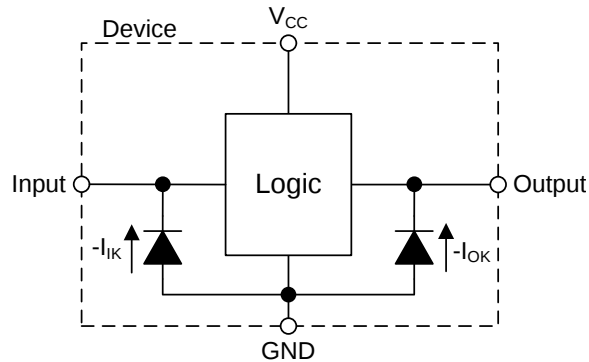


Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Absolute Maximum Ratings](#).

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of SN74LVC1G79.

Table 1. Function Table

INPUTS		OUTPUT Y
CLK	D	
↑	H	H
↑	L	L
L	X	Q_0

9 Application and Implementation

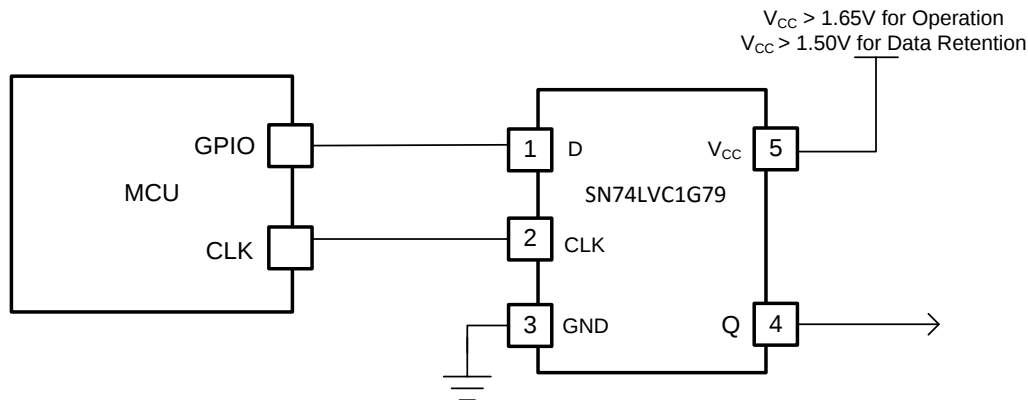
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A useful application for the SN74LVC1G79 is using it as a data latch with low-voltage data retention. This application implements the use of a microcontroller GPIO pin to act as a clock to set the output state and a second GPIO to provide the input data. If the SN74LVC1G79 is being powered from 1.8 V and there is concern that a power glitch could exist as low as 1.5 V, the device will retain the state of the Q output. An example of this data retention is shown in [Figure 8](#) where the V_{CC} drops to 1.5 V and the Q output maintains the HIGH output state when V_{CC} returns to 1.8 V. If the V_{CC} voltage drops below 1.5 V, data retention is not guaranteed.

9.2 Typical Application



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Figure 7. Low Voltage Data Retention With SN74LVC1G79

9.2.1 Design Requirements

The SN74LVC1G79 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in [Recommended Operating Conditions](#).
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
 - Input voltages are recommended to not go below 0 V and not exceed 5.5 V for any V_{CC} . See [Recommended Operating Conditions](#).
2. Recommended output conditions:
 - Load currents should not exceed ± 50 mA. See [Absolute Maximum Ratings](#).
 - Output voltages are recommended to not go below 0 V and not exceed the V_{CC} voltage. See [Recommended Operating Conditions](#).

Typical Application (continued)

9.2.3 Application Curve

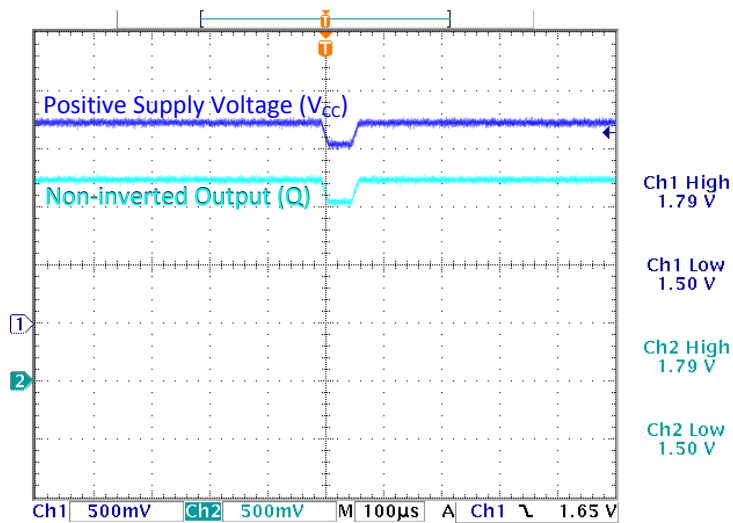


Figure 8. Data Retention With V_{CC} Glitch Down to 1.5 V

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in [Recommended Operating Conditions](#). A 0.1- μ F bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 9](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

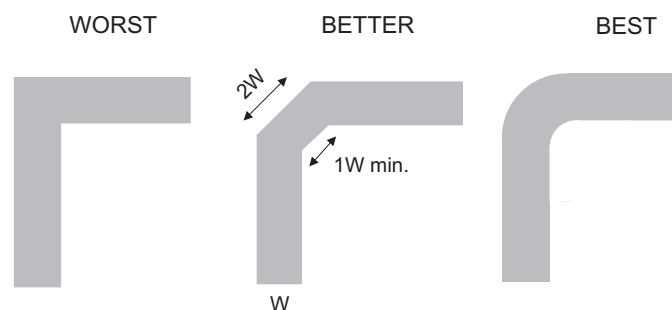


Figure 9. Trace Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档请参阅以下部分：

- 《慢速或浮点 CMOS 输入的影响》，SCBA004
- 《了解和解读标准逻辑器件数据表》，SZZA036
- 《计时器件的加电行为》，SCHA005

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

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12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G79DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C795, C79F, C79J, C79R)	Samples
SN74LVC1G79DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C795, C79F, C79J, C79R)	Samples
SN74LVC1G79DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C79F	Samples
SN74LVC1G79DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CR5, CRF, CRJ, CR R)	Samples
SN74LVC1G79DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR5	Samples
SN74LVC1G79DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR5	Samples
SN74LVC1G79DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CR5, CRF, CRJ, CR R)	Samples
SN74LVC1G79DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR5	Samples
SN74LVC1G79DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CR7, CRR)	Samples
SN74LVC1G79YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CR7, CRN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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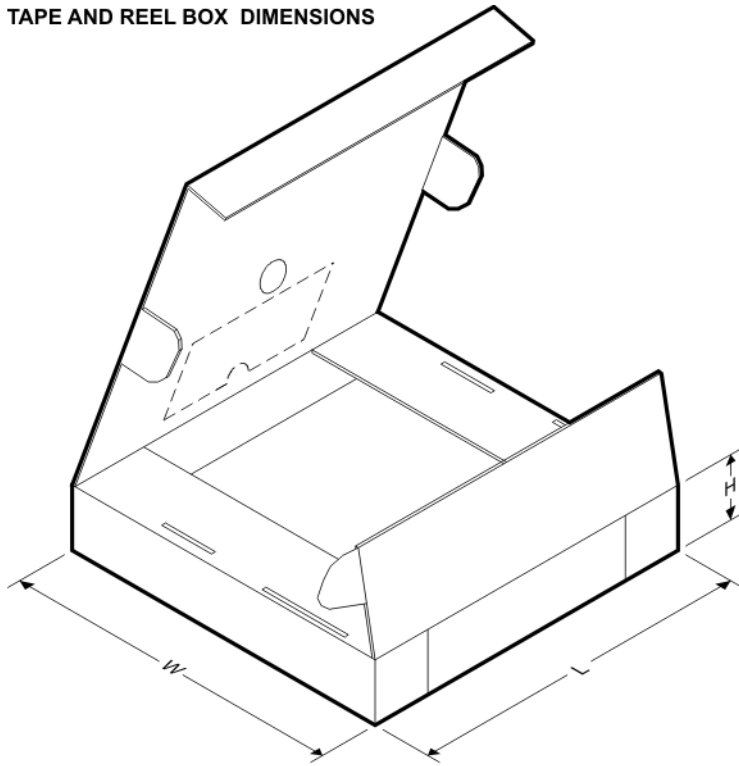
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G79DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G79DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G79DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G79DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G79DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G79YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

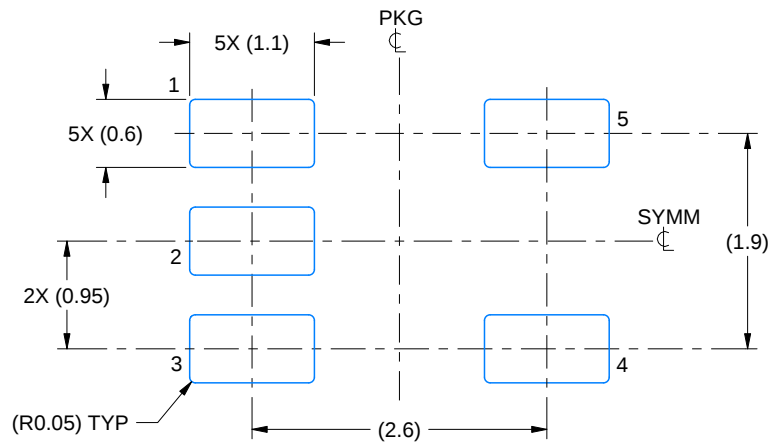
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G79DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G79DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G79DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G79DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G79DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G79DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G79YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

EXAMPLE BOARD LAYOUT

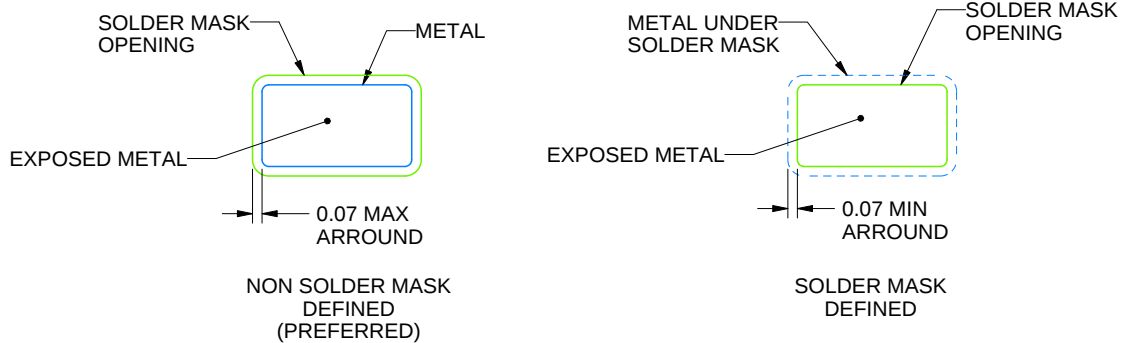
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

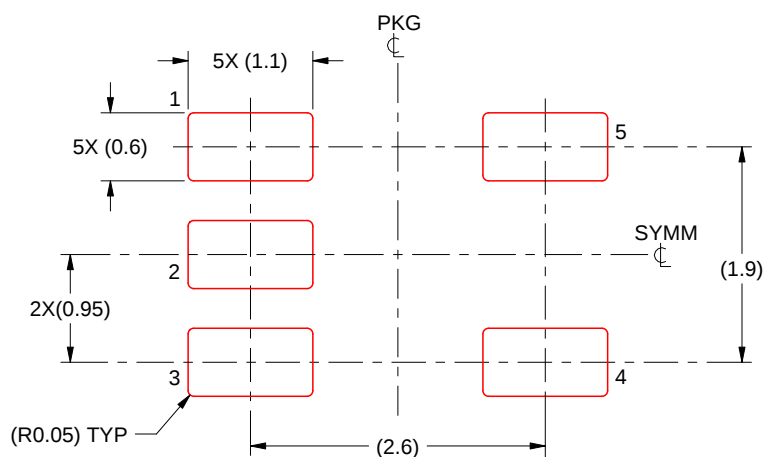
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

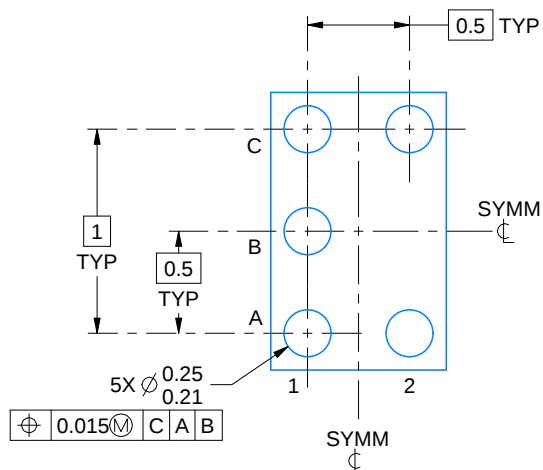
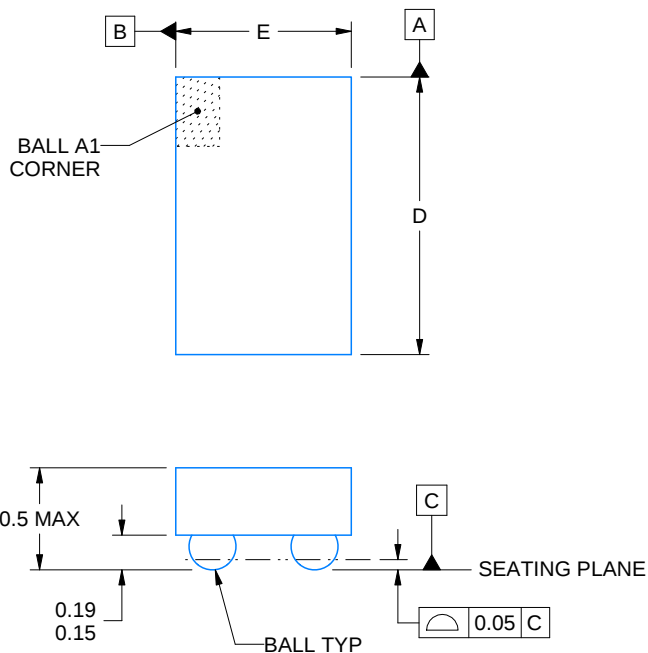
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm

E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

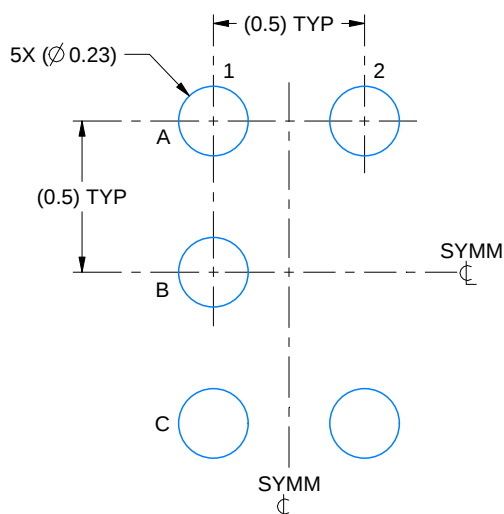
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

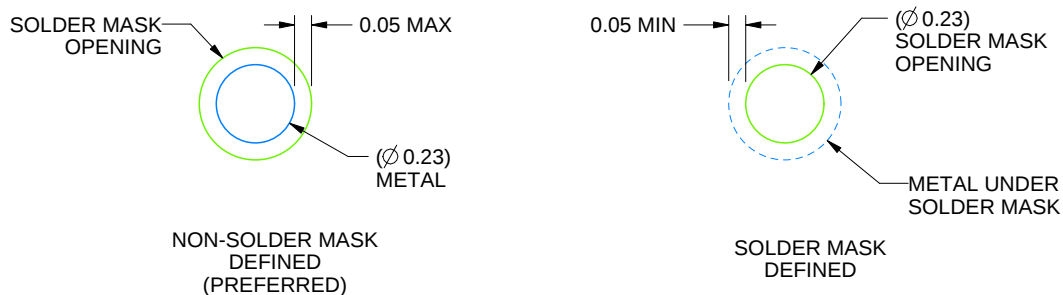
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

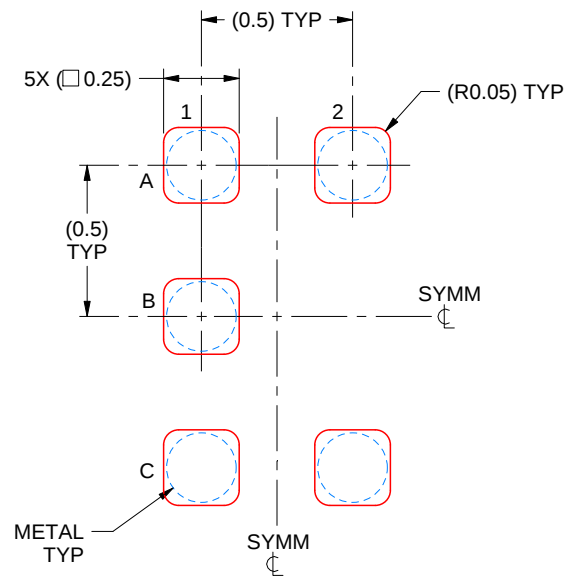
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



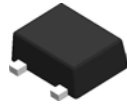
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

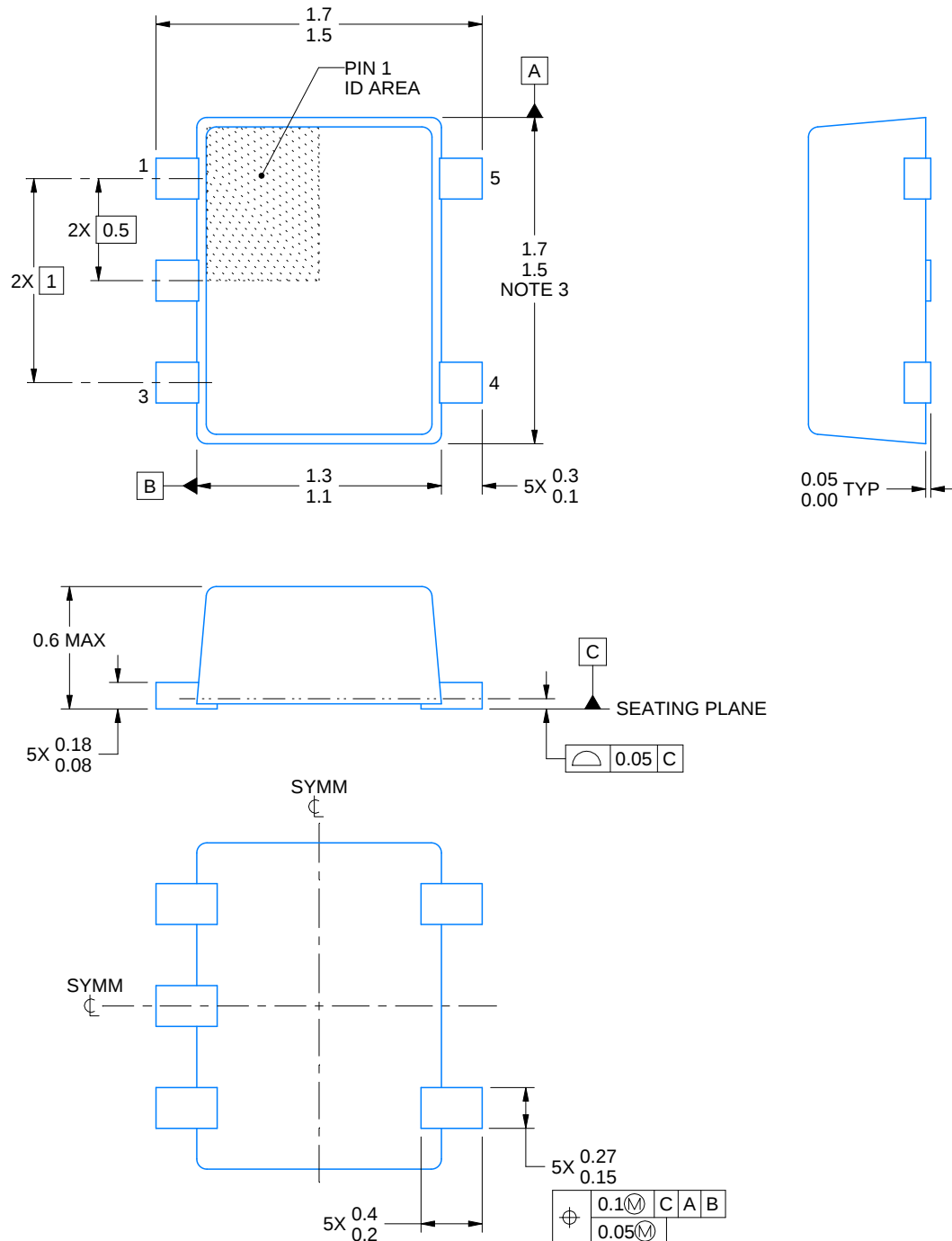
DRL0005A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/B 12/2020

NOTES:

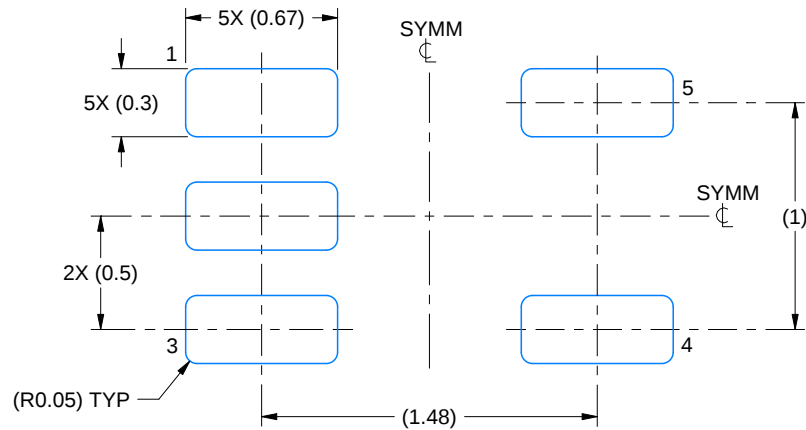
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

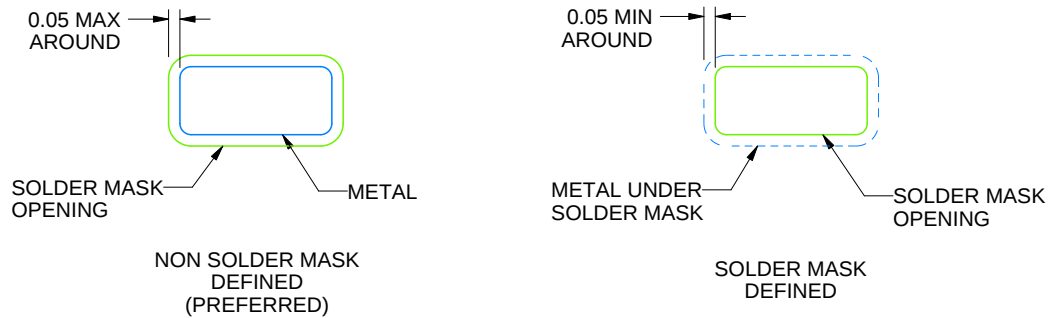
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

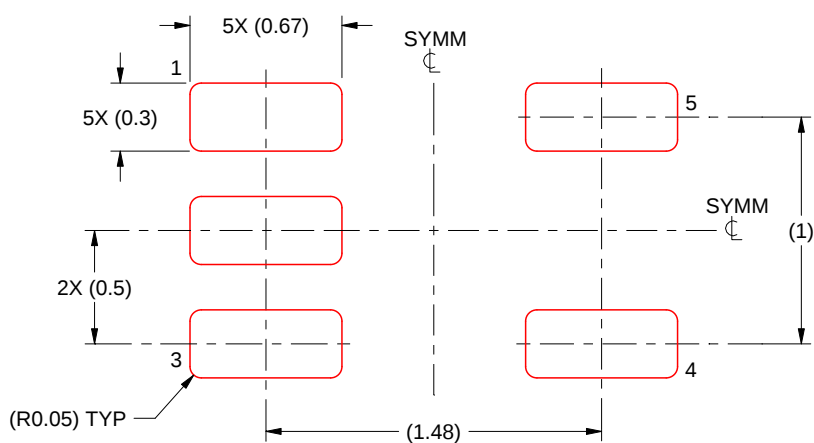
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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